Memory™ Merchant

IEEE 696/S-100

MM16K14

16K STATIC RAM

USER'S MANUAL

(REV 1)

14666 DOOLITTLE DR. SAN LEANDRO, CA. 94577 (415) 483-1008

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Limited Warranty

Memory Merchant warrants its products to be free from defects in workmanship and materials for a period of One (1) year from the date of shipment/Invoice from Memory Merchant or Dealer/Agent to the original end user. If any memory board becomes defective within the first six (6) months from the date of shipment/Invoice, Memory Merchant will replace, not repair, that unit. Should any memory board become defective after the initial six (6) month warranty period, Memory Merchant reserves the right to replace or repair that unit which proves to be defective. The warranty is Void if, in the sole opinion of Memory Merchant, the product has been subject to abuse, misuse, unauthorized modification, Serial No. modification, or if the unit is used in any other manner than intended. All warranties are non-transferable and are Void if any Memory Merchant product is sold by the original end user to any other end user.

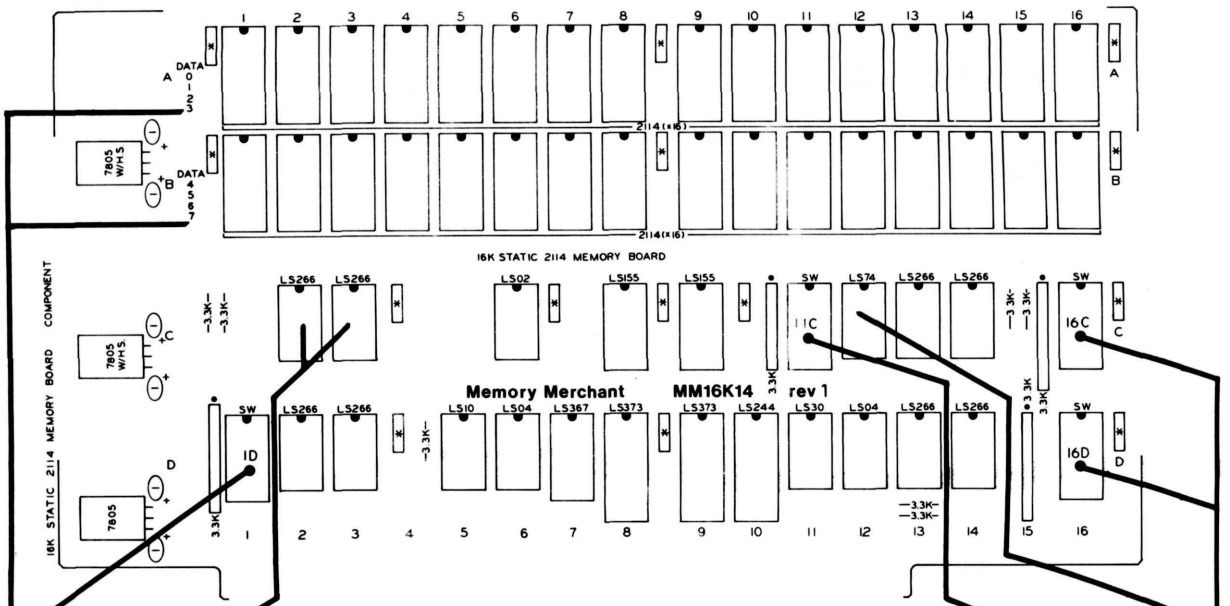
Return Policy:

1) All defective products in question, whether purchased directly from Memory Merchant or through a Dealer/Agent, must be returned to Memory Merchant for repair or replacement according to the conditions set forth in the above warranty.
2) Prior to shipping any defective product for replacement or repair, you must receive a Return Material Authorization (RMA) number from Memory Merchant. When requesting an RMA No., please provide the following information: A discription of the problem with as much detail as possible; Serial No.(s) of the unit(s); where the unit was purchased along with the date of purchase.
3) Upon receiving an RMA No. from Memory Merchant, pack the unit(s) along with a copy of your proof of purchase and ship it prepaid to Memory Merchant. Items received without proof of purchase will be returned at senders expense. The RMA No. MUST BE MARKED on the OUTSIDE of the shipping container or it will be refused.
4) Repaired or replacement products, still in warranty, will be shipped prepaid by UPS Surface. Customer requests for any method of shipment other than UPS Surface will be chargeable to the Customer. All requests for Air Freight will be shipped Collect.
5) All out of warranty products returned for repair or testing will be assessed a minimum of $50.00 service charge. If the charge for repair is to exceed $50.00, the customer will be notified (For Authorization) prior to starting the actual repair. An RMA No. is required for out-of-warranty returns!

The foregoing warranty is in lieu of all other warranties either expressed or implied and, in any event, is limited to product repair or replacement.

Effective 6/15/81

All prices, Terms, Specifications are subject to change without notice.



IC's #2C,3C
Board comes loaded for Bank Select (Pg.9). For Extended Addressing remove and insert into Loc. #2D & #3D (Pg.6,7)

Switch "11C"
This switch is for:
Phantom (Pg.12)
Strobe (Pg.12)
System Init.(Pg.10)
Segment Dis.(Pg.11)

74LS74
This part remains for Bank Select(Pg.9),and is removed for Extended Addressing (Pg.6).

Switch "1D"
Used for both Bank Select (see Pg.9,10), and Extended Addressing (see Pg.7,8).

Switch "16C" & "16D"
These two switches are for Memory Addressing. (See Pg. 4,5,6)

Data Bit Enable
(Headers)

See Pg.9

INTRODUCTION

With the introduction of the sophisticated and powerful microcomputer system, the demand for flexibility and cost effective memory systems has surfaced. The Memory Merchants' MM16K14 Static RAM board has been engineered to these specifications and more. Not only can the MM16K14 meet all existing memory requirements, but any, if not all, requirements that may present themselves in the future.

The Memory Merchants MM16K14 is, without a doubt, the most versatile board on the market today. With features like Segment Disable, Bank Select, Extended Addressing, and Phantom there is virtually no application where the MM16K14 could not be used.

By using the popular 2114 Static RAM array with an access time that is guaranteed to run at 4MHZ, the MM16K14 is compatible with all 8080, Z80, and 8085 processors. Of course, by using Static RAM instead of Dynamic RAM, the MM16K14 allows the processor to run at full speed without any wait states or cycle stealing.

Bank Select or Extended Addressing? You have a choice with the Memory Merchants memory board. The Bank Select feature allows the board to be set up at any of 256 I/O Addresses and respond to any one of 8 data bits desired. The Extended Addressing allows the MM16K14 to reside anywhere in the memory map either above or below the 64K boundary limitations imposed by most microcomputer systems.

A unique feature of the MM16K14 memory is the segment disable logic. With the use of DIP switches up to four (4) 1K segments of memory can be disabled within a specified 4K block. By addressing the specified block "over" memory mapped controllers, 1K segments can then be disabled anywhere within that particular 4K block to allow both the controller board and the memory board to co-exist in the same block of the memory map. By setting up the system in this manner, the maximum amount of memory can be added to the memory map and present system configuration need not be altered.

Of course, the Memory Merchants MM16K14 offers reliability and economy that is unsurpassed in the industry. Because of this, Memory Merchant offers a 6 month, no hassle, warranty exchange program designed to keep your system up and running.

WARNING.....NEVER INSERT OR REMOVE THE MEMORY MERCHANT BOARD WITH POWER ON. ALWAYS REMOVE POWER FROM THE BUSS AS SERIOUS ELECTRICAL DAMAGE COULD OCCUR TO THE SYSTEM AND THE MEMORY BOARD.

MEMORY ADDRESSING

The Memory Merchant MM16K14 is configured as 4 blocks of 4K bytes each. Each of the 4K blocks can be addressed at any 4k boundary in the memory map. Thus, blocks of memory can be assigned at Address location 0000H, 1000H, 2000H, and so on up to memory Address F000H. With the addressing on 4K boundaries, memory addressing need not be consecutive, which allows for "filling" holes in the map.

The DIP switch arrays located at 16C and 16D perform the Address selection. These DIP switches locate each of the 4 individual 4K blocks within a 64K page or block of memory space. There are 8 paddles in each DIP array, so therefore each DIP array controls the addressing of 2 blocks of memory.

The individual paddles of the switches are tied to a pull-up resistor (to set a zero) when the switch is positioned OFF and to Ground (to set a one) when the switch is in the ON position. The output of the switch is then fed to the input of a 74LS266 Exclusive NOR gate along with the corresponding inverted Address line (A12 thru A15). When the switch is in the OFF position (zero) in order for the gate to respond to the signal, the Address line on the buss must be a low level. Likewise, when the switch is in the ON (one) position the corresponding Address line must be high for the gate to respond.

The following truth table of the 74LS266 will help explain how the block select functions.

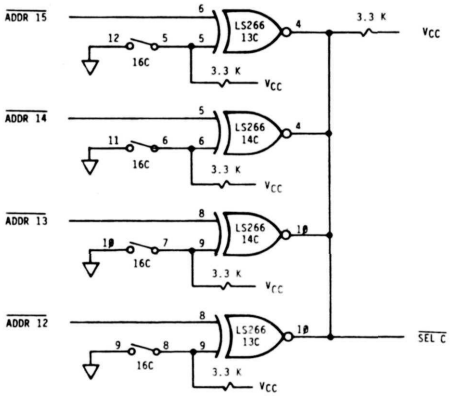
INPUT A	INPUT B	OUTPUT
HIGH	HIGH	HIGH
HIGH	LOW	LOW
LOW	HIGH	LOW
LOW	LOW	HIGH

What this truth table shows is that when INPUT A and INPUT B are the same levels, the output of the gate goes HIGH. When the inputs are at different levels, the output remains at a LOW level.

One other important point to remember is that the 74LS266 is an open collector gate. This means that the gate must have an external pull-up resistor in order for the output to attain a high level. The advantage of course, is that many of these gates can have their outputs wired together to make circuits that respond to very specific circumstances. That is what the Memory Merchants MM16K14 card does.

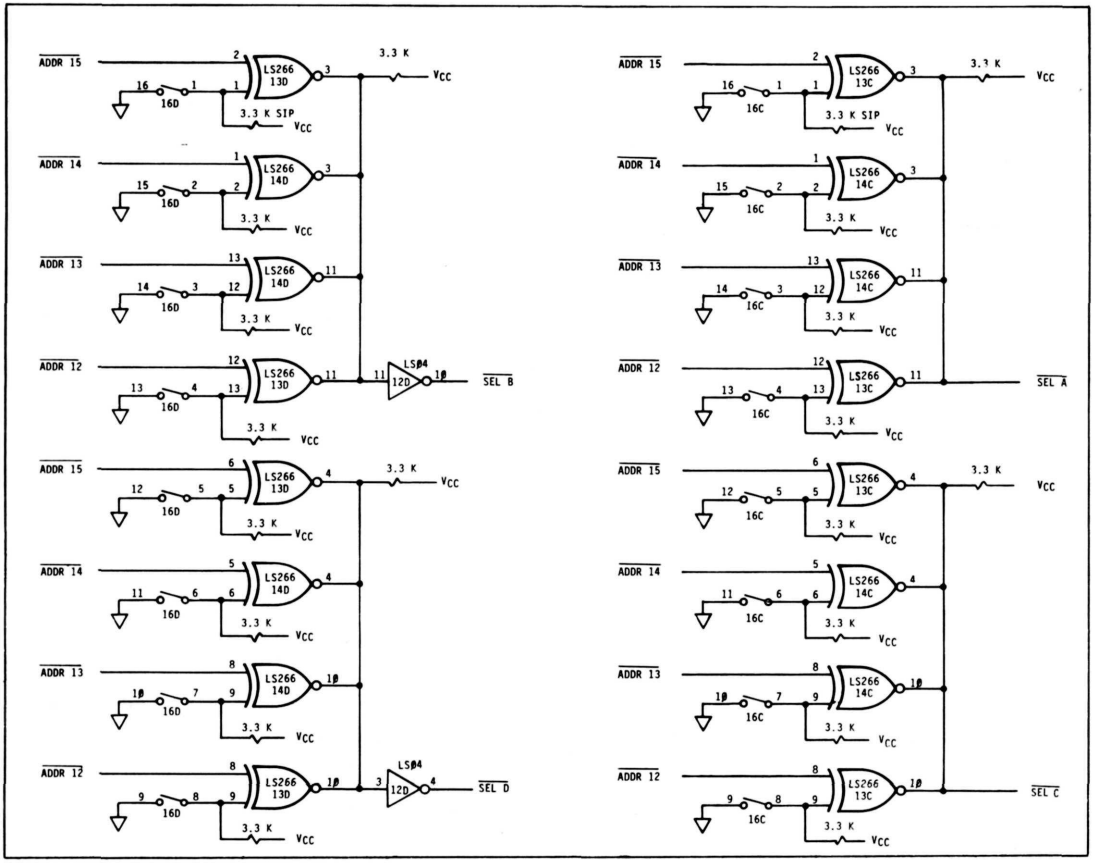
The drawing below shows the basic SELECT logic and the switch arrangement for 1 4K block of RAM (reference DIP array 16C).

(BLOCK "C")



By observing the above drawing of the block select logic, it becomes evident (use the truth table Pg.2) how the block select logic works. For example, if paddle #1 is in the ON position that would mean that the corresponding Address line would have to be a HIGH level on the buss in order to be recognized. If paddle #2, paddle #3, and paddle #4 were in the OFF position, then the 3 remaining Address lines would then have to be a LOW level in order for the output to go HIGH. If any of the four input Address lines did not match the switch setting, the output of the gate will remain LOW and the block would not be selected or recognized by the computer.

The diagram below shows the switch settings and the corresponding Address lines .



MEMORY ADDRESSING TABLE

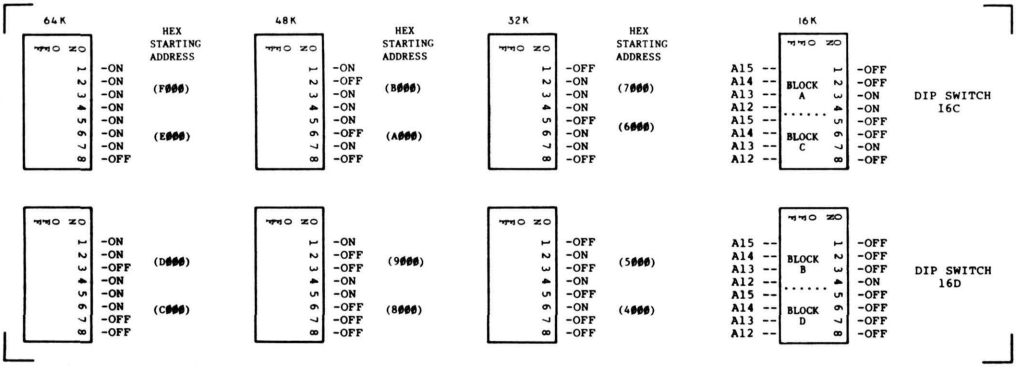
The following table shows the relationship between the DIP switch settings and the block location located within the memory map.

STARTING ADDRESS HEX	OCTAL	A15	A14	A13	A12
0000	000:000	OFF	OFF	OFF	OFF
1000	020:000	OFF	OFF	OFF	ON
2000	040:000	OFF	OFF	ON	OFF
3000	060:000	OFF	OFF	ON	ON
4000	100:000	OFF	ON	OFF	OFF
5000	120:000	OFF	ON	OFF	ON
6000	140:000	OFF	ON	ON	OFF
7000	160:000	OFF	ON	ON	ON
8000	200:000	ON	OFF	OFF	OFF
9000	210:000	ON	OFF	OFF	ON
A000	220:000	ON	OFF	ON	OFF
B000	240:000	ON	OFF	ON	ON
C000	260:000	ON	ON	OFF	OFF
D000	300:000	ON	ON	OFF	ON
E000	310:000	ON	ON	ON	OFF
F000	320:000	ON	ON	ON	ON

EXAMPLE OF MEMORY ADDRESSING

The following example will show the switch settings of the Memory Merchant MM16K14 Memory board addressed to occupy the first 16K of the memory map.

Also, below are the switch settings (16C & 16D) for 32K, 48K, and 64K



EXTENDED ADDRESSING

The Memory Merchant MM16K14 conforms to the IEEE standard 696 (S-100) and therefore, can recognize 24 memory Address lines. The use of Extended Addressing does away with the 64K limit and allows the memory board to reside in the memory map at any 64K boundary up to Address FF0000.

In order for the Extended Addressing to be enabled, IC locations 2D and 3D MUST have 74LS266's installed. These two IC's must be removed from locations 2C and 3C (Bank Select logic). Also, the 74LS74 at location 12C must be removed from its' socket.

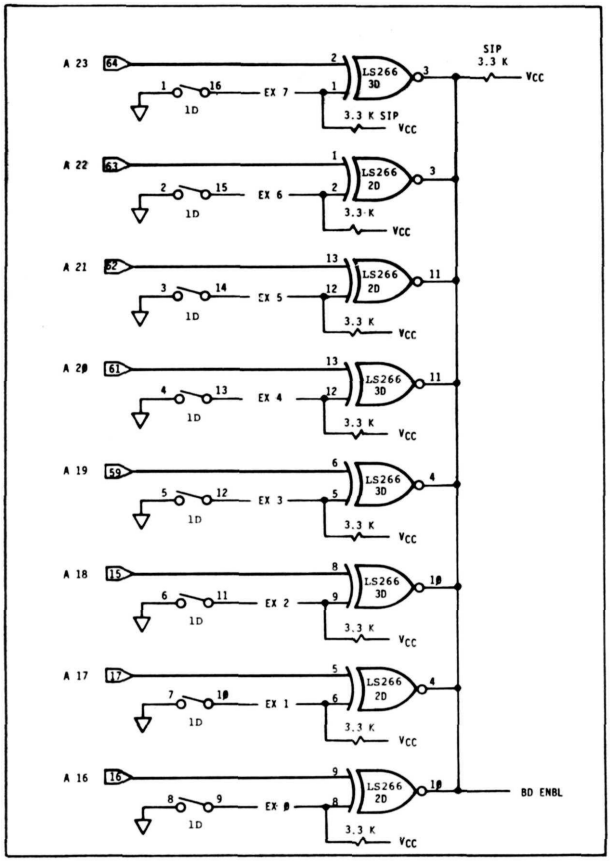
NOTE: On some production boards, IC locations 2C, 2D, 3C, and 3D were mistakenly labeled on the silk screen as 74LS136 instead of 74LS266.

The DIP switch array at location ID sets the Extended Address. This switch sets the board to recognize addresses on 64K boundaries. The switches at locations 16C and 16D address the 4K blocks within the boundaries set by the switch at location 1D.

The Extended Addressing allows the board to be addressed in 64K increments starting at Address 000000H, 010000H, 020000H, up to Address FF0000H. The logic involved in setting the Extended Addressing mode is identical to the logic that sets up the 4K blocks, with one major exception. Instead of using four (4) Address lines (A12 thru A15) the Extended Addressing uses eight (8) Address lines (A16 thru A23) to select the the proper memory map location.

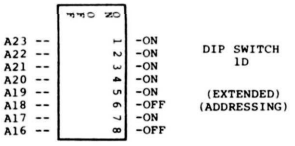
The circuitry consists of a DIP switch and 2 74LS266 Exclusive NOR gates. The DIP switch inputs are tied to a pull-up resistor (to set a one) when the switch is OFF and to Ground (to set a zero) when the switch is in the ON position. The output of the switches are then fed to the inputs of 2 74LS266's in order to get the proper board select signal.

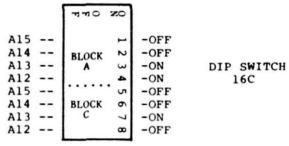
Referring back to the truth table in the MEMORY ADDRESSING SECTION and to the the example below, it is obvious that the Extended Address works on the same principle.

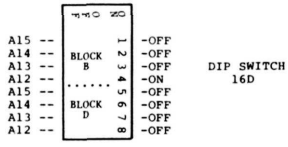


When the switches are set to the appropriate Address, that Address and the Address generated by the CPU must be identical for the board to be enabled. If the switch is set to the ON position the CPU generated address must be low, likewise if the switch is set to the OFF position the CPU address must be a high level. As in the block enables, ALL addresses must match the switch settings before the board will recognize an address generated by the CPU.

The following is an example of extended addressing. The board will be addressed to occupy the first 16K of a 64K block that resides in the memory map at memory location 050000H.







BANK SELECT

For many existing systems built before the creation of the IEEE 696 S-100 standard, use of Bank Select memory is a must since most existing CPU boards do not generate Extended Addresses. Again, the Memory Merchants MM16K14 memory rises to the occasion. Using the same DIP switch array the MM16K14 is able to recognize any of 256 I/O port Addresses and enable/disable itself using any of the 8 data bits.

In order for the Bank Select option to function properly IC locations 2C and 3C must have 74LS266's installed. These two IC's must be removed from location 2D and 3D (Extended Memory logic). Also, the 74LS74 at location 12C should be installed in its' socket.

The DIP switch at location 1D sets the I/O port address for Bank select. One might wonder how the same switch that set the Extended Addressing is now setting the Bank Select. Remember, to enable the Bank Select, 2 IC's were moved from locations 2D and 3D. When these IC's are in those locations the switch controls Extended Addressing, when the IC's are in locations 2C and 3C they control Bank Select. Because the board can only be set up for Bank select or Extended Addressing, by moving the IC's only one DIP switch array is needed.

The Bank select logic is identical to the Extended Addressing logic in almost every respect. The main difference is the Bank Select logic uses Address Lines 0 thru 7 and Extended Addressing uses Address Lines 16 through 23 to enable. In the Bank Select mode of operation, to properly enable the board three conditions must be met. First, the paddles of the DIP switch array at location 1D must be set to the proper I/O Address that matches the software being used. Second, the board must have been issued an I/O command by the processor. And third, the data bit used in the I/O command must have sent the proper bit to the board. Only when all three conditions are met will the Bank Select logic enable the board.

DATA BIT ENABLE

Setting the data bit for Bank Select is accomplished by the installation of a "shunt" on the data headers. These headers are located on the top left of the board (by the regulators) and are marked DATA 0-3 and DATA 4-7. A shorting jumper must be installed horizontally across one of these data bits. When an I/O command is sent to the board, a one in the accumulator bit position corresponding to the shunt position will select the board and a zero in this position will deselect the board.

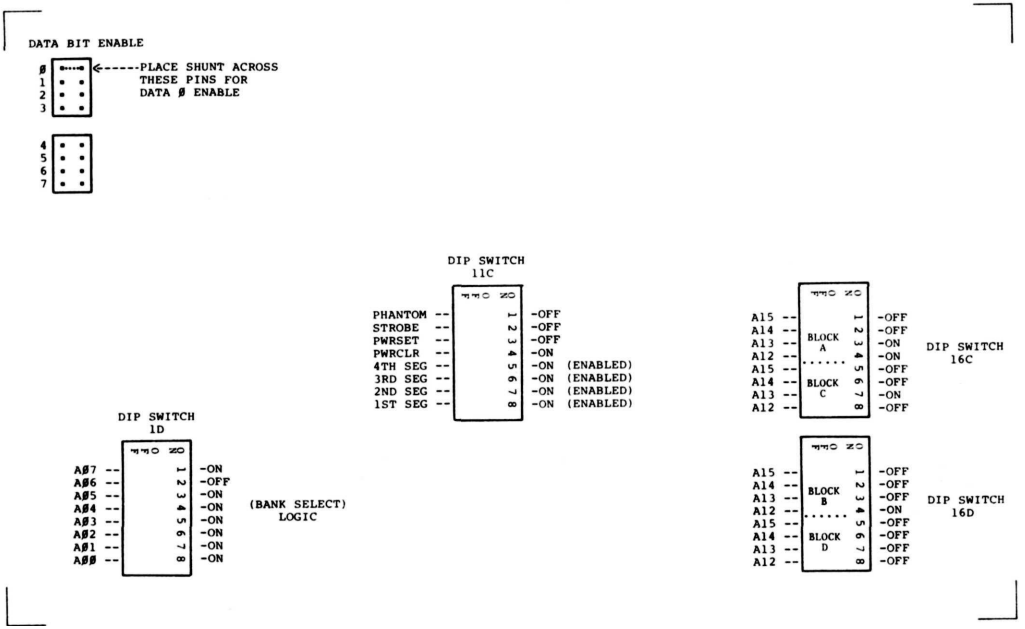
BANK SELECT ENABLE/DISABLE AT SYSTEM RESET OR POWER ON

In the Bank Select configuration, the MM16K14 board has the option of being enabled or disabled when the system is initialized. This feature allows the board to remove itself (disabled) from the buss when the system is first powered on or when the system is initialized. Cromemco for example, switches in a ROM monitor and disables the top 16K of memory so that the Disk boot routine can function. Once the loader has completed, the ROM is switched out and the Memory is switched back in. In a situation such as this, the memory should be set to disable on initialization. This is accomplished by setting paddle 3 on DIP switch array 11C to the ON position and paddle #4 on of 11C to the OFF position. If the system does not need this feature, then set paddle #4 on DIP switch 11C to the ON position and paddle #3 on 11C to the OFF position and the memory will be enabled and on the buss whenever the system is initialized or at power on.

DO NOT SET BOTH SWITCHES IN THE SAME POSITION. THIS WILL CREATE UNPREDICTABLE RESULTS.

The following is an example of Bank Select. The Board will be set to recognize the memory at port address 40H. The board will also be set to respond to data bit 0. Also, memory will be enabled at power on or initialization.

The memory will be set in the map to occupy the first 16K of the memory map.



SEGMENT DISABLE

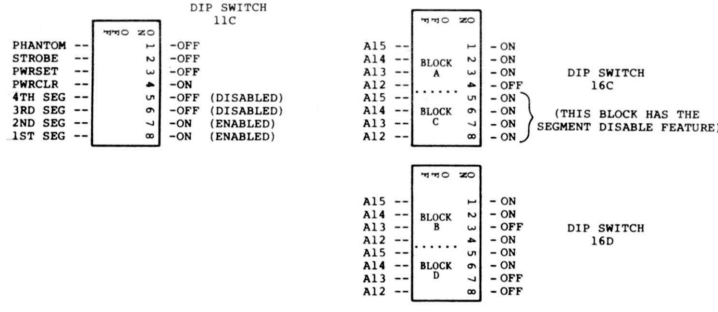
A unique feature of the Memory Merchant MM16K14 is the Segment Disable ability. This feature allows up to four individual 1k segments of memory can be disabled within a specified block.

Block C is the specific area on the board that has been endowed with the segment disable feature. This does not present any limitations since each of the four 4K blocks of memory can be addressed anywhere within a 64K page. Therefore, if it was necessary to disable 2K at Address D000, simply Address block C at Address D000 and disable the first two 1K segments of this block.

The DIP switch array located at position 11C controls the segment disabling. By setting the DIP switch to the ON position, the 1K segments will be enabled. To disable a 1K segment the DIP switch should be set to the OFF position. Paddles 5,6,7, and 8 correspond to the 1K segments to be disabled. Paddle 8 disables the 1st 1K segment, Paddle #7 disables the 2nd, Paddle #6 disables the 3rd ,and Paddle #5 disables the last 1K segment.

The segment disable is a feature that allows users of Memory mapped devices to have the maximum amount of memory possible in the system. If a Disk Controller is located at F800, then all that would be necessary is to disable the top two 1K segments of RAM in the C block, to "shadow" the board. This would then leave 62K of contiguous memory for the operating system and programs.

The following is an example showing the memory board residing in the memory map from location C000H to FFFFH with 2K disabled to allow for the Disk Controller that resides in the memory map at F800H. (Don't care about Ext Add or Bank Sel.--Board will be set to initialize in the active mode of operation.)



PHANTOM ENABLE

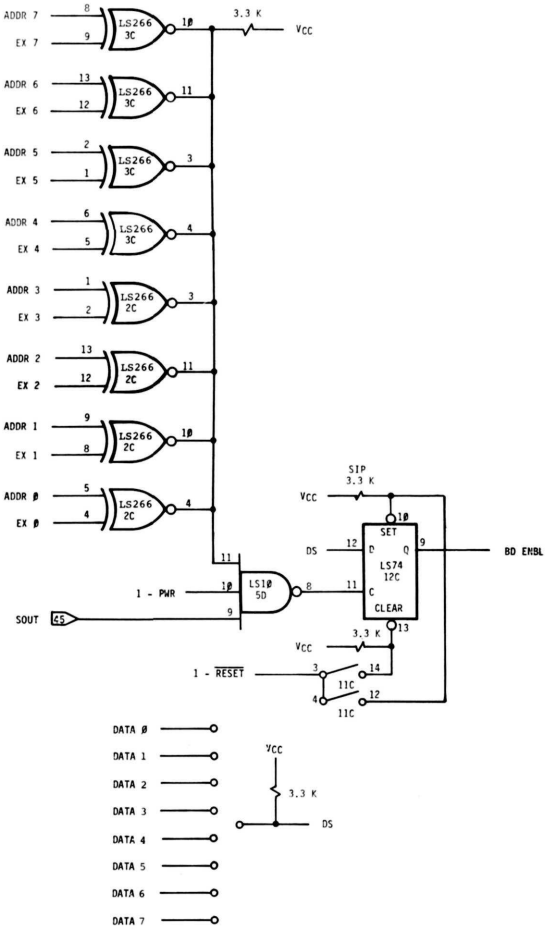
The MM16K14 memory is also capable of recognizing Phantom. The Phantom option is enabled by setting paddle #1 of the DIP switch array located at 11C to the ON position.

The purpose of the Phantom signal is to remove memory from the buss during specific operations. Some of these operations might be the enabling of a bootstrap monitor, ROM Monitor, or a Power on Jump command.

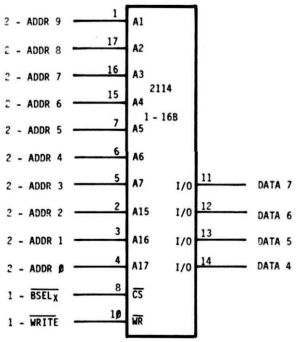
USE OF STROBE

The STROBE signal is used to delay the data from the RAM to the buss. It is controlled by paddle #2 on DIP switch array 11C. If the computer system that is in use, generates MWRITE, either through the front panel or processor card, the paddle must be in the OFF position. If the front panel or processor boards do not generate MWRITE then the STROBE switch should be in the ON position.

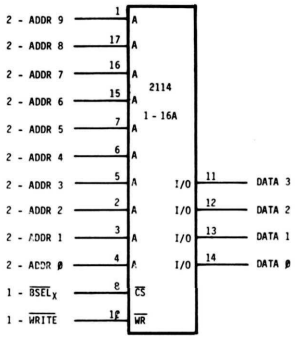
If the STROBE switch is left in the ON position and the system does generate MWRITE, unpredictable results could occur. Likewise if the system does not generate MWRITE and the switch is left in the OFF position, the same type of results could be expected.

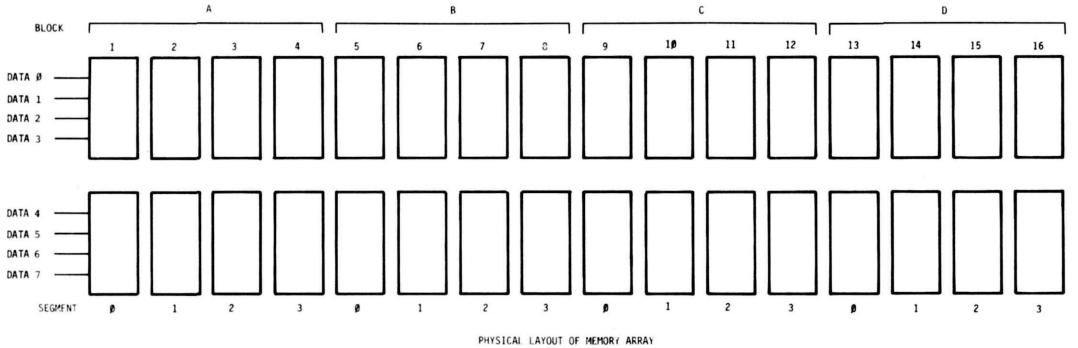


TYPICAL OF 16 PAIRS OF 2114 MEMORY CHIPS

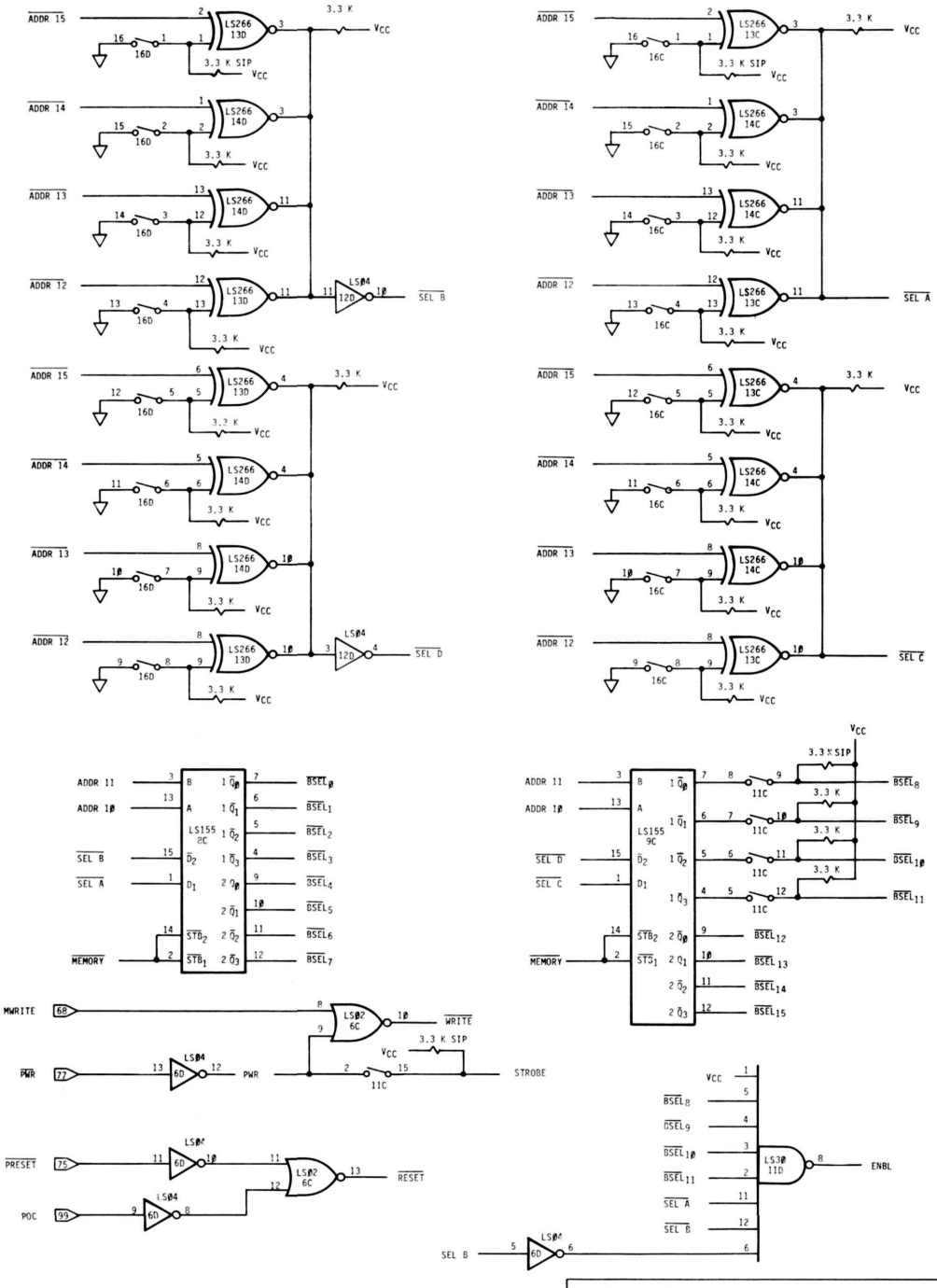


BSEL$_X$ ORIGINATES ON PAGE 1 FROM DECODERS 8C & 9C WHERE X HAS VALUES 0,1, ... 14,15





PHYSICAL LAYOUT OF MEMORY ARRAY



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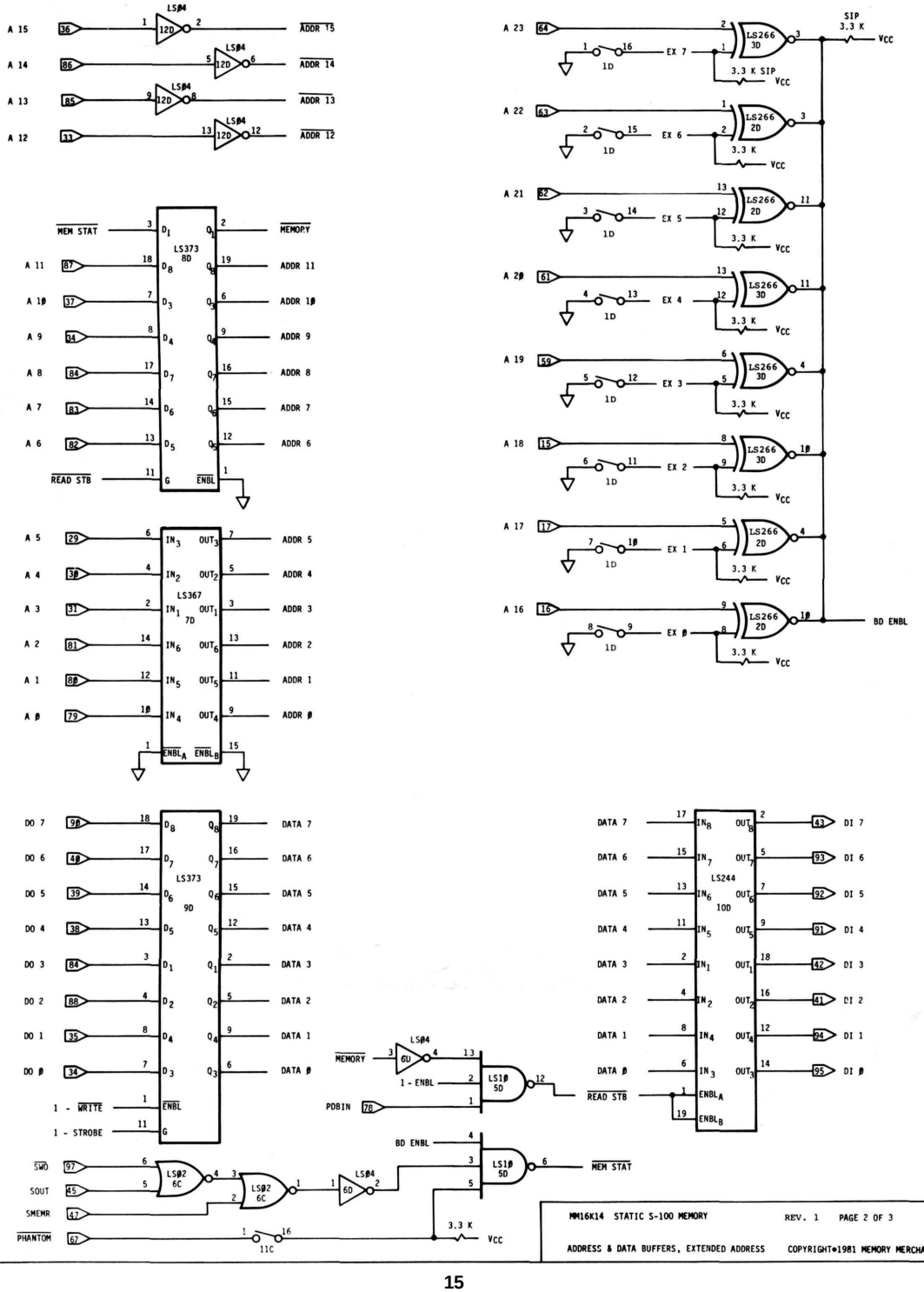

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ADDRESS & DATA BUFFERS, EXTENDED ADDRESS

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