LOMAS DATA PRODUCTS, INC.

LDP72 OWNER'S MANUAL

REV. 0

PROPRIETARY NOTICE

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Tech. Support
"hardware" : Luis

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1.0 GENERAL INFORMATION

1.1 Introduction

The LDP72 has been designed to take advantage of the newest technology available in a floppy disk controller (FDC). The FDC used by the LDP72 offloads the processor of many functions previously handled by the processor. The LDP72 is designed to work in an interrupt driven system or through a polling approach which simulates DMA transfers to and from the FDC. While servicing data requests from the FDC, the processor must respond in 32 us normally or 29 us worst case in single density mode or 16 us normally and 13 us worst case in double density mode when using standard 8" floppies. The LDP72 provides IBM compatible formats in both single and double density modes. Sector lengths may be programmed to be 128, 256, 512, or 1024 byte lengths. Additionally, non-IBM standard record lengths of 2048, 4096, or 8192 may be programmed. The use of 8192 byte block lengths provide a 23% increase in storage capacity over block lengths of 256 bytes. This advantage may be utilized in hard disk backup systems. The LDP72 provides the capability of transferring multiple sectors on the same sector without multiple command phases. This capability saves considerable time in multi-sector transfers and eliminates the need for sector interleaving. The LDP72 may also transfer data from multiple tracks on a double sided drive further improving system throughput. Using only one command, the LDP72 may transfer up to 16,384 bytes of data.

The LDP72 may control up to four disk drives which may be any mixture of standard of mini floppy drives. Software may select either mini or standard drives as well as select between single and double density modes. The same drive may be used in single and double density modes under software control.

The LDP72 uses the IEEE S100 Bus standard interface and conforms to all timing, signals and physical specifications of the IEEE spec.

1.2 Specification

1.2.1 Bus Interface

The LDP72 uses the signals and timing specified in the IEEE S100 Bus standard. See Table 1.1.

1.2.2 Addressing

The LDP72 uses 4 I/O address which may be selected on any

TABLE 1.1

S100 Bus Signals Required

A0 thru A7	Required for masters that use a 256 port I/O space
A8 thru A15	Required for masters that use a 64K port I/O space
DOØ thru DO7	Data lines from processor
DIØ thru DI7	Data lines to processor
SLAVE CLR*	Reset for board initialization
SOUT	Output Status
SINP	Input Status
pDBIN	Input Data Enable
pWR*	Output Data Strobe
UIØ thru U17	Vector Inputs
INT	Interrupt for masters without vectored interrupts
READY	Processor synchronization with read data
GND	Voltage Common
8V	Unregulated Voltage Input

boundry divisable by 4. The address may be an 8 bit address in the range of 0 to FB_H as the starting address. Alternately, the I/O address may be in the range $FFØØ_H$ to $FFFB_H$ for systems using a 16 bit address for I/O devices.

1.2.3 Data Synchronization

1.2.3.1 Interrupt Synchronization

The LDP72 may be programmed to generate an Interrupt for each data transfer to or from the FDC during the execution phase of the FDC command. Interrupts must be serviced in 33 us worst case for single density operation or 13 us worst case for double density operation.

1.2.3.2 Ready Line Synchronization

The FDC is programmed to operate in DMA mode. The processor then reads the port at BASE+Ø. The FDC causes the processor to insert wait states until either a DMA request is made or an interrupt request is generated by the FDC. The Interrupt Request and Service Request lines are input during this operation. The INTERRUPT signal is Bit Ø and Data Request Signal is Bit 1.

1.2.4 Floppy Disk Interface Signals

1.2.4.1 FDC to Standard Floppy Signals

See Table 1.2 for Standard Floppy interface signals.

1.2.4.2 FDC to Mini Floppy Signals

See Table 1.3 for mini floppy interface signals.

TABLE 1.2

J1 - Standard Floppy

Pin No.	Function
2	Low Current
4	Fault Reset
6	Fault
8	Not Used
10	Two-Sided
12	Not Used
14	Side Select
16	Special Function Ø
18	Head Load Ø
20	Index
22	Ready
24	Head Load 1
26	Drive Select Ø
28	Drive Select 1
30	Drive Select 2
32	Drive Select 3
34	Direction
36	Step
38	WR Data
40	WR Enable
42	Track Ø
44	WR Protect
46	RD Data
48	Head Load 2
50	Head Load 3

TABLE 1.3

J2 - Mini-Floppy

Pin No.	Function
2	Not Used
4	Not Used
6	Ready
8	Index
10	Drive Select Ø
12	Drive Select 1
14	Drive Select 2
16	Motor On 2
18	Direction
20	Step
22	WR Data
24	WR Enable
26	Track Ø
28	WR Protect
30	RD Data
32	Side Select
34	Two-Sided

2.0 PREPARATION FOR USE

2.1 Introduction

This section provides instructions for preparing the LDP72 for use in the particular user environment. Before the LDP72 is installed, the user should be familiar with this entire manual.

2.2 Unpacking and Inspection

Inspect the shipping carton immediately upon receipt for evidence of damage during shipment. If the carton is damaged when received, open the carton in the presence of the carrier's agent. If the carrier's agent is not present, save the packing carton for inspection of the carrier. The LDP72 is shipped insured to prepaid customers. Any damage incurred during shipment is covered by this insurance. In addition assembled and tested boards are warranteed for 30 days. If repairs are required, return the LDP72 in a suitable package to:

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It is suggested that the original packaging carton and material be saved in the event service should be required.

2.3 Installation Considerations

The LDP72 is designed to be IEEE S100 Bus compatible. Be aware that pins 20, 53 and 70 are used for Ground. If these grounds conflict with other uses of these pins, they may be cut at the edge connector without adversely affecting its operation.

2.4 User Furnished Components

The user must provide the cable from the floppy disk controller to the floppy disk drives. Assembled and tested boards and full kits contain all other necessary components. Partial kits include only the necessary documentation, the P.C. board and the 8272 floppy disk controller I.C.

2.5 Power Requirements

The LDP72 requires .75 amps at 8 Volts only.

2.6 Cooling Requirements

The LDP72 dissipates 6 Watts of power. When the LDP72 is

used in an enclosure that restricts normal airflow, sufficient cooling should be provided to prevent the temperature within the enclosure from exceeding 50°C.

2.7 Jumper Installations

When shipped, the LDP72 is jumpered for operation with up to 4 Shugart 800 drives, operated in single density mode. Data transfers are accomplished through READY line synchronization. No interrupts are connected, and the board is jumpered to respond to 8 bit addresses. See Table 2.1 for a list of jumpers and their purpose.

2.8 Board Installation

Always turn off the computer system power before inserting the board in the card cage.

TABLE 2.1

Jumper	Function
VI 1 through VI 8	Generates an interrupt request on the selected vectored interrupt line.
INT	Generates an interrupt on the INT line for processors without vectored interrupts.
A	When installed, 16 bit address are decoded for I/O instruction.
B	When installed, only the low order 8 bits are used for the decode of I/O addresses.
C	Installed to use ready line synchronization of data transfers.
D,E,F	Not used.
G	When installed without H causes mini drives to be selected after a reset.
H	When installed without G causes standard drives to be selected after a reset.
J	Enables the READY signal from the FDD to the FDC.
K	When both J and K are installed, the drive READY signal is always asserted.
L	When installed, enables the two sided signal from the FDD to the FDC.
M	When installed, enables the FAULT RESET signal to the FDC.
N	Enables the HEAD LOAD Ø signal.
P	Enables the HEAD LOAD 1 signal.
R	Enables the HEAD LOAD 2 signal.
S	Enables the HEAD LOAD 3 signal.

3.0 PROGRAMMING INFORMATION

3.1 Introduction

This section provides the necessary programming information for the user to develop device drivers for the LDP72. The primary emphasis will be on the features unique to the LDP72. The 8272 spec sheet is included in Appendix A and provides the information necessary to program the 8272 FDC.

3.2 I/O Addressing

The following table lists the I/O address of the 4 ports on the board along with their function.

TABLE 3.1

Address		Function
BASE+0	Write:	External control port
	Read:	Ready Synchronization and Status
BASE+1	Write:	Data to be written on the floppy disk
	Read:	Data recovered from the floppy disk
BASE+2	Write:	Not allowed
	Read:	8272 Status Register
BASE+3	Write:	Command and parameters to the 8272. In the interrupt mode Data is also written to this port.
	Read:	Result bytes from 8272 or data in the interrupt mode

3.2.1 External Control Port

The external control port has several functions. The FDC transfers multiple sectors from the disk beginning at the specified sector and continuing until the end of the track. Transfers may be terminated by asserting the TC signal to the FDC. This is accomplished by writing a value of 4ØH to BASE+Ø. When data bit 4 is a Ø, then data may be written to the external 4 bit latch. Data bit Ø asserts the MOTOR ON Ø signal for mini drives, it may alternately be used on standard floppies to provide special functions.

Writing a 1 to bit Ø with bit 4 clear asserts the MOTOR ON Ø signal.

Data bit 1 is used to assert the MOTOR ON 1 signal which may be used to provide separate motor control to a second floppy disk. The signal may also be used on standard floppy disks to provide a second special function. A 1 written to bit 1 asserts this function.

Data bit 2 is the wait enable bit. When asserted by writing a 1 to it, a read to Base+Ø causes wait states to be inserted until there is a data request (SERVREQ) from the FDC or Interrupt (INT) is asserted by the FDC denoting that the command has terminated. When disabled, no wait states are generated when Base+Ø is read.

Data bit 3 selects between standard and mini floppies. This allows the selection of drive type to be accomplished under program control. When jumpered as shipped, (Jumper H installed) a Ø selects standard drives and a 1 selects mini drives. If Jumper G is installed, the meaning is reversed. A reset causes standard drives to be selected when Jumper G is installed and mini drives to be selected when Jumper H is installed.

When read, data bit 0 represents the state of the 8272 Interrupt signal (a 1 is asserted) and data bit 1 represents the state of the DRQ signal from the 8272, again a 1 is asserted. If the wait Flip Flop is enabled, wait states are inserted until either DRQ or INT are asserted. A watch guard timer is used to prevent wait states from being inserted for more than 100 ms. When a read is done from BASE+Ø and the wait Flip Flop is enabled and the two low order bits are Ø's when tested, the expiration of the timer is indicated.

3.2.2 Data Port

A read or write to this port causes the FDC DACK signal to be asserted simulating DMA cycles to the FDC. This port is used when ready line synchronization is used to synchronize data transfers to and from the FDC.

3.2.3 FDC Status Port

The FDC Status Port address is BASE+2 and is a read only port. The meaning of the bits are defined in the 8272 spec sheet in Appendix A.

3.2.4 FDC Command/Data Port

The command/data port is addressed at BASE+3. Commands are

written to this port and results are read from this port. Before data may be written to or read from the command/ data port, the status from the Status Port must be tested to ascertain whether the FDC is ready for a data transfer. Bit 7 of the status register must be a 1 before transfers may take place. Bit 6 of the status register indicates the direction of the transfer the FDC expects. A Ø indicates the FDC expects data from the processor and a 1 indicates that the FDC expects to transfer data to the processor. When the FDC is programmed to the transfer data read and written from/to the floppy drive by interrupts data is read from or written to this port.

3.3 FDC Commands

See Appendix A for a description of the commands executable by the FDC.

4.0 PRINCIPLES OF OPERATION

4.1 This chapter provides a functional description of the LDP72 Floppy Disk Controller. Figure 4.1 is a block diagram of the LDP72. In addition, the reader should have the schematic of the LDP72 which was shipped with the LDP72.

4.2 Functional Blocks

The following are the functional blocks of the LDP72:

Data Buffers
Address Decoders
Ready Line Synchronizer
External Port
FDC
Data Separator
Write Compensation

4.3 Data Buffers

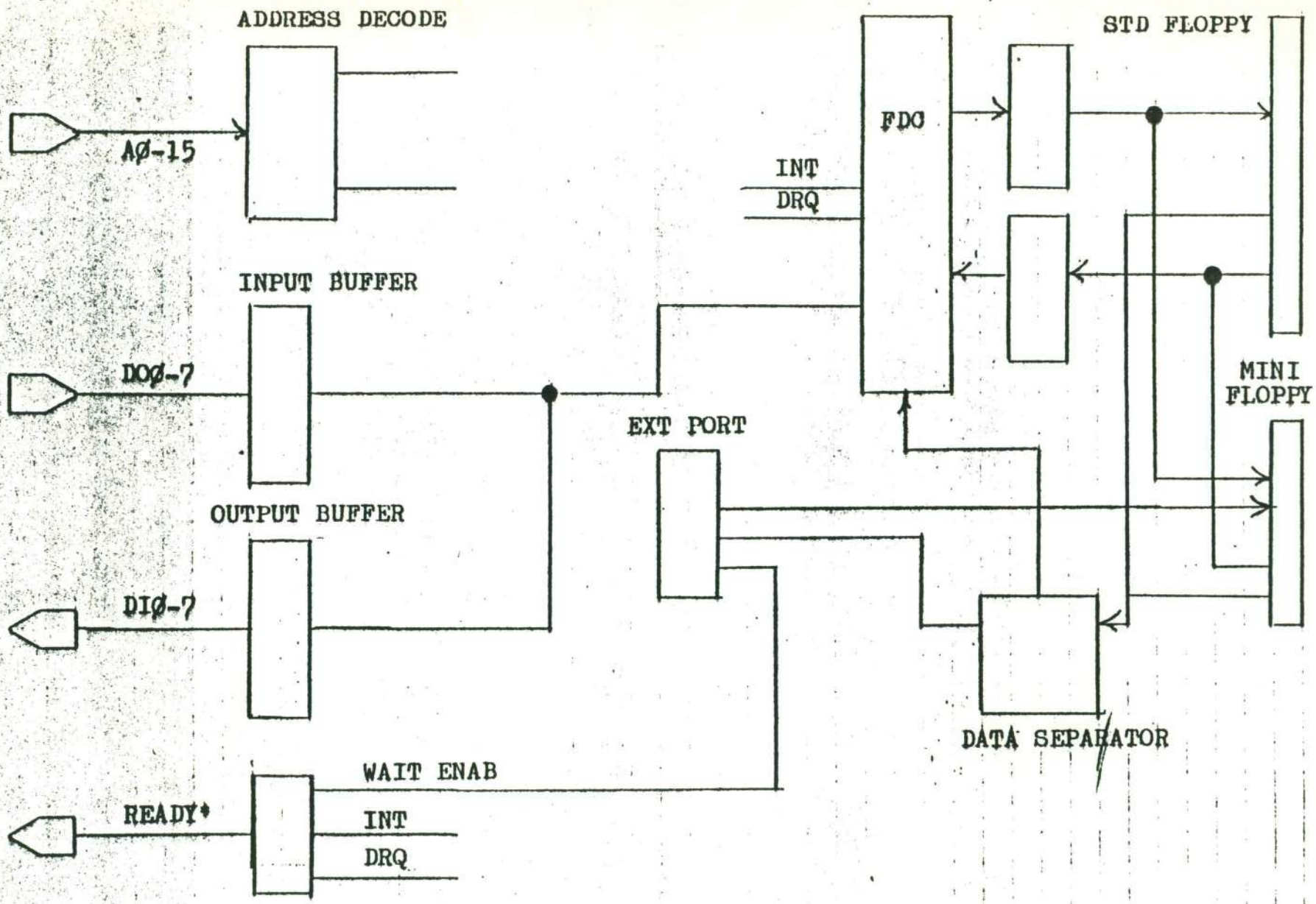
A pair of 74LS244's are used to buffer the data bus to and from the board. The data bus is bi-directional on the board and U29 buffers the data from the DO bus and U3Ø buffers the data to the DI bus.

4.4 Address Decoding

The high order eight address bits are ANDed together and input to one of a group of 8 Open Collector XNOR gates used as a comparator. If a system is not using 64K I/O address space, the input from the high order eight bits may be disabled by installing Jumper B. The eight position dip switch, positions 3 through 8 are used as the other inputs to the comparator. When the selected port address is decoded SLCT is asserted high enabling a 3 line to 8 line decoder. The two select lines for BASE+2 and BASE+3 are ORed together to provide the chip select for the FDC.

4.5 Ready Data Synchronization

With Jumper C installed, data transfers to and from the FDC are synchronized by inserting wait states when port BASE+Ø is accessed for input. The insertion of wait states is terminated when either INT or SERVREQ are asserted. SERVREQ indicates that the FDC is ready for a data transfer and INT indicates the termination of the command in progress. In order to insert wait states, the wait enable flip flop U17 pin 14 must be enabled and the one shot U12 must not have timed out. U12 prevents the FDC from causing the suspension of bus activity for more than 100 ms



LDP72 BLOCK DIAGRAM

in the case of a hardware malfunction.

4.6 External Control Port

The port at BASE+Ø provides two additional signals for the control of floppy drives, enables the switching between single and double density drives and enables the Ready line data synchronization circuit. The Register, U17, accepts data from the low 4 data bits when bit 4 is a Ø. Writing to BASE+Ø with bit 4 equal to a 1 does not affect the data already in the register. A Write to BASE+Ø with bit 4 set and bit 7 equal to a zero causes a TC pulse to be issued to the FDC. This causes the FDC to terminate the command it is presently executing. All data reads and writes are multisector operations. If only one sector or a number of sectors less than those remaining on the track are to be read, a TC pulse causes the termination of data transfers after the desired number of bytes are read. (See Appendix A).

When a disk transfer operation is complete, the WAIT flip flop may be disabled and a TC pulse issued with one output instruction with the data equal to Ø.

4.7 Floppy Disk Controller

A detailed description of the 8272 FDC may be found in Appendix A.

4.8 Data Separator

The Data Separator is a synchronous counter data recovery circuit. The circuit is made up of U31 and U9. The synchronous counter circuit consists of a binary counter which is preloaded with a fixed value on each read pulse from the drive. The counters output, FDCRDW, is the data window signal to the 8272. The two flip flops of U9 merely synchronize the data from the drive to the clock provided by U19. The clock frequency depends on whether the drives are single or double density and whether they are standard or mini-drives. For double density 8" drives, the clock is 8 MHz, for 8" single density drives, the clock is 4 MHz, for double density 5 1/4" drives, the clock is 2 MHz and for single density 5 1/4" drives the clock is 1 MHz. U9 pin 8 controls the width of the Sync pulse so that it overlaps only one positive edge of the clock (see Figure 4.1 for circuit timing).

The VCO Sync signal, VCO, from the 8272 ingibits the read data and data window signals from being generated until valid information is detected from the drive. It also

masks out write current glitches which would otherwise appear on each side of the data field.

4.9 Write Compensation

Write precompensation is performed by a combination of the 8272 FDC, U32 and U33. The FDC outputs FDCPS1 and FDCPS2 to select the write precompensation required.

5.0 DISK DRIVE CONSIDERATIONS

5.1 Seek Operations

In order for disk seeks to function properly, the power to the stepper motor must not be gated by the drive select signal. This is required because the 8272 allows seek operations to happen in parallel on multiple drives and the drive select status is valid only during the step pulse and not during the whole time necessary for the step movement to occur.

5.2 Mini Floppy Drives

Not all mini drives provide a READY status signal to the FDC. If your mini drive does not provide this signal, install both Jumpers J and K to keep the READY status to the FDC asserted. The issueing of a command to the 8272 controller without the drive being ready may cause the 8272 to hang up until a reset occurs. When keeping the READY status signal low, be certain the drive is in a ready state when use is expected or results will be unexpected.

6.0 SERVICING

Table 6.1 is a complete list of replaceable parts for the LDP72. Should your board require service, it should be packaged in the original container or in another container of suitable strength and shipped to:

LOMAS DATA PRODUCTS
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MARLBORO MA 01752

To obtain technical assistance for board repair and to obtain our latest repair rates, call (617) 366-4335 during normal working hours of 8:30 to 5:00 Monday through Friday.

LDP72 PARTS LIST

IC's

74LS155	U1
7407	U2, U3, U4
74LS240	U5
74LS14	U6, U24
8272	U7
74LS74	U8,
74LS04	U10, U18, U22
74LS125	U11
74LS123	U12
74LS32	U13
74LS08	U14
74LS138	U15
74LS32	U16
74LS175	U17, U32
74LS157	U19, U20
7406	U23
8 position switch	U25
74LS266	U26, U27
74LS30	U28
74LS244	U29, U30
74LS161	U21,
74LS153	U33
9216B	U34

CAPACITORS

22 uf	15V or greater	C1
.1 uf	6V or greater	C3 thru C12, C13 thru C34
22 uf	6V or greater	C2

RESISTORS

1K	1/4 w 5%	R1, R7, R8 , R3, R4
150	1/4 w 5%	R2
390	1/4 w 5%	R3, R4, R6
100K	1/4 w 5%	R5
270	8 pin SIP	RN1
1K	8 pin SIP	RN2

MISCELLANEOUS

Connector Ansley 50 pin right angle	J1
Connector Ansley 34 pin right angle	J2
Heat Sink Thermalloy #6071	
Heat Sink Thermalloy #6072	
Screw 4-32 3/8"	
Nut 4-32	
Washer 4-32 Lock Washer	
Crystal 8.00 MHz	Y1
Regulator 7805	Q1

intel

PRELIMINARY

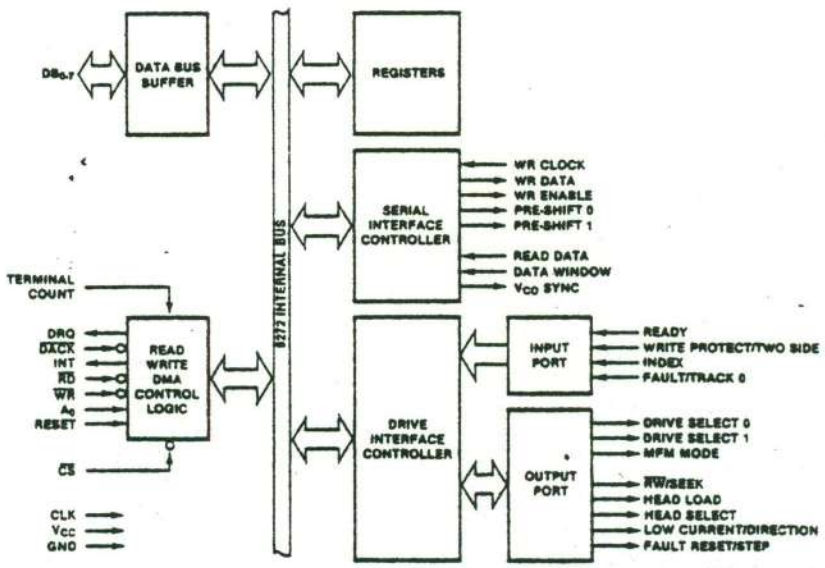
8272
SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability — Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, 8086 and 8088
- Single-Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40-Pin Plastic Dual-in-Line Package

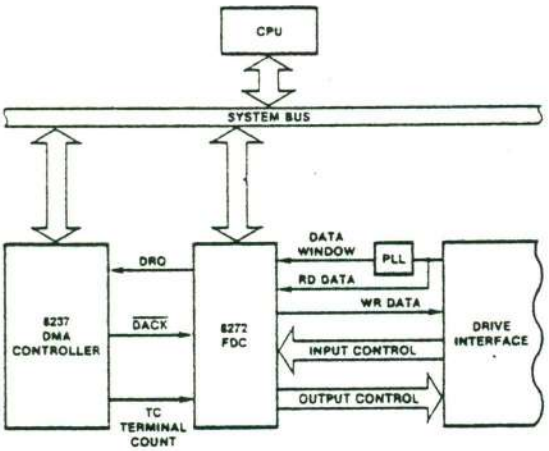
The 8272 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The 8272 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive Interface.

PIN CONFIGURATION

8272 INTERNAL BLOCK DIAGRAM



8272 SYSTEM BLOCK DIAGRAM



DESCRIPTION

Hand-shaking signals are provided in the 8272 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the 8237. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor for every transfer of a data byte between the CPU and the 8272. In the DMA mode, the processor need only load a command into the FDC and all data transfers occur under control of the 8272 and DMA controller.

There are 15 separate commands which the 8272 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available.

- Read Data
- Read ID
- Read Deleted Data
- Read a Track
- Scan Equal
- Scan High or Equal
- Scan Low or Equal
- Specify
- Write Data
- Format a Track
- Write Deleted Data
- Seek
- Recalibrate (Restore to Track 0)
- Sense Interrupt Status
- Sense Drive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The 8272 offers many additional features such as multiple sector transfers in both read and write modes with a single command, and full IBM compatibility in both single (FM) and double density (MFM) modes.

8272 REGISTERS — CPU INTERFACE

The 8272 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and 8272.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode.
DB_4	FDC Busy	CB	A read or write command is in process.
DB_5	Non-DMA mode	NDM	The FDC is in the non-DMA mode. This bit is set only during the execution phase in non-DMA mode. Transition to "0" state indicates execution phase has ended.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

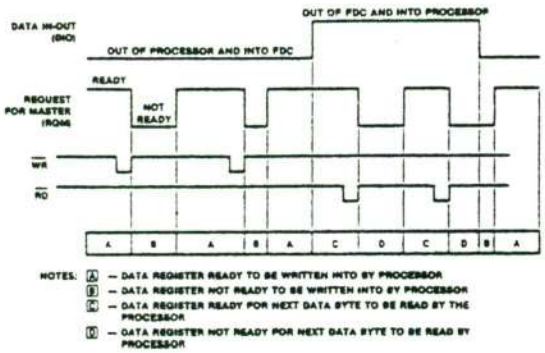
PIN DESCRIPTION

PIN NO.	PIN SYMBOL	I/O	CONNECTION TO	DESCRIPTION
1	RST	I	µP	Reset: Places FDC in idle state. Resets output lines to FDD to "0" (low)
2	$\overline{RD}$	I[1]	µP	Read: Control signal for transfer of data from FDC to Data Bus, when "0" (low)
3	$\overline{WR}$	I[1]	µP	Write: Control signal for transfer of data to FDC via Data Bus, when "0" (low)
4	$\overline{CS}$	I	µP	Chip Select: IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled
5	A_0	I[1]	µP	Data/Status Reg Select: Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) content be sent to Data Bus
6-13	DB_0-DB_7	I/O[1]	µP	Data Bus: Bidirectional 8-Bit Data Bus
14	DRQ	O	DMA	Data DMA Request: DMA Request is being made by FDC when DRQ "1"
15	$\overline{DACK}$	I	DMA	DMA Acknowledge: DMA cycle is active when "0" (low) and Controller is performing DMA transfer
16	TC	I	DMA	Terminal Count: Indicates the termination of a DMA transfer when "1" (high)
17	IDX	I	FDD	Index: Indicates the beginning of a disk track
18	INT	O	µP	Interrupt: Interrupt Request Generated by FDC
19	CLK	I		Clock: Single Phase 8 MHz Squarewave Clock
20	GND			Ground: D.C. Power Return

Note 1: Disabled when $\overline{CS}$ = 1.

PIN NO.	PIN SYMBOL	I/O	CONNECTION TO	DESCRIPTION
40	V_{CC}			D.C. POWER +5V
39	$\overline{RW}$/SEEK	O	FDD	Read Write/SEEK: When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected
38	LCT/DIR	O	FDD	Low Current/Direction: Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode
37	FR/STP	O	FDD	Fault Reset/Step: Resets fault FF in FDD in Read/Write mode, provides step pulses to move head to another cylinder in Seek mode
36	HDL	O	FDD	Head Load: Command which causes read/write head in FDD to contact diskette
35	RDY	I	FDD	Ready: Indicates FDD is ready to send or receive data
34	WP/TS	I	FDD	Write Protect/Two-Side: Senses Write Protect status in Read/Write mode, and Two Side Media in Seek mode
33	FLT/TRK0	I	FDD	Fault/Track 0: Senses FDD fault condition in Read/Write mode and Track 0 condition in Seek mode.
31,32	PS_1,PS_0	O	FDD	Precompensation (pre-shift): Write precompensation status during MFM mode. Determines early, late, and normal times.
30	WR DATA	O	FDD	Write Data: Serial clock and data bits to FDD
28,29	DS_1,DS_0	O	FDD	Drive Select: Selects FDD unit
27	HDSEL	O	FDD	Head Select: Head 1 selected when "1" (high) Head 0 selected when "0" (low)
26	MFM	O	PLL	MFM Mode: MFM mode when "1", FM mode when "0"
25	WE	O	FDD	Write Enable: Enables write data into FDD
24	VCO	O	PLL	VCO Sync: Inhibits VCO in PLL when "0" (low), enables VCO when "1"
23	RD DATA	I	FDD	Read Data: Read data from FDD, containing clock and data bits
22	DW	I	PLL	Data Window: Generated by PLL, and used to sample data from FDD
21	WR CLK	I		Write Clock: Write data rate to FDD FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM Must be enabled for all operations, both Read and Write

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus.



STATUS REGISTER TIMING

The 8272 is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the 8272 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the 8272. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the 8272. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the 8272 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the 8272 is in the Non-DMA Mode, then the receipt of each data byte (if 8272 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. For example, if the processor cannot handle interrupts fast enough (every 13 μs for MFM mode) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

If the 8272 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The 8272 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The 8272 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The 8272 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the 8272 to form the Command Phase, and are read out of the 8272 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the 8272 the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the 8272 is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the 8272's attention even if the disk system hangs up in an abnormal manner.

POLLING FEATURE OF THE 8272

After the Specify command has been sent to the 8272, the Drive Select Lines DS0 and DS1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the 8272 polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the 8272 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the 8272 occurs continuously between instructions, thus notifying the processor which drives are on or off line.

TABLE 1. 8272 COMMAND SET

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MFM	SK	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information during Execution Phase
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: 1. Symbols used in this table are described at the end of this section.

2. A_0 = 1 for all operations.

3. X = Don't care, usually made to equal binary 0.

TABLE 1. COMMAND SET (Continued)

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID information prior Command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data compared between the FDD and main-system
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after Command execution
	R				H					
	R				R					
	R				N					
SCAN HIGH OR EQUAL										
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID information prior Command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				STP					
Execution										Data compared between the FDD and main-system
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after Command execution
	R				H					
	R				R					
	R				N					

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R					ST 0				Status information at the end of each seek operation about the FDC
	R					PCN				
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W			SRT				HUT		
	W			HLT					ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R					ST 3				Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W					NCN				
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W					Invalid Codes				Invalid Command Codes (NoOp — FDC goes into Standby State)
Result	R					ST 0				ST 0 = 80 (16)

TABLE 2. COMMAND MNEMONICS

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register ($A_0 = 0$) or Data Register ($A_0 = 1$).
C	Cylinder Number	C stands for the current selected Cylinder track number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus where D_7 is the most significant bit, and D_0 is the least significant bit.
DS0, DS1	Drive Select	DS stands for a selected drive number 0 or 1.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number of a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HDS	Head Select	HDS stands for a selected head number 0 or 1 (H = HDS in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MFM	FM or MFM Mode	If MF is low, FM mode is selected and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed (a cylinder under both HD0 and HD1 will be read or written).
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). The same Stepping Rate applies to all drives (F=1 ms, E=2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.

COMMAND DESCRIPTIONS

During the Command Phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (DB6) and RQM (DB7) bits in the Main Status Register must be in the "0" and "1" states respectively, before each byte of the command may be written into the 8272. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to "1" and "0" states respectively.

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 3 below shows the Transfer Capacity.

TABLE 3. TRANSFER CAPACITY

Multi-Track MT	MFM/FM MFM	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to 0FFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM Mode, and every 13 µs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 4 shows the values for C, H, R, and N, when the processor terminates the Command.

TABLE 4. ID INFORMATION WHEN PROCESSOR TERMINATES COMMAND

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.

2. LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same; refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag

- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command.

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high) and the command is terminated.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the 8272 for each sector on the track. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 5 shows the relationship between N, SC, and GPL for various sector sizes:

TABLE 5. SECTOR SIZE RELATIONSHIPS

FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2]	REMARKS
FM Mode	128 bytes/Sector	00	$1A_{(16)}$	$07_{(16)}$	$1B_{(16)}$	IBM Diskette 1
	256	01	$0F_{(16)}$	$0E_{(16)}$	$2A_{(16)}$	IBM Diskette 2
	512	02	08	$1B_{(16)}$	$3A_{(16)}$	
FM Mode	1024 bytes/Sector	03	04	—	—	
	2048	04	02	—	—	
	4096	05	01	—	—	
MFM Mode	256	01	$1A_{(16)}$	$0E_{(16)}$	$36_{(16)}$	IBM Diskette 2D
	512	02	$0F_{(16)}$	$1B_{(16)}$	$54_{(16)}$	
	1024	03	08	$35_{(16)}$	$74_{(16)}$	IBM Diskette 2D
	2048	04	04	—	—	
	4096	05	02	—	—	
	8192	06	01	—	—	

Note: 1. Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

2. Suggested values of GPL in format command.

RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

TABLE 7. SEEK, INTERRUPT CODES

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms .... OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms .... FE = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the 8272 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the 8272 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find a 80H indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

(duplicate page)

TABLE 8. STATUS REGISTERS

BIT NO.	NAME	SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command Issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of SCAN.

TABLE 6. SCAN STATUS CODES

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors STP = 01, or alternate sectors STP = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC terminates the command.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and performs the following operation if there is a difference:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

TABLE 8. STATUS REGISTERS

BIT NO.	NAME	SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command Issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a
D_0	Unit Select 0	US 0	Drive Unit Number at Interrupt
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

BIT NO.	NAME	SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −10°C to +70°C
Storage Temperature ..... −40°C to +125°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage V_{CC} ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

*T_A = 25°C

COMMENT: *Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%

SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
V_{IL_1}	Input Low Voltage	−0.5	0.8	V	
V_{IH_1}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{IL_2}	(CLK & WR CLK)	−0.5	0.65	V	
V_{IH_2}	(CLK & WR CLK)	2.4	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −200 μA
I_{CC}	V_{CC} Supply Current		150	mA	
I_{IL}	Input Load Current (All Input Pins)		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0V
I_{LOH}	High Level Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{LOL}	Low Level Output Leakage Current		−10	μA	V_{OUT} = +0.45V

CAPACITANCE

T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V

SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX		
$C_{IN(\Phi)}$	Clock Input Capacitance		20	pF	All Pins Except Pin Under Test Tied to AC Ground
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		20	pF	

A.C. CHARACTERISTICS

t_A = 0°C to 70°C, V_{CC} = +5.0V ± 5%

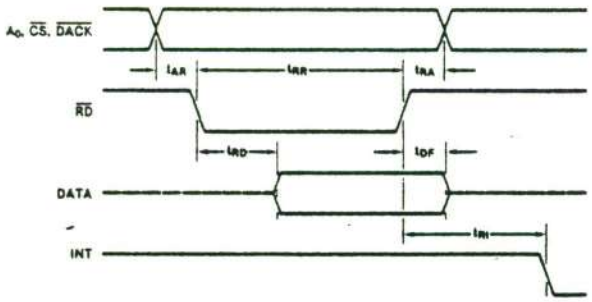
SYMBOL	PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS
t_{CY}	Clock Period		125		ns	
t_{CH}	Clock High Period		40		ns	Note 4
t_{RST}	Reset Width		14		t_{CY}	
Read Cycle						
t_{AR}	Select Setup to $\overline{RD}\downarrow$		0		ns	
t_{RA}	Select Hold from $\overline{RD}\uparrow$		0		ns	
t_{RR}	$\overline{RD}$ Pulse Width		250		ns	
t_{RD}	Data Delay from $\overline{RD}\downarrow$			200	ns	C_L = 100 pF
t_{DF}	Output Float Delay		20	100	ns	C_L = 100 pF
Write Cycle						
t_{AW}	Select Setup to $\overline{WR}\downarrow$		0		ns	
t_{WA}	Select Hold from $\overline{WR}\uparrow$		0		ns	
t_{WW}	$\overline{WR}$ Pulse Width		250		ns	
t_{DW}	Data Setup to $\overline{WR}\uparrow$		150		ns	
t_{WD}	Data Hold from $\overline{WR}\uparrow$		5		ns	
Interrupts						
t_{RI}	INT Delay from $\overline{RD}\uparrow$			500	ns	
t_{WI}	INT Delay from $\overline{WR}\uparrow$			500	ns	
DMA						
t_{ROCY}	DRQ Cycle Period		13		µs	
t_{AKRQ}	$\overline{DACK}\downarrow$ to DRQ↓			200	ns	
t_{RQR}	DRQ↑ to $\overline{RD}\downarrow$		800		ns	8 MHz clock
t_{RQW}	DRQ↑ to $\overline{WR}\downarrow$		250		ns	8 MHz clock
t_{RQRW}	DRQ↑ to $\overline{RD}\uparrow$ or $\overline{WR}\uparrow$			12	µs	8 MHz clock
FDD Interface		TYP 1				
t_{WCY}	WCK Cycle Time	2 or 4			µs	MFM = 0 Note 2
		1 or 2				MFM = 1
t_{WCH}	WCK High Time	250	80	350	ns	
t_{CP}	Pre-Shift Delay from WCK↑		20	100	ns	
t_{CD}	WDA Delay from WCK↑		20	100	ns	
t_{WDD}	Write Data Width		t_{WCH} − 50		ns	
t_{WE}	WE↑ to WCK↑ or WE↓ to WCK↓ Delay		20	100	ns	
t_{WWCY}	Window Cycle Time	2			µs	MFM = 0
		1				MFM = 1
t_{WRD}	Window Setup to RDD↑		15		ns	
t_{RDW}	Window Hold from RDD↓		15		ns	
t_{RDD}	RDD Active Time (HIGH)		40		ns	
FDD SEEK/ DIRECTION/ STEP						
t_{US}	$US_{0,1}$ Setup to $\overline{RW}$/SEEK↑		12		µs	8 MHz clock
t_{SD}	$\overline{RW}$/SEEK Setup to LCT/DIR		6.8		µs	
t_{DS}	$\overline{RW}$/SEEK Hold from LCT/DIR		30		µs	
t_{DST}	LCT/DIR Setup to FR/STEP↑		1		µs	
t_{STD}	LCT/DIR Hold from FR/STEP↓		24		µs	
t_{STU}	$DS_{0,1}$ Hold from FR/Step↓		5		µs	
t_{STP}	STEP Active Time (High)	5			µs	
t_{SC}	STEP Cycle Time		33		µs	Note 3
t_{FR}	FAULT RESET Active Time (High)		8	10	µs	
t_{IDX}	INDEX Pulse Width	625			µs	
t_{TC}	Terminal Count Width		1		t_{CY}	

NOTES:

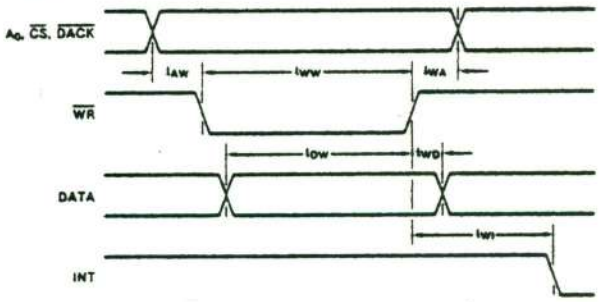
1. Typical values for T_A = 25°C and nominal supply voltage.
2. The former values are used for standard floppy and the latter values are used for mini-floppies.
3. t_{SC} = 33 µs min. is for different drive units. In the case of same unit, t_{SC} can be ranged from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
4. From 2.0V↑ to +2.0V↓.

TIMING WAVEFORMS

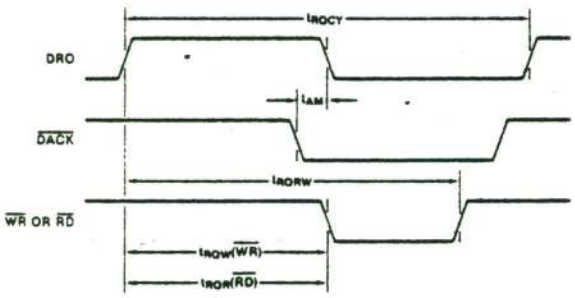
PROCESSOR READ OPERATION

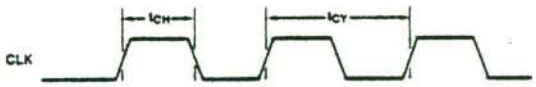


PROCESSOR WRITE OPERATION

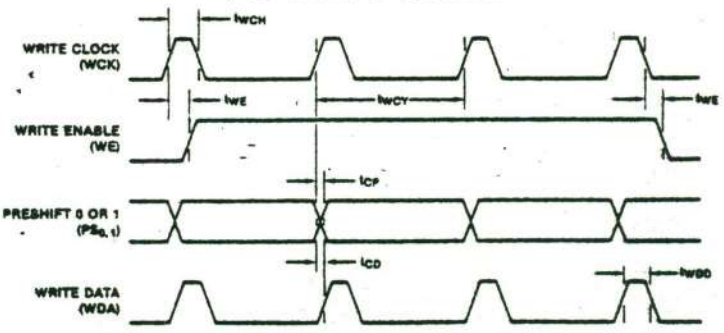


DMA OPERATION



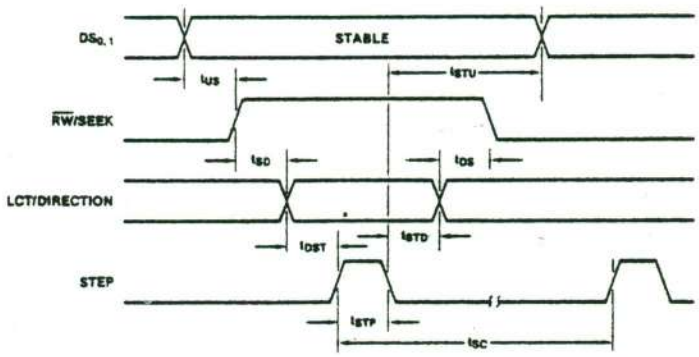


FDD WRITE OPERATION

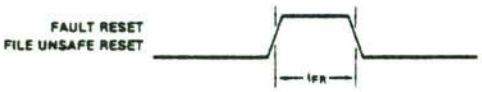


	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

SEEK OPERATION

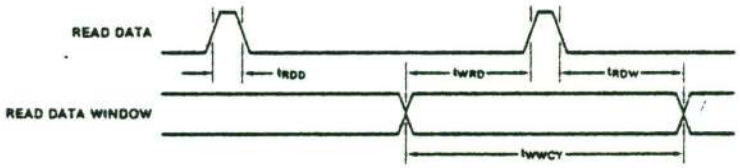


FLT RESET



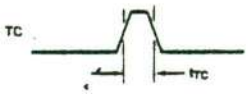
INDEX

FDD READ OPERATION

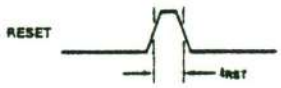


NOTE: EITHER POLARITY DATA WINDOW IS VALID.

TERMINAL COUNT



RESET



A.C. TIMING MEASUREMENT CONDITIONS

INPUT WAVEFORM

MEASUREMENT POINT
INPUT: 2.0V ≈ 0.8V
OUTPUT: 2.0V ≈ 0.8V

LDP72 REV 2 CHANGES

The data separator formed by U9 and U31 has been replaced by a SMC 9216B. U9 and U31 may still be used by removing U33 and installing U9 and U31. When U33 is installed, U9 and U31 should be removed. U33 provides increased jitter tollerance which allows better performance on the last few tracks.

DRIVE JUMPERING FOR LDP72

QUME DATA TRACK 8:

On Qume Data Track 8 drives, the mini jumpers should be installed and removed as shown below, and the DIP should be altered as specified.

Installed (C, 2S, DL, DSx) Removed (T4O, GND, DS, D, DC, Y HA)

Shunt: Cut HL and X, all others intact. Terminator resistors should be installed on the last drive of the cable.

SHUGART 800/801:

On a Shugart 800/801 drive, the following mini mumpers should be installed and removed on all drives:

Installed (T2, A, B, C, Z, 800) Removed (D, DC, X, Y, HL, DS)

Drive select (DSx) should be installed appropriately and the terminators T1, and T3-T6 should be installed on the last drive of the cable.

SHUGART 850/851:

On a Shugart 850/851 drive, the mini jumpers should be installed and removed as shown below and the DIP shunt should be altered as required.

Installed (C, 2S, S2, IW, RS, DL, IT, AF, M, 850)

Removed (FS, TS, Y, DS, HLL , HI, D, DC, NF)

Shunt: Cut HL and X, all others intact. Terminator resistors should be installed on the last drive of the cable.

SIEMENS MODEL FDD 100-8:

On Siemens Model D drives, the mini jumpers should be installed and removed as shown.

Installed (SS, SE, E, D, RR, O, 2, F, RI, L, U, H)

Removed (HS, 8, 16, 32, 1, TE, A, V, B, J, K, M, G)

The following modifications to the PC board are required for using two or more drives:

1. Remove the PC board and cut the trace leading to IC 6C Pin 9.
2. Connect IC 6C Pin 9 to IC 6C Pin 12 and reinstall the PC board.

MITSUBISHI M2894

Install E, Z, 2S, I, R, S2, D, ON, H.

Install the correct device select.

Remove any other shunts.

Cut PJ4 and PJ5.

NOTE: For more reliable operation, set your Thunder186 or LDP72 for 125 ns precomp.

TANDON 848

Install DC, 2S, S2, C, RR, RI, WP, M3.

Install the correct device select.

Remove any other shunts.

Cut HL and H.

NOTE: For more reliable operation, set your Thunder186 or LDP72 for 125ns precomp.

MITSUBISHI M2896

Install JFG, PS, SE, M2, S2, I, R, B, A, X, RS, HY, Z, WP, RFa, 2S.

Install the correct device select (DS).

Remove any other shunts.

NEC 1165

Install BS2, BU2, HD1, HL2, RX2, FR2, PR1, DR1, DH1, DL1, SS1, T1.

Install the correct device select (DX).

Remove any other shunts.

NOTE: C3-35 ARE .1μF
P1
J1
J2
U1 74LS155
U2 7407
U3 7407
U4 7407
U5 74LS240
U6 74LS14
U7 8272
U8 74LS74
U9 74LS157
U10 74LS04
U11 74LS125
U12 74LS123
U13 74LS32
U14 74LS08
U15 74LS138
U16 74LS32
U17 74LS175
U18 74LS04
U19 74LS157
U20 74LS157
U21 74LS161
U22 74LS04
U23 7406
U24 74LS14
U25 8 Pos. SW.
U26 74LS266
U27 74LS266
U28 74LS30
U29 74LS244
U30 74LS244
U31 74LS161
U32 74LS175
U33 74LS153
Q1 7805
Y1 8MHz
RN1
RN2 1K
R1 4.7K
R2 150Ω
R3 330Ω
R4 330Ω
R5 33K
R6 330Ω
R7 1K
R8 1K
C1 22μF
C2 10μF
SPARE
SPARE
INT

```
READ AND WRITE A SECTOR WITH THE LDP72.

READ:
        DO;
        RETRY=9 (RETRY NINE TIMES IF AN ERROR OCCURS)
TRY AGAIN:
        CALL SENSE (CLEAR ANY PENDING INTERRUPTS)
        CALL SEEK  (SEEK THE SPECIFIED TRACK)
        CALL WAIT FOR INTERRUPT
        CALL SENSE (CLEAR INTERRUPT JUST GENERATED)
        COMMAND=READ (SET COMMAND IN IO BLOCK TO READ)
        CALL OUTPUT IOP BLOCK
        CALL READ SECTOR
        CALL GET RESULTS
        CALL CHECK RESULTS
        IF NO ERRORS THEN RETURN ELSE
                DO
                RETRY=RETRY - 1
                IF RETRY = 0 THEN RETURN WITH  ERROR STATUS
                ENDDO
        ENDIF
        GO TO TRY AGAIN

SENSE:
( ISSUES A SENSE INTERRUPT COMMAND TO THE FDC TO CLEAR ANY PENDING INTERPUPTS)
        DO
        OUTPUT SENSE INTERRUPT COMMAND TO FDC
        GET FIRST RESULT BYTE
        GET SECOND RESULT BYTE
        RETURN
        ENDDO

WAIT FOR INTERRUPT:
        DO
        DISABLE WAIT FF
        INPUT FROM BASE + 0
        IF BIT 0=0 DO AGAIN
        ENDDO

READ:
(THIS IS A SAMPLE OF A POSSIBLE READ ROUTINE ENABLEING A PROCESSOR,
4MHZ Z80 OR 5MHZ 8085, TO READ A DOUBLE DENSITY DISK SECTOR)
        LXI     D,BUFFER        ;GET A POINTER TO THE INPUT BUFFER
                                ;WHICH MUST BE ON THE SECOND HALF OF A PAGE
                                ;BOUNDRY I.E. XX80H
        LXI     H,LOOP          ;POINTER TO REPEAT ADDRESS
        MVI     B,02H           ;CONSTANT FOR TESTING THE SERVICE REQUEST BIT
        MVI     A,84H           ;CONSTANT TO ENABLE THE WAIT FF
        OUT     BASE+0
LOOP:   IN      BASE+0          ;WAIT FOR SERVICE REQUEST OR INTERRUPT
        ANA     B               ;CHECK FOR SERVICE REQUEST
        JZ      DONE            ;IF NOT SERVICE REQUEST MUST BE INTERRUPT
                                ;SIGNIFYING THE COMPLETION OF READ
        IN      BASE+1          ;GET RECEIVED BYTE FROM FDC
        STAX    D               ;PUT IT IN MEMORY
        INR     E               ;INCREMENT POINTER AND BYTE COUNTER
                                ;IN THIS CASE A 128 BYTE COUNTER AS IN
                                ;IN SINGLE DENSITY MODE, FOR DOUBLE DENSITY
                                ;SET DE TO XX00H AND GET 256 BYTES.
        PCHL                    ;LOOP UNTIL INTERRUPT IS ASSERTED BY THE FDC
DONE:   RET
                                ;THE SERVICE LOOP REQUIRES 48 CLOCKS OR
                                ;12 US. IN A 4MHZ Z80 AND 9.6US IN A 5MHZ
                                ;8085
```

```
SEEK:
        DO
        OUTPUT SEEK COMMAND TO THE FDC
        OUTPUT THE FDD UNIT NUMBER TO THE FDC
        OUTPUT THE TRACK NUMBER TO THE FDC
        RETURN
        ENDDO

OUTPUT IOP BLOCK:
(THE IOP BLOCK IS 9 BYTES INCLUDING THE PARAMETERS REQUIRED TO START THE
FDC OPERATION. THE EOT BYTE SHOULD BE SET TO THE SECTOR FROM WHICH YOU ARE
REQUESTING DATA IN ORDER THAT THE FDC WILL GENERATE AN INTERRUPT WHEN THE
TRANSFER OF THE SECTOR IS COMPLETE. THE COMMAND BLOCK IS TREATED AS A
9 ELEMENT ARRAY)
        DO
        FOR I=0 TO 8 DO
                CALL OUTPUT FDC(COMMAND(I))
                ENDDO
        ENDDO

GET RESULTS:
(THIS ROUTINE WILL INPUT THE RESULT BYTES AFTER A COMMAND COMPLETION)
        DO
        I=0
        DO FOREVER
        CALL INPUT FDC
        IF FDC IN OUTPUT MODE RETURN ELSE
                DO
                RESULT(I)= FDC INPUT
                I=I+1
                END
        ENDDO

CHECK RESULTS:
        DO
        IF RESULT(1)<>0 THEN RETURN ERROR STATUS
        ELSE RETURN STATUS OK
        ENDDO
```

```
                        TITLE   'CUSTOMIZED BASIC I/O SYSTEM'

                        ;*********************************************
                        ;*                                           *
                        ;* THIS CUSTOMIZED BIOS ADAPTS CP/M-86 TO    *
                        ;* THE FOLLOWING HARDWARE CONFIGURATION      *
                        ;*     PROCESSOR: 8088                       *
                        ;*     BRAND: LOMAS DATA PRODUCTS            *
                        ;*     CONTROLLER: LDP72 (8272)              *
                        ;*                                           *
                        ;*                                           *
                        ;*     PROGRAMMER: R. LOMAS                  *
                        ;*     REVISIONS : 3/6/81                    *
                        ;*                                           *
                        ;*********************************************

FFFF                    TRUE            EQU -1
0000                    FALSE           EQU NOT TRUE
000D                    CR              EQU 0DH ;CARRIAGE RETURN
000A                    LF              EQU 0AH ;LINE FEED
000A                    RETRY   EQU     10
0000                    CONDAT  EQU     0H
0001                    CONSTA  EQU     01H

                        ;*********************************************
                        ;*                                           *
                        ;* LOADER_BIOS IS TRUE IF ASSEMBLING THE     *
                        ;* LOADER BIOS, OTHERWISE BIOS IS FOR THE    *
                        ;* CPM.SYS FILE.                             *
                        ;*                                           *
                        ;*********************************************

0000                    LOADER_BIOS     EQU FALSE
00E0                    BDOS_INT        EQU 224 ;RESERVED BDOS INTERRUPT

                                IF      NOT LOADER_BIOS
                        ;-------------------------------------------
                        ;:                                         :
2500                    BIOS_CODE       EQU 2500H
0000                    CCP_OFFSET      EQU 0000H
0B06                    BDOS_OFST       EQU 0E06H ;BDOS ENTRY POINT
                        ;:                                         :
                        ;-------------------------------------------
                                ENDIF   ;NOT LOADER_BIOS

                                IF      LOADER_BIOS
                        ;-------------------------------------------
                        ;:                                         :
                        BIOS_CODE       EQU 1200H ;START OF LDBIOS
                        CCP_OFFSET      EQU 0003H ;BASE OF CPMLOADER
                        BDOS_OFST       EQU 0406H ;STRIPPED BDOS ENTRY
                        ;:                                         :
```

```
                        ;----------------------------------------
                                ENDIF   ;LOADER_BIOS

                                CSEG
                                ORG     CCPOFFSET
                        CCP:
                                ORG     BIOS_CODE

                        ;*****************************************
                        ;*                                       *
                        ;* BIOS JUMP VECTOR FOR INDIVIDUAL ROUTINES *
                        ;*                                       *
                        ;*****************************************

2500 E93C00     253F    JMP INIT        ;ENTER FROM BOOT ROM OR LOADER
2503 E97900     257F    JMP WBOOT       ;ARRIVE HERE FROM BDOS CALL 0
2506 E98500     258E    JMP CONST       ;RETURN CONSOLE KEYBOARD STATUS
2509 E98E00     259A    JMP CONIN       ;RETURN CONSOLE KEYBOARD CHAR
250C E99500     25A4    JMP CONOUT      ;WRITE CHAR TO CONSOLE DEVICE
250F E9D400     25E6    JMP LISTOUT     ;WRITE CHARACTER TO LIST DEVICE
2512 E9D300     25E8    JMP PUNCH       ;WRITE CHARACTER TO PUNCH DEVICE
2515 E9D100     25E9    JMP READER      ;RETURN CHAR FROM READER DEVICE
2518 E90101     261C    JMP HOME        ;MOVE TO TRK 00 ON CUR SEL DRIVE
251B E9E300     2601    JMP SELDSK      ;SELECT DISK FOR NEXT RD/WRITE
251E E9FF00     2620    JMP SETTRK      ;SET TRACK FOR NEXT RD/WRITE
2521 E90201     2626    JMP SETSEC      ;SET SECTOR FOR NEXT RD/WRITE
2524 E90C01     2633    JMP SETDMA      ;SET OFFSET FOR USER BUFF (DMA)
2527 E96E01     2698    JMP READ        ;READ A 128 BYTE SECTOR
252A E9BA01     26E7    JMP WRITE       ;WRITE A 128 BYTE SECTOR
252D E9B700     25E7    JMP LISTST      ;RETURN LIST STATUS
2530 E9F900     262C    JMP SECTRAN     ;XLATE LOGICAL->PHYSICAL SECTOR
2533 E90201     2638    JMP SETDMAB     ;SET SEG BASE FOR BUFF (DMA)
2536 E90401     263D    JMP GETSEGT     ;RETURN OFFSET OF MEM DESC TABLE
2539 E9AE00     25EA    JMP GETIOBF     ;RETURN I/O MAP BYTE (IOBYTE)
253C E9AF00     25EE    JMP SETIOBF     ;SET I/O MAP BYTE (IOBYTE)

                        ;*****************************************
                        ;*                                       *
                        ;* INIT ENTRY POINT, DIFFERS FOR LDBIOS AND *
                        ;* BIOS, ACCORDING TO "LOADER_BIOS" VALUE  *
                        ;*                                       *
                        ;*****************************************

                        INIT:   ;PRINT SIGNON MESSAGE AND INITIALIZE HARDWARE
253F 8CC8                       MOV AX,CS       ;WE ENTERED WITH A JMPF SO USE
2541 8ED0                       MOV SS,AX       ;CS: AS THE INITIAL VALUE OF SS:,
2543 8ED8                       MOV DS,AX       ;DS:,
2545 8EC0                       MOV ES,AX       ;AND ES:
                                ;USE LOCAL STACK DURING INITIALIZATION
2547 BCD429                     MOV SP,OFFSET STKBASE
254A FC                         CLD             ;SET FORWARD DIRECTION
```

```
                        IF      NOT LOADER_BIOS
                    ;-----------------------------------------
                    ;;                                       ;
                        ; THIS IS A BIOS FOR THE CPM.SYS FILE.
                        ; SETUP ALL INTERRUPT VECTORS IN LOW
                        ; MEMORY TO ADDRESS TRAP

254B 1E                 PUSH DS         ;SAVE THE DS REGISTER
254C C6062B2800         MOV IOBYTE,0    ;CLEAR IOBYTE
2551 B80000             MOV AX,0
2554 8ED8               MOV DS,AX
2556 8EC0               MOV ES,AX       ;SET ES AND DS TO ZERO
                        ;SETUP INTERRUPT 0 TO ADDRESS TRAP ROUTINE
2558 C70600008225       MOV INT0_OFFSET,OFFSET INT_TRAP
255E 8C0E0200           MOV INT0_SEGMENT,CS
2562 BF0400             MOV DI,4
2565 BE0000             MOV SI,0        ;THEN PROPAGATE
2568 B9FE01             MOV CX,510      ;TRAP VECTOR TO
256B F3A5               REP MOVS AX,AX  ;ALL 256 INTERRUPTS
                        ;BDOS OFFSET TO PROPER INTERRUPT
256D C7068003060B       MOV BDOS_OFFSET,BDOS_OFST
2573 1F                 POP DS          ;RESTORE THE DS REGISTER

                    ;       (ADDITIONAL CP/M-86 INITIALIZATION)
                    ;;                                       ;
                    ;-----------------------------------------
                        ENDIF   ;NOT LOADER_BIOS

                        IF      LOADER_BIOS
                    ;-----------------------------------------
                    ;;                                       ;
                        ;THIS IS A BIOS FOR THE LOADER
                        PUSH DS         ;SAVE DATA SEGMENT
                        MOV AX,0
                        MOV DS,AX       ;POINT TO SEGMENT ZERO
                        ;BDOS INTERRUPT OFFSET
                        MOV BDOS_OFFSET,BDOS_OFST
                        MOV BDOS_SEGMENT,CS ;BDOS INTERRUPT SEGMENT
                        CALL    CONINI
                    ;       (ADDITIONAL LOADER INITIALIZATION)
                        POP DS          ;RESTORE DATA SEGMENT
                    ;;                                       ;
                    ;-----------------------------------------
                        ENDIF   ;LOADER_BIOS

2574 BB3128             MOV BX,OFFSET SIGNON
2577 E87900     25F3    CALL PMSG       ;PRINT SIGNON MESSAGE
257A B100               MOV CL,0        ;DEFAULT TO DR A: ON COLDSTART
257C E981DA     0000    JMP CCP         ;JUMP TO COLD START ENTRY OF CCP

257F E984DA     0006 WBOOT: JMP CCP+6   ;DIRECT ENTRY TO CCP AT COMMAND LEVEL
```

```
                        IF      NOT LOADER_BIOS
                    ;-----------------------------------------
                    ;;                                      :
                    INT_TRAP:
2582 FA                     CLI             ;BLOCK INTERRUPTS
2583 8CC8                   MOV AX,CS
2585 8ED8                   MOV DS,AX       ;GET OUR DATA SEGMENT
2587 BB5028                 MOV BX,OFFSET INT_TRP
258A E86600         25F3    CALL PMSG
258D F4                     HLT             ;HARDSTOP
                    ;;                                      :
                    ;-----------------------------------------
                        ENDIF   ;NOT LOADER_BIOS

                    ;*****************************************
                    ;*                                       *
                    ;*   CP/M CHARACTER I/O INTERFACE ROUTINES   *
                    ;*                                       *
                    ;*****************************************

                    CONST:          ;CONSOLE STATUS
258E E401                   IN      AL,CONSTA
2590 A802                   TEST    AL,02           ;CHARACTER READY
2592 7403           2597    JZ      NOCHAR          ;NO CHARACTER IF BIT=0
2594 0CFF                   OR      AL,0FFH         ;INDICATE CHARACTER AVAIL
2596 C3                     RET
2597 32C0           NOCHAR: XOR     AL,AL           ;ZERO AL TO INDICATE NO CHAR
2599 C3                     RET

                    CONIN:                  ;CONSOLE INPUT
259A E8F1FF         258E    CALL CONST
259D 74FB           259A    JZ CONIN        ;WAIT FOR RDA
259F E400                   IN      AL,CONDAT       ;GET CHARACTER
25A1 247F                   AND     AL,7FH          ;MASK TO 7 BITS
25A3 C3                     RET

                    CONOUT:         ;CONSOLE OUTPUT
25A4 8AC1                   MOV     AL,CL
25A6 50                     PUSH    AX
25A7 3C08                   CMP     AL,08H
25A9 7502           25AD    JNE     CONR
25AB B01A                   MOV     AL,1AH
25AD 50             CONR:   PUSH    AX
25AE E401           CON1:   IN      AL,CONSTA
25B0 A801                   TEST    AL,01H
25B2 74FA           25AE    JZ      CON1
25B4 58                     POP     AX
25B5 E600                   OUT     CONDAT,AL
25B7 58                     POP     AX
25B8 C3                     RET

                    CONINI:
```

```
                        ;INITILIZES THE USART FOR THE CONSOLE DEVICE.
                        ;8 BITDATA,2 STOP BITS NO PARITY, X16 MODE.
25B9 B000                       MOV     AL,0
25BB E601                       OUT     CONSTA,AL
25BD E81D00     25DD            CALL    DELAY
25C0 E601                       OUT     CONSTA,AL
25C2 E81800     25DD            CALL    DELAY
25C5 E601                       OUT     CONSTA,AL
25C7 E81300     25DD            CALL    DELAY
25CA B040                       MOV     AL,40H
25CC E601                       OUT     CONSTA,AL
25CE E80C00     25DD            CALL    DELAY
25D1 B0CE                       MOV     AL,0CEH
25D3 E601                       OUT     CONSTA,AL
25D5 E80500     25DD            CALL    DELAY
25D8 B037                       MOV     AL,37H
25DA E601                       OUT     CONSTA,AL
25DC C3                         RET

25DD 50                 DELAY:  PUSH    AX
25DE B8E803                     MOV     AX,1000
25E1 48                 DEL1:   DEC     AX
25E2 75FD       25E1            JNZ     DEL1
25E4 58                         POP     AX
25E5 C3                         RET
                        LISTOUT:                ;LIST DEVICE OUTPUT
25E6 C3                         RET

                        LISTST:                 ;POLL LIST STATUS
25E7 C3                         RET

                        PUNCH:          ;WRITE PUNCH DEVICE
25E8 C3                         RET

                        READER:
25E9 C3                         RET

                        GETIOBF:
25EA A02B28                     MOV AL,IOBYTE
25ED C3                         RET

                        SETIOBF:
25EE 880E2B28                   MOV IOBYTE,CL   ;SET IOBYTE
25F2 C3                         RET             ;IOBYTE NOT IMPLEMENTED

                        PMSG:
25F3 8A07                       MOV AL,[BX]     ;GET NEXT CHAR FROM MESSAGE
25F5 84C0                       TEST AL,AL
25F7 7422       261B            JZ RETURN       ;IF ZERO RETURN
25F9 8AC8                       MOV CL,AL
25FB E8A6FF     25A4            CALL CONOUT     ;PRINT IT
25FE 43                         INC BX
```

```
25FF EBF2       25F3        JMPS PMSG       ;NEXT CHARACTER AND LOOP

                        ;*********************************************
                        ;*                                           *
                        ;*         DISK INPUT/OUTPUT ROUTINES        *
                        ;*                                           *
                        ;*********************************************

                        SELDSK:         ;SELECT DISK GIVEN BY REGISTER CL
 0002                   NDISKS  EQU     2 ;NUMBER OF DISKS (UP TO 16)
2601 2E880E1828                 MOV UNIT,CL     ;SAVE DISK NUMBER
2606 BB0000                     MOV BX,0000H    ;READY FOR ERROR RETURN
2609 80F902                     CMP CL,NDISKS   ;N BEYOND MAX DISKS?
260C 730D       261B            JNB RETURN      ;RETURN IF SO
260E B500                       MOV CH,0        ;DOUBLE(N)
2610 8BD9                       MOV BX,CX       ;BX = N
2612 B104                       MOV CL,4        ;READY FOR *16
2614 D3E3                       SHL BX,CL       ;N = N * 16
2616 B96C28                     MOV CX,OFFSET DPBASE
2619 03D9                       ADD BX,CX       ;DPBASE + N * 16
261B C3                 RETURN: RET             ;BX = .DPH

                        HOME:   ;MOVE SELECTED DISK TO HOME POSITION (TRACK 0)
261C E8D601     27F5            CALL    RECAL
261F C3                         RET

                        SETTRK: ;SET TRACK ADDRESS GIVEN BY CX
2620 2E880E1928                 MOV CYL,CL
2625 C3                         RET

                        SETSEC: ;SET SECTOR NUMBER GIVEN BY CX
2626 2E880E1B28                 MOV SECT,CL
262B C3                         RET

                        SECTRAN: ;TRANSLATE SECTOR CX USING TABLE AT [DX]
262C 8BD9                       MOV BX,CX
262E 03DA                       ADD BX,DX       ;ADD SECTOR TO TRAN TABLE ADDRESS
2630 8A1F                       MOV BL,[BX]     ;GET LOGICAL SECTOR
2632 C3                         RET

                        SETDMA: ;SET DMA OFFSET GIVEN BY CX
2633 890E2D28                   MOV DMA_ADR,CX
2637 C3                         RET

                        SETDMAB: ;SET DMA SEGMENT GIVEN BY CX
2638 890E2F28                   MOV DMA_SEG,CX
263C C3                         RET
                        ;
                        GETSEGT:  ;RETURN ADDRESS OF PHYSICAL MEMORY TABLE
263D BB6728                     MOV BX,OFFSET SEG_TABLE
2640 C3                         RET
```

```
=                               INCLUDE PRINT.A86
=2641 E84900        268D PERR:  CALL    CRLF
=2644 2EA02028                  MOV     AL,CS:ST0
=2648 E81800        2663        CALL    OUTB
=264B E83900        2687        CALL    SPACE
=264E 2EA02128                  MOV     AL,CS:ST1
=2652 E80E00        2663        CALL    OUTB
=2655 E82F00        2687        CALL    SPACE
=2658 2EA02228                  MOV     AL,CS:ST2
=265C E80400        2663        CALL    OUTB
=265F E82B00        268D        CALL    CRLF
=2662 C3                        RET
=
=2663 50            OUTB:       PUSH    AX
=2664 24F0                      AND     AL,0F0H
=2666 B104                      MOV     CL,04
=2668 D2C8                      ROR     AL,CL
=266A E81100        267E        CALL    CVT
=266D 8AC8                      MOV     CL,AL
=266F E832FF        25A4        CALL    CONOUT
=2672 58                        POP     AX
=2673 240F                      AND     AL,0FH
=2675 E80600        267E        CALL    CVT
=2678 8AC8                      MOV     CL,AL
=267A E827FF        25A4        CALL    CONOUT
=267D C3                        RET
=
=267E 0430          CVT:        ADD     AL,30H
=2680 3C39                      CMP     AL,39H
=2682 7E02          2686        JLE     CVTR
=2684 0407                      ADD     AL,07H
=2686 C3            CVTR:       RET
=
=2687 B120          SPACE:      MOV     CL,' '
=2689 E818FF        25A4        CALL    CONOUT
=268C C3                        RET
=
=268D B10D          CRLF:       MOV     CL,CR
=268F E812FF        25A4        CALL    CONOUT
=2692 B10A                      MOV     CL,LF
=2694 E80DFF        25A4        CALL    CONOUT
=2697 C3                        RET
```

```
;*****************************************
;*                                       *
;*  ALL DISK I/O PARAMETERS ARE SETUP:   *
;*     UNIT     IS DISK NUMBER     (SELDSK) *
;*     CYL      IS TRACK NUMBER    (SETTRK) *
;*     SECT     IS SECTOR NUMBER   (SETSEC) *
;*     DMA_ADR  IS THE DMA OFFSET  (SETDMA) *
;*     DMA_SEG  IS THE DMA SEGMENT (SETDMAB)*
```

```
                        ;*  READ READS THE SELECTED SECTOR TO THE DMA*
                        ;*  ADDRESS, AND WRITE WRITES THE DATA FROM  *
                        ;*  THE DMA ADDRESS TO THE SELECTED SECTOR   *
                        ;*  (RETURN 00 IF SUCCESSFUL, 01 IF PERM ERR)*
                        ;*                                           *
                        ;*********************************************

                        READ:
2698 2EC606172806               MOV     CMND,06H        ;PUT READ COMMAND IN IOPB
269E E8A400     2745            CALL    SEEK            ;SEEK THE CORRECT CYLINDER
26A1 06                         PUSH    ES              ;SAVE SEG REG
26A2 2EA12F28                   MOV     AX,CS:DMASEG    ;GET SEGMENT INFO FOR TRANSFER
26A6 8EC0                       MOV     ES,AX           ;PUT IN SEGMENT REG
26A8 2E8B3E2D28                 MOV     DI,CS:DMAADR    ;GET DMA OFFSET INFO
26AD E8EF00     279F            CALL    OUTIOP          ;START THE OPERATION
26B0 B98000                     MOV     CX,128          ;GET NUMBER OF BYTES TO TRANSFER
26B3 E80101     27B7            CALL    INDATA          ;GET THE DATA FROM THE DISK
26B6 07                         POP     ES              ;GET BACK SEGMENT
26B7 83F900                     CMP     CX,0            ;SHOULD BE 0 IF ALL TRANSFERED
26BA 7514       26D0            JNE     ERR1            ;IF NOT 0 GO TO ERROR ROUTINE
26BC E86000     271F            CALL    TC              ;STOP THE PRESENT COMMAND
26BF E84901     280B            CALL    WTINT           ;WAIT FOR INTERRUPT TO HAPPEN
26C2 E86B00     2730            CALL    INRSLT          ;GET RESULTS FROM FDC
26C5 E85C00     2724            CALL    CHECK           ;CHECK THE RESULTS FOR ERRORS
26C8 7312       26DC            JNB     ERRET           ;IF ERROR GO TO ERROR RETURN
26CA E81401     27E1            CALL    SENSE           ;CLEAR INTERRUPT
26CD 32C0                       XOR     AL,AL           ;ZERO AL TO INDICATE SUCCESS
26CF C3                         RET
26D0 E84C00     271F ERR1:      CALL    TC              ;TERMINATE OPERATION
26D3 E83501     280B            CALL    WTINT           ;WAIT FOR INTERRUPT
26D6 E85700     2730            CALL    INRSLT          ;GET THE RESULTS
26D9 E865FF     2641            CALL    PERR
26DC E80201     27E1 ERRET:     CALL    SENSE           ;CLEAR INTERRUPT
26DF E85FFF     2641            CALL    PERR
26E2 32C0                       XOR     AL,AL           ;SET AL TO 0
26E4 0C01                       OR      AL,01           ;SET ERROR INDICATOR
26E6 C3                         RET

                        WRITE:
                        ;WRITES A 128 BYTE BLOCK OF DATA TO THE SECTOR,CYLINDER,AND UNIT
                        ;SPECIFIED IN THE GLOBAL VARIABLES.
26E7 2EC606172805               MOV     CMND,05H        ;SET IOPB TO WRITE COMMAND
26ED E85500     2745            CALL    SEEK            ;SEEK THE RIGHT CYLINDER
26F0 1E                         PUSH    DS              ;SAVE THE SEGMENT REG
26F1 2EA12F28                   MOV     AX,CS:DMASEG    ;GET TRANSFER SEGMENT INFO
26F5 8ED8                       MOV     DS,AX           ;PUT IT INTO DATA SEGMENT
26F7 2E8B362D28                 MOV     SI,CS:DMAADR    ;GET OFFSET INFO
26FC B98000                     MOV     CX,128          ;GET NUMBER OF BYTES
26FF E89D00     279F            CALL    OUTIOP          ;START WRITE OPERATION
2702 E8C700     27CC            CALL    OTDATA          ;WRITE DATA TO DISK
2705 1F                         POP     DS              ;GET BACK SEG INFO
2706 83F900                     CMP     CX,0            ;CHECK FOR COMPLETION OF TRANSFER
```

```
2709 75C5       26D0        JNE     ERR1            ;GO TO ERROR ROUTINE IF NOT DONE
270B E81100     271F        CALL    TC              ;STOP THE COMMAND
270E E8FA00     280B        CALL    WTINT           ;WAIT FOR THE INTERRUPT
2711 E81C00     2730        CALL    INRSLT          ;GET RESULTS FROM THE FDC
2714 E80D00     2724        CALL    CHECK           ;CHECK THE RESULTS
2717 73C3       26DC        JNB     ERRET           ;IF ERROR TAKE THE ERROR RETURN
2719 E8C500     27E1        CALL    SENSE           ;CLEAR THE INTERRUPT
271C 32C0                   XOR     AL,AL           ;SET TO 0 TO INDICATE OK
271E C3                     RET
=                           INCLUDE         DISKIO.A86
=  0084             ENAWT   EQU     84H
=  0080             DISWT   EQU     80H
=  0010             FDCEXT  EQU     10H
=  0011             FDCDAT  EQU     11H
=  0012             FDCST   EQU     12H
=  0013             FDCRSL  EQU     13H
=  0013             FDCCMD  EQU     13H
=
=                   TC:
=                   ;TC TERMINATES THE COMAND PRESENTLY BEING EXECUTED BY THE DISK
=                   ;CONTROLLER BY GENERATING A TC PULSE TO THE FDC.
=271F B010                  MOV     AL,10H
=2721 E610                  OUT     FDCEXT,AL
=2723 C3                    RET
=
=                   CHECK:
=                   ;CHECK CHECKS THE RESULTS OF THE PREVIOUS DISK OPERATION
=                   ;BY TESTING THE RESULT REGISTER ST1
=2724 2EA02128              MOV     AL,CS:ST1
=2728 247F                  AND     AL,07FH
=272A 7502      272E        JNZ     ERR
=272C F9                    STC
=272D C3                    RET
=272E F8            ERR:    CLC
=272F C3                    RET
=
=                   INRSLT:
=                   ;INRSLT INPUTS THE RESULT BYTES AFTER THE COMPLETION OF
=                   ;A DISK OPERATION
=2730 06                    PUSH    ES              ;SAVE SEGMENT INFO
=2731 57                    PUSH    DI              ;SAVE DESTINATION REG
=2732 FC                    CLD                     ;SET TO INCREMENTING DIRRECTION
=2733 8CC8                  MOV     AX,CS           ;GET CODE SEGMENT INFO
=2735 8EC0                  MOV     ES,AX           ;SET UP FOR INPUTING TO RESULT BUFFER
=2737 BF2028                MOV     DI,OFFSET ST0   ;GET ADDRESS OF BUFFER
=273A E85200    278F B005:  CALL    INFDC           ;GET RESULT BYTE
=273D 7303      2742        JNB     B004            ;IF IN WRONG MODE THEN DONE
=273F AA                    STOS    AL              ;PUT IN RESULT BUFFER
=2740 EBF8      273A        JMPS    B005            ;GET NEXT RESULT BYTE
=2742 5F            B004:   POP     DI              ;RESTORE REGISTORS
=2743 07                    POP     ES
=2744 C3                    RET
```

```
=
=                       SEEK:
=                       ;SEEK THE DISK TRACK SPECIFIED IN THE PARAMETER CYL.
=                       ;IF IT IS DISK B: AND IT HAS NOTBEEN  USED BEFORE  HOME IT
=                       ;FIRST.
=2745 E89900        27E1        CALL    SENSE           ;MAKE SURE NO INTERRUPTS PENDING
=2748 2E803E182800              CMP     CS:UNIT,0       ;IS IT DISK A:
=274E 7411          2761        JE      SEEK1           ;IF A: THEN GO SEEK
=2750 2EA01628                  MOV     AL,CS:UNIT1     ;ELSE CHECK TO SEE IF B: USED
=                                                       ;ALREADY
=2754 0AC0                      OR      AL,AL           ;CHECK FOR 0
=2756 7409          2761        JZ      SEEK1           ;IF 0 THEN OK TO USE WITHOUT RECAL
=2758 E89A00        27F5        CALL    RECAL           ;RECAL IF NOT USED BEFORE
=275B 2EC606162800              MOV     CS:UNIT1,0      ;SET TO SHOW USED
=2761 B00F              SEEK1:  MOV     AL,0FH          ;GET RECAL COMAND
=2763 E81700        277D        CALL    OUTFDC          ;SEND IT TO THE FDC
=2766 2EA01828                  MOV     AL,CS:UNIT      ;GET THE UNIT NUMBER TO SEEK
=276A 2403                      AND     AL,03H          ;MAKE SURE UNIT #<4
=276C E80E00        277D        CALL    OUTFDC
=276F 2EA01928                  MOV     AL,CS:CYL       ;GET TRACK TO SEEK
=2773 E80700        277D        CALL    OUTFDC          ;STARTS SEEK OPERATION
=2776 E89200        280B        CALL    WTINT           ;WAIT FOR SEEK TO BE COMPLETED
=2779 E86500        27E1        CALL    SENSE           ;CLEAR THE INTERRUPT
=277C C3                        RET                     ;SEEK DONE RETURN TO CALLUR
=
=                       OUTFDC:
=                       ;OUTPUTS THE VALUE IN AL TO THE FDC AFTER DETERMINING THE FDC
=                       ;IS READY AND IT IS IN THE OUTPUT MODE.
=277D 50                        PUSH    AX              ;SAVE DATA TO SEND
=277E E412              B006:   IN      AL,FDCST        ;GET THE FDC STATUS
=2780 A880                      TEST    AL,80H          ;CHECK THE FDC READY BIT
=2782 74FA          277E        JZ      B006            ;IF NOT READY WAIT TILL READY
=2784 A840                      TEST    AL,40H          ;CHECK DIRRECTION BIT
=2786 58                        POP     AX              ;GET DATA BACK
=2787 7504          278D        JNZ     B007            ;IF BIT WAS A ONE THEN WRONG DIR
=2789 E613                      OUT     FDCCMD,AL       ;OTHERWISE OUTPUT THE DATA
=278B F9                        STC                     ;INDICATE SUCCESS
=278C C3                        RET
=278D F8                B007:   CLC                     ;INDICATE WRONG DIRRECTION
=278E C3                        RET
=
=                       INFDC:
=                       ;INPUTS A BYTE FROM THE FDC AFTER WAITING FOR IT TO BE READY
=                       ;AND CHECKING THE DIRRECTION BIT FOR THE CORRECT DIRRECTON.
=
=278F E412                      IN      AL,FDCST        ;GET THE FDC STATUS
=2791 A880                      TEST    AL,80H          ;CHECK THE READY BIT
=2793 74FA          278F        JZ      INFDC           ;WAIT TILL READY
=2795 A840                      TEST    AL,40H          ;CHECK DIRRECTION FLAG
=2797 7404          279D        JZ      B009            ;IF 0 THEN WRONG DIR
=2799 E413                      IN      AL,FDCRSL       ;OK SO GET BYTE FROM FDC
=279B F9                        STC
```

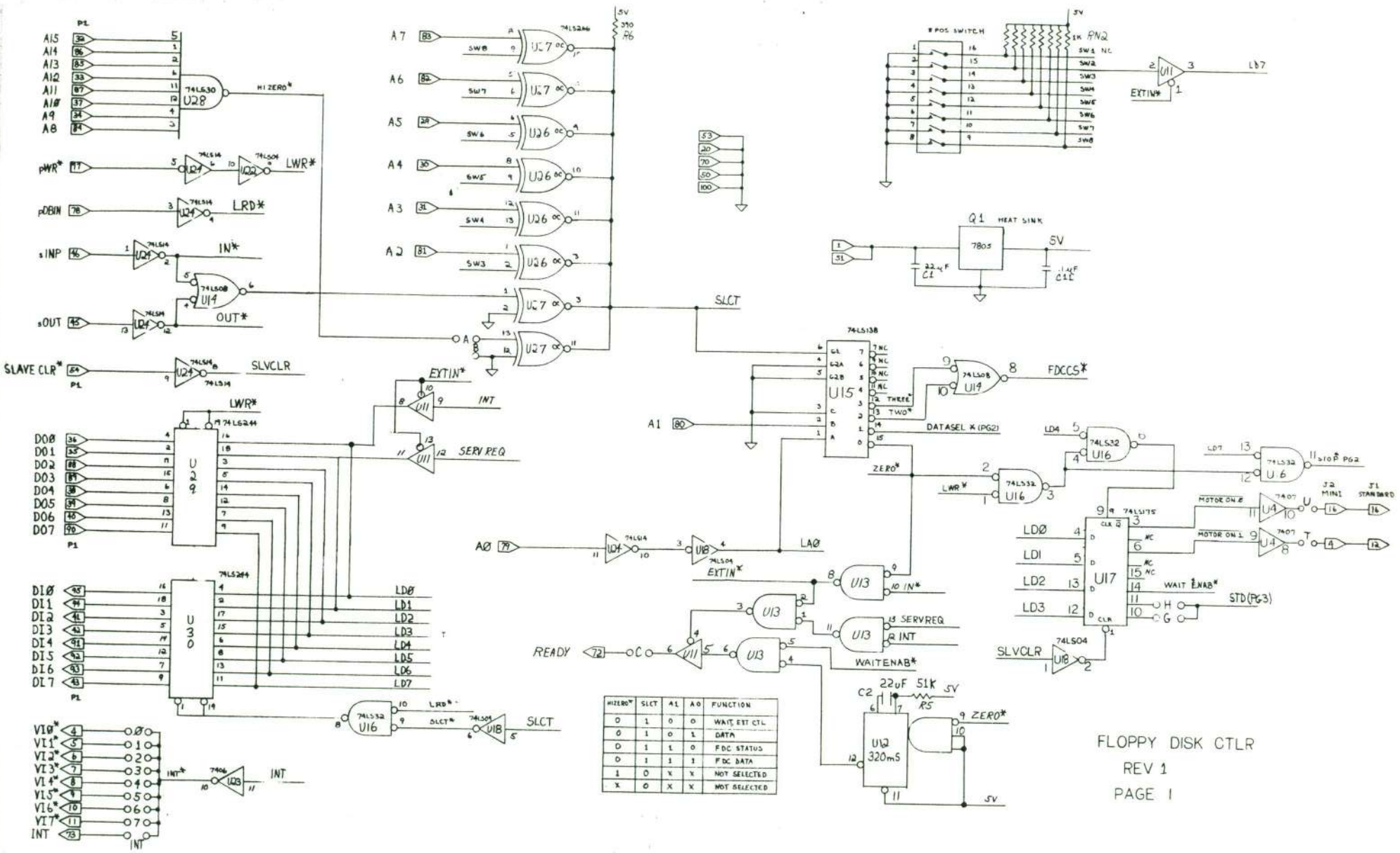
```
=279C C3                    RET
=279D F8              B009: CLC
=279E C3                    RET
=
=                     OUTIOP:
=                     ;OUTPUTS THE IOPARAMETER BLOCK TO THE FDC TO INITIATE A READ,
=                     ;WRITE, OR FORMAT OPERATION.
=279F 51                    PUSH    CX              ;SAVE WORKING REGS
=27A0 1E                    PUSH    DS
=27A1 56                    PUSH    SI
=27A2 FC                    CLD                     ;SET FOR INCREMENTING STRING OP
=27A3 B90900                MOV     CX,09H          ;NUMBER OF BYTES TO TRANSFER
=27A6 8CC8                  MOV     AX,CS           ;GET PRESENT CODE SEGMENT
=27A8 8ED8                  MOV     DS,AX           ;SET DATA SEG TO CODE SEG
=27AA BE1728                MOV     SI,OFFSET IOPB  ;GET POINTER TO IOPB
=27AD AC              B001: LODS    AL              ;GET BYTE FROM IOPB
=27AE E8CCFF    277D        CALL    OUTFDC          ;SEND IT TO THE FDC
=27B1 E2FA      27AD        LOOP    B001            ;DO UNTILL 9 BYTES OUTPUT
=27B3 5E                    POP     SI              ;RESTORE REGISTERS
=27B4 1F                    POP     DS
=27B5 59                    POP     CX
=27B6 C3                    RET
=
=                     INDATA:
=                     ;GETS THE DATA FROM A SECTOR ON THE DISK. IF THE INTERRUPT SIGNAL
=                     ;ON THE FDC GOES ACTIVE THE TRANSFER IS ABORTED.
=27B7 FC                    CLD                     ;SET FOR INCREMENTIN TRANSFER
=27B8 B084                  MOV     AL,ENAWT        ;SET ENABLE WAIT FF ON THE FDC
=27BA E610                  OUT     FDCEXT,AL
=27BC E410            B002: IN      AL,FDCEXT       ;INPUT FROM WAIT PORT
=27BE A802                  TEST    AL,02H          ;TEST FOR INTERRUPT
=27C0 7405      27C7        JZ      B003            ;IF INTERRUP ABORT THE TRANSFER
=27C2 E411                  IN      AL,FDCDAT       ;GET THE BYTE
=27C4 AA                    STOS    AL              ;PUT IT IN MEMORY
=27C5 E2F5      27BC        LOOP    B002            ;DECREMENT COUNT AND DO AGAIN IF
=                                                   ;NOT 0
=27C7 B080            B003: MOV     AL,DISWT        ;
=27C9 E610                  OUT     FDCEXT,AL       ;DISABLE THE WAIT FF
=27CB C3                    RET
=
=                     OTDATA:
=                     ;OTDATA OUTPUTS A BLOCK OF DATA FROM MEMORY TO A SECTOR ON THE
=                     ;DISK. CX CONTAINS THE NUMBER OF BYTES TO OUTPUT.
=27CC FC                    CLD                     ;SET FOR INCREMENTING TRANSFER
=27CD B084                  MOV     AL,ENAWT        ;
=27CF E610                  OUT     FDCEXT,AL       ;ENABLE WAIT FF
=27D1 E410            B011: IN      AL,FDCEXT       ;WAIT TILL INTERRUPT OF DREQ ASSERTED
=27D3 A802                  TEST    AL,02H          ;TEST FOR INTERRUPT ASSERTED
=27D5 7405      27DC        JZ      B012            ;IF DMAREQ NOT ASSERTED ABORT
=27D7 AC                    LODS    AL              ;GET DATA TO SEND
=27D8 E611                  OUT     FDCDAT,AL       ;SEND BYTE TO FDC
=27DA E2F5      27D1        LOOP    B011            ;DECREMENT COUNT AND DO AGAIN IF
```

```
=                                                   ;NOT 0
=27DC B080              B012:   MOV     AL,DISWT    ;
=27DE E610                      OUT     FDCEXT,AL   ;DISABLE WAIT FF
=27E0 C3                        RET
=
=                       SENSE:
=                       ;SENSE INTERRUPT COMAND: ISSUSE A SENSE INTERRUPT COMAND TO THE
=                       ;FDC. THIS WILL CLEAR A PENDING INTERRUPT SIGNAL FROM THE
=                       ;FDC OR ACT AS A NOP IF AN INTERRUPT IS NOT PENDING. THIS IS
=                       ;USEFUL FOR PLACING THE FDC IN A KNOWN STATE
=27E1 B008                      MOV     AL,08H      ;GET SENSE INTERRUPT COMMAND
=27E3 E897FF        277D        CALL    OUTFDC      ;OUTPUT THE COMMAND
=27E6 E8A6FF        278F        CALL    INFDC       ;GET FIRST RESULT BYTE
=27E9 2EA22028                  MOV     CS:ST0,AL   ;SAVE BYTE
=27ED E89FFF        278F        CALL    INFDC       ;GET SECOND RESULT BYTE
=27F0 2EA22128                  MOV     CS:ST1,AL   ;SAVE IT
=27F4 C3                        RET
=
=                       RECAL:
=                       ;RETURNS THE DRIVE SPECIFIED IN UNIT TO THE HOME POSITION.
=27F5 E8E9FF        27E1        CALL    SENSE       ;GET FDC TO KNOWN STATE
=27F8 B007                      MOV     AL,07H      ;GET RECAL COMMAND
=27FA E880FF        277D        CALL    OUTFDC      ;SEND TO FDC
=27FD 2EA01828                  MOV     AL,CS:UNIT  ;GET UNIT TO HOME
=2801 E879FF        277D        CALL    OUTFDC      ;STARTS RECAL OPERATION
=2804 E80400        280B        CALL    WTINT       ;WAIT TILL DONE
=2807 E8D7FF        27E1        CALL    SENSE       ;CLEAR INTERRUPT
=280A C3                        RET
=
=                       WTINT:
=                       ;WAITS FOR THE INTERRUPT SIGNAL FROM THE FDC TO BECOME VALID
=280B B080                      MOV     AL,DISWT    ;
=280D E610                      OUT     FDCEXT,AL   ;MAKE SURE WAIT ENABLE FF OFF
=280F E410              WTINT1: IN      AL,FDCEXT   ;GET FDC STATUS FROM ENTERNAL PORT
=2811 A801                      TEST    AL,01H      ;TEST FOR INTERRUP ASSERTED
=2813 74FA          280F        JZ      WTINT1      ;IF NOT ASSERTED WAIT
=2815 C3                        RET
=
=
=                       ;DATA AREA PART OF CODE SEGMENT
=
=2816 FF                UNIT1   DB      0FFH
=  2817                 IOPB    EQU     $
=2817 00                CMND    DB      0
=2818 00                UNIT    DB      0
=2819 00                CYL     DB      0
=281A 00                HEAD    DB      0
=281B 00                SECT    DB      0
=281C 00                NBYTES  DB      0
=281D 1A                EOT     DB      26          ;LAST SECTOR NUMBER
=281E 07                GPL     DB      07
=281F 80                DTL     DB      128         ;NUMBER OF BYTES PER SECTOR
```

```
= 2820                  RSLT    EQU     $
=2820 00                ST0     DB      0
=2821 00                ST1     DB      0
=2822 00                ST2     DB      0
=2823                   RS      8



                        ;*********************************************
                        ;*                                           *
                        ;*              DATA AREAS                   *
                        ;*                                           *
                        ;*********************************************
  282B                  DATA_OFFSET     EQU OFFSET $

                        DSEG
                        ORG     DATA_OFFSET     ;CONTIGUOUS WITH CODE SEGMENT
 282B 00                IOBYTE  DB      0
 282C 00                DISK    DB      0       ;DISK NUMBER
 282D 0000              DMA_ADR DW      0       ;DMA OFFSET INTO DMA BASE SEG
 282F 0000              DMA_SEG DW      0       ;DMA BASE SEGMENT

                        IF      LOADER_BIOS
                        ;---------------------------------------
                        ;!                                     !
                        SIGNON  DB      CR,LF,CR,LF
                        DB      'CP/M-86 VERSION 1.0',CR,LF,0
                        ;!                                     !
                        ;---------------------------------------
                        ENDIF   ;LOADER_BIOS

                        IF      NOT LOADER_BIOS
                        ;---------------------------------------
                        ;!                                     !
 2831 0D0A0D0A          SIGNON  DB      CR,LF,CR,LF
 2835 53595354454D              DB      'SYSTEM GENERATED 3/06/81'
      2047454E4552
      415445442033
      2F30362F3831
 284D 0D0A00              -     DB      CR,LF,0
                        ;!                                     !
                        ;---------------------------------------
                        ENDIF   ;NOT LOADER_BIOS

 2850 0D0A              INT_TRP DB      CR,LF
 2852 494E54455252              DB      'INTERRUPT TRAP HALT'
      555054205452
      41502048414C
      54
 2865 0D0A                      DB      CR,LF

                        ;       SYSTEM MEMORY SEGMENT TABLE
```

```
2867 01              SEGTABLE DB 1   ;1 SEGMENTS
2868 DE02                     DW TPA_SEG      ;1ST SEG STARTS AFTER BIOS
286A 220D                     DW      TPA_LEN

=                           INCLUDE SINGLES.LIB ;READ IN DISK DEFINITIONS
=                    ;              DISKS 2
= 286C               dpbase  equ     $               ;Base of Disk Parameter Blocks
=286C 9B280000       dpe0    dw      xlt0,0000h      ;Translate Table
=2870 00000000               dw      0000h,0000h     ;Scratch Area
=2874 B5288C28               dw      dirbuf,dpb0     ;Dir Buff, Parm Block
=2878 54293529               dw      csv0,alv0       ;Check, Alloc Vectors
=287C 9B280000       dpe1    dw      xlt1,0000h      ;Translate Table
=2880 00000000               dw      0000h,0000h     ;Scratch Area
=2884 B5288C28               dw      dirbuf,dpb1     ;Dir Buff, Parm Block
=2888 83296429               dw      csv1,alv1       ;Check, Alloc Vectors
=                    ;              DISKDEF 0,1,26,6,1024,243,64,64,2
=                    ;
=                    ;       1944: 128 Byte Record Capacity
=                    ;        243: Kilobyte Drive  Capacity
=                    ;         64: 32 Byte Directory Entries
=                    ;         64: Checked Directory Entries
=                    ;        128: Records / Extent
=                    ;          8: Records / Block
=                    ;         26: Sectors / Track
=                    ;          2: Reserved  Tracks
=                    ;          6: Sector Skew Factor
=                    ;
= 288C               dpb0    equ     offset $        ;Disk Parameter Block
=288C 1A00                   dw      26              ;Sectors Per Track
=288E 03                     db      3               ;Block Shift
=288F 07                     db      7               ;Block Mask
=2890 00                     db      0               ;Extnt Mask
=2891 F200                   dw      242             ;Disk Size - 1
=2893 3F00                   dw      63              ;Directory Max
=2895 C0                     db      192             ;Alloc0
=2896 00                     db      0               ;Alloc1
=2897 1000                   dw      16              ;Check Size
=2899 0200                   dw      2               ;Offset
= 289B               xlt0    equ     offset $        ;Translate Table
=289B 01070D13               db      1,7,13,19
=289F 19050B11               db      25,5,11,17
=28A3 1703090F               db      23,3,9,15
=28A7 1502080E               db      21,2,8,14
=28AB 141A060C               db      20,26,6,12
=28AF 1218040A               db      18,24,4,10
=28B3 1016                   db      16,22
= 001F               als0    equ     31              ;Allocation Vector Size
= 0010               css0    equ     16              ;Check Vector Size
=                    ;              DISKDEF 1,0
=                    ;
=                    ;       Disk 1 is the same as Disk 0
```

```
=                       ;
= 288C                  dpb1    equ     dpb0            ;Equivalent Parameters
= 001F                  als1    equ     als0            ;Same Allocation Vector Size
= 0010                  css1    equ     css0            ;Same Checksum Vector Size
= 289B                  xlt1    equ     xlt0            ;Same Translate Table
=                       ;               ENDEF
=                       ;
=                       ;       Uninitialized Scratch Memory Follows:
=                       ;
= 28B5                  begdat  equ     offset $        ;Start of Scratch Area
=28B5                   dirbuf  rs      128             ;Directory Buffer
=2935                   alv0    rs      als0            ;Alloc Vector
=2954                   csv0    rs      css0            ;Check Vector
=2964                   alv1    rs      als1            ;Alloc Vector
=2983                   csv1    rs      css1            ;Check Vector
= 2993                  enddat  equ     offset $        ;End of Scratch Area
= 00DE                  datsiz  equ     offset $-begdat ;Size of Scratch Area
=2993 00                        db      0               ;Marks End of Module

 2994                   LOC_STK RW  32  ;LOCAL STACK FOR INITIALIZATION
   29D4                 STKBASE EQU OFFSET $

   29D4                 LASTOFF EQU OFFSET $
   02DE                 TPA_SEG EQU (LASTOFF+0400H+15) / 16
   0D22                 TPA_LEN EQU 01000H - TPA_SEG
 29D4 00                        DB 0    ;FILL LAST ADDRESS FOR GENCMD

                        ;*****************************************
                        ;*                                       *
                        ;*         DUMMY DATA SECTION            *
                        ;*                                       *
                        ;*****************************************
   0000                         DSEG    0       ;ABSOLUTE LOW MEMORY
                                ORG     0       ;(INTERRUPT VECTORS)
 0000                   INT0_OFFSET     RW      1
 0002                   INT0_SEGMENT    RW      1
                        ;       PAD TO SYSTEM CALL VECTOR
 0004                           RW      2*(BDOS_INT-1)

 0380                   BDOS_OFFSET     RW      1
 0382                   BDOS_SEGMENT    RW      1
                                END


END OF ASSEMBLY.  NUMBER OF ERRORS:  0.  USE FACTOR:  4%
```



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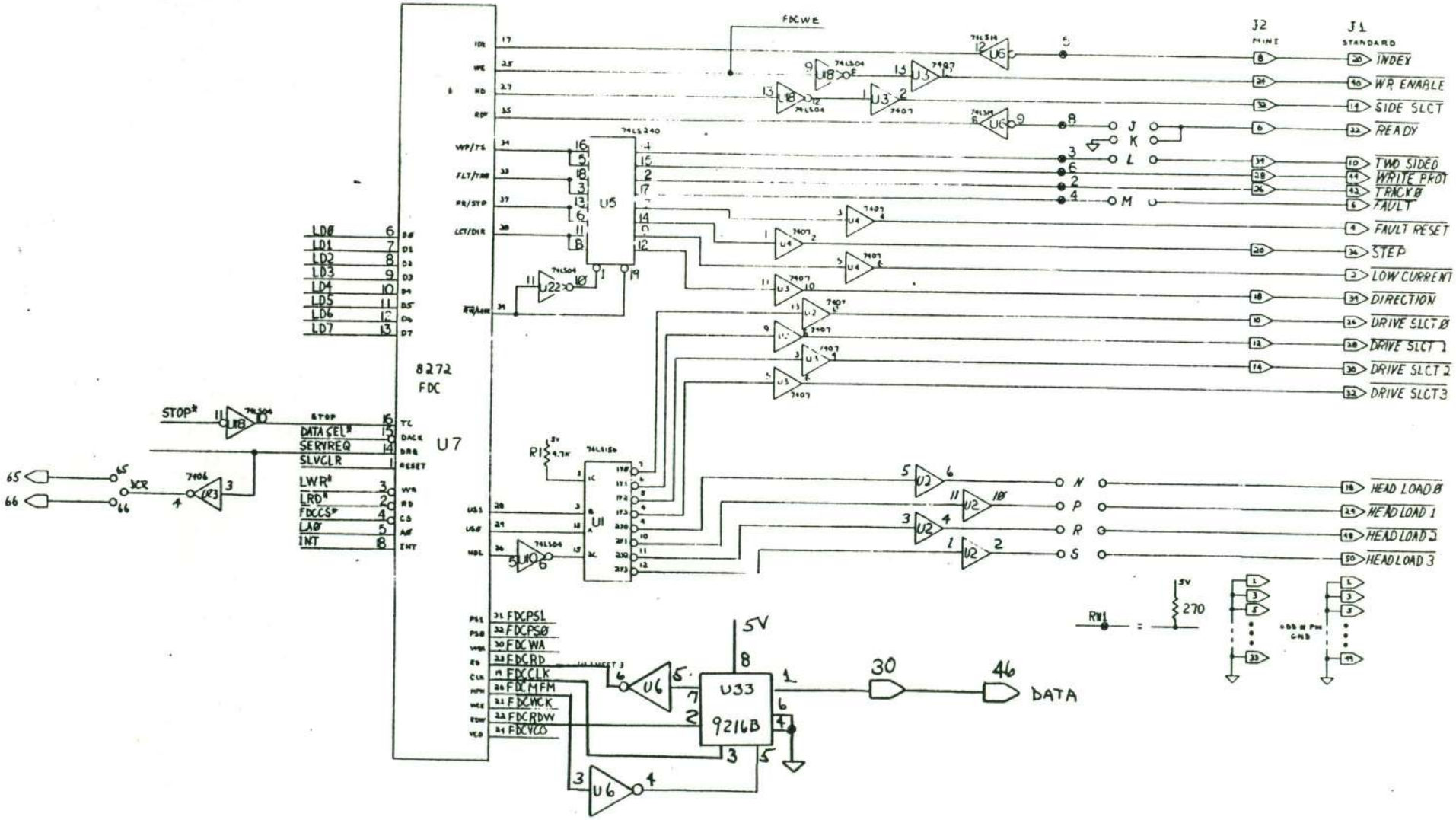
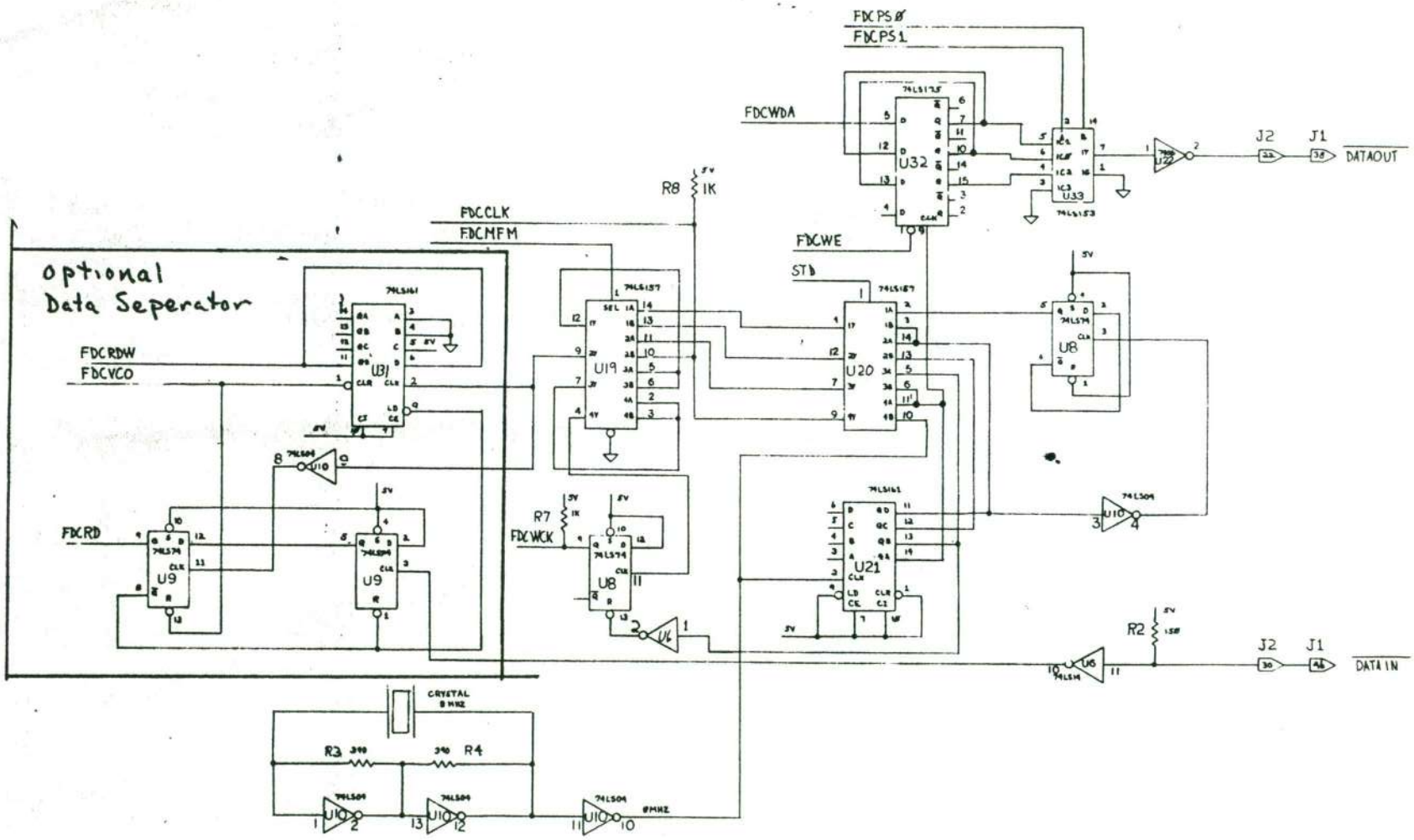

FDCWE
J2
MINI
J1
STANDARD
INDEX
WR ENABLE
SIDE SLCT
READY
TWO SIDED
WRITE PROT
TRACK Ø
FAULT
FAULT RESET
STEP
LOW CURRENT
DIRECTION
DRIVE SLCT Ø
DRIVE SLCT 1
DRIVE SLCT 2
DRIVE SLCT3
HEAD LOAD Ø
HEAD LOAD 1
HEAD LOAD 2
HEAD LOAD 3
8272
FDC
U7
U5
U1
U33
9216B
U22
U8
U6
U3
U4
U2
74LS240
74LS04
74LS86
7406
7407
STOP*
DATACEL*
SERVREQ
SLVCLR
LWR*
LRD*
FDCCS*
INT
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
FDCPSL
FDCPSØ
FDCWA
FDCRD
FDCCLK
FDCMFM
FDCWCK
FDCRDW
FDCVCO
5V
270
DATA
30
46


FDCPS0
FDCPS1
FDCWDA
U32
U33
J2
J1
DATAOUT
R8
1K
FDCCLK
FDCMFM
FDCWE
STB
optional
Data Seperator
FDCRDW
FDCVCO
U31
U19
U20
U8
FDCRD
U9
R7
FDCWCK
U21
R2
DATA IN
CRYSTAL
8 MHZ
R3
R4
8MHZ