system reliability/system integrity
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NONVOLATILE HIGH-SPEED MEMORY

FOR S-100 COMPUTER SYSTEMS

MODELS CMEM-32K
CMEM-16K
CMEM-8K

USER'S MANUAL

REVISED 1/21/82

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*Patent Being Sought

SECTION 1. INTRODUCTION AND GENERAL INFORMATION

1.1 INTRODUCTION

The Dual Systems CMEM series memory boards are nonvolatile, high-speed CMOS static memory units for S-100 bus computers. These memory boards are designed to retain any programs and data stored in them, even if the power to the computer is turned off. The CMEM memory boards are available in the following sizes:

MODEL:	MEMORY CAPACITY:
CMEM-8K	8,192 BYTES (8K BYTES)
CMEM-16K	16,384 BYTES (16K BYTES)
CMEM-32K	32,768 BYTES (32K BYTES)

These memories incorporate large-scale CMOS static memory integrated circuits (IC's), which enable the CMEM boards to store programs and data for well over three years with the factory supplied on-board battery. When the power to the computer system is turned off (or fails), this battery keeps the CMOS IC's supplied with power, preventing them from losing their data.

The Dual Systems CMEM memories are the first S-100 memory boards which do not sacrifice performance for nonvolatility. The 220 nanosecond (ns) access time allows them to run at full speed in all 4 megahertz S-100 computers (and also virtually all 6 MHz systems) with no need for wait states.

The CMEM memories have a software programmable "Write Protect Window*" (WPW), which can be used to enable a selected region of memory to be written to, while protecting other areas from being overwritten. This allows part of a program, or selected data, to be changed without the risk of accidently writing over other data which must be protected. With this safety feature, the CMEM boards can be made to behave virtually like EPROM boards, while retaining the speed and instant writeability of high-speed read/write memory.

The data protection system in the CMEM memories includes an on-board circuit that generates an interrupt when a drop is detected in the computer system power. This interrupt enables suitably programmed systems to store critical data (eg. program counter and register contents) before the power fails completely.

The CMEM boards have been designed to make use of the advanced features contained in the proposed IEEE-696 standard for the S-100 bus. Data path widths of either 8 or 16 bits may be selected by the computer. Extended addressing may be done either through 24-bit direct addressing, or through the bank select feature used with most pre-standard S-100 computers. Hence, the CMEM memories meet the IEEE proposed specification for new computers while remaining compatible with most existing systems.

*Patent Being Sought

1.2 FEATURES

* Up to 32K bytes of nonvolatile high-speed read/write memory on one S-100 board.

* 8 or 16 bit wide data paths

* 220 ns access time allows use in 6 MHz systems without wait states. (On board wait state generator allows operation in even faster systems)

* Software programmable "Write Protect Window"(WPW)* allows memory to be partitioned into write protected and write-enabled areas. This makes accidental overwriting of data by the computer very unlikely.

* Full compliance with I.E.E.E. 696 Proposed Standard for the S-100 bus, while remaining compatible with almost all pre-standard S-100 computers (eg. Cromemco SCC, Systems 2 and 3, Northstar Horizon, etc.)

* Extended 24 bit addressing may be used.

* BankSelect, with automatic enable or disable on system reset

* Starting address may be set on any 4K byte boundary in the address space.

* Any 4K byte block of memory may be disabled or enabled by means of a DIP switch.

* Power-fail interrupt-generating circuitry allows suitably programmed systems to store critical information in the CMEM memory before the power fails.

*Patent Being Sought

1.3 SPECIFICATIONS

Memory Capacity:

CMEM-32K:	32,768 Bytes
CMEM-16K:	16,384 Bytes
CMEM-8K:	8,192 Bytes

Memory type: CMOS 2048 x 8 bit static random access memory (Hitachi HM-6116LP3 or equiv. 150 nS)

Access Time: 220 nanoseconds maximum from time ADDRESS lines on bus become stable. Address decoding begins immediately upon address becoming stable, allowing full speed (no wait state) operation even in some 8 Mhz systems (eg. Dual Systems CPU/68000 and CPU/68000M). Requires no wait states in 6 MHz Z-80, 8085, 68000, Z-8000 systems. 1 optional wait state may be invoked in faster systems.

Bus Compatibility: S-100 as defined in IEEE-696 proposed spec.
IEEE-696 Compliance level:
Slave D8/D16 LO/LE M24 I8 VI F6 T220 W1

Also compatible with almost all pre-existing S-100 systems.

Memory Data Protection Scheme:

1. Generates optional interrupt when 8 volt power falls below 7.4 volts nominal (adjustable). May be used by computer to store critical data in CMEM memory.
2. Prevents any writing to CMEM memory when powerfalls below 7.0 volts, thus protecting memory contents from erroneous access when computer's power is lost.
3. Software programmable write protect window can be set to cause the CMEM memory to power up automatically in a write-protected state, and then can be programmed to write-enable only selected regions in memory, and then dynamically move the boundaries of the write-enabled area throughout the 64K byte global address space. Several other modes of operation are also available.
4. A single switch can be set to write-protect the whole CMEM memory board, for the highest possible degree of data protection.
5. On board battery back-up maintains data for 3 years (minimum) at 30 degrees C.

Address Selection: Memory arranged as single 32K byte block (CMEM-32K) or single 16K block (CMEM-16K) or single 8K block (CMEM-8K).

Starting address may be set for any 4K byte boundary within 64K byte address space, by means of switches.

Any 4K byte block of memory may be enabled or disabled by means of switches.

Extended Addressing (24 bit): When enabled, uses address lines A16 through A23 to determine which 64K byte page the CMEM will reside on, in a 16 megabyte address space.

Bank Select: An I/O-mapped output port is used to enable or disable the CMEM board. The CMEM's bank select is compatible withmost current bank-select schemes. The output port address is switch-selectable on any even address in the I/O address space.

Phantom: When the phantom line is asserted, the CMEM can be set to disable itself, regardless of the state of the address lines.

Write Protect Window (WPW) (Pat. Being Sought): The WPW uses an I/O port which automatically assumes an address that is 1 above that of the bank-select port (whether or not bank select is used)

Operating Power:

Voltage: Operates on +8 volts (nominal) as supplied on S-100 bus. Minimum voltage 7.5 volts, maximum 14 volts.

Current: 650 milliamperes typical, 1000 mA maximum for all CMEM series boards.

Standby Power: Supplied by one 3.9 volt lithium cell (supplied on-board the CMEM). Electrochem Industries Model 3B50, or similar.

Current consumption: (30 degrees C)	Typical:	Maximum:
CMEM-8K:	3 microamperes	15 microamperes
CMEM-16K:	6	30
CMEM-32K:	10	40

Data Retention Duration under Standby Power:

3 years minimum from date of shipment from Dual at a maximum board temperature of 30 degrees celsius.

CALCULATED (not guaranteed) TYPICAL battery life, and data retention duration: 10 yrs.

NOTE: Accidental short-circuiting of battery caused by inadvertantly placing the CMEM on a metal surface will ruin the battery (greatly shorten its life) and void the warranty.

Environmental Requirements:

Operating Temperature: 0 to 55 degrees Celsius
Note: Continued operation above 30 degrees C will seriously shorten battery life.

Relative Humidity: 90 % maximum, without condensation

SECTION 2. BOARD SETUP AND INSTALLATION

2.1 UNPACKING

All CMEM memory boards are burned in at the factory for 200 hours, and then thoroughly tested before being shipped. Therefore, these boards should work when you receive them.

When unpacking the CMEM boards, a brief visual inspection should be made. If there is any obvious physical damage to the units, or to the packaging materials, a claim should be filed with the carrier.

To protect the battery backup circuitry from possiible damage caused by an accidental short circuit, DO NOT PLACE THE CMEM BOARDS DIRECTLY ON A BARE METAL SURFACE.

Before plugging the CMEM memories into your S-100 system, it will be necessary to configure the board for the system, by setting the on board DIP switches and jumpers as described in the following section.

2.2 OVERVIEW OF SWITCH AND JUMPER SETTINGS

Five groups of switches and five jumpers control the selection of all options on the CMEM board. Figure 1 shows the function of all switches and jumpers.

This section of the manual gives a brief explanation of the switch settings which is sufficient for most applications. The following three examples of typical configurations are given:

1. A "NO OPTIONS" mode, in which the CMEM is used in an 8 BIT computer, without the need for multiple memory banks or extended addressing, and without the need for the software-programmable write-protect window.
   THIS SIMPLE CONFIGURATION IS ALL THAT IS REQUIRED IN MOST APPLICATIONS. SEE FIGURE 2.

2. An example using the new 24-BIT EXTENDED ADDRESSING scheme found in new systems which make use of the features specified in the IEEE proposed S-100 standard. SEE FIGURE 3.

3. An example using the BANK SELECT option, which allows the computer to access multiple memory banks. This feature is used in most "pre-IEEE standard" systems where more than 64K bytes of memory are needed, or in certain multi-user systems. SEE FIGURE 4.

Detailed descriptions of the advanced data protection features, such as the WRITE PROTECT WINDOW and the POWER-FAIL INTERRUPTS are given in sections 2.2.10 and 2.2.11.

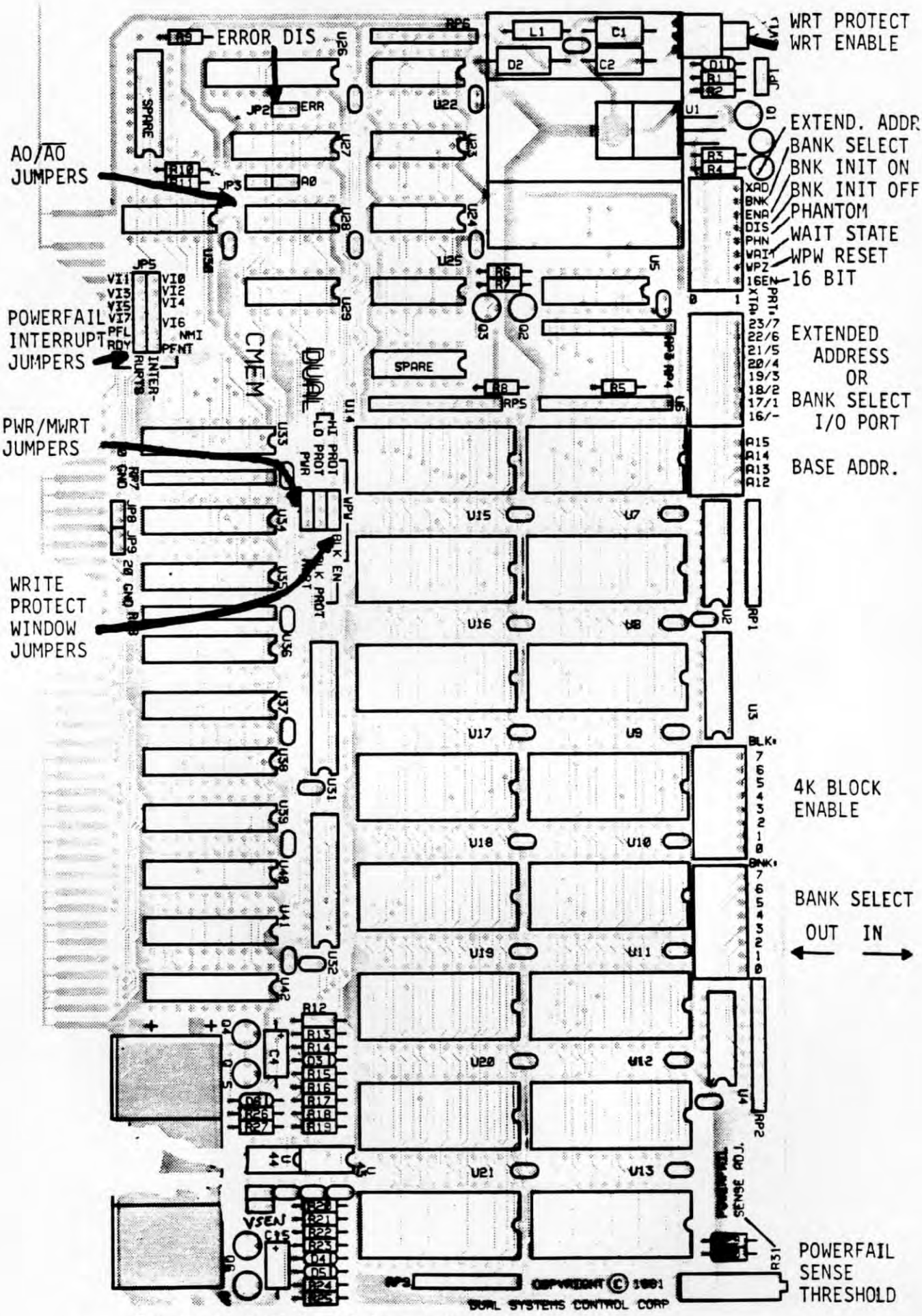


Figure 1. Switch and Jumper Overview

2.2.1 SETTING THE BASE ADDRESS (STARTING ADDRESS) (SWITCH S3, POSITIONS 1 THROUGH 4)

Positions 1 through 4 of switch S3 are used to select the starting address of the CMEM board. This address may be set for any 4K byte boundary within the 64K byte "global" address space (eg. 0, 4096, 8192, ..., 61440). The settings of these switches are independent of any extended addressing scheme (ie. bank select, phantom, 24-bit extended addressing, or no extended addressing at all). Positions 1 through 4 of SP3 merely specify the starting address of the CMEM board WITHIN THE 64K BYTE ADDRESS SPACE CURRENTLY BEING ACCESSED BY THE COMPUTER.

The following are the possible switch settings and the resulting starting address for each:

	S3 SWITCH POSITION: 1	2	3	4	STARTING ADDRESS:	
ADDRESS BIT:	A15	A14	A13	A12	DECIMAL	HEXIDECIMAL
	0	0	0	0	0	0000H
	0	0	0	1	4096 (4K)	1000H
0=OFF	0	0	1	0	8192 (8K)	2000H
	0	0	1	1	12288 (12K)	3000H
1=ON	0	1	0	0	16384 (16K)	4000H
	0	1	0	1	20480 (20K)	5000H
	0	1	1	0	24576 (24K)	6000H
	0	1	1	1	28672 (28K)	7000H
	1	0	0	0	32768 (32K)	8000H
	1	0	0	1	36864 (36K)	9000H
	1	0	1	0	40960 (40K)	A000H
	1	0	1	1	45056 (44K)	B000H
	1	1	0	0	49152 (48K)	C000H
	1	1	0	1	53248 (52K)	D000H
	1	1	1	0	57344 (56K)	E000H
	1	1	1	1	61440 (60K)	F000H

```
********** I M P O R T A N T ! **********
*                                        *
*  MOST "PROBLEMS" WITH MEMORY BOARDS RESULT FROM THE ADDRESS   *
*  SWITCHES BEING SET INCORRECTLY.  CHECK THESE SWITCHES        *
*  CAREFULLY TO BE SURE THAT THE ADDRESS SPAN OF THE CMEM       *
*  DOES NOT OVERLAP WITH THE ADDRESS SPAN OF ANY OTHER BOARDS   *
*  IN THE SYSTEM                                                *
*                                                               *
*****************************************************************
```

ALSO: If the starting address of the CMEM is set to a sufficiently high value (eg 9000H or higher for a CMEM-32K), the memory may extend over the 64K upper boundary of the global address space (ie. above FFFFH). This will cause the extra memory beyond FFFFH to wrap around and begin at 0000H.

2.2.2 WAIT STATE (OPTIONAL, SP1 POSITION 6) "WAIT"

The WAIT switch is used to add an optional wait state, which is only required for VERY fast (eg. 8MHz) computer systems. The CMEM memories will run in virtually all 6MHz systems with NO wait state. THEREFORE, THE WAIT SWITCH SHOULD BE SET TO OFF IN MOST CASES. If the CMEM does not work in a high-speed system, this switch may be turned to ON and will cause the read or write cycle generated by the computer to be lengthened by one clock cycle.

2.2.3 ERROR DESELECT (JUMPER JP2) "ERR"

This jumper, when installed, will cause the CMEM to be deselected when the error line on the S-100 bus is activated. This signal is rarely used in present S-100 systems. THEREFORE, JUMPER "ERR" SHOULD GENERALLY NOT BE USED.

2.2.4 PHANTOM DESELECT (SWITCH SP1 POSITION 5) "PHN"

This switch, when turned ON will cause the CMEM to be deselected when the PHANTOM line on the S-100 bus is activated. If your system requires that the read/write memory be deselected in response to PHANTOM, this switch should be turned ON. OTHERWISE, PHN SHOULD BE SET TO OFF.

2.2.5 SETTING FOR 8-BIT OR 8/16-BIT OPERATION (SP1, POS 8) "16EN"

This switch, when ON, allows the CMEM to transfer data to and from the new 16-bit CPU's in either 8-bit or 16-bit chunks, depending on the state of the SXTRQ line of the S-100 bus. If SXTRQ is asserted while the CMEM board is addressed, and the 16EN switch is ON, then the CMEM will assert SIXTN (sixteen acknowledge) on the bus, and will transfer data in one 16-bit word. Generally speaking:

IF YOU HAVE AN 8-BIT SYSTEM (EG. Z-80), SWITCH "16EN" SHOULD ALWAYS BE TURNED OFF.
IF YOU HAVE A 16-BIT SYSTEM (EG. 8086, Z-8000 or 68000), "16EN" SHOULD BE TURNED ON.

2.2.6 ENABLING AND DISABLING 4K BYTE BLOCKS OF MEMORY (SWITCH SP4 POSITIONS 1 THROUGH 8) "BLK"

Switch SP4 is used to enable or disable 4K byte blocks of memory. Switch positions 1 through 8 correspond to memory blocks 7 through 0, respectively. When a switch is ON, its corresponding block is enabled. When OFF, its block is disabled. Block 0 is the lowest 4096 bytes of memory on the CMEM. Block 1 is the next, and so on. In a CMEM-8K there are only two blocks (blocks 0 and 1) while in a CMEM-32K, all 8 blocks are used.

The most common reason for disabling a block of memory is to create a "hole" in the memory address space to make room for a ROM (read-only-memory) or a memory-mapped I/O device (eg. a disk controller).

If the full memory capacity is desired, with no blocks disabled, the following switch settings should be observed.

BLK:	CMEM-8K	CMEM-16K	CMEM-32K
0	ON(ENABLED)	ON	ON
1	ON	ON	ON
2	OFF(DISABLED)	ON	ON
3	OFF	ON	ON
4	OFF	OFF	ON
5	OFF	OFF	ON
6	OFF	OFF	ON
7	OFF	OFF	ON

NOTE FROM THE ABOVE TABLE THAT IN ANY CMEM (EXCEPT THE CMEM-32K), ALL HIGHER BLOCKS MUST BE DISABLED, SINCE THERE IS NO MEMORY INSTALLED FOR THESE BLOCKS. IF THESE SWITCHES ARE ACCIDENTLY TURNED ON, THE CMEM'S BUS BUFFERS WILL TURN ON EVEN WHEN THE CMEM IS NOT BEING ADDRESSED, CAUSING A PROBABLE CONFLICT BETWEEN THE CMEM AND OTHER BOARDS IN THE SYSTEM.

2.2.7 SETTING THE CMEM FOR STANDARD "GLOBAL" 16-BIT ADDRESSING (NON-EXTENDED ADDRESSING)

In the majority of S-100 systems, the computer only needs to address a maximum of 64K bytes of memory. For these cases, extended addressing and bank select need not, AND SHOULD NOT, be used. To be sure that they are not invoked, the following switches should be turned off:

BANK SELECT ENABLE (SP1 POS. 2 -"BNK") = OFF
EXTENDED ADDR. ENABLE (SP1 POS. 1 - "XAD") = OFF

In this mode, there is no need to set switch SP5 as well as "ENA" or "DIS" of SP1, since their positions are not important.
THIS SIMPLE MODE IS USED IN MOST COMMON S-100 SYSTEMS.

An example of the switch settings for a system that is set up for simple 16 bit addressing is shown in figure 2. In this case, the user is configuring a CMEM-8K as follows:

STARTING ADDRESS AT 32768 (8000 IN HEXADECIMAL)
NO WAIT STATES
NO PHANTOM
8-BIT MACHINE
NO ERROR DISABLE
WRITE PROTECT WINDOW PORT ADDRESS AT 41 (HEX.) via SP2
NO VECTORED INTERRUPTS
BOTH 4K BYTE BLOCKS OF MEMORY ENABLED

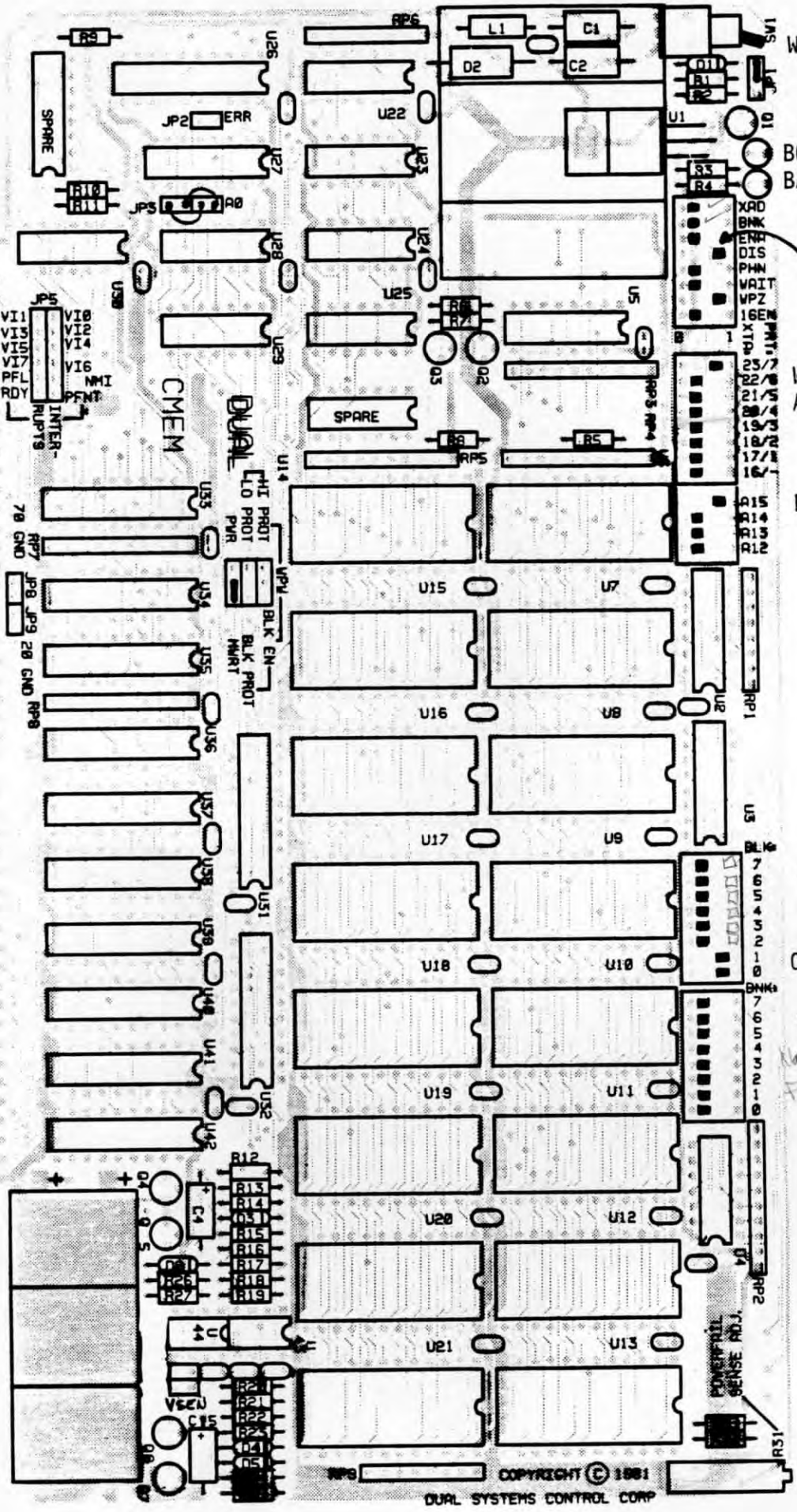


Figure 2. Example of simplest configuration of CMEM-8K

2.2.8 SETTING FOR 24-BIT EXTENDED ADDRESSING

If your computer system allows 24-bit extended addressing (as specified in the IEEE proposed S-100 standard), the CMEM memory may be located in any 64K byte section in the 16 megabyte address space. To use EXTENDED ADDRESSING, SET SWITCH SP1 POS. 1 (XAD) to ON, and set SP1 Pos. 2 (BNK) to OFF. Then, the extended address bits A16 through A23 may be set on switch SP2 (Positions 1 through 8 respectively). The CMEM will then be selected in use any time the address bits A16 through A23 match the switch settings of SP2 postions 1 through 8, respectively (assuming, of course, that the global address bits also match, and the correct 4K blocks are enabled).

As an example, if you would like a CMEM-32K to be accessed in the address range of:

260000 through 267FFF (Hexadecimal)

then switch SP2 should be set to 26 (Hex.), which is 00100110 in binary. Also, A12 through A15 should be set to 0000 (binary) for this example, using switch SP3 positions 1 through 4. THE SWITCH SETTINGS FOR THIS EXACT EXAMPLE ARE ILLUSTRATED IN FIGURE 3. THIS FIGURE DEPICTS THE FOLLOWING HYPOTHETICAL CONFIGURATION OF A CMEM-32K SET UP FOR EXTENDED ADDRESSING:

16 BIT COMPUTER
NO WAIT STATES
NO PHANTOM OR ERROR DISABLE
EXTENDED STARTING ADDRESS OF 260000 (HEX.)

Note that switch SP2 has the following two functions:

1. Sets the address of the BANK SELECT PORT or the EXTENDED ADDRESS, whichever mode was chosen via "BNK" or"XAD".

2. SP2's setting also also inherently determines the address of the WRITE PROTECT WINDOW control port, which automatically assumes an address of 1 above the setting (when the setting is for an even number), or an address that is equal to the setting (when it is for an odd number). SEE SECTION 2.2.10 FOR MORE DETAILS.

Hence, in the above example, since SP2 (XTA) is set to 26 (hex), the Write Protect Window output port automatically assumes an I/O address of 27 (hex).

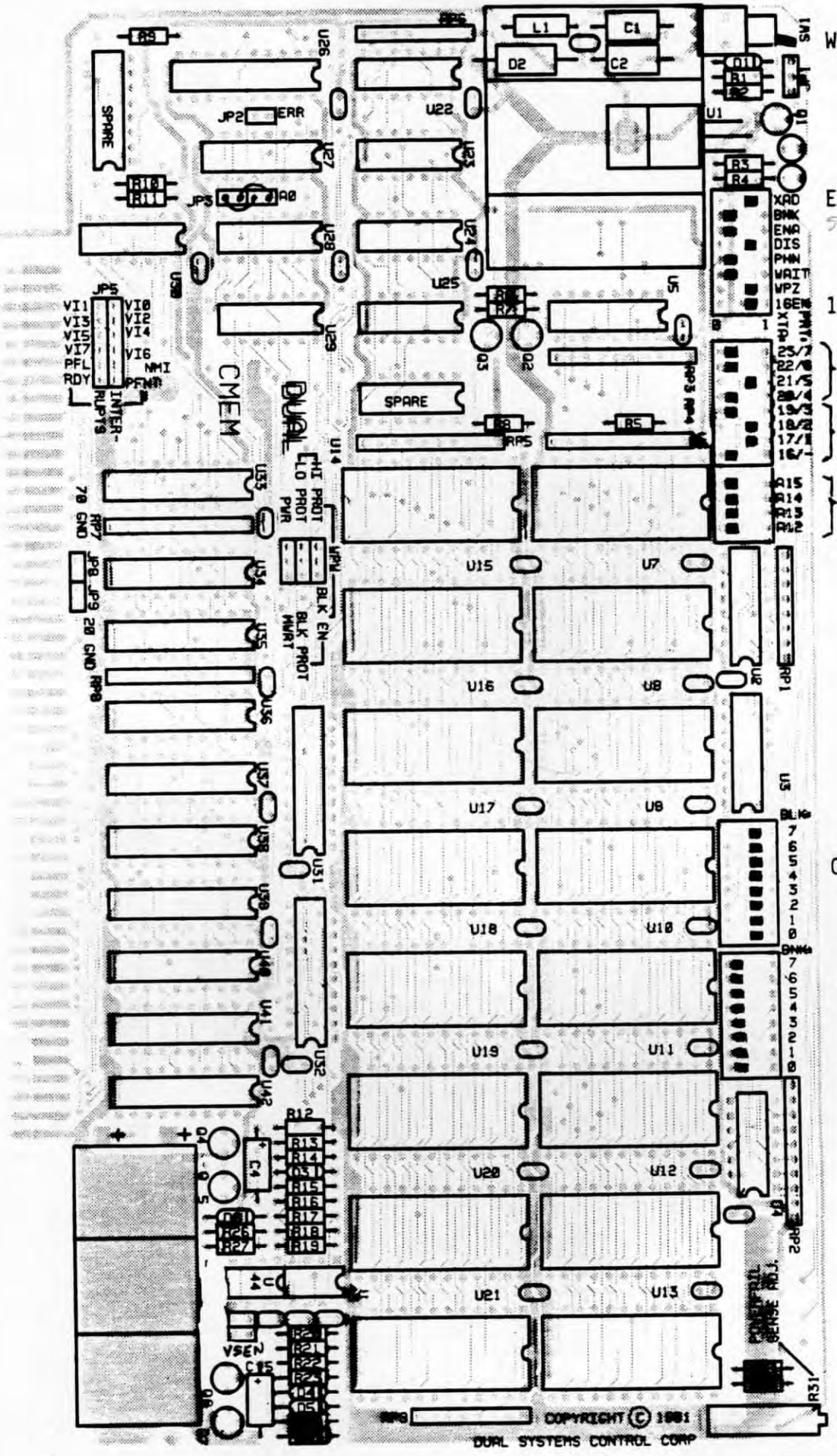


FIGURE 3. Example of CMEM-32K set up for 24-bit extended addressing in a 16-bit Computer

2.2.9 SETTING FOR BANK SELECT

Bank select is used in many large "pre-IEEE standard" S-100 systems. In this scheme, memory is organized in up to eight 64K byte memory BANKS (Bank 0 through Bank 7). This allows up to 512 K bytes (8 x 64K) to be addressed by the CPU.

One or more CMEM memory cards can be set to appear in a given bank (as long as the total memory in the bank does not exceed 64 K bytes). Also, a CMEM memory can be set to appear in more than one bank. Memory banks are activated and deactivated under software control via the bank select output port. Switch SP5 determines which bank(s) the CMEM appears in. Switch SP2 is used to specify the I/O address of the bank select output port. THIS ADDRESS MUST BE EVEN and is usually set to 40 (Hex.)

Setting SP5 so that a given bank is in the ON position places the CMEM board in that bank. In operation, when the computer outputs a byte to the bank select output port, the CMEM is either activated or disabled, depending on whether this byte has a 1 or a 0 at the bit corresponding to the switch that is in the ON position. For example, suppose the address of the bank select output port is set to 40 (hex) via switch SP2, and the CMEM is set, via SP5, to reside in banks 0 and 4, as shown in figure 4. Then, any time the computer outputs a byte to port 40, which has a 1 in either bits D0 or D4, the bank containing the CMEM is enabled, and the CMEM may now be addressed as if it were in a global (64K byte) address space. Later, if a new byte is sent to port 40, which has binary zeroes in both bits D0 and D4, the bank becomes deactivated and the CMEM will not be enabled, regardless of the state of the "global" address bits A0 to A15.

BANK SELECT IS INVOKED BY SETTING SP1 POS 2 (BNK) TO ON
AND SETTING SP1 POS 1 (XAD) TO OFF

The CMEM board may be set so that it AUTOMATICALLY COMES UP ENABLED when the computer is turned on (or a system reset occurs) by turning SP1 POS 3 (ENA) to ON and POS. 4 (DIS) to OFF.

The CMEM may be set to come up DISABLED by setting DIS to ON and ENA to OFF.

NOTE: DO NOT set BOTH DIS and ENA to ON at the same time.

Figure 4 shows an example of switch settings for a CMEM-16K set up for BANK SELECT, with the CMEM board set to appear in BANKS 0 and 4, and the BANK SELECT I/O PORT set for an address of 40(Hex.). The CMEM is set to come up ENABLED in this example. For this example the following bytes are typical of data that could be outputted to I/O addr. 40 to ENABLE or DISABLE the CMEM:

BINARY DATA:	D7 6 5 4 3 2 1 0	
TO ENABLE THE CMEM:	X X X 1 X X X 0	
	X X X 0 X X X 1	X=DON'T CARE
	X X X 1 X X X 1	
TO DISABLE THE CMEM:	X X X 0 X X X 0	

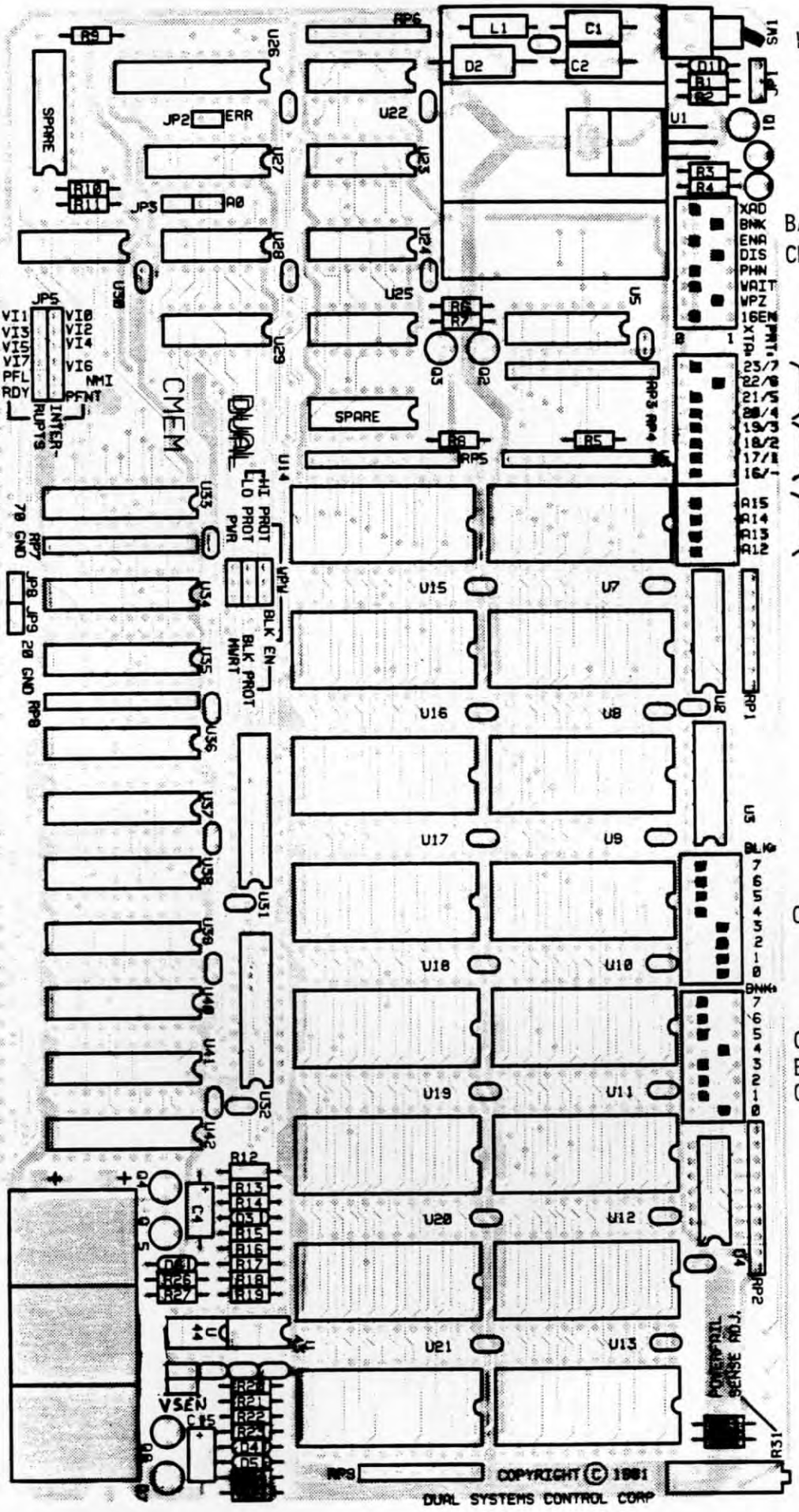
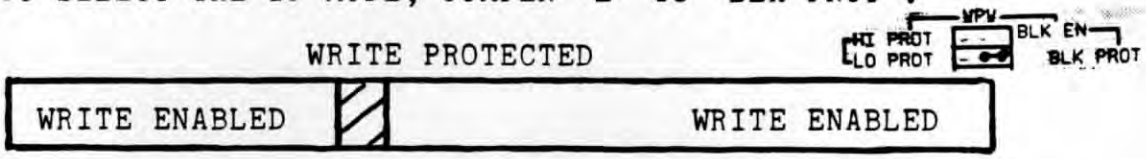


Figure 4. Example of CMEM-16K set up for Bank Select, and appearing in banks 0 and 4.

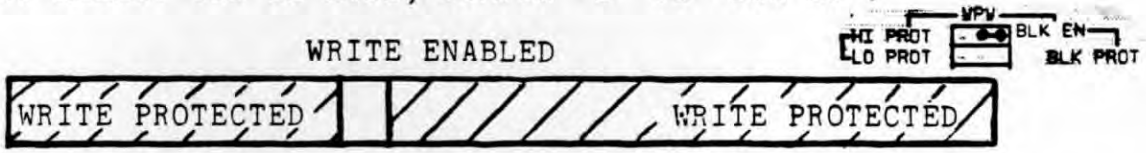
2.2.10 WRITE PROTECT WINDOW (WPW) JUMPERS

The software programmable WRITE PROTECT WINDOW (WPW) (Patent being sought) gives the Dual Systems CMEM memories a degree of data protection which approaches that of a disk or magnetic tape unit, while retaining the speed of a high-speed RAM. In fact, if properly used, the CMEM can be made to behave like an EPROM board, while having the advantage of instant writeability. With the WPW there are four basic modes of operation which are selected using the "WPW" jumpers shown in figure 1.

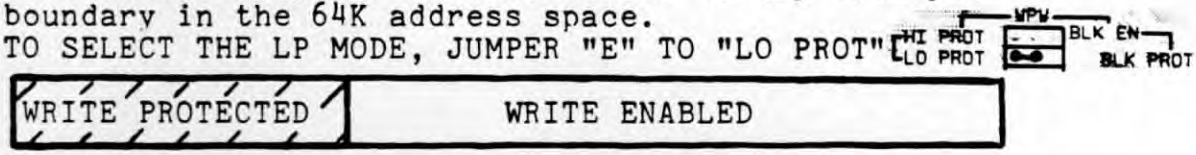
1. BP (BLOCK PROTECT) MODE - Write protects (prevents writing to) a 256 byte block of memory which can be programmed in software to occur on any 256 byte boundary in the 64K byte global address space, as shown below.
   TO SELECT THE BP MODE, JUMPER "E" TO "BLK PROT".



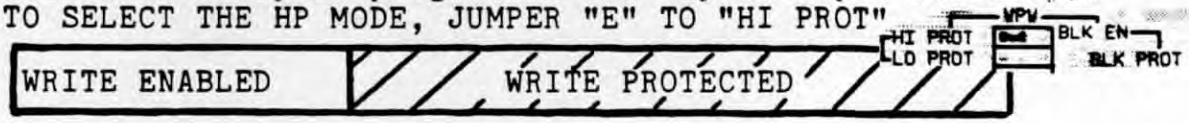
2. BE (BLOCK ENABLE) MODE - Write protects all of the CMEM EXCEPT for a 256 byte block of memory which can be software programmed to occur on any 256 byte boundary.
   TO SELECT THE BE MODE, JUMPER "E" TO "BLK EN".



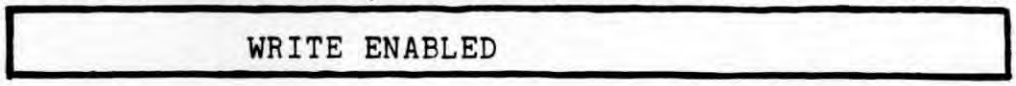
3. LP (LOW PROTECT) MODE - Write protects all addresses of the CMEM memory which are BELOW a specified address. This address may be set in software to any 256-byte boundary in the 64K address space.
   TO SELECT THE LP MODE, JUMPER "E" TO "LO PROT"



4. HP (HIGH PROTECT) MODE - Write protects all addresses of the CMEM memory which are AT OR ABOVE a specified address (which may be programmed for any 256 byte boundary).
   TO SELECT THE HP MODE, JUMPER "E" TO "HI PROT"



5. NO WPW - ALLOWS ALL OF THE CMEM MEMORY TO BE WRITTEN TO.
   TO SELECT THIS MODE, NO WPW JUMPERS SHOULD BE INSTALLED.



The starting location of the 256-byte block (modes BP or BE) or the boundary between the write-protected and write-enabled regions (modes LP or HP) are programmed easily in software by outputting a single byte to an I/O-mapped output port on the CMEM whose address is determined by the setting of switch SP2. This address is specified as follows:

WPW addr. = 1 + setting of SP2(PRT) IF SP2 SET FOR EVEN ADDR.

WPW addr. = setting of SP2 (PRT) IF SP2 SET FOR ODD ADDR.

If the CMEM has been configured for BANK SELECT mode, then the WPW address inherently assumes an I/O address that is 1 address above the bank select port. Note that since the bank select port must have an even address, THE WPW I/O PORT ALWAYS WILL ASSUME AN ODD ADDRESS as illustrated below.

EVEN ADDR. EG. 40	ODD ADDR EG. 41
BANK SEL PORT	WPW PORT

If EXTENDED ADDRESSING has been enabled on the CMEM, then the WPW address inherently assumes an I/O address that is the same as the most significant 8 bits of the extended address, if these bits represent an ODD number, or 1 above the extended address, if the most significant 8 bits represent an EVEN number. For example:

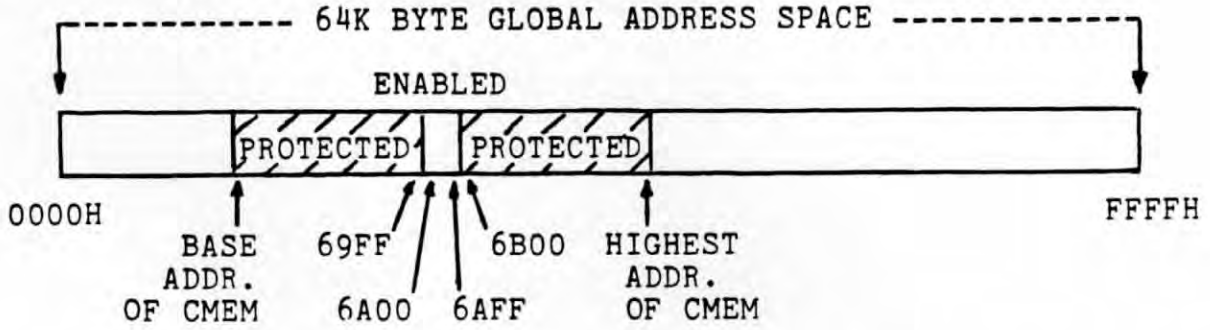
IF THE EXTENDED ADDRESS IS SET, VIA SP2, TO BE 26XX00 (HEX)
THEN THE WPW I/O ADDRESS WILL ASSUME A VALUE OF 27 (HEX)

or: IF THE EXTENDED ADDRESS IS SET, VIA SP2, TO BE 27XX00 (HEX)
THEN THE WPW I/O ADDRESS WILL ALSO ASSUME A VALUE OF 27

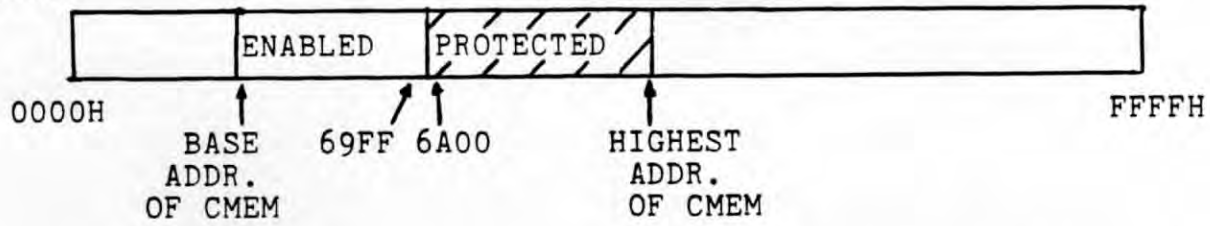
NOTE: X = don't care

The data byte outputted to the WPW I/O port determines the position of the write-enabled (or protected) block, or the position of the boundary between write-protected and write-enabled areas. This data byte may have any value from 00 (Hex) to FF (Hex), and specifies global addresses froom 0000 (Hex) to FF00 (hex), respectively. Hence, if the number 6A is outputted, the address 6A00 is specified.

If, for example, the BE mode has been jumper-selected, and the number 6A has been outputted to the WPW I/O port, then this will cause all of the CMEM memory to be write-protected EXCEPT ADDRESSES 6A00 through 6AFF, as shown below:



If, instead, the HP mode has been jumper selected, then CMEM memory locations BELOW 6A00 will be write- enabled, while locations AT and ABOVE 6A00 will be write-protected, as shown below:



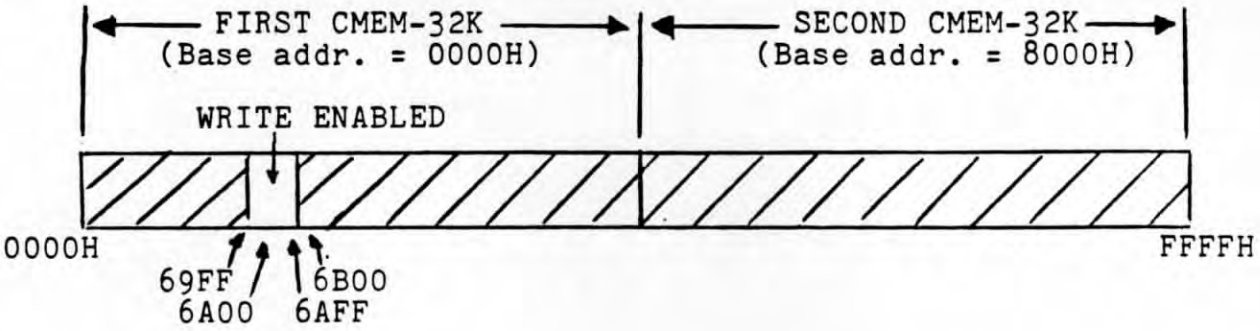
Note that the address controlled by the WPW I/O port is an ABSOLUTE ADDRESS within the 64K global address space, and is independent of the starting and ending location of the CMEM (as long as the address is contained somewhere in the address space occupied by the CMEM). This use of absolute addressing has the following advantages:

1. Ease of programming. For a WPW address of 6A00, you merely output "6A" to the WPW I/O port.

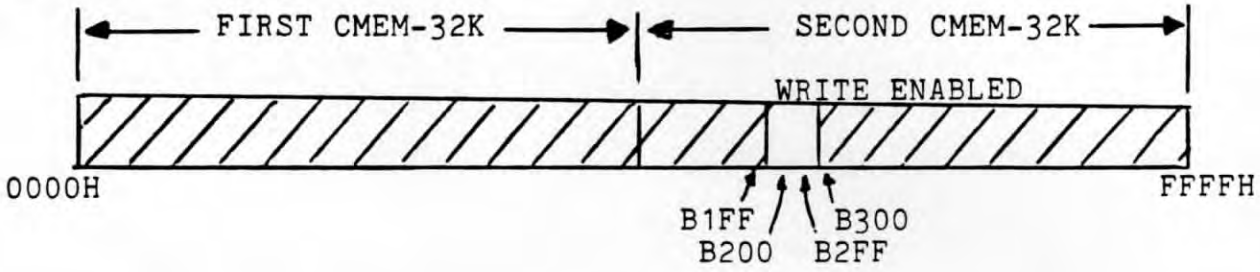
2. Enables a single write protect window address to span more than one CMEM. In this way a single byte outputted to the WPW I/O port can move the write protect window or boundary anywhere in the 64K byte global address space.

The following examples show how, using 2 CMEM-32K's, a single WPW address automatically controls the position of the WPW throughout the entire 64K byte global address space.

EXAMPLE 1 - BE MODE, WPW DATA BYTE = 6A Hex):

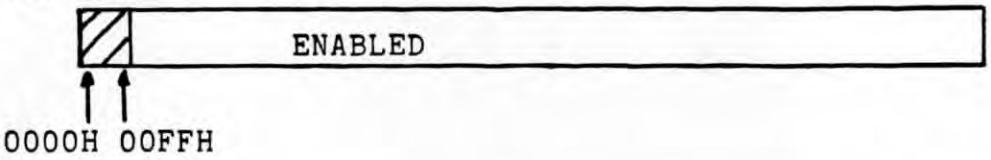


EXAMPLE 2 - BE MODE, WPW BYTE = B2:

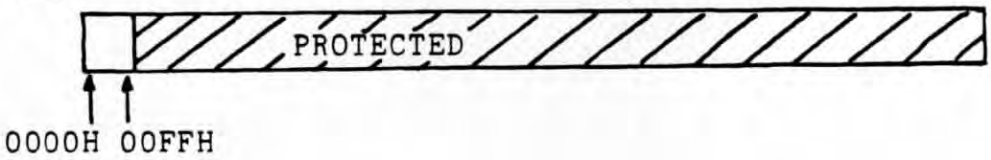


When the system power is first turned on, or upon system reset, the WPW port can be configured via switch SP1 POS 7 (WPZ) to come up reset to 00 Hex. This results in the following initial states for the WPW:

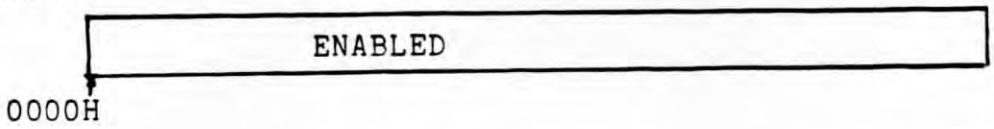
BP MODE:



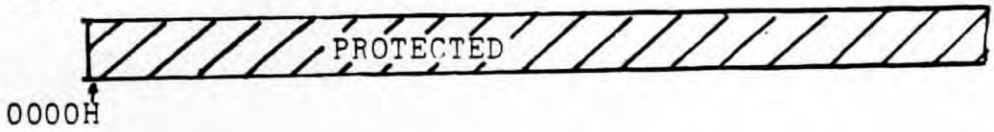
BE MODE:



LP MODE:



HP MODE:



These initial WPW states can be modified in software by outputting a byte to the WPW port, as discussed earlier in this section. For example, using the BE mode, the system can be made to come up with only the first 256 bytes write-enabled (Assuming the base address of the CMEM is 0000H). Then, under program control, any byte (let's say 3D) may be outputted to the WPW port whenever a piece of critical data needs to be stored in the CMEM at an address somewhere between 3D00 and 3DFF. After this data is stored, the program can return the WPW to its starting position (0000H) by outputting "00H" to the WPW port. THIS EXAMPLE ILLUSTRATES A MODE OF OPERATION WHICH PROVIDES GOOD DATA PROTECTION.

THE WPW IS IMPORTANT TO USE, IF A HIGH DEGREE OF DATA PROTECTION IS NEEDED.

SEE CHAPTER 3 FOR MORE DETAILS ON THE USE OF THE WRITE PROTECT WINDOW.

2.2.11. POWERFAIL INTERRUPT Jumpers (VIO-VI7, NMI, PWRFAIL, PFIN)

One important benefit of using nonvolatile high-speed memory is to allow the computer system to quickly store its status and any critical data at the first sign of an impending power failure.

Typically, when a computer system is turned off (or if a.c. power suddenly fails) the power supply filter capacitors have enough energy stored in them for 10 or more milliseconds of operation of the CPU and memory. During this short time, a suitably programmed computer system can execute an interrupt routine which stores all register contents in the CMEM. Then, when power is later restored, the computer can, if properly configured, BEGIN PROGRAM EXECUTION AT THE SAME PLACE IT LEFT OFF WHEN THE POWER STARTED TO FAIL. This is possible, since the program counter contents stored in the CMEM tell the address of the last instruction executed (at the time of the interrupt). This sequence is illustrated in figure 5.

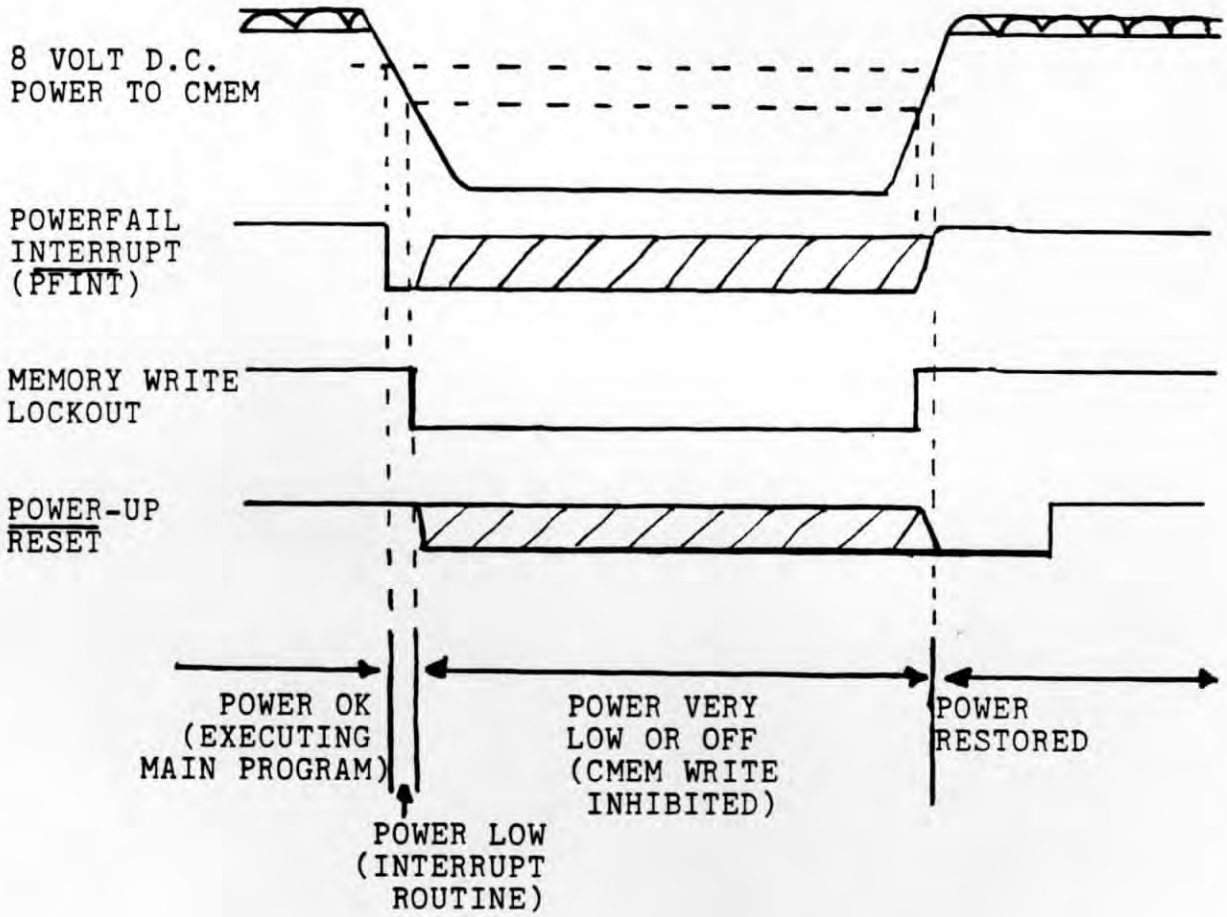


Figure 5. Power failure sequence, with power later restored

In order to cause an interupt to occur at the first sign of an impending loss of d.c. power, the POWERFAIL INTERRUPT jumpers on the CMEM must be used. These jumpers are installed on wire-wrap posts on the board, as shown in figure 6.

Two possible sources of power failure interrupts may be used:

1. The PWRFAIL pin on the S-100 bus of CERTAIN computer systems, which provides a signal telling that a.c. power has been lost. This signal unfortunately is not present in most present S-100 systems. THIS SIGNAL, IF PRESENT, IS AVAILABLE AT THE JUMPER POST "PFL" ON THE CMEM BOARD.

2. A circuit on the CMEM board, which senses the 8 volt power, can provide an interrupt signal (PFNT) when this voltage goes below a preset threshold (eg. 7.4 volts). PFNT IS AVAILABLE AT THE "PFNT" JUMPER POST ON THE CMEM.

The on-board power failure sensing circuitry (#2, above) is recommended for most systems, since the S-100 bus PWRFAIL signal is so rarely provided in commercial systems.

The interrupt signal source (either PFNT or PFL) may be used to trigger any of the following interrupts:

1. VI0 (Vectored interrupt #0 on S-100 bus)
2. VI1
3. VI2
4. VI3
5. VI4
6. VI5
7. VI6
8. VI7
9. NMI (Non-maskable interrupt on S-100 bus)

The type of interrupt selected depends on the type of software running on your particular S-100 system. In most systems which are dedicated to one particular task, and do not use disks, the NMI should be used.

To configure the board for a particular type of interrupt, it is necessary to install a jumper wire between PFNT (or PFL if that is chosen) and one of the interrupt destination posts listed above (eg. VI4 or NMI). Figure 6a shows a CMEM memory that has been configured to use the S-100 bus PWRFAIL signal to cause a non-maskable interrupt (NMI). Figure 6b shows a CMEM memory that has been configured to use its own internally generated power-fail interrupt (PFIN) to caused a vectored interrupt on VI4.

Chapter 3 discusses the use of these interrupts in more detail.

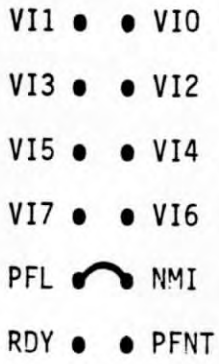


Figure 6.a. CMEM configured so that the S-100 Bus PWRFAIL signal causes a non-maskable interrupt.

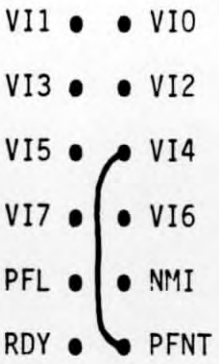


Figure 6.b. CMEM configured so that its own PFNT signal causes an interrupt on VI4 when power goes down.

2.2.12 A0, DELAY, CSEN and MWRT/PWR JUMPERS

The jumpers described in this section are ones which will rarely need to be changed from the factory settings. They are used as follows:

A0 CUTTABLE TRACES

The A0 jumpers (JP3) are actually cuttable Printed circuit board traces, and are only important in 16 bit computer systems which mix 8 and 16 bit data transfers. The traces are connected in such a way that the CMEM meets the IEEE-696 proposed S-100 standard, which requires the following relationship between BYTE and 16-bit WORD addressing:

> THE EVEN-ADDRESSED BYTE OF A 16-BIT WORD SHOULD BE GATED TO THE "DO" BUS
>
> THE ODD-ADDRESSED BYTE OF A 16-BIT WORD SHOULD BE GATED TO THE "DI" BUS

At one time, the IEEE proposed standard required that the exact opposite of the above be true. In other words, the EVEN addressed byte was gated to the DI bus and the ODD was gated to the DO bus. If the CMEM is used with a CPU board which conforms to that obsolete convention, the A0 jumpers may be changed as shown below.

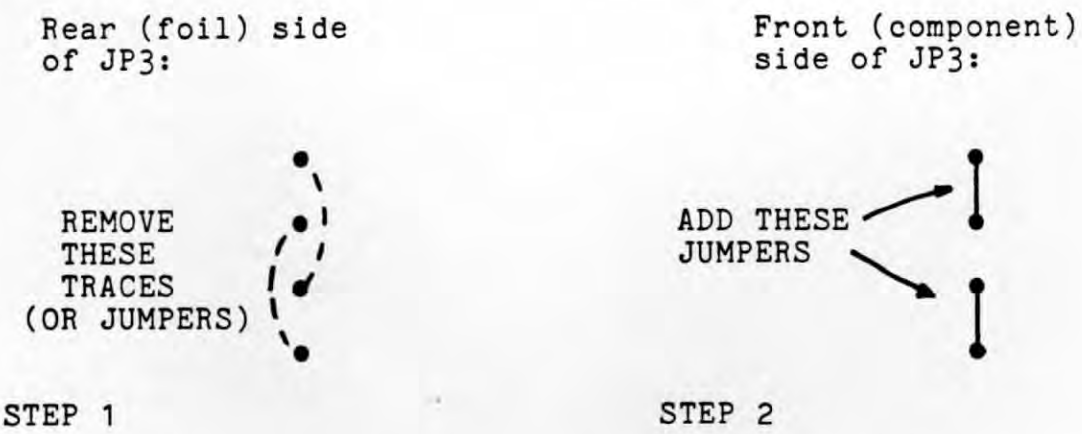


Figure 7. Reversing the order of the HIGH and LOW bytes.

DELAY jumper

The delay jumper serves to make the Write Lockout occur a fixed delay (2 milliseconds approx.) after the powerfail interrupt is generated, even if the +8 volt unregulated voltage has not fallen below the normal write lockout threshold (approx 7.0 volts). Furthermore, upon power-up, it prevents the memory from being written to until the power has stabilized (gone above the powerfail interrupt threshold (approx. 7.5v) and remained above the threshold for over 2 milliseconds.

The delay jumper should not normally be used, since it places much tighter timing constraints on any powerfail interrupt routine which may be used. Furthermore, upon power-up it may prevent writing when the system is trying to boot. For this reason, THE DELAY JUMPER SHOULD ONLY BE INSTALLED IF THE CMEM IS NOT BEING USED TO STORE THE BOOT PROGRAM OR OTHER PROGRAMS THAT ARE EXECUTED DURING THE FIRST FEW MILLISECONDS THAT THE SYSTEM HAS BEEN ON.

The DELAY jumper SHOULD be used in cases where data appears to be getting lost from the CMEM when the power is turned off.

The DELAY jumper should be installed as shown below:

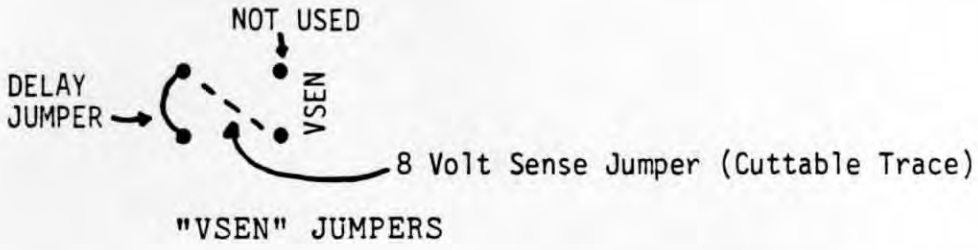


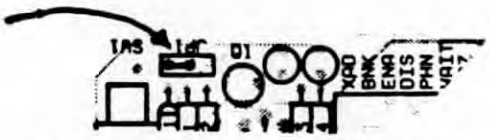
Figure 8. Adding the DELAY jumper

NOTE: In most cases, the "+8 VOLT SENSE" cuttable trace (on the foil side of the P.C. Board should be LEFT INTACT, since this trace enables the CMEM to write-protect all of its contents when the +8 volt S-100 supply goes below approximately +7 volts.

CSEN jumpers (JP1)

The CSEN jumper is a factory set jumper, and normally does not need to be modified. It is used to control the chip select lines on the memory. The factory set position of the CSEN jumper is as follows.

FACTORY SETTING



In this position, the memory chip selects are enabled whether or not the board is selected.* This allows for faster operation, since the memory chip selects may be enabled solely in response to address bits A11 through A15 without having to wait for the board enabled signal (BE). However, this "trick" results in slightly higher power supply current consumption, since two memory chips are always enabled at a given time, whether or not the board is being addressed.

If the CSEN jumper is moved into the alternate position shown below, the chip selects will only be enabled when the CMEM board has been selected. However, the access time will be approximately 270 nS (worst case), instead of 220 (the access time with the factory setting of CSEN).

The CMEM boards should work perfectly in all 4 megahertz (or slower) computer systems with the CSEN jumper in either position. In 5 Megahertz or faster computers, the CSEN jumper should be left in the factory set position. If slightly less power dissipation is desired, the jumper may be moved to the alternate position.

ALTERNATE SETTING

---

*NOTE: It is perfectly acceptable to enable the memory chips, even when the CMEM is not being addressed by the computer (via the higher order bits), since the following precautions were taken in designing the CMEM:

1. The write lines of the memory chips are not activated unless the board is being addressed.

2. The data buffers are not activated unless the board is being addressed.

MWRT/PWR jumpers

These jumpers are set at the factory to the MWRT position, which means that the CMEM will store data when the MWRT line on the S-100 bus is strobed. This factory setting is correct for the vast majority of S-100 computers. If your system does not use this signal, the memory will not work, and the jumper should be modified as shown below.

FACTORY SETTING ALTERNATE SETTING

NOTE: Before changing this jumper (because the CMEM appears not to work), first check to see that ALL SWITCHES have been set correctly on both the CMEM AND all other boards in the system. Almost all problems with new memory boards result from the switches being incorrectly set.

2.4. Adjusting the Powerfail Sense Threshold

The potentiometer at the right top corner of the CMEM may be used to adjust the threshold power supply voltage below which the CMEM causes an interrupt (and later locks out all attempts to write data into it).

The powerfail sense adjust is set at the factory, and normally does not need to be readjusted. It is factory set to cause an interrupt to be generated when the +8 volt unregulated input falls below 7.4 volts (actually 7.2-7.5V). This setting automatically causes the whole CMEM board to write-protect itself when the voltage falls further by approximately 0.4 volts. (Hence, the write lockout occurs when the input voltage falls below approx. 6.8-7.1 volts).

The powerfail sense threshold voltage should be DECREASED, BY TURNING THE ADJUSTMENT SCREW COUNTERCLOCKWISE if the following problems occur with the system:

A. The system sometimes "crashes", especially during voltage dips (eg. when another nearby piece of equipment is suddenly turned on)

B. The unregulated "8-volt" power on the S-100 bus normally measures less than 8 volts during normal operation. This sometimes occurs in heavily loaded systems.

The powerfail sense threshold voltage should be INCREASED, BY TURNING THE ADJUSTMENT SCREW CLOCKWISE if the following problem occurs with the system:

A. Data is lost from the CMEM when the power is turned off. This is usually caused by the computer erroneously writing to the CMEM as the CPU loses its power.

SECTION 3. PROGRAMMING THE CMEM FOR MAXIMUM DATA PROTECTION

When data stored in a CMEM appears to get changed when it should not, there are three possible causes:

1. The CPU board is issuing erroneous write commands to memory during the time that the system power is rising or falling.

2. The system "crashes" due to faulty software or power line dropouts or spikes, and deliberately writes "garbage" into memory.

3. The CMEM memory is defective.

The CMEM board attempts to prevent problem #1 by write-protecting all of its contents when the +8 volt bus power falls below approximately 7 volts during system power-down. Also, the CMEM refuses to allow data to be written into itself until the power rises above approx. 7.2 volts when the system is first turned on. However, in some computer systems, the system crashes at the first sign of power failure, while the bus power is still within its normal operating range. Clearly, the CMEM cannot know whether the data written to it under these circumstances is legitimate information or erroneous "trash". To solve this problem, try the technique outlined in the "MODERATE DATA SAFETY" section, below. If that fails, try the measures specified in the "HIGH DATA SAFETY" or "VERY HIGH DATA SAFETY" sections below.

Problem #2 above is more difficult to prevent, since the CMEM has no way of knowing whether data written to it is valid, or erroneous. The best way to protect critical data from being overwritten is to follow the guidelines in the "HIGH DATA SAFETY" section below. If this is inconvenient, and if the CMEM is being used for storage of programs only (with no data which has to be changed during execution), the ultimate degree of protection may be invoked by turning switching the large "PROT" switch on the upper left corner of the CMEM board to the "PROT" position. This WRITE-PROTECTS THE ENTIRE BOARD, causing it to behave virtually the same as an "INSTANTLY WRITABLE EPROM BOARD". This is discussed further in the "VERY HIGH DATA SAFETY" section below.

Problem #3 above is fairly unlikely. If all of the above measures fail to prevent data from being "lost" during power-off periods, the CMEM should be returned to DUAL SYSTEMS for repair or replacement.

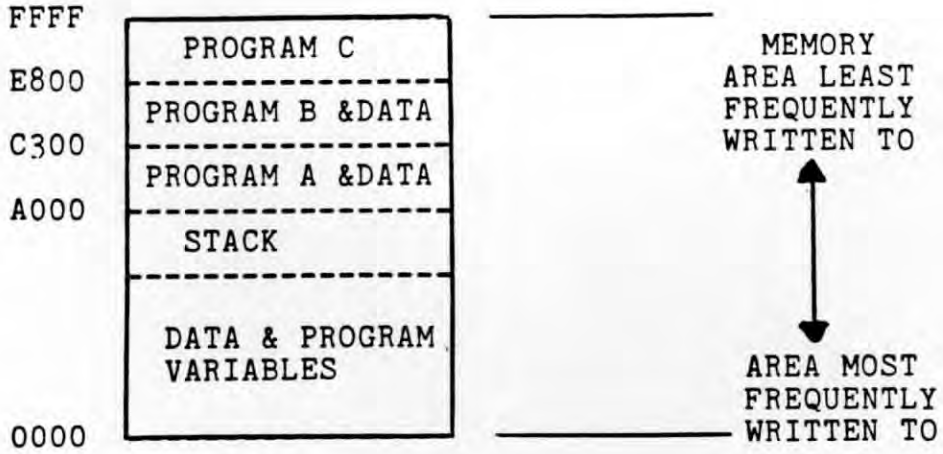
3.1 MODERATE DATA SAFETY

Moderate protection of data and programs is inherent in the CMEM memories, even without following special instructions. Since the CMEM memory write protects itself automatically when the power falls below its normal operating range, programs and data will remain intact under most circumstances, even if the system power is turned on and off thousands of times - AS LONG AS THE COMPUTER DOES NOT CRASH BEFORE THE POWER FALLS OUT OF RANGE.

If, however, data is occasionally lost during power shutdowns, the powerfail adjust may be readjusted by turning the potentiometer clockwise, a QUARTER TURN at a time, as described in section 2.4, and then rechecking the board's operation.

3.2. HIGH DATA SAFETY

The WRITE PROTECT WINDOW (WPW) can be used to prevent the majority of instances of data loss caused by system crashes. Basically, a good way to use the write protect window is to use the "HIGH PROTECT" mode* (see section 2.2.10) and turn the WPZ switch to ON. This causes the CMEM board to come up fully write protected. Then, the power-up routine should have as its first instruction an OUT command to change the write protect boundary to allow writing to the desired areas of memory. Once writing to the CMEM has been completed, another OUT instruction should be included in the program which again write protects the entire region of memory where the critical data is stored. This is illustrated by the following example.



MEMORY MAP OF ADDRESS SPACE

*Alternately, the LOW PROT mode could be used, depending on where the important programs are located.

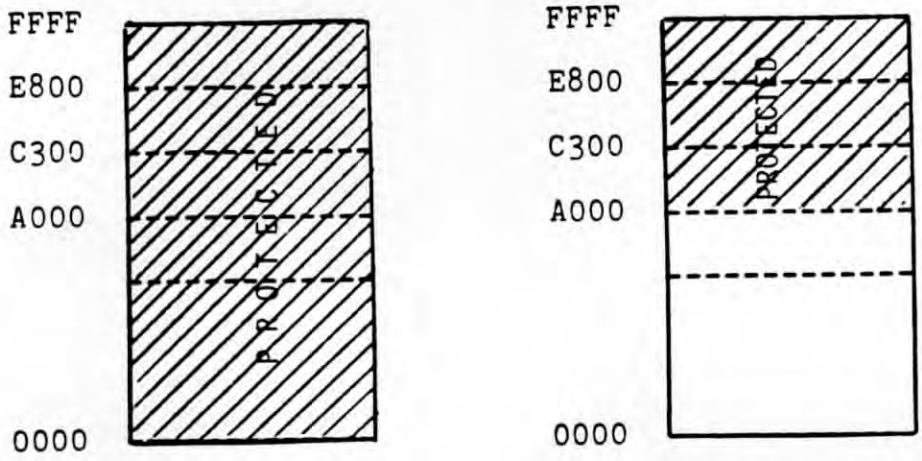
In this example, let us assume that the area from A000 to FFFF rarely or never has to be written to. The following is a fairly typical sequence of events.

1.) The system is turned on. Since the HIGH PROTECT mode is being used, and the WPZ switch is on, the entire nonvolatile memory (in this case, 2 CMEM-32K's) comes up fully write protected (but fortunately still READABLE), as shown above.

2. Let's say that the power-on routine is PROGRAM C. The first line of this program might then be a statement to move the WPW so that the area from 0000 to 9FFF is now write enabled, to allow for proper program execution. In other words, all memory at or above A000 is write protected. The following 8080 assembly language instructions would accomplish this:

```
MVI     A,0A0H          ;OUTPUTS THE BYTE A0 (HEX)
OUT     081H            ;TO THE WPW PORT (ADDR=81)
```

This would cause the WPW to move as shown below:



1.POWER FIRST TURNED ON 2.AFTER OPENING WINDOW

3. Now the computer will be able to execute the remainder of the power up routine. After this, other programs (eg. PROGRAM B or PROGRAM A) can be executed. During execution, the WPW should be moved as much as is practical, so as to write protect any memory which does not have to be written to during execution. The control of the WPW can be done either by the operating system (it will have to be modified to use the WPW) or manually, using the monitor or using BASIC's out statement.

4. After program execution is complete, the WPW should be

reset so as to protect as much memory as possible. If possible, the very last statements should be,

```
MVI     A,000H
OUT     081H            ;PROTECT ALL OF MEMORY
```

For maximum protection, this "closing of the window" should be incorporated into a power-down interrupt routine. This routine should be entered using the NMI, which can be generated by the CMEM (see section 2.2.11).

The above is merely an example of the strategies which can be employed to provide maximum protection of programs and data stored in CMEM's. There are many other possibilities, using the various modes of the WPW. The exact choice of protection strategy will depend on the type of system (ie. whether disk-based or not, whether CP/M operating system, etc.)

The task of developing software for controlling the WPW is quite involved. In some cases, for example, two CMEM's may have to be jumpered for different WPW modes (eg one set for LOW PROTECT and one for HIGH PROTECT) in order to obtain the necessary flexibility.

3.3. VERY HIGH DATA SAFETY

For the highest degree of data protection, the CMEM may be totally write protected, and will then behave essentially like an "instantly writable EPROM board". For this mode of operation, the following should be done:

1. Store the desired programs or data in the CMEM.
2. Turn the "PROT" switch (upper left corner of board) to the "PROT" position. The memory is no longer writable.

Once the CMEM is write-protected in this manner, it is immune from any accidental erasures, and should hold data until the batteries are dead (minimum 1 year, typically 2-5 years after date of purchase.).

To alter these stored programs, simply turn the PROT switch OFF, and make the necessary changes. Then turn it to PROT again.

NOTE: This "fully protected" mode can only be used in systems in which other memory exists, besides the protected CMEM. This other memory must be writable, since virtually all software requires some read/write RAM for execution.

SECTION 4. THEORY OF OPERATION

The CMEM non-volatile memory boards all have the following 10 basic sections.

1. Upper and lower MEMORY ARRAYS
2. DATA BUFFERS and control circuitry
3. ADDRESS BUFFERS and control circuitry
4. EXTENDED ADDRESSING circuitry
5. BANK SELECT circuitry
6. BOARD ENABLE circuitry
7. WRITE PROTECT WINDOW (WPW) circuitry*
8. WAIT STATE generator
9. BATTERY BACKUP and POWERFAIL sensing circuitry
10. Powerfail INTERUPT generator

Figure 4.1 is a block diagram of the CMEM memory board. Each of the above sections is described separately.

4.1. Memory arrays

The memory integrated circuits in the CMEM are Hitachi HM6116 or similar chips. They are arranged in two arrays, as illustrated in figure 4.1 and 4.2b. This structure makes either 8 bit or 16 bit wide data transfers convenient, which is necessary for compliance with the proposed S-100 specification (I.E.E.E 696).

The upper array contains the byte of data which is gated to the DI bus if 16-bit transfers are done (i.e. with 68000 or other 16 bit processors), or the ODD address (A0=1) if 8-bit transfers are used (i.e. 8080 and Z80 processors). The lower array is gated to the DO bus for 16 bit transfers, or the EVEN address (A0=0) for 8-bit transfers. A further discussion of this convention for data transfers on the S-100 bus is contained in the IEEE-696 proposed specification.

4.2. Data Buffers and Control Circuitry

Figure 4.2a shows the buffer control circuitry. Figure 4.2b is a simplified diagram showing the logic of the data buffers.

For 8-bit memory read operations, buffers A and B are used (for reading even and odd memory addresses, respectively). For example, if an EVEN memory address is being read, buffer B is enabled. The logic equations in figure 4.2b show that buffer B is enabled by the following conditions:

*Patent being sought

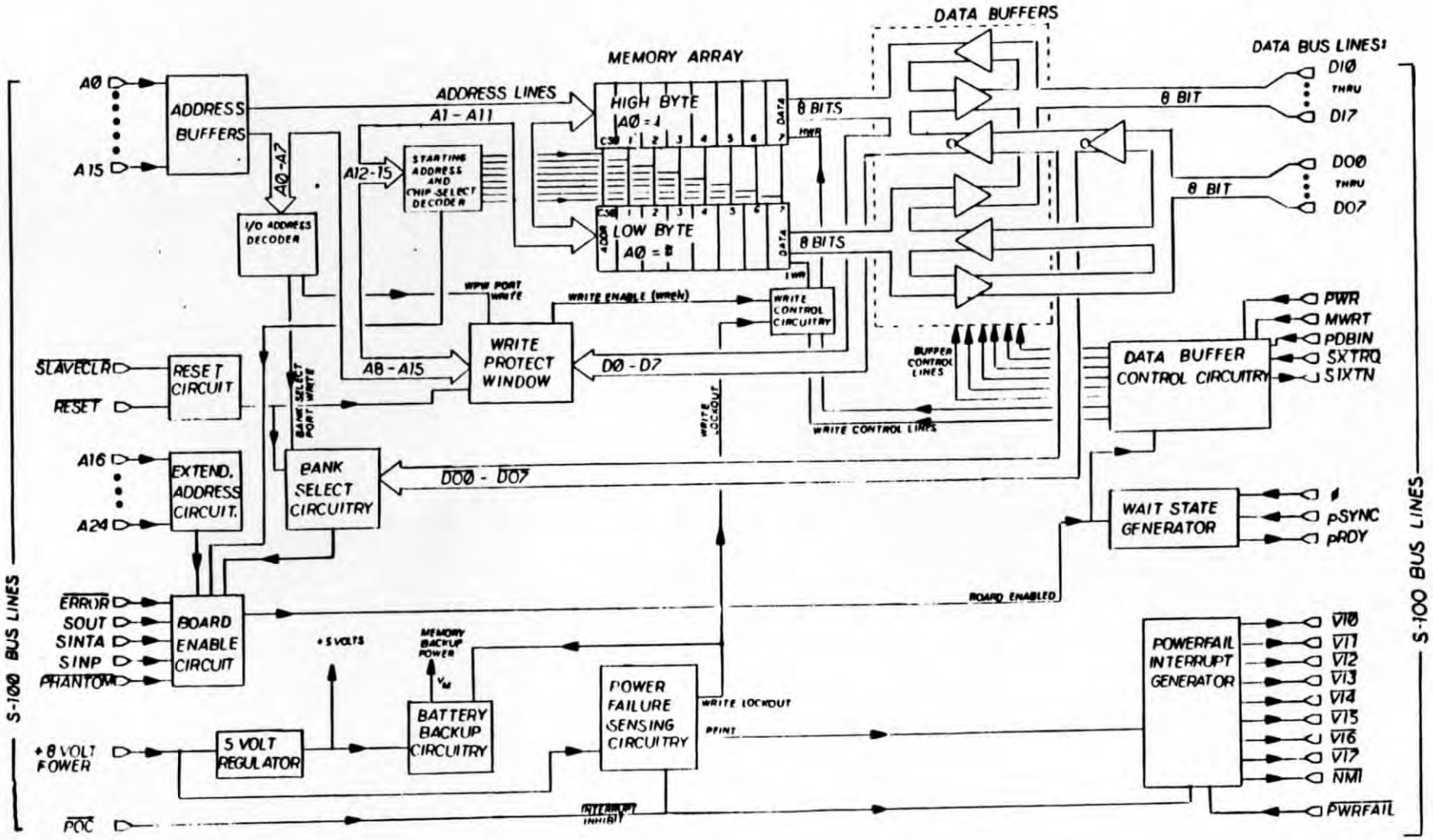


Figure 4.1. Block Diagram of the CMEM series of Nonvolatile Memories

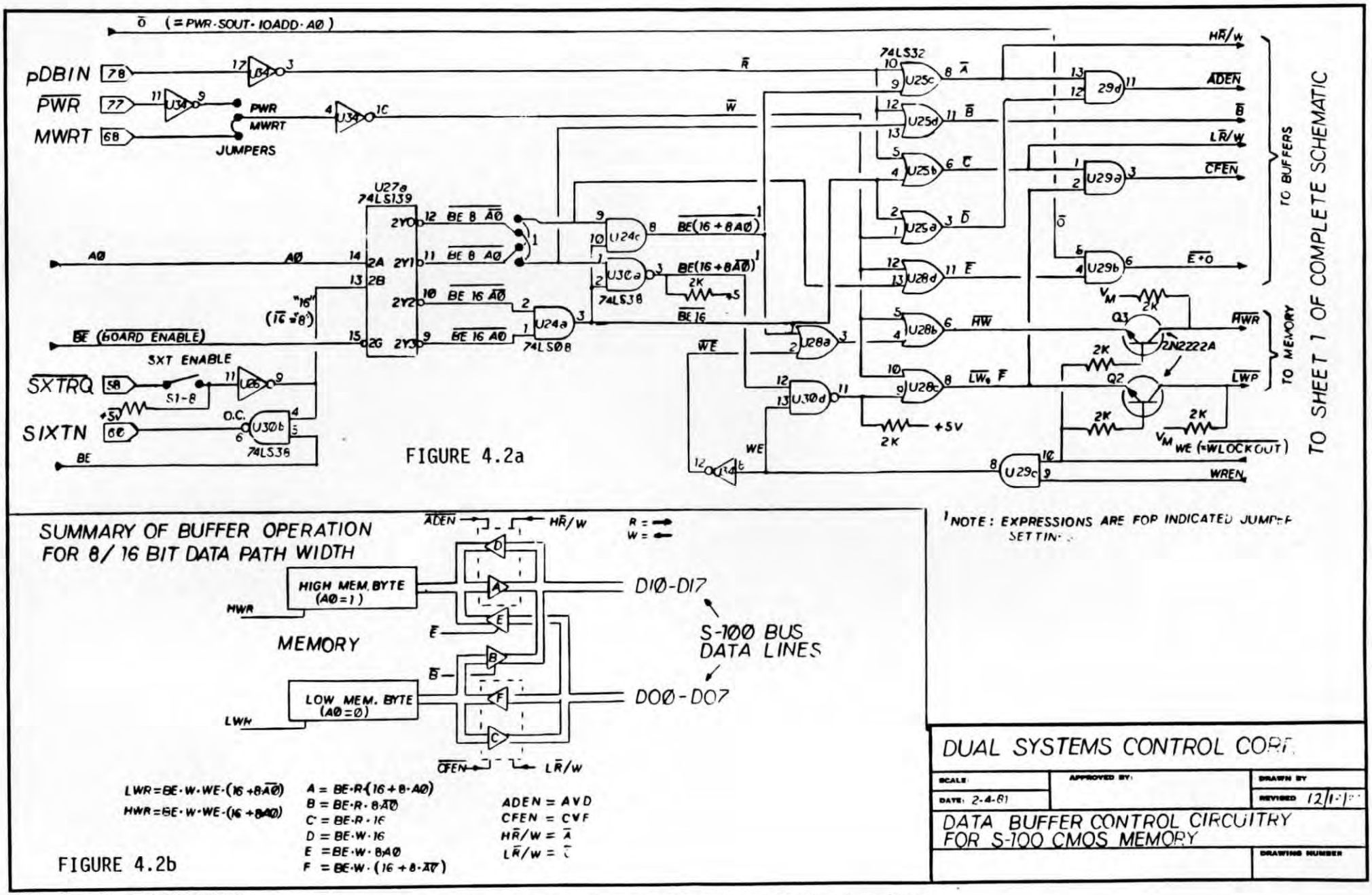


Figure 4.2a. Circuit diagram of data buffer control circuitry.
b. Block diagram of data buffer structure, showing 8/16-bit data path scheme.

$$B = BE \cdot R \cdot 8 \cdot \overline{A0}$$

In other words, buffer B is turned on when:

1. The CMEM board is being addressed (BE=1)
2. A READ operation is being done (R=1)
3. A BYTE transfer is desired (as opposed to 16 bits)
4. An EVEN address is being addressed (A0=1)

For 8-bit memory WRITE operations, buffers F and E are used for writing to EVEN and ODD addresses, respectively.

For 16-bit memory READ operations, buffers A and C are simultaneously used, and the S-100 bus lines DI0-DI7 and D00-D07 are all used as one 16-bit data bus.

For 16-bit memory WRITE operations, buffers D and F are both simultaneously used, and transfer data from the 16 S-100 data lines (DI0-DI7 and D00-D07) into both CMEM memory arrays at the same time. For 16-bit wide data transfer, address bit A0 is ignored.

4.3. Address Buffers and control circuitry

Address lines A0-A15 from the S-100 bus are buffered by IC's U36 and U38. From these buffers, address lines A1-A11 are fed simultaneously into all of the memory IC's (since each memory holds 2^{11} (2048) bytes). Address line A0 goes to the data buffer control circuitry, where it is used to select whether the upper or lower memory arrays will be accessed. Address lines A12-A15 are fed into the starting address and chip select decoder circuitry. Address lines A0-A7 are also fed into the I/O address decoder circuitry, and A8-A15 are fed to the write protect window circuitry.

The starting address and chip select decoder is basically composed of an adder (U2) and two decoders (U3 and U5). The adder is used to compare address bits A12-A15 with the base address switch settings (switch S3). The adder effectively subtracts these two 4-bit numbers, and causes the board to be enabled when the S4 output of the adder is zero. The other three outputs of the adder (S1-S3) are fed to the chip select decoder, U5. This decoder has 8 outputs which are used to enable the 8 memory chips which make up each array. The corresponding chips in the two arrays have chip selects which are tied together. This adder/decoder scheme allows the CMEM board to start on any 4K byte boundary. U3 is another decoder, which is used in conjunction with switch S4 to allow any 4K byte block of memory to be disabled. When a given switch in S4 is turned on the corresponding 4K byte block of memory is enabled.

4.4 Extended Addressing Circuitry

This circuitry, composed mainly of integrated circuit U33, allows the CMEM to respond to a 24-bit extended address. U33 is an 8-bit magnitude comparator which compares address bits A16-A23 on the S-100 bus with the settings of the switches in DIP switch S2. When the two are equal, and if the XAD switch in S1 is ON, the board is enabled.

4.5 Bank Select Circuitry

The bank select circuitry is basically a 1-bit port, which enables the CMEM when it is set to a "1", and disables it when set to "0". The port is basically made up of flip-flop U23a, and is written to when the I/O address bits (bits A0-A7) match up with the settings of the switches in S2. The flip-flop is set to a "1" whenever the data word (on lines D00-D07) has "1's" at any bit locations corresponding to the switches in S5 that are in the ON position. Basically, this is done by passing the complements of D00-D07 through the eight switches in S5 and into an 8-input NAND gate. Hence, if any bit for which a switch is closed is a "1" the board is enabled. This enable enable signal is only fed to the board enable circuitry when the BNK switch in S1 is ON.

4.6 Board Enable Circuitry

The board enable circuitry is basically an 8-input NAND gate (U22) whose output enables most of the data buffers, and other circuitry on the board. The following conditions are required for the board to be enabled:

1. S-100 Phantom signal is not active (or S1-5 is OFF)
2. S-100 SINP signal is not active
3. S-100 SINTA signal is not active
4. S-100 SOUT signal is not active
5. S-100 ERROR signal is not active (or JP2 is open)
6. Extended address is correct (or XAD switch is OFF)
7. CMEM is in selected bank (or BNK switch is OFF)
8. 4K block enable signal from address control circuit is active (see section 4.3).

Each of the eight conditions above corresponds to an input of NAND gate U22. When all eight inputs are high, the BOARD ENABLED signal (see fig. 4.1) is activated.

4.7 Write Protect Window (WPW) circuitry*

The write protect window basically compares the high byte of the 16 bit global address (A8-A15) with the data stored in the WPW port (register U31). The comparison is done with an 8-bit binary magnitude comparator (U37). U37 has two outputs, "P=Q" and "P Q". These two outputs and their complements are fed to the four jumper posts which select the WPW functions. The "P=Q" output goes to the BLOCK PROTECT jumper. Since this line goes low when P=Q (i.e. when address bits A8-A15 match the byte outputted to the WPW port), it disables writing to the CMEM in a 256 byte block of memory specified by the WPW port. The "P=Q" output does the exact opposite, and is used whenever the BLOCK ENABLE jumper is enabled. The "P Q" output goes to the LO PROTECT jumper, and prevents the CMEM from being written to whenever A8-A15 is less than the data byte in the WPW port register (U31). The "P Q" output goes to the HI PROTECT jumper, and write protects the CMEM whenever A8-A15 is greater than the contents of U31. To select any of these four WPW modes, one of the above jumper posts is connected to the "WREN" line, which goes to the write control circuitry.

4.8 Wait State Generator

The wait state generator merely negates the pRDY line on the S-100 bus for one extra clock cycle when the board is selected (assuming, of course, that the WAIT switch is turned on). It consists of a flip-flop (U23b) which is clocked by $\overline{9}$ on the S-100 bus, and uses the pSYNC signal as a data input. Its output is NANDed with the Board Enable line and is fed to the pRDY line. Hence, when selected, the wait state generator pulls the pRDY line low for one clock cycle after pSYNC occurs.

4.9 Battery Backup and Powerfail Sensing Circuitry

The powerfail sensing circuitry is composed of two similar voltage comparator IC's, U43 and U44. Both comparators sense the +8 volt power supply voltage which is present on the S-100 bus and is used to power the CMEM.

The first comparator, U43, and its associated components, are set to create a high-going output signal when the voltage goes below approximately 7.4 volts (slightly below the I.E.E.E specified minimum voltage of 7.5 volts). This output goes to the powerfail interrupt generating circuitry, which is described in section 4.10. The threshold for this interrupt is set by the POWERFAIL THRESHOLD potentiometer (R31).

*Patent Being Sought

The second comparator, U44, and its associated components are fed from a voltage divider network, so that its threshold voltage is approximately 0.4 volts below the threshold for U43. In other words, U44 produces a high-going output signal when the +8 volt supply goes below 7.0 volts. This output serves the following two purposes:

1.) It locks out all attempts to write data to the CMEM, thereby protecting the CMEM from possibly erroneous write commands from the failing (due to power loss) CPU.

2.) It switches the memory array chips from regular power to battery power, so that the data is protected after the system power completely fails.

The write lockout function (item 1) is done when U44 activates the WRITE LOCKOUT line, which goes to the write control circuitry, preventing any write commmands from reaching the memory chips.

The switch to battery power (item 2) is done with the aid of a transistor switch (Q6), which disconnects the main (5 volt) power from the memory arrays, and lets the battery voltage be coupled to the memory by diode D5. In the case where nickel-cadmium rechargeable batteries are used, the charging current is simply removed, and the battery current automatically flows, through resistor R23, into the memory chips.

4.10 Powerfail Interrupt Generator

The powerfail interrupt generator is simply an open-collector transistor which can be connected (by means of jumpers) to any selected interrupt line on the S-100 bus. This transistor is simply turned on when the output of U43 goes high (when the power goes below 7.4 volts), generating the PFNT signal.

Figure 4.3 shows the timing of the signals which occur in the powerfail sensing and interrupt circuitry.

Warranty and Service

Dual Systems Control Corporation guarantees its products, under normal use and service as described in the manufacturer's product literature, free from defects in material and workmanship, for a period of one year from date of shipment. This warranty is limited to the repair or replacement of the product, or any part of the product found to be defective at the manufacturer's factory, when returned to Dual Systems Control Corporation, transportation charges prepaid by customer. This warranty does not apply to any equipment that has been repaired or altered, except by Dual Systems Control Corporation, or which has been misused or damaged by accident. In no case shall the manufacturer's liability exceed the original cost of the product.

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