PARTS LIST

72	16 Pin Low Profile sockets
1	14 Pin " " socket
4	Heatsinks (w/hdwr.) for regulators
64	.01 Mfd. Disc caps
9	10 Mfd. Tantalum caps
2	2.2K Pull up resistors
4	7805 5VDC Regulators
64	2112-1 Low power static RAM
5	74LS367 (or 8T97) Tri-state buffers
2	74S138 (or 74LS138) 3 to 8 TTL decoders
1	74LS10 TTL dual 3 input NAND gate
1	Printed Circuit Board

GENERAL CONSTRUCTION HINTS

For soldering we recommend a 32 Watt soldering pencil. DO NOT use a soldering GUN !!! Use small diameter (such as 22 GA.) rosin core 60/40 alloy solder.

Keep your soldering pencil tip CLEAN with a wet sponge or cloth.

After such components as resistors or capacitors have been soldered, use a small pair of diagonal cutters to remove the excess lead length.

Observe all capacitor polarities.

If you notice any discrepencies between the parts received and the parts listing, please notify DRC immediately.

LIMITED WARRANTY

DRC Electronics warrants all components in this kit to be free from defects in material or workmanship for a period of 90 days. The defective part must be returned to DRC and will be replaced at no charge. Any board purchased as a kit which malfunctions during the warranty period which has not been subject to abuse and that has been assembled with reasonable care will be repaired or replaced at no charge.

Any unassembled kit purchased from DRC may be returned within 14 days of receipt for a full "no questions asked" refund. The above 90 day warranty also applies to assembled kits sold by DRC.

Any board which is not covered by the above warranty will be repaired at a cost commensurate with the work required. This charge will not exceed $20 without prior approval.

This warranty is made in lieu of any other warranty either expressed or implied, and is limited in all cases to the repair or replacement of the kit involved.

INTRODUCTION:

The 8K. RAM kit you have just purchased is one of the best RAM bargains available to today's home computerist. We have gone to great lengths to combine the right mix of features that are most often required in an S-100 system. And yet, in no instance have we scrimped on quality just to save a few cents as you may have observed on some other kits now being sold by others.

FEATURES:

S-100 Buss Compatible.

Uses popular 21L02-1 Static RAM's

FULLY BUFFERED !!!

Addressable on 8K boundaries

500 ns RAM. No Wait states needed!

FOUR on board resulators that run cool.

PC Board is solder masked and silk screened.

Gold plated contact fingers for long life.

Supply lines are extensively bypassed.

Jumper selectable PHANTOM provided.

ALL sockets are included.

LOW current drain. (1.75 A. typical)

PDBIN strobe is used for reliable operation.

MWRITE is buffered to minimize loading.

PC board has large GROUND plane to reduce noise.

ASSEMBLY INSTRUCTIONS:

( ) Give the PC board a good visual inspection for any obvious shorts or opens. There should be none, but a few seconds spent here could save hours later.

( ) Using an ohmmeter insure that there are no shorts between Buss pins 1 and 50.

( ) Install and solder 16 pin sockets for IC #1 through 64. Note that there is a notch or indentation on each of the IC sockets. This should be oriented in the same direction as the notch shown on the silk screened component legend for each IC location.

( ) Install and solder 16 pin sockets for IC #65 through 67.

( ) Install and solder a 14 pin socket for IC #68.

( ) Install and solder 16 pin sockets for IC #69 through 73.

( ) Install and solder 64 .01 mfd disc caps in the locations shown on the silk screened legend.

( ) Install and solder two 2.2K resistors in locations marked R1 and R2.

( ) Install and solder the four 7805 voltage regulators and heatsinks using the hardware provided.

( ) Install and solder the nine 10 mfd caps for locations marked C1 through C9. Be sure to observe the polarity of each tantalum as indicated by the white dot on the silk screened legend and the lead marked + on the capacitor.

( ) Using any of the regulator mounting tabs as ground, measure the output from each of the 7805's when the board is installed in your system. The output pin on the regulators is the pin that is farthest to the right. The measured outputs should be between 4.75 and 5.25 VDC. Any out of spec regulators must be replaced prior to installation of the rest of the IC's.

( ) Install into their sockets the 64 2102-1 RAM chips (IC #1 through 64). Be careful not to bend any of the pins up under the chip while plusing them into the sockets. Also observe the notch on each of the RAM chips and orient them in the right direction.

( ) Install the optional DIP switch in socket #65, with switch #1 down.

( ) Install two 74S138 's in locations 66 and 67.

( ) Install a 74LS10 in location 68.

( ) Install five 74LS367 's in locations 69 through 73.

( ) Double check again that all IC's are oriented in the proper direction.

This completes assembly of the 8K RAM board.

USING THE 8K RAM BOARD:

There are eight different 8K blocks of memory available in an S-100 system. Your DRC 8K board may be strapped for any one of these eight. If you have an optional eight position DIP switch installed in location 65 then closing switch position #1 will select the first 8K (0000 through 1FFF Hex). Closing switch position 2 will select the second 8K block (2000 through 3FFF Hex) , and so on. A jumper wire may be used in place of a DIP switch in location 65. A wire between the bottom pin on the left hand side of the socket and the bottom pin on the right side corresponds to switch position #1 and would select the first 8K block. Close only one switch at a time.

Now that you have selected where your board will reside in memory, it may be installed in your system. Using either your front panel or system monitor check that you can examine and write into this memory (a few trial locations). If you notice a bit hung high or low look for a solder bridge, pin curled up under an IC, or a bad 21L02.

If you have a memory test, run it now. If you do not have a memory test then by all means GET ONE! A good test program is an invaluable diagnostic aid since more often than not a system problem can be traced to a memory problem. Due to the mind boggling number of combinations presented by a memory chip, there is no such thing as one all inclusive memory testing program. However, some we have found useful are located in Interface Age Jan. 1976, Interface Age Dec. 1976, and Popular Electronics March 1977.

It has been our experience over the last couple of years that ANY vendor's RAM chips may arrive defective. Granted it is a remote possibility (we buy the BEST parts we can find, factory direct) but it DOES happen occasionally. So you must be prepared for it. If you have found a bad byte of RAM, it is important to note which BIT is bad. Knowing the location of the bad byte will tell you which ROW the bad part is in. The top ROW on the board is the first 1K of RAM on the board while the bottom ROW is the 8th 1K block. Knowing which bit is bad will allow you to find the bad chip since the bits are arranged in COLUMNS and are numbered at the top of the board.

THEORY OF OPERATION:

The 21L02 RAM chips used on the DRC 8K board are arranged as 1024 by 1 bits. Eight of these chips are "parralled" to give a storage of 1024 8 bit words or bytes. There are eight of these groups on the board giving a total board storage capacity of 8192 (8K) 8 bit words. These eight 1K blocks can be refered to as eight 1K "pages" of RAM.

It takes 10 address lines (A0 through A9) to address any of the 1024 locations within any 1K page. This is true because 2 raised to the 10th power is 1024. If your system RAM consisted of only one page (1K) of RAM then most of the circuitry on the board would not be needed, and only the low order 10 address lines would be used. But since we want to have up to 64K available for use, the higher order address lines must be decoded to tell us which PAGE and which BOARD is being addressed by the CPU. Address lines A10 through A12 tell which PAGE and A13 through A15 tell which BOARD. Note that the PAGE can be one-of-eight and the BOARD is also one-of-eight.

The low order 10 address lines (A0-A9) are common to all eight pages. A0-A9 come off the Buss and are buffered on the 8K board (IC's 69 and 70) to minimize loading. These buffers have enable lines on pins 1 or 15 but these are grounded , constantly enabling these address buffers.

The 21L02 has a chip enable (CE) pin ideally suited for page selection. If this pin is not LOW then the 21L02 can neither be read or written in. The CE pin is common within any one page as can be noted on the schematic. We thus have eight pages each having a CE line which could be called the PAGE enable line.

The 74LS138 is a 3 line to 8 line decoder. Depending on the binary input on pins 1,2, and 3 then one of the eight outputs is pulled low. A10-A12 are connected as inputs to IC67 with the eight outputs going to the PAGE enable lines.

Note that a 74LS138 has 3 control or enable lines itself. These are pins 4,5, and 6. Pins 4 and 5 must be LOW for the decoder to operate and pin 6 must be HIGH. The use of these control lines will be discussed later.

The second 74LS138 (IC66) is used as the BOARD select decoder. Its inputs are tied to A13-A15 and its eight outputs are tied to the board address switches. Only one of the switches is closed. This corresponding to which 8K block of memory is occupied by the board. When the proper output of IC66 that is connected to the closed switch, goes low, the BOARD is selected. This BOARD select signal is used in two places. The first and most obvious is to pull LOW the control lines (pins 4,5) on IC67 that were mentioned earlier. This action insures that a PAGE can be selected ONLY when the BOARD is selected, thus ruling out ambiguous

operation. The second use of BOARD select is on IC68. BOARD select is inverted by 1/3 of IC68 then NANDed with PDBIN and SMEMR to control the Data IN buffers (DI0-DI7).

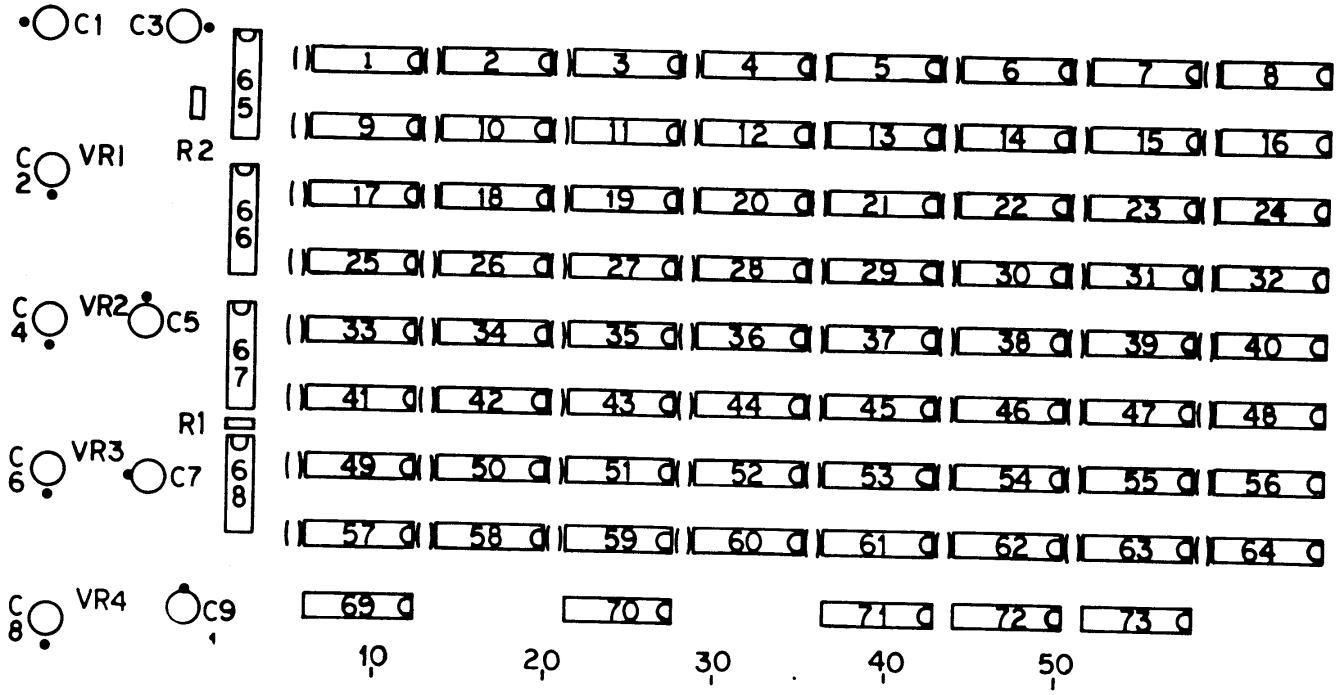
SMEMR (Status Memory Read) is a status signal sent out by the CPU indicating that the next operation will be a memory read. PDBIN (Processor Data Buss IN) is a strobe signal indicating WHEN the CPU will be reading off the data buss. All references to IN or OUT are with respect to the CPU.

As mentioned, inverted BOARD select is NANDed with PDBIN and SMEMR to enable the DATA IN buffers. This insures that data can only be sent IN to the CPU at the proper time. That is, when the board is selected, during a read operation, when the CPU requests data (during PDBIN).

Pin 3 on the 21L02 is the read/write line. It is normally HIGH indicating READ. A MWRITE pulse from the CPU is inverted by 1/3 of IC68 and buffered by 1/6 of IC69 and pulls pin 3 LOW allowing the RAM to be written in. The data written is provided by the CPU on the Data OUT buss (DO0-DO7) and is buffered by portions of IC 70,71, and 73. These buffers are always enabled since data cannot be written without an MWRITE pulse.

Four 7805 voltage regulators provide the +5VDC used on the board. The combination of tantalum and disc caps provide the necessary bypassing.

PHANTOM: Jumper Selected from Buss Pin 67
Normally when an 8080 is RESET it will then begin execution of the program at 0000H. A system without a front panel runs on a monitor in ROM, but it is usually not handy to have this ROM start at 0000H. Some manufacturers have provided ROM boards that put out a PHANTOM signal upon a system RESET. This signal is used to turn OFF the RAM that resides at 0000H and turn ON the ROM board where the system monitor is stored. This in effect fools the CPU and causes it to run the monitor after a RESET. Pin 67 can be jumpered to the control line on IC66 pin 6 which will turn off the board during PHANTOM. Only ONE board is ever jumpered for PHANTOM. The jumper is located just to the right of C9. Unless your ROM board provides PHANTOM do not use this jumper !!!


C1
C3
65
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
C2
VR1
R2
66
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
C4
VR2
C5
67
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
R1
C6
VR3
C7
68
49
50
51
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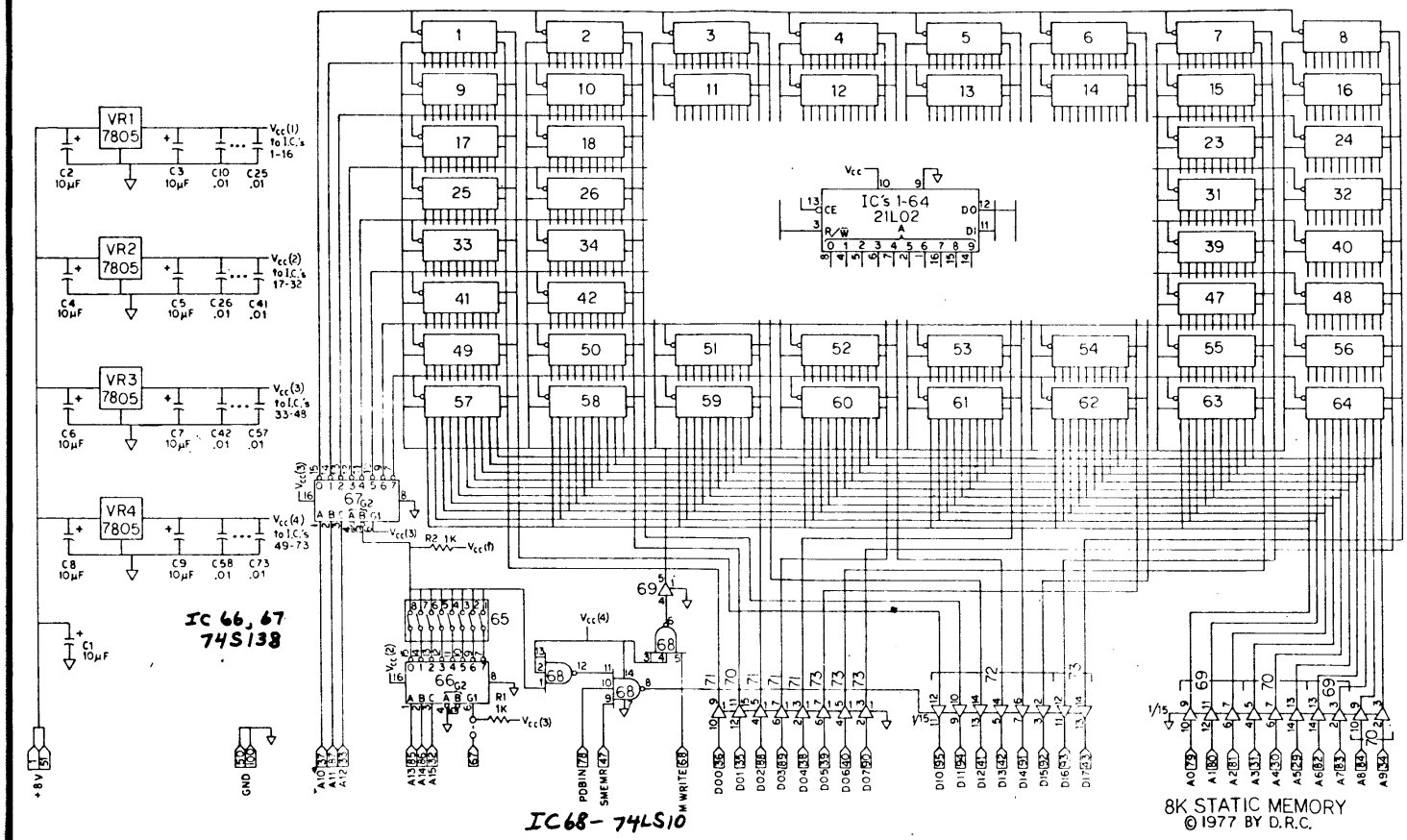
60
61
62
63
64
C8
VR4
C9
69
70
71
72
73
10
20
30
40
50


VR1 7805
VR2 7805
VR3 7805
VR4 7805
C1 10µF
C2 10µF
C3 10µF
C10 .01
C25 .01
C4 10µF
C5 10µF
C26 .01
C41 .01
C6 10µF
C7 10µF
C42 .01
C57 .01
C8 10µF
C9 10µF
C58 .01
C73 .01
IC 66, 67 74S138
IC68- 74LS10
IC's 1-64 21L02
8K STATIC MEMORY
©1977 BY D.R.C.
+8V
GND
R1 1K
R2 1K