MEM8PLUS v2f

Display Board

Main Board

BCSTech LLC
2016.03.06

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Active Memory Bank
Address Bus A23 – A16
Address Bus A15 – A8
Address Bus A7 – A0

sOUT sINP sMEMR sWO
sM1 sINTA sINTE
pDBIN pWR Probe
Phntm HALT HOLD
RDY XRDY WAIT

TTL Logic Probe
IN
GND

A16–A23 Ext. Sw.
Data In D7 – D0 Ext. Sw.
A7–A0 Ext. Sw.
A15–A8 Ext. Sw.

Displays ON / OFF

11-pin RNets:
See notes in schematic

Address BP Compare Normal ∨ – ∧ Don't Care
Address Compare Length
16 bits
24 bits
ActiveLo
ActiveHI
Input Switch Type – set both the same

Breakpoint Address A23–A16
Breakpoint Address A15–A8
Breakpoint Address A7–A0

Data In D7 – D0

Install Jumper for 5V operation (no regulators)

Cable 1 from Main Board
Cable 2 from Main Board

Data In Buss
Data Out Buss / Output

Cable 1 to Display Board
Cable 2 to Display Board

MemEx MemExNxt Deposit DepNxt Normal Run Step Any SlwStp BPOn DispIP
FPnt Stop M1 Off Off DispDO
Control Pod

SlowStep Speed
SlowStep Options
RHi RLo CLo CHi

ROM Config
2 Start
0
1 Addr
0
1 Size
0
0
1 Option
0
0
Spare 1

Install 4 Jumpers if RAM battery ICs not used

RAM/MMU Config
1 Chip
0 Size
EAddrON
ROM Opt
1 MMUC
0 Size
BS Mode
Spare 2

No MMU

Extended Address Board Select
A20
A21
A22
A23

Bank Select Port Addr. Config
A0
A1
A2
A3
A4
A5
A6
A7

Test I/O Port Addr. Config
A0
A1
A2
A3
A4
A5
A6
A7

Jumper if no pwr regs

Pin 53 Gnd
Pin 70 Gnd
Pin 20 Gnd

No FP

ROM Wait-States
8
7
6
5
4
3
2
1

Battery Type 2032

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