- 1. USER GUIDE
  - a. Introduction
  - b. System Description
  - c. Operation
  - d. High speed operation
  - e. Compatability
- 2. ASSEMBLY
  - a. General Construction
  - b. Handling MOS Devices
  - c. Photo of ZPU Card
  - d. Parts List
  - e. Detailed Assembly Instructions
  - f. Parts Layout Diagram
  - g. ZPU Schematic
- 3. THE ZAP MONITOR
  - a. Features
  - b. Loading Procedure
  - c. Command Set and Usage
  - d. ZPU Final Checkout Using Monitor
  - e. Source Listing
- 4. GENERAL INFORMATION
  - a. Customer Service
  - b. Troubleshooting Tips
  - c. Warranty
- 5. APPENDIX
  - a. Pinout diagrams of all ICs on the ZPU
  - b. Bus Diagram of ZPU Card

## USER GUIDE

## A. INTRODUCTION

The ZPU Card, TDL's Altair/IMSAI compatible Z-80 CPU card was designed to allow the Z-80 microprocessor to run, without modification to the mainframe, in either an Altair 8800 or an IMSAI 8080. At the same time, the design was configured to allow maximum versatility to the user, allowing the full potential of the Z-80 to be available to the user.

The ZPU Card is constructed of only the finest materials throughout. All components are first quality prime and obtained from reputable distributors, factories, or their representatives. No surplus material is used anywhere in the design.

In order to complement the Z80, which requires only a regulated +5 Volt supply, no components were used which require any other voltage. The total current drain is typically 750ma.

Separate jacks are provided to accomodate the front panel connectors of both the Altair and the IMSAI, and the ZPU user may at his discretion elect to install either one, or both during assembly.

### **B. SYSTEM DESCRIPTION**

1. The Z-80

The specifications and details of the Z-80 are covered in depth in Zilog's Z-80 CPU Technical Manual which is provided with this kit. A complete understanding of the theory of operation for this board requires a careful study of this manual.

## 2. Theory of Operation

Proper operation of the Z-80 in the Altair Bus requires the generation of a number of bus signals not generated by the Z-80. The ZPU Card creates these by interaction and gating of the Z-80's status signals and the clock lines. The most important status signals generated by the Z-80 are:

- 1. Memory Request
- 2. I/O Request
- 3. Read
- 4. Write
- 5. Ml

These 5 signals properly gated are used in conjunction with the clock to generate all of the required control timing.

The Z-80, unlike the 8080, outputs continuous status information wheras the 8080 information is strobed into an 8 bit latch (usually an 8212) during "Sync" time. Consequently, the Z-80 generates no sync pulse. In order to retain the Altair Bus structure, a "psuedo-sync pulse" was created.

Specifically, PSYNC is generated by gating I/O request and Memory Request thru a NAND gate (IC21) whose output goes to the input of a 74LS74 (IC16) which is clocked by the Phase 2 signal. PSYNC is taken off of the  $\overline{Q}$ of IC16.

A wait is accomplished by gating the PRDY signal and forcing a low into the wait control line of the Z80. In addition, an extra PRDY line has been made available which may be jumpered to any unused bus line for future applications. When not in use these lines should be jumpered together. (Pins 3 and 5 of IC17) The wait signal is initiated by the coincidence of the clock pulse with the pulling down of any of the 3 ready lines (PRDY,XRDY, LRDY)

The Interrupts Enabled flag is not provided on the Z-80. This has been simulated by the use of an 8 input NAND gate (ICl4) and some decode gating (ICl7) feeding a set-reset flip flop (ICl8) to provide the user with a proper indication when the interrupts are enabled.

The interrupt pin of the Z-80 is handled in exactly the same fashion as that of the 8080, coming to the same bus pin. However, the non-maskable interrupt pin of the Z-80, which represents a significant feature of the Z80 is brought out to a pull-up resistor, and may be jumpered to pin 4 on the bus, VIØ, the highest priority interrupt line. Thus configuring the Z-80 into the Altair Bus does not detract from this Z-80 feature.

The SSTACK status signal of the 8080 is not generated. Instead, the Z-80 REFRESH signal may be jumpered out to this line for use with future dynamic memory designs.

Processor write is generated by the Z-80, however in this application we have added some additional delay in order that the STATUS OUT or MWRITE may be properly decoded.

Handling of the remaining control timing is straightforward. HALT ACK is generated by the Z-80. The MREAD signal is a function of the Z-80 READ and MREQ signals. STATUS OUTPUT is a function of WRITE in conjunction with an I/O Request. STATUS INPUT is a function of a READ in conjunction with an I/O Request. PDBIN is a function of the READ signal. The Interrupt Acknowledge signal is a function of a simultaneous M1 and I/O request.

All processor signals with the exceptions of Phase One, Phase Two and Not CLOCK are tri-statable thru the normal Altair Bus Signal.

3. The Clock

The ZPU card features two clocks on-board. The first is fixed at 2Mhz thru crystal control, and the second is variable between less than 1 and greater than 4 Mhz by means of a 20 turn trimpot.

The 2Mhz crystal controlled clock is selected by placing a jumper between the augat pins labeled "C" and "2M".

The variable speed clock is selected by jumpering between "C" and "V". (The pins "C","2M" and "V" are located in area A on the ZPU Card.)

The crystal oscillator is a parallel resonant circuit using a 2Mhz crystal in conjunction with several gates of IC24, a 4049 CMOS oscillator chip. This clock generates Phase One, Phase Two, and system Not CLOCK.

The variable oscillator utilizes the remaining sections of IC24 in a free-running oscillator whose frequency is controlled by a precision RC network, and the frequency may be varied by adjusting R33, a 20K 20 turn trimpot. The variable oscillator presents Phase One and Two to the bus. Not CLOCK is always a function of the crystal oscillator and is always maintained at 2Mhz by that clock so that peripheral cards may be made to operate correctly regardless of processor speed. See the section on High-speed operation for details on this.

Regardless of which clock is selected, if the variable clock is tuned to within 100Khz or so of the crystal, there is a tendency for the 2 clocks to "lock in" to each other, that is to go into a fixed resonance. The operational effect of this is that when the variable clock is selected in this condition, initial frequency change either up or down will tend to be resisted, until the frequency "jumps" roughly 50khz, at which point smooth frequency adjustment may be made.

Two augat pins (in area "B" and "C" respectively on the board) are provided for observation of the Phase One and Phase Two signals. These points are test points only and not intended for adjustment of clock speed. Clock speed should always be measured at point C in area A.

By removing the jumper choosing either of the two on-board clocks and connecting the common pin (C) to an external frequency source, the ZPU card may be synchronized with another system if the user chooses. This also makes it possible to run the processor at very low speeds (down to DC) which on occassion can be tremendously useful. (For example, individual T-states may be observed on the front panel.)

### 4. I/O Operation

A visual inspection of the ZPU card reveals more buffers (8T97s or 74367s, ICs 1 - 10) than are usually seen on a CPU card. This additional buffering was necessary to reduce bus loading and to assure normal front panel operation.

The front panels of both the Altair and the IMSAI look at the high order addresses for information about the I/O port number during I/O operations. This was optional with the original designers of the 8080 systems because the I/O port number is output to both the high and low order addresses by the 8080.

The Z-80 outputs I/O port information only to the low order addresses. (Contents of the accumulator are then present on the high order addresses.) So, in order for the sense switches to operate normally 8 additional buffers have been added which transfer the lower 8 bits to the high order address lines during I/O operations.

## C. OPERATION

The normal configuration of the ZPU card is that which enables it to operate in an Altair or IMSAI with other peripheral boards. The kit as supplied and the instructions as given result in a CPU card which may act as a direct replacement for your current 8080 processor. There are however some options which may be exercised by the user which take advantage of several of the 2-80 options. These are:

- 1. Connecting the REFRESH signal to pin 98 on the bus.
- 2. Connecting the Non-maskable interrupt to vectored interrupt lines.
- 3. Altering the processor speed.
- 4. Use of the duplicate PRDY line.

## 1. The Refresh Line

Pin 28 of the 2-80 outputs a RFSH signal, which may be used to provide refresh timeing for dynamic memories. This signal may be placed on pin 98 of the bus. Pin 98 is normally occupied by SSTACK on your 8080 system, however, this status indicator is not terribly useful and was ommitted on the 2-80 altogether. So, we chose this line for RFSH.

The RFSH signal may be picked up at Area F, immediatly to the left of the Z-80, and jumpered to the pad in Area G, straight down and slightly to the left from the Z-80. This places the signal on the bus.

When the signal is on the bus, the status light on your front panel, labeled STACK will now stay lit when the processor is running, indicating that the REFRESH signal is on the bus.

For the exact timing information about the RFSH signal, see the Z-80 manual.

### 2. The Non-maskable interrupt

On the Z-80, pin 17 is NMT, the non-maskable interrupt. To quote the Z-80 manual:

"The non maskable interrupt request line has a higher priority than  $\overline{\text{INT}}$  and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMT automatically forces the Z-80 CPU to restart to location  $0066_{\mu}$ ."

This powerful interrupt capability is made available to the ZPU user.

Pin 17 of the Z-80 and pin 4 of the bus (VIØ) are normally both held high by pullups. Solder pads at location H and location E may be jumpered together, thus making the NMI available at VIØ, the highest priority vectored interrupt line.

## 3. Altering the Processor Speed.

The Z-80 has the capability of operating from DC on up to some maximum limit greater than 2.5Mhz due to its static nature. To take full advantage of this capability the ZPU card has been designed with a variable speed clock on-board.

Pl, an augat pin pin soldered to a wire represents the phase one and two inputs to the processor. If the pin is placed in J2, the augat pin labeled "V" in area A, then by adjusting the trimpot located above the crystal, the frequency may be varied over a range of approximatly 3 Mhz.

Normally, when one is reducing the speeds, simply turning the speed down is sufficient, and no problems will be encountered. For individuals whose systems may currently be marginal at 2Mhz, reducing the processor speed may well greatly increase reliability of your system.

When speed is increased it is sometimes necessary to readjust the timing of the 74123 for stable operation. This RC network (R36 and C26) effects the Phase one and Phase two relationships, which become more critical as processor speed is increased.

The procedure for speed adjustment is covered in the section on high-speed operation.

4. Use of the duplicate PRDY line.

This line was included in order to facilitate operation with the Altair 8800B, or for any other use the user might dream up.

The extra PRDY line comes off of IC17. Area D, immediatly to the left of the IC has 2 pads which are normally jumpered together. If one wishes to use the extra PRDY line, remove the jumper, and take the PRDY signal off of pin 3, the top of the two pads.

The 8800B requires 2 additional RDY lines. XRDY2 is on bus line 12. If operation with the 8800B is desired, jumper the additional RDY line on the ZPU to this bus pin. The other RDY line is FRDY, which is pin 58 on the bus. The user may use this line as he wishes.

- 1. Single stepping the processor
- 2. Use of 500ns memory

The Z-80, unlike the 8080 does not necessarily stop on an ML. The processor however must be in an ML for the front panel to operate normally. Rather than create circuitry to stop the Z-80 on an ML, we felt the simpler approach was simply to single step the processor to an ML, and then operate the front panel.

With the 280, system integrity is even more important than with the 8080. In part due to its more efficient architecture (remember that the Z-80 executes 8080 software 10% faster at the same 2Mhz clock speed) and also due to slight timing variations, the Z-80 is more demanding of your system at 2Mhz. The primary practical importance of this occurs when 500ns memory is in use.

Memory manufacturers rate their memory speed as chip access time, neglecting to add the select and enable logic time. These add up with chip access time to what may be termed board access time. While the 8080 may not note the difference, the Z-80 may. Therefore, it is recommended that when 500ns memory is in use, if any problems in running programs are encountered, the simple addition of one wait state will resolve it. If the small reduction of execution time is of any importance, switch the Z80 to its variable clock, and increase the processor speed to accomodate for the difference. (It is due to the presence of otherwise minor inefficiencies in current systems that TDL implemented the variable speed clock. It allows you to get the most out of your system.)

The best approach to system integrity when using a faster, more efficient chip such as the Z-80 is to gradually upgrade your system to very high speed memory such as TDL's Z16K.

Other than these mentioned points, operation of your ZPU is rather identical to that of your 8080.

#### D. HIGH SPEED OPERATION

Among the many features of the Z80 is its ability to operate at clock speeds higher (and lower) than that of the 8080. The ability to have a Z-80 operate in your system which was originally designed for a 2Mhz processor at clock speeds higher than 2Mhz is determined by 4 primary variables: 1. The Z80 chip itself, 2. The access time of your memory 3. The integrity of your system as a whole, 4. Your own technical knowledge.

The Z-80 chip itself is guaranteed to operate up to speeds of 2.5MHz. In practice we have found that the overwhelming majority of Z-80 chips operate comfortably at 3MHz. A good many operate at 4MHz. It is expected that Zilog will release Z80's tested good for 4MHz, at slightly higher cost. Pending the general availability of these chips, the ZPU is designed to operate at clock speeds up to 4Mhz.

Operation at 4Mhz requires a memory access time of 250ns. 3 Mhz requires 333ns. 2MHz requires 500ns. The quality and rated access time of the memory you possess should give a fair estimate of the maximum processor clock speed without wait states at which you can expect to operate your 280 successfully. Bear in mind however that most manufacturers rate memory access time as chip access time, not board access time, as was described earlier. The Z-80 is less tolerant of slightly slow memory than is the 8080.

NOTE: Do not try to operate the Z-80 at higher than 2Mhz with unbuffered memory. This create excessive loading.

The integrity of your system is affected by many variables. Bear in mind that the Altair/IMSAI systems were not designed for 2MHz+ operation, and the system itself presents a final limit beyond which increased processor speed will be useless. The problems of noise, inductive and capacitive coupling, impedence matching etc. become increasingly significant as processor speed is increased.

A system of high integrity can operate at 4Mhz. High integrity impiles that the common faults which a home built computer may suffer from are absent. Such factors as sloppy construction, cold solder joints, or out of spec, but not quite "bad" components which might go un-noticed at 2MHz would be likely to present serious problems at 4MHz. Your own technical skill is the only solution to these problems.

Your own ability is the greatest variable you will encounter. A thorough understanding of how your

system operates, and in particular how the ZPU and the Z80 operate is the best guarantee of successful operation at 2MHz+. The better you understand your hardware, the more success you'll have at getting the last bit of speed from your processor.

The simplest procedure for increasing the speed of your processor is as follows:

- 1. Place Pl (from point C Area A) into the augat pin marked V.
- Using an insulated adjustment tool, adjust the processor speed to 2MHz as measured at Point C.
- 3. If no accurate frequency measuring instrument is available, turn the 20 turn trimpot clockwise to maximum resistance which gives you the lowest clock speed, and then proceed.
- 4. Load a program into the processor which will show if the processor is operating properly. A listing of some sort would be ok. The DISPLAY MEMORY command of the monitor is very good.
- 5. Increase the processor speed by turning the trimpot counter-clockwise until the processor bombs. Turn the adjustment screw back ½ turn or so.
- 6. Run various programs on the processor at this speed and test for reliability. If any problems show up, reduce the speed a bit more.

Your processor is now running at the maximum speed which your system, without tune-up or adjustment, and without tweaking the values of any components, is capable of handling. Your own skill, of course, can cause this figure to rise.

It is important to note here that although the system CLOCK line is maintained at 2MHz regardless of processor speed, some boards, particularly I/O boards, use Phase 1 or Phase 2 for their timing, and will not operate correctly when the Z-80 speed is altered. In this case, the fix is very simple - cut the malfunctioning board trace from the phase 1 or 2 and jumper it to the CLOCK line. It will now operate correctly at processor speeds other than 2MHz and will still operate with your 8080 as well.

## E. COMPATIBILITY

Due to the pin for pin compatibility which the ZPU shares with the Altair Bus structure, it is highly compatible with existing hardware. Bear in mind that the design of the ZPU was aimed at simulating the bus while not impeding the Z-80 in any way, or confining it by hardware compromises. Generally this has been achieved.

You will find that the front panel of your system will operate in the usual fashion with all switches serving their normal function and all lights (save STACK) indicating their normal signal conditions.

The only hardware "incompatibility" ever noted is that slightly out of spec memory which the 8080 will tolerate at 2Mhz will on rare occassions be found unacceptable to the Z-80. The solution would be to introduce one wait state in the memory, or slowing the processor down by a small fraction.

The Z-80 is 100% machine code compatible with the 8080's 78 instructions. Thus standard 8080 software will run without modification on the Z-80.

However, where the actual execution time (in real time) of each machine cycle is used to create a timing loop, 100% compatibility may not be found. This situation is created by a feature of the Z-80.

The architecture of the Z-80 is more efficient than that of the 8080. In its design, many instructions of the 8080, while having the same machine code, have fewer "T-states" and thus the instruction is executed faster in real time. It should be clear then, that 8080 software timing loops where real time length of execution is controlled in software will have to be readjusted to the higher real time execution speed of the Z-80. Note that this is true when the 8080 and the Z-80 are both run at 2MHz.

While this feature of the Z-80 may require minor software modifications for an occassional user, in general it is a very useful feature. For example, a member of the Amateur Computer Group of NJ has a benchmark program in basic which he has run on a large array of machines, both minis and micros. This program was run using Altair Basic using both the 8080 processor and the ZPU. Only the 8080 instructions of the Z-80 were used, and both processors were maintained at a 2MHz clock speed. However, the ZPU executed the same program in 10% less time. This is a significant improvement.

As for 8080 languages, TDL procured and tested versions of virtually every language yet written for an 8080 processor. With one exception, they ran without a hitch.

This sole exception is Altair Basic. This basic has as part of its routines several occassions where the Parity Flag is checked as part of the function. In the Z-80, the parity flag indicates OVERFLOW during math routines, not Parity. As a result, Altair basic will not run on the Z-80.

The exact mechanics of this bug may be examined by studying the sections on Flags in the 8080 and Z-80 Technical Manuals.

Since the several routines which cause this bug to occur were written to reduce program space by several bytes, and are not required by the structure of the language, it can be patched by those who wish to do so. Appendix C of this manual describes the patching technique.

For those who do not wish to go to the trouble of generating the patch, it is advised that they procure TDL's 8K basic which is Altair compatible and which has a large number of exclusive and desirable features. It will be available as of Mid-September 1976.

No software incompatibilities other than the above have been encountered. In any applications of existing software, if a problem is found please inform us of the exact details in writing and we will be pleased to advise you on a proper solution.

## (12)

### ASSEMBLY

## CAUTION

THE ZPU KIT CONTAINS TWO STATIC SENSITIVE DEVICES. DO NOT REMOVE THESE DEVICES FROM THEIR PROTECTIVE PACKING UNTIL NEEDED IN ASSEMBLY. HANDLE ONLY AS PER THE INSTRUCTIONS IN THIS MANUAL. FAILURE TO HEED THIS PRECAUTION MAY RESULT IN PERMENANT DAMAGE TO THESE DEVICES AND AUTOMATICALLY VOIDS THE WARRANTY.

ALSO, THE Z-80 IS NOT PIN FOR PIN COMPATIBLE WITH THE 8080. ATTEMPTING TO RUN THE Z-80 IN YOUR 8080 CPU CARD WILL DESTROY THE Z-80.

## A. General Kit Building

It's a good feeling to construct a kit on your own, plug it in, and have it work the first time up. Two factors are of the utmost importance in this: quality engineering which makes the kit easy to build, and careful construction. We've taken care of the engineering, the construction is up to you. We've listed here some construction tips which are considered standard operation in most commercial shops. Following these procedures in your own construction will increase the likelyhood that your kits will work first time, every time.

- 1. ALWAYS read all of the instructions before starting construction.
- 2. Always work in a clean, well-lit area.
- 3. Use only high quality rosin core solder of a guage similar in size to the leads being soldered.
- Ensure that you have all the necessary parts for a given stage of construction before starting that stage.
- 5. Use the lowest power soldering iron that will get the job done. A 25 watt iron is quite adequate for this kit.
- 6. Use a fine point soldering iron, and keep the tip clean and well tinned.
- 7. Avoid overheating the PC board and components.
- 8. Before soldering, check and make sure that the right component is in the right place. Having to remove and resolder a wrongly placed component is difficult, and there is a great likelyhood of damage to the board or component.

- 9. Apply the solder to the iron tip, the pad and the component lead at the same time. The solder will melt and flow in a second or two. If it doesn't, stop and find out why before continuing.
- 10. Use only enough solder to assure electro-mechanical integrity. 1/8th inch or so of the solder supplied with this kit is generally adequate around IC pads.
- 11. Look carefully at each joint both during and after soldering it. It should have a clean, bright appearance. If the surface is rough or dull it might be a "cold" solder joint. If so, reheat and apply very little or no additional solder.
- 12. Don't work on construction if you're very tired.
- 13. Always check the voltages on the appropriate IC pins after soldering and before installing the ICs in their sockets.
- 14. Never install ICs in sockets when there is voltage on the board.
- 15. ALWAYS install MOS/CMOS devices LAST, when you're sure that all else is perfect.
- 16. NEVER insert the board into its socket when power is on the machine.

## B. Handling MOS/CMOS Devices

When handled correctly, static damage to these sensitive devices is quite unlikely to occur. The rules for correct handling are simple:

- Keep everything in contact with everything else. While the IC is still in its case, hold it in your hand, touch both to the table, the PC board etc. This allows any static to discharge.
- Work on a conductive surface. Bare grounded metal (a cookie tin or piece of aluminum foil will do.) is best. Glass very bad, plastic the worst.
- 3. Wear cotton clothes instead of synthetics.
- 4. A medium humidity environment is better than a very dry room.

These Rules are very simple. Remember: the most basic rule is to keep everything in contact with everything else. If you adhere to this rule and the others, plus add some common sense, it's very unlikely that you will ever damage a static-sensitive component.



## (16)

## ZPU PARTS LIST

IC 1 to 10 IC 11,12,20 IC 13,15,19 IC 14 IC 16 IC 17 IC 18,21,22 IC 23 IC 24 IC 25 IC 26	8T97 or 74367 74LS02 74LS04 74LS30 74LS74 74LS10 74LS00 74LS00 74123 4049 Z-80 7805
R l to 10	<pre>1K, 5%, Brown, Black, Red, Gold</pre>
R 12 to 20	1K, 5% " "
R 30	1K, 5% " "
R 11,31	100 ohm, 5%, Brown, Black, Brown, Gold
R 21	47 ohm, 5%, Yellow, Violet, Black, Gold
R 22 to 29	4.7K, 5%, Yellow, Violet, Red, Gold
R 32	4.7K, 5% " "
R 34	3.3K, 5%, Orange, Orange, Red, Gold
R 35	10K, 5%, Brown, Black, Orange, Gold
R 36	12K, 5%, Brown, Red, Orange, Gold
R 33	20K, 20 turn trimpot
C 1,2,14	<pre>47Mf, 25V, dipped tantalum electrolytic</pre>
C 3 to 13	.1Mf disc ceramic
C 16,18,19	.1Mf " "
C 15,17	.001Mf Disc Ceramic
C 20	33Mf,25V dipped tantalum electrolytic
C 21,24	.1Mf Disc Ceramic
C 27 to 31	.1Mf Disc Ceramic
C 22	10Pf " "
C 23	6 Pf " "
C 25	27 Pf Disc Ceramic
C 26	47 Pf " "
Y1	2Mhz Crystal
J1A	10 pin molex connector
J1B	16 pin high profile DIP socket
J3,4,5,6	Augat pins
P1	Augat Pin

1 Heatsink 1 ea. 6/32 x 5/16" machine screw, lockwasher, nut 1 ZPU PC board 12 14 pin low profile IC sockets 12 16 pin low profile IC sockets 1 40 pin high profile IC socket

Miscellaneous

6"	jumper wire
5'	solder
1	Zilog Z80 CPU Technical Manual
1	ZPU Documentation Manual
1	Paper tape of the ZAP monitor

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## E. Detailed Assembly Instructions

- () 1. Read these instructions through once from beginning to end before continuing.
- () 2. Inventory all parts against the parts list.
- () 3. Open out the board layout diagram at the end of this section, and place the board so that it is similarly oriented in front of you. Compare the two and familiarize yourself with the layout.
- () 4. Install the twenty 1K resistors (R 1 to 10, 12 to 20 and 30) in the appropriate locations, and solder.
- NOTE: In soldering in large numbers of similar components, it is quickest to perform all similar actions on all of the components at the same time. For the above, you can bend the leads, insert the resistors, pull them close and bend the leads out to hold them in place, and then solder as 4 actions for all the resistors.
- () 5. Repeat the above for the nine 4.7K resistors. (R 22 to 29, 32)
- ( ) 6. Install the two 100 ohm resistors (R11,31); the 10K resistor (R35); the 47 ohm resistor (R21); the 12K resistor (R36); the 3.3K resistor (R34)
- () 7. Insert the twelve 14 pin IC sockets and the twelve 16 pin IC sockets in their respective positions, with all pin 1s toward the top of the board. (IC sockets have a notch or chamfer to indicate pin 1.)
- () 8. Invert the board and solder all of the pins. Make sure each socket is all the way in before you solder - it's difficult to correct not fully inserted sockets after soldering.
- NOTE: If the sockets tend to fall out, either bend two diagonally opposite leads on each, or place a piece of thin stiff cardboard over all the sockets and turn the board over holding them in place with the card board. Then slide the cardboard out.
- () 9. Insert the 20K trimpot (R33) and solder in place.
- () 10. Insert the 40 pin high profile socket in place, and solder. (NOTE: PIN ONE OF THE Z-80 GOES <u>DOWN</u> ALL OTHER PIN ONES ARE UP.)

- () 11. Insert the 16 pin high profile socket (J1B) and solder. Pin one goes to the upper right.
- () 12. Solder a 1<sup>1</sup>/<sub>4</sub>" piece of jumper wire into the top of one of the Augat pins. Be sure to not get any solder on the tip of the pin.
- () 13. Trim back 4" of insulation from the other end of the wire and insert this end into hole C of Area A on the board and solder. The pin is now Pl.
- () 14. Place another Augat pin on the tip of Pl. Insert the tip of this second Augat pin into Hole V in Area
   A. Using the stiffness of the wire to hold the pin in position, solder the pin in Hole V.
- () 15. Again using Pl as a holder, repeat the above procedure placing Augat pins in hole 2M of Area A and Hole 1 of Area B.
- () 16. Cut another piece of jumper wire about 2" long. Use it as a holder while soldering the remaining Augat pin into hole 2 in Area C.
- ( ) 17. Install the 4 small disc ceramic capacitors (C22, 10pf; C23, 6pf; C25, 27pf; C26, 47pf) in their respective positions and solder.
- () 18. Install the two .001Mf disc ceramic capacitors (C15 and 17) in position and solder.
- ( ) 19. Install the twenty-one .lMf disc ceramic capacitors (C 3 to 13, 16, 18-19, 21, 24 and 27 to 31) in their respective positions and solder.
- NOTE: The leads of C3 need to be left 3/16ths of an inch or so, and the disc pushed in toward the center of the board in order for the board edge to clear any card guides. Also, to get the discs close to the board, it may be necessary to bend the leads inward from the base slightly. If the insulation on the leads is too far down, grasp the lead in the teeth of long-nose pliers, rotate the lead, and pull the insulation off.
- () 20. Install the three 47Mf dipped tantalum electrolytics in their positions and solder. Make sure that they are properly oriented for polarity.
- () 21. Install the 33Mf dipped tantalum electrolytic (C20) and solder. Insure that the polarity is correct.
- NOTE: Polarity of tantalums is marked in 3 ways. PLUS is either the lead with the dot next to it, the side of the component with the + stamped on it, or if the unit has one large dot on it, it is the right hand lead when the dot is oriented towards you.

- () 22. Install the 7805 voltage regulator. Refer to the picture for correct orientation. The shortest distance to the hole in the heatsink goes under the 7805. The longest distance goes toward the top of the board. The leads of the 7805 should be bent down at 90 degree angles to go into the holes. Solder the leads.
- NOTE: The screw holding the 7805 is inserted with the nut and lockwasher on the component side of the PC board.
- () 23. Install a short jumper between the two solder pads to the left of IC17 in Area D. (This is an option - only install if the extra PRDY line is NOT being used.)
- () 24. If you are using or plan to use the ZPU Board with an Altair 8800, now install the 10 pin molex connector (J1A) at the upper right hand corner of the board.
  - () 25. Install the crystal (Y1) immediatly below the 3 augat pins in area A. Bend the leads approximatly 3/16ths of an inch from the crystal body down 90 degrees in a smooth arc. Solder. (Don't overheat - it can damage the crystal.)

This compleats soldering of the board.

- () 26. Trim all leads, including IC socket pins down as close to the board as you can using the flat side of diagonal cutters.
- () 27. Using Acetone, Alcohol, or some other solvent, plus a stiff ½ inch artist's brush and a clean cloth, clean all the residue from the soldering operation off of the board.
- NOTE: This is the construction step most often ommitted by the unwise. Cleaning the board will handle 95% of those "solder splashes" that can cause so much trouble, and make finding the remaining few a snap. Start in a corner, apply the solvent liberally by pouring on and "scrubbing" with the bruch. Before all the solvent evaporates, BLOT off the remainder with the cloth. (You can't rub over the sharp cut edges.) Repeat if necessary. Then apply some solvent to the rag and clean the board edges, connector etc. well.

- () 28. Now examine the board carefully for solder shorts, cold solder joints, unsoldered leads etc. Corrent any problems which you find.
- () 29. Check once more to be sure that you have all the right components in the correct spot.

Now you are ready to proceed with electrical checkout.

- () 30. Measure the resistance between pins 1 and 50 on the edge connector. It should measure a fairly high resistance, 20,000 ohms or so. Completly open means the voltage regulator is not connected, or broken. A dead short indicates that either the regulator is blown, or you have a solder short.
- () 31. If the resistance is OK, now insert the ZPU card (with no ICs other than the 7805) into your motherboard (with no other cards in the slots.) apply voltage, and measure the voltage between the center lead and the right lead of the 7805, pin 7 and pin 14 of the 14 pin IC sockets, and pin 8 and 16 of the 16 pin IC sockets. All should measure within a very small fraction of +5 volts. If they do not, find the problem and correct it before proceeding.
- () 32. When these voltages are correct, install all the ICs except the 4049 and the Z-80. Put the board back in the motherboard, turn on the power and check the voltages again. They should be the same.
- () 33. If the voltages are OK, now install the 4049 and then the Z-80. Be sure to adhere strictly to the procedure for handling MOS/CMOS devices outlined at the beginning of this section.
- () 34. Insert Pl into pin 2M in area A (this places the clock on the 2MHz crystal.

This completes mechanical construction and electrical checkout of the ZPU card. Now go to the ZAP MONITOR section for procedure to checkout the operation of the Z80 board itself.

WARNING: <u>NEVER</u> INSERT ANY IC OR BOARD INTO ITS SOCKET WHEN POWER IS APPLIED. THIS IS LIKELY TO SEVERLY DAMAGE THE BOARD OR COMPONENT.



## THE ZAP MONITOR

## A. FEATURES

The ZAP Monitor is a 1K version of TDL's 2K ZAPPLE Monitor. It is relocatable (can be placed anywhere in memory), expandable ("modules" of additional commands can be tacked on at the end, like cars on a freight train.), and quite powerful as a system executive.

The expandable feature should be of great interest to the user. Since it is designed in a modular fashion, and since the ZAPPLE is its direct parent, this monitor features tremendous expandability - either of routines generated by the user, or by routines provided by Technical Design Labs. Several "modules" which will be of great interest include powerful "breakpoint", "search" and "register display" commands. Paper tapes of these modules will be available from TDL in the early fall. (Contact us for the latest word on availability.)

### B. LOADING PROCEDURE

The loading procedure is presented on the following two pages exactly as it was prepared on the computer.

TDL 280 RELOCATING ASSEMBLER VERSION 1.2 APPENDIX A. SUPPORT PROGRAMS FOR RELOCATING BOOT LOADER, V3.2 GENERAL DESCRIPTION

> .LIST .REMARK / THIS VERSION OF THE TDL BOOT LOADER AND TDL RELOCATING LOADER SHOULD MAKE IT EASIER FOR PEOPLE WITH WIDELY DIVERGENT HARDWARE TO LOAD THE MONITOR. THE GENERAL MEMORY MAP LOOKS LIKE THIS: 0000 - 00FF BOOT LOADER 0100 - 01FF RELOCATING LOADER 0200 - FFFF WHERE MONITOR MAY BE PLACED THE BOOT LOADER MEMORY MAP: 0000 - 0019 HARDWARE INITIALIZATION ROUTINE 001A - 001C LXI SP, 200H 001D - 001F LXI H, 01F3H (CHANGED BY UPPER LOADER) 0020 - 0022 CALL READER (CALL CHANGED TO JMP) 0023 - 00FF BOOT LOADER AND READER ROUTINES THE THREE INSTRUCTIONS SHOWN IN THE BOOT LOADER

THE THREE INSTRUCTIONS SHOWN IN THE BOOT LOADER MEMORY MAP ARE FIXED AND MUST BE AS SHOWN, BECAUSE THE RELOCATING LOADER USES OR MODIFIES THEM.

THE READER ROUTINE IS EXPECTED TO RETURN AN 8 BIT CHARACTER FROM THE TAPE EACH TIME IT IS CALLED.

THE BOOT LOADER ROUTINE LOADS THE RELOCATING LOADER INTO MEMORY STARTING AT 01F3H AND DOWNWARD TO 0100H.

/ . Page

## TDL 280 RELOCATING ASSEMBLER VERSION 1.2 APPENDIX A. SUPPORT PROGRAMS FOR RELOCATING BOOT LOADER, V3.2 UART STYLE BOOT LOADER ROUTINES

.

		.LIST				
0000	C31A00	; ; INIT:	JMP	LOAD	NO INITIALIZATION NEED	DED
001A		, LOC 1A	E			
001A 001D 0020 0023 0024 0026 0027 0028	310002 21F301 CD2B00 BD 28FA 2D 77 20F6	LOAD: RDR:	LXI LXI CALL CMP JRZ DCR MOV JRNZ	SP,200H H,01F3H .READ L .RDR L M,A .RDR	;SET STACK ;LOAD LOADER ;GET A CHARACTER ;TEST LEADER ;WALK OVER LEADER ;MOVE POINTER ;SAVE DATA ;GET MORE DATA OR	
002A	E9	; ; ALTA: ;	PCHL IR SIOA H	REV 1.0 P	; GO TO LOADER READER ROUTINE	
002B 002D 002F 0031 0033	DB00 E601 20FA DB01 C9	READ:	IN ANI JRNZ IN RET	0 1 READ 1	;STATUS PORT ;DATA AVAILABLE BIT ;O=DATA AVAILABLE ;DATA PORT ;DONE	
		; .LIST ;				I
		; PTCO	3P+S REA	ADER ROUT	INE	
002B 002D 002F 0031 0033	DB00 E640 28FA DB01 C9	READ:	IN ANI JRZ IN RET	0 040H READ 1	;STATUS PORT ;DATA AVAILABLE BIT ;l=DATA AVAILABLE ;DATA PORT ;DONE	
		; ; . PAGE				

PAGE 2

PAGE 3

## TDL 280 RELOCATING ASSEMBLER VERSION 1.2 APPENDIX A. SUPPORT PROGRAMS FOR RELOCATING BOOT LOADER, V3.2 MOTOROLA ACIA BOOT LOADER ROUTINE

ı.

		.LIST			
		7 7			
		; THIS ; THAT ; SUCH	ROUTINE USES A M AS AN AL	WOULD BE OTOROLA A TAIR 2SI(	USED FOR AN I/O BOARD ACIA. D.
0000 0002 0004 0006 0008	3E03 D320 3E11 D320 C31A00	INIT:	MVI OUT MVI OUT JMP	A,003H 20H A,011H 20H LOAD	;RESET ;CLOCK/16, 8 DATA BITS ;NO PARITY
001A		LOC 1A	E		
001A 001D 0020 0023 0024 0026 0027 0028 002A	310002 21F301 CD2B00 BD 28FA 2D 77 20F6 E9	LOAD: RDR:	LXI LXI CALL CMP JRZ DCR MOV JRNZ PCHL	SP,200H H,01F3H .READ L .RDR L M,A .RDR	;SET STACK ;LOAD LOADER ;GET A CHARACTER ;TEST LEADER ;WALK OVER LEADER ;MOVE POINTER ;SAVE DATA ;GET MORE DATA OR ;GO TO LOADER
		; READE	R ROUTINI	Ē.	
002B 002D 002F 0031 0033	DB20 E601 28FA DB21 C9	READ: ; ; .PAGE	IN ANI JRZ IN RET	20H 1 READ 21H	;STATUS PORT ;DATA AVAILABLE BIT ;l=DATA AVAILABLE ;DATA PORT ;DONE

PAGE 4

## TDL 280 RELOCATING ASSEMBLER VERSION 1.2 APPENDIX A. SUPPORT PROGRAMS FOR RELOCATING BOOT LOADER, V3.2 INTEL USART BOOT LOADER ROUTINE

<pre></pre>			.LIST			
<pre>; THIS ROUTINE WOULD BE USED FOR AN I/O BOARD ; THAT USES AN INTEL USART. ; SUCH AS AN IMSAI 2SIO. ; 0000 3ECE 0002 D303 0004 3E17 0006 D303 0008 C31A00 001A 001A 001A 001A 001A 001A 001A</pre>			7			
00003ECEINIT: MVIA,OCEH;CLOCK/16, 8 DATA BITS0002D303OUT3;NO PARITY, 2 STOP BITS00043E17MVIA,017H;ENABLE XMIT & REC0006D303OUT3;RESET ERROR FLAGS0008C31A00JMPLOAD001A.LOC 1AH7.LOAD:LXISP,200H0020CD2B00RDR:CALL002121F301RDR:CALL0022CD2B00RDR:CALL0023BDCMPREAD002428FAJRZRDR002520F6DCRRDR002620F6JRNZRDR02777MOVM,A02820F6JRNZRDR7READER ROUTINE; GO TO LOADER7JRZREAD; 1=DATA AVAILABLE BIT002728FAJRZREAD0028DB03READ:IN2.DATA AVAILABLE BITJAZ0031DB02IN2033C9READ; bONE7PAGEREAD			; THIS I ; THAT ( ; SUCH A	ROUTINE USES AN AS AN IM	WOULD BE INTEL USA SAI 2SIO.	USED FOR AN I/O BOARD ART.
001A.LOC 1AH001A310002LOAD: LXISP,200H;SET STACK001D21F301LOAD: LXIH,01F3H;LOAD LOADER0020CD2B00RDR: CALLREAD;GET A CHARACTER0023BDCMPL;TEST LEADER002428FAJRZRDR;WALK OVER LEADER00262DDCRL;MOVE POINTER002777MOVM,A;SAVE DATA002820F6JRNZRDR;GET MORE DATA OR0029DB03READ: IN3;STATUS PORT0020E602ANI2;DATA AVAILABLE BIT002128FAJR2READ;I=DATA AVAILABLE0031DB02IN2;DATA PORT0033C9RET;DONE;.PAGE;	0000 0002 0004 0006 0008	3ECE D303 3E17 D303 C31A00	INIT:	MVI OUT MVI OUT JMP	A,0CEH 3 A,017H 3 LOAD	;CLOCK/16, 8 DATA BITS ;NO PARITY, 2 STOP BITS ;ENABLE XMIT & REC ;RESET ERROR FLAGS
001A310002LOAD:LXISP,200H;SET STACK001D21F301LXIH,01F3H;LOADLOADER0020CD2B00RDR:CALLREAD;GET A CHARACTER0023BDCMPL;TEST LEADER002428FAJRZ.RDR;WALK OVER LEADER00262DDCRL;MOVE POINTER002777MOVM,A;SAVE DATA002820F6JRNZRDR;GET MORE DATA OR002820F6JRNZREAD;GO TO LOADER//.READER ROUTINE//;GO TO LOADER//.READ:IN3;STATUS PORT0021E602ANI2;DATA AVAILABLE BIT0031DB02IN2;DATA PORT0033C9RET;DONE//READREAD;DONE	001A		LOC 1A	I		
; READER ROUTINE ; READER ROUTINE ; 002B DB03READ: IN 3 ;STATUS PORT 002D E602 ANI 2 ;DATA AVAILABLE BIT 002F 28FA JRZREAD ;l=DATA AVAILABLE 0031 DB02 IN 2 ;DATA PORT 0033 C9 RET ;DONE ; ; .PAGE	001A 001D 0020 0023 0024 0026 0027 0028 0028	310002 21F301 CD2B00 BD 28FA 2D 77 20F6 E9	LOAD:	LXI LXI CALL CMP JRZ DCR MOV JRNZ PCHL	SP,200H H,01F3H .READ L .RDR L M,A .RDR	;SET STACK ;LOAD LOADER ;GET A CHARACTER ;TEST LEADER ;WALK OVER LEADER ;MOVE POINTER ;SAVE DATA ;GET MORE DATA OR ; GO TO LOADER
002BDB03READ: IN3;STATUS PORT002DE602ANI2;DATA AVAILABLE BIT002F28FAJR2READ;l=DATA AVAILABLE0031DB02IN2;DATA PORT0033C9RET;DONE;;READ;L=DATA AVAILABLE			; ; READEI	R ROUTIN	E	
. PAGE	002B 002D 002F 0031 0033	DB03 E602 28FA DB02 C9	READ:	IN ANI JRZ IN RET	3 2 READ 2	;STATUS PORT ;DATA AVAILABLE BIT ;l=DATA AVAILABLE ;DATA PORT ;DONE
			. PAGE			

TDL 280 RELOCATING ASSEMBLER VERSION 1.2 APPENDIX A. SUPPORT PROGRAMS FOR RELOCATING BOOT LOADER, V3.2 CONTROLED PARALLEL READER

		LIST			
		; THIS ; "MIGH" ; READE	IS AN EX T" BE US R.	AMPLE OF ED TO COI	A ROUTINE THAT NTROL A PARALLEL
0000 0002 0004 0006 0008 0008 0008 0008 0008 0008	3E20 D31B 3E30 D31B 3E28 D31B 3E20 D31B C31A00	. INIT:	MVI OUT MVI OUT MVI OUT JMP	A,20H 01BH A,30H 01BH A,28H 01BH A,20H 01BH LOAD	;INITIALIZE THE HARDWARE
001A		LOC 1A	Ħ		,
001A 001D 0020 0023 0024 0026 0027 0028 002A	310002 21FE01 CD2B00 BD 28FA 2D 77 20F6 E9	LOAD: RDR:	LXI LXI CALL CMP JRZ DCR MOV JRNZ PCHL	SP,200H H,01FEH READ L RDR L M,A RDR	;SET STACK ;LOAD LOADER ;GET A CHARACTER ;TEST LEADER ;WALK OVER LEADER ;MOVE POINTER ;SAVE DATA ;GET MORE DATA OR ;GO TO LOADER
		; READE	R ROUTIN	E	
002B 002F 0031 0035 0035 0037 0039 003B 003C 003D	3E20 D31B 3E30 D31B DB1B E601 28FA DB1A 2F F5 3E28	LOOP:	MVI OUT MVI OUT IN ANI JRZ IN CMA PUSH MVI	A,20H 1BH A,30H 1BH 1BH 1 LOOP 1AH PSW A,28H	;STATUS ;DATA ;UPSIDE DOWN
003F 0041 0043 0045 0045 0046	D301 3E20 D31B F1 C9	7	out MVI Out Pop Ret	18 A,208 188 PSW	

END

;					
;	TITLE / APPEN 3.2 - DEC. 28,	DIX B. 1976*>/	<*TDL RELOCATING	LOADER,	VERSION
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;	STAND-AL AS A BIN	ONE VERS	ION, TO BE USED -STRAP LOADER.		
7 •	PABS	;ABSOLUT	E ASSEMBLY		
00FF Si 001E Hi 0020 Ui 0200 T	ENSE = 0FFH LMOD = 01EH SER = 0020H OP = 0200H	;ALTAIR/ ;ADDRESS ;USER WR ;STACK A	IMSAI/TDL/ETC SENSE MODIFIED TO A JMP ITTEN I/O ROUTINE REA	SWITCHES	
0100	LOC 100H	;LOADER	ON PAGE ONE		
· · · · · · · · · · · · · · · · · · ·	SET-UP				
0100 3EC3 BI 0102 32 001D 0105 21 0100 0108 22 001E	EGIN: MVI STA LXI SHLD	A,JMP HLMOD-1 H,BEGIN HLMOD	; IN CASE OF TROUBLE ; STORE A JMP TO HER ; AT BOTTOM ;	RE	
0108 32 0020	STA	USER	; ;MODIFY READER CALL		
010E 31 0200 0111 DBFF 0113 FE02 0115 DA 0159 0118 47 0119 0E00 011B D9	LXI IN CPI JC MOV MVI EXX	SP,TOP SENSE 2 ERROR B,A C,0	; TO A JMP ; INSURE A STACK ;SEE WHERE TO LOAD ;CAN'T BE LESS THAN ;ABORT IF SO ;SAVE RELOCATION ;FORCE PAGE BORDER ;SAVE IT IN BC'	PAGE 2	
;	ACTUAL L	OADER CO	DE		
011C CD 01BE L0 011F D63A 0121 47 0122 E6FE 0124 20F6 0126 57 0127 CD 01A0 0128 CD 01A0 0128 F5 012F CD 01A0 0132 E1 0133 6F 0134 E5 0135 DDE1 0137 D9 0139 C5	DD0: CALL SUI MOV ANI JRNZ MOV CALL MOV CALL PUSH CALL POP MOV PUSH POP EXX DUCU	RDR ':' B,A OFEH LODO D,A SBYTE E,A SBYTE PSW SBYTE H L,A H X	;GET A CHARACTER ;ABSOLUTE FILE? ;SAVE INFO ;KILL BIT ZERO ;FILE NOT STARTED YE ;ZERO CHECKSUM ;GET FILE LENGTH ;SAVE IN E ;LOAD MSB ;SAVE IT ;LOAD LSB ;H=MSB ;L=LSB ;INDEX X=LOAD ADDR ;ALTERNATE REG.'S	ST	•
0139 D9 013A CD 01A0	EXX CALL	d Sbyte	GET FILE TYPE		

TDL 280 RELOCATING ASSEMBLER VERSION 1.2 PAGE 2 APPENDIX B. <\*TDL RELOCATING LOADER, VERSION 3.2 - DEC. 28, 1976\*>

013D 013E 013F 0140 0142 0144 0145 0146 0147 0148	3D 78 C1 2003 DD09 09 1C 1D 2822	A:	DCR MOV POP JRNZ DADX DAD INR DCR JRZ DCR	A A,B B A B B E E DONE	;1=REL. 0=ABS. ;GET OLD INFO ;RELOCATION FACTOR ;MUST BE ABSOLUTE LOAD ;ELSE RELOCATE ; BOTH HL & X ;TEST LENGTH ;0=DONE
0149 014A 014C 014F 0152	2824 CD 01A0 CD 01C4 20F8	Ll:	JRZ CALL CALL JRNZ	LODR SBYTE STORE	RELATIVE FILE NEXT STORE IT MORE COMING
0154 0157	CD 01A0 28C3	LOD4:	CALL JRZ	SBYTE Lodo	;GET CHECKSUM ;ALL O.K.
0159 015A	AF 2F	ERROR:	XRA CMA	A	;FLASH ADDRESS & SENSE LINES
015B 015D 015E 015F 0160	D3FF 18 7A 83 20FB D3FF	SIT1:	out DCX Mov ORA JRNZ	SENSE D A,D E SIT1 SENSE	
0162 0165 0165 0166 0167 0169	18 7A B3 20FB 18EE	SIT2:	DCX MOV ORA JRNZ JMPR	D A,D E SIT2 ERROR	
		7 1			
016B 016C 016D 016F	7C B5 28FE E9	DONE :	MOV ORA JRZ PCHL	A,H L •	;CAN'T GO TO ZERO ;TIGHT LOOP HERE ;ELSE SIGN ON PROGRAM
0170 0172 0175 0177 017A 017C	2E01 CD 0190 3807 CD 01C4 20F6 18D6	) LODR: L1: L5:	MVI CALL JRC CALL JRNZ JMPR	L,1 LODCB .L3 STORE .L1 LOD4	;GET CONTROL BYTE ;DOUBLE BIT ;WRITE IT ;MORE TO GO ;TEST CHECKSUM
017E 017F 0182 0183	4F CD 0190 47 D9	; L3:	MOV CALL MOV EXX	C,A LODCB B,A	;LOW BYTE ;NEXT ;HIGH BYTE
0184 0185 0186	C5 D9 E3	,	PUSH EXX XTHL	B	;GET RELOCATION
0187 0188 0189 018C	7D CD 01C4 7C		MOV CALL MOV	A,L STORE A,H	;RELOCATE LOW BYTE ;SAVE IT ;RELOCATED HIGH BYTE

TDL 280 RELOCATING ASSEMBLER VERSION 1.2 PAGE 3 APPENDIX B. <\*TDL RELOCATING LOADER, VERSION 3.2 - DEC. 28, 1976\*>

• .

018D 018E	El 18E7		POP JMPR	H L5	;RESTORE HL ;SAVE HIGH, REPEAT
0190 0191 0193 0196 0197	2D 2007 CD 01A0 1D 67 2508	; LODCB:	DCR JRNZ CALL DCR MOV MVI	L LC1 SBYTE E H,A L B	;COUNT BITS ;MORE LEFT ;GET NEXT ;COUNT BYTES ;SAVE THE BITS .8 BITS /BYTE
0198 019A 019D 019F	CD 01A0 CB24 C9	LC1:	CALL SLAR RET	SBYTE H	GET A DATA BYTE TEST NEXT BIT
01A0 01A1 01A4 01A5 01A6 01A7	C5 CD 01B3 07 07 07 07	Sbyte:	PUSH CALL RLC RLC RLC RLC	b Ribble	;PRESERVE BC ;GET 1/2 BYTE
01A8 01A9 01AC 01AD 01AE 01AF 01B0 01B1 01B2	4F CD 01B3 B1 4F 82 57 79 C1 C9	· · ·	MOV CALL ORA MOV ADD MOV MOV POP RET	C,A RIBBLE C C,A D D,A A,C B	;SAVE LEFT HALF ;GET OTHER HALF ;MAKE WHOLE ;IN C ;UPDATE CHECKSUM ;NEW VALUE ;CONVERTED BYTE
0183 0186 0188 0188 0188 0188	CD 01BE D630 FE0A D8 D607 C9	; RIBBLE:	CALL SUI CPI RC SUI RET	RDR '0' 10 'A'-'9'-1	ADJUST
01BE 01C1 01C3	CD 0020 E67F C9	7 RDR:	CALL ANI RET	user 7fh	;USER WRITTEN ROUTINE AT 10H
01C4 01C7 01CA 01CC 01CE 01CF	DD7700 DDBE00 208D DD23 1D C9	; STORE: ;	MOV CMP JRNZ INX DCR RET	0(X),A 0(X) ERROR X E	WRITE TO MEMORY VALID WRITE? NO. ADVANCE POINTER DECREMENT COUNT

. END

TDL 280 RELOCATING ASSEMBLER VERSION 1.2 PAGE 4 APPENDIX B. <\*TDL RELOCATING LOADER, VERSION 3.2 - DEC. 28, 1976\*> +++++ SYMBOL TABLE +++++

BEGIN	0100	DONE	016B	ERROR	0159	HLMOD	001E
LODO	011C	LOD4	0154	LODCB	0190	LODR	0170
RDR	Olbe	RIBBLE	01B3	SBYTE	01A0	SENSE	OOFF
STORE	01C4	TOP	0200	USER	0020		

## ADDENDUM:

Here is a DUMP of the LOADER, Version 3.2. It may be used to insure proper loading after the boot part of the tape has been read. This should not be required unless you are having trouble loading the monitor.

Remember: The new format requires the monitor be loaded at 0200H minimum. We strongly urge that you load at 0F000H. If you still wish to locate the monitor between 0 and 0200H, first load a temporary copy up higher, and then use THAT one to load it elsewhere. This monitor runs ANYWHERE when loaded by a copy of itself, but when using an initial boot strap, it is forced to a page boundry. Running the monitor on other than a page border sounds a little pointless in any case.

addr	0	1	2	3	4	5	6	7	8	9	A	B	С	D	E	F
0100	3E	С3	32	1D	00	21	00	01	22	1E	00	32	20	00	31	00
0110	02	DB	FF	FΕ	02	DA	59	01	47	0E	00	D9	CD	BE	01	D6
0120	3A	47	Ε6	FE	20	F 6	57	ĊD	Α0	01	5F	CD	ΑO	01	F 5	CD
0130	AO	01	Ēl	бF	Ε5	DD	El	D9	C5	D9	CD	A0	01	3D	78	Cl
0140	20	03	DD	09	09	1C	lD	28	22	3D	28	24	CD	A 0	01	CD
0150	C4	01	20	F 8	CD	A0	01	28	C3	AF	2F	D3	FF	1B	7A	В3
0160	20	FB	D3	EE	18	7A	<b>B</b> 3	20	FΒ	18	EΞ	7C	B5	28	FE	E9
0170	2E	01	CD	90	01	38	07	CD	C4	01	20	Fб	18	D6	4F	CD
0180	90	01	47	D9	C5	D9	ЕЗ	09	7D	CD	C4	01	7C	El	18	Ε7
0190	2D	20	07	CD	A 0	01	lD	67	2E	08	CD	A 0	01	СВ	24	C 9
01A0	C 5	CD	В3	01	07	07	07	07	4F	CD	<b>B</b> 3	01	B1	4F	82	57
0180	79	Ċ1	C 9	CD	ΒE	01	D6	30	FΕ	ØΑ	D8	D6	07	C9	CD	20
0100	00	E6	7F	C 9	DD	77	00	DD	ΒE	00	20	8D	DD	23	1D	C9

C. COMMAND SET AND USAGE

The following are the commands and operating symbols of the ZAP Monitor.

#### COMMAND

D

#### DESCRIPTION

DISPLAY COMMAND - this command displays the contents of memory in base hex. Memory is displayed 16 bytes per line, with the starting address of the line given as the first information on the line.

> In use, first the command is given, then the starting address, the ending address and a carriage return. The form is:  $D\emptyset\emptyset$ , FFF(cr). (This would display memory from  $\emptyset\emptyset$  to FFF.)

Ε

END OF FILE - this command outputs the end of file pattern for the checksum loader. It is used after punching a block of memory with a "W" command. An address parameter for the End of File may be given. For use, when the file being dumped is finished, type: E(cr).

F

FILL - This command fills a block of memory with a specific value. It is handy for initializing a block to a specific value (such as for tests, zeroing memory when starting up, etc.)

In use, first the command, then the starting address, ending address, and the value to be entered, followed by a carriage return. The form is  $Fl \emptyset \emptyset \emptyset$ , lFFF, AA(cr). This would fill the block  $l \emptyset \emptyset \emptyset$  to lFFF with AA.

G

GOTO - this command causes the processor to go to the specific address named and start executing. If a Return command is included in the program, the processor may jump back to the monitor after execution of the program. (RETURN is C9 hex). To use, the command is followed by the address chosen to execute from and a carriage return. The form is: G2FD4(cr). The processor will goto address 2FD4 and execute. MEMORY TEST - this is a "hard" memory test which will locate bad bits and represent them in their binary form. It is not meant to be the definitive memory test, but rather serves as an aid. It can also serve to very quickly locate accidentally or mistakenly protected areas of memory. It is non destructive of the memory contained in the area being examined.

In use, the command is followed by starting and ending addresses. A read/ complement/write is executed and if any errors are found, the bad address will be printed followed by the binary representation of the bit pattern. The form is:  $J\emptyset\emptyset$ , FF(cr). If address AA were bad on its fourth bit, the processor will print back AA 00010000, the "1" representing the bad bit found.

LOAD A BINARY FILE - This reads a binary file, either from cassette or tape. The form is:  $L\emptyset\emptyset\emptyset$  (cr). This would load a binary file starting at address 000. To use, enter the command and the starting address, type carriage return, and start the reader with nulls on the tape.

MOVE COMMAND - this command can move a block of memory from one location to another. This command should be used with some caution as careless placing could "smash" memory locations containing wanted data.

To use, type M followed by the starting address of the memory block to be moved, the ending address of the block to be moved, and the starting address of the new location. The form is:  $M\emptyset\emptyset$ , AA, CC. This would move the block of memory starting at location  $\emptyset\emptyset$  and extending to location AA up to location CC.

NULL - this command may be used to print nulls on paper tape as a leader. To use simply type N - and nulls will be punched.

Ŀ

J

М

N

OUTPUT OR DISPLAY FROM/TO I/O PORTS this command instructs the processor where to look for or where to send data to.To use, enter the command, indicating wether the processor is to input or cutput, name the port, and name the value to be output, if you are outputting. The form is:  $QO\emptyset$ , AA or  $QI\emptyset$ . The first would cutput an AA to port  $\emptyset$ , the second would input from port zero.

READ CHECKSUMMED HEX FILE - this command reads the check-summed hex files for both the normal Intel format and the TDL relocating format. On both files, a "bias" ( a shift in the address) may be added which will allow the object code to be placed in a location other than its intended execution location. The bias is added to what would have been the normal loading location and may wrap around. When used with the TDL relocating assembler, it allows generating a program to execute anywhere, and to be stored anywhere When loading a relocatable file, else in memory. an additional parameter may be added which represents the actual execution address desired. This may also be any location in memory.

To use, with a normal file, type R(cr) and start the reader. With a relocating file, the following examples should clarify the use of bias.

 $R(cr) = \emptyset$  bias,  $\emptyset$  execution address Rl(cr) = l bias,  $\emptyset$  execution address  $R,l(cr) = \emptyset$  bias, l execution address Rl,l(cr) = l bias, l execution address

SINGLE BYTE INSPECT AND MODIFY - this command allows single bytes of memory to be examined and modified or not as the user desires.

To use, give the command followed by an address and push the space bar - the data at that address will be displayed followed by a "-". If you wish to change the data at that address, simply type in the new data in hex and press the space bar. The old data will be replaced, and then the next byte of data will appear. If you wish to retain the old data,

R

0

S

simply press the space bar and the next byte will appear. Typing a carriage return ends the sequence.

BINARY DUMP - this command simply dumps core to the punch device. It may be used with a cassette system as well, with no startup problems. It does not generate checksum. The format which will be generated is a leader,  $8-\emptyset$ FFH's, and a trailer. The rub-outs are called file ques and are detected and counted to determine the start and end of files. To use, type the command followed by the starting and ending addresses, start the reader and (cr). The form is:  $U\emptyset\emptyset$ , FF(start reader - cr). This would generate a binary tape in the above format of the core contained in memory location  $\emptyset\emptyset$  to FF.

HEX DUMP - this routine dumps memory in the standard Intel-style hex file format. The start and end parameters are required and the End of File should be separately generated with the "E" command. To use, enter the command, starting address, ending address, start the reader, (cr). When dump finished, type E(cr) to generate end of file. The form is: WØØ, FF(start punch - cr) ----E(cr). (N here is optional).

TOP OF MEMORY - this command locates and names the top byte of RAM in the system. It does not include the space the monitor is occupying. Simply type Z - no (cr) is needed. The top of memory will be displayed in hex.

HEXIDECIMAL MATH - this command allows hex addition and subtraction to be executed. To use, type H, and the two hex figures to be added and subtracted. The form is:H00,ll(cr). The computer will print out first the hex sum and then the hex difference, in hex.

This concludes the command set of the ZAP Monitor.

In addition to these commands there are two symbols which you will observe. The first is an \*, which is an error message. The second is a > (greater than) which is a prompter basically saying "OK, continue...".

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U

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To interrupt a routine such as a D or J command, just type a CONTROL C. This ends the routine.

### D. ZPU FINAL CHECKOUT USING MONITOR

Assembly and electrical checkout of the ZPU was conducted elsewhere. However, only operation will show if the ZPU is actually operating correctly. The monitor is the best means of achieving this. Load the monitor as per the preceeding instructions, and experiment with its various commands. The FILL and DISPLAY, plus MOVE and J commands provide good exercise for the processor and if they seem to function normally, all is probably well.

### E. SOURCE LISTING

The following pages are an "off the printer" copy of the ZAP Monitor source code. It is provided for your understanding, plus as an invitation to experiment with Z-80 programming which can be quite exciting given 696 opcodes.

	; ;	<< ZAP	1-K MONI by	TOR SYSTEM >>
	3 5 5	TECHN IC RESEARC	CAL DESIG	N LABS, INC.
	i i	PRINCET	LUN, NEW	JERSEY 08540
	<b>;</b>	COPYRIG	HT JAN.	1977 TDL INC.
	;	ASSEMBL	ED by Ro	ger Amidon
	PREL	; THIS M	ION ITOR S	UPPLIED IN RELOCATING FORMAT
0400*	LENG TH	= Z	SIZE O	F THIS MONITOR
	.TITLE .SBTTL	" <z / Copy</z 	ap Monit right 19	or, Version 2.0, Jan. 16 1977>" 77 by TECHNICAL DESIGN LABS, INC./
	÷	<i 0="" de<="" td=""><td>VICES&gt;</td><td></td></i>	VICES>	
	;-TELEP	RINTER		
0001 0001 0000 0001 0080	TTI TTD TTS TTY DA TTY BE	= 1 = 1 = 0 = 1 = 80H	FDATA 1. FDATA O FSTATUS FDATA A FMTR B	N PORT JT PORT PORT (IN) VAILABLE MASK BIT JFFER EMPTY MASK
0003	; RCP	= 3	READER THIS PO FOR EAC TO SUPP READER	CONTROL PORT. DRT IS PULSED ONCE CH READER REQUEST PORT A CONTROLLED
	• •	< CONS TA	NTS>	
0000 FFFF 000D 000A 0007 00FF 0000 0007	I FALSE TRUE CR LF BELL RUB FIL MAX	= 0 = 0 = # FAL: = 0DH = 0AH = 7 = 0FFH = 00 = 7	SE	<pre>:'I' REG. VALUE :ISN'T SO :IT IS SO :ASCII CARRIAGE RETURN :ASCII LINE FEED :DING :RUB OUT :FILL CHARACTERS AFTER CRLF :NUMBER OF QUES IN EOF</pre>
	;	PROGRAM	CODE BEC	INS HERE
0000* C3 0308*	Z AP :	ЛМР	BEGIN	;GO AROUND VECIORS ; GET MEMORY SIZE, ; AND CONTINUE AHEAD

.

ţ

PAGE 1

	;	4		
	;	<vector< td=""><td>S FOR CA</td><td>LL ING PROGRAMS&gt;</td></vector<>	S FOR CA	LL ING PROGRAMS>
	; THESE ; PROGR ; FROM ; ASSIG ; THE R ; THE C	VECTORS AMS TO S SYSTEM T NED DEVI EQUIRED ALLING P	MAY BE IMPLIFY D SYSTEM CE, THESI I/O OPER ROGRAM.	USED BY USER WRITTEN THE HANDLING OF I/O • WHATEVER THE CURRENT E VECTORS WILL PERFORM ATION, AND RETURN TO (RET)
	THE R	EGISTER	CONVENTI	ON USED FOLLOWS-
	ANY I	NPUT OR CHARACT CHARACT RETURNI	OUIPUT DI ER TO BE ER WILL I NG FROM A	EVICE- OUTPUT IN *C* REGISTER. BE IN *A* REGISTER UPON AN INPUT OR OUTPUT.
	; ~ (5 15 ; ;	RE TURNS SOME IHI	TRUE (OF NG WAITIN	FFH IN 'A' REG.) IF THERE IS NG, AND ZERO (OO) IF NO.T.
	; / IOCH ; ;	RETURNS. BY TE IN	WITH THE 'A' REG	E CURRENT I/O CONFIGURATION
	; /IOSE ;	1'- 1/0 CANI	NOT BE MO	DIFIED IN THIS IK VERSION
	; /MEMCI ; ;	K'- Returns Memory 1	WITH THE LOCATION	E HIGHESI ALLOWED USER • B'=HIGH BYTE, • A'=LOW.
	∕ IR AP	'- IHIS IS NOT USE 'ERROR' S TACK.	THE 'BRE D IN THE ROUTINE	EAKPOINT' ENTRY POINT. IK VERSION, GOES IO THE TO RESET THE MONITOR'S
0003' C3 0374' 0006' C3 037D' 0009' C3 0222' 000C' C3 0233' 000F' C3 0222' 0012' C3 0282' 0015' 3E00 0017' C9 0018' C3 0017' 0018' C3 02FF' 001E' CD 0313' E	IOSET: ERROR:	JMP JMP JMP JMP JMP MV I RET JMP JMP CALL	CI RI CO PO CO CSTS A.O IOSET MEMCK MEMSIZ	<pre>;CONSOLE INPUT ;READER INPUT ;CONSOLE OUTPUT ;PUNCH OUTPUT ;LIST OUTPUT ;CONSOLE STATUS ;I/O CHECK ;SEI TO TTY CONFIGURATION ;CAN-T SET I/O ON 1K VERSION ;MEMORY LIMIT CHECK ;RESET BACK TO MONITOR (TRAP)</pre>
0021/ F9 0022/ 0E2A 0024/ CD 0222/ 0027/ 1815		SPHL MVI CALL JMPR	C,'*' CO SIART	RE-ESTABLISH A STACK FANNOUNCE ERROR

PAGE 2

		;;		NAME & V	VERSION
00294 002E4 00334	0D0A000000 5A61702056 322E30	MSG:	.BYTE .ASCII .ASCII	CR,LF,F 'Zap V' '2.0'	IL,FIL,FIL
000D		MSGL	=MSG		
00.34 /		SIACK	<b>=</b> 2		A FAKE STACK TO GET STARTED
00364	0038*	Ŧ	WORD	AHEAD	AFTER MEMORY SIZE
0038 0039 0038 0040 0043 0044 0047 0047 0047 0047 0047	F9 060D CD 01F2' 0E3E 21 003E' E5 CD 0278' CD 0222' CD 03DC' E67F 28F9 0E02 FE44 2017	* AHE AD * S TART *	SPHL MVI CALL MVI LXI PUSH CALL CALL CALL CALL ANI JRZ MVI CPI JRNZ	B, MSGL TOM C, '>' H, START H CRLF CO TI 7FH STARO C, 2 'D' EOF	SET TRUE STACK SAY HELLO TO THE FOLKS OUTPUT SIGN-ON MSG PROMPT CHARACTER MAIN 'WORK' LOOP SET UP A RETURN TO HERE GET A CONSOLE CHARACTER IGNORE NULLS GET ANOTHER SET-UP C REG. SEE IF 'DISPLAY' COMMAND
•		; THIS C ; WITH T ; THE IW	DISPLAYS THE STARI 10 PARAME	THE CONT TING LOCA TERS GIV	TENTS OF MEMORY IN BASE HEX TION ON EACH LINE.(BETWEEN MEN). 16 BYTES PER LINE MAY.
0057- 005A 005D 0060- 0061- 0064- 0067- 0068- 006A- 006C	CD 0273' CD 021A' CD 0220' 7E CD 02E3' CD 02BD' 7D E60F 20F1 18EC	DISP: DO: DI:	CALL CALL CALL MOV CALL CALL MOV ANI JRNZ JMPR	E JLF LF ADR BLK A.M LBYTE HILOX A.L OFH DI DO	GET DISPLAY RANGE CRLF & PRINT ADDR. SPACE OVER RANGE CHECK SEE IF TIME TO CRLF
		THIS O FOR TH PUNCHI COMMAN WHICH	UTPUTS T E CHECKS NG A BLO D. AN A WILL BE	HE END O UM LOADE CK OF ME DDRESS P INCLUDED	FFILE (EOF) PATTERN R. IT IS USED AFTER MORY WITH THE 'W' ARAMETER MAY BE GIVEN, IN THE END FILE.
006E 0070 0072 0075 0075 0078	FE45 201A CD 0296* CD 022C* 0E3A CD 0233*	EOF:	CPI JRNZ CALL CALL MVI CALL	YEY FILL EXPRI PEOL C,/:/ PO	SEE IF 'EOF' GET OPTIONAL ADDR. CRLF TO PUNCH FILE MARKER CUE

-

007D* 007E* 0081* 0082* 0085* 0086*	AF CD 034D* E1 CD 0348* AF CD 034D* C3 025F*	•	XRA CALL POP CALL XRA CALL JMP	A PBY TE H PADR A PBY TE NULL	<pre>#ZERO LENGTH #PUNCH OP TIONAL ADDR. #FILE TYPE=0 #PUNCH IT #TRAILER &amp; RETURN</pre>
		; THIS ; WITH ; <1> ; INIT ; MEMO ; A PRO	COMMAND A VALUE IO <2> W IALIZING RY IO A ( OGRAM. (	WILL FIL IE: FO, ITH THE B A BLOCK CONSTANT ZERO IS E	L A BLOCK OF MEMORY IFFF.0 FILLS FROM YTE <3>. HANDY FOR TO A SPECIFIC VALUE. OR VALUE BEFORE LOADING SPECIALLY USEFUL.)
008C* 008E* 0090* 0093* 0094* 0097* 0099*	FE46 200C CD 0288* 71 CD 02C3* 30FA D1 18A2	FILL: F:	CPI JRNZ CALL MOV CALL JRNC POP JMP.R	GOTO EXPR3 M.C HILO F D START	<pre>\$SEE IF 'FILL' GET 3 PARAMETERS \$STORE IHE BY TE RESTORE STACK IN CASE OF ACCIDENTS</pre>
		THIS	.COMMAND }AM ∙	ALLOWS E	XECUTION OF ANOTHER
009C* 009E* 00 A0* 00 A3*	FE47 2006 CD 0296 C3 0278	GOTO:	CPI JRNZ CALL JMP	G TEST E JP R 1 CRLF	\$SEE IF 'GOTO' \$GET AN ADDRESS TO GO TO \$CRLF & EXECUTE
		<pre># THIS # HARD # PROTE # MEAN # IT IS # PRINT # " &lt; ADD # BIT L # DETER # &lt; ADDF #</pre>	IS A C MEMORY CTED MEN TO BE TO BE ED ON TO R> 04" W LE, BIT OCATION MINED. N S> FF	JICKIE' M FAILURES, (ORY LOCA IHE DEFIN ER, NON-D HE CONSOL (HERE, IN 2 IS THE OF THE F NON-R/W M ALL BITS	EMORY TEST TO SPOT OR ACCIDENTLY TIONS. IT IS NOT ITIVE MEMORY DIAGNOSTIC. ESTRUCTIVE. ERRORS ARE E AS FOLLOWS- THIS PARTICULAR BAD BIT. AILURE IS EASILY EMORY WILL DISPLAY BAD)
00 A6' 00 A8' 00 AA' 00 AD' 00 AE' 00 B0' 00 B0' 00 B1' 00 B2' 00 B4' 00 B5'	FE4A 201B CD 0273* 7E 47 2F 77 AE 280B 08 CD 021D*	TEST:	CPI JRNZ CALL MOV MOV CMA MOV XRA JRZ EXAF CALL	/J/ MOVE EXLF A.M B.A M.A MT2 HLSP	<pre>SEE IF 'TEST' GET TWO PARAMS READ A BYTE SAVE IN B REG. READ/COMPLIMENT/WRITE &amp; COMPARE SKIP IF ZERO (OK) SAVE BAD BYTE PRINT BAD ADDR</pre>

0088* 08 0089* CC 008C* CD 008F* 70 00C0* CD 00C3* 18	3 0 02E3* 0 0278* 0 02BD* 3E8	EXAF CALL CALL 2: MOV CALL JMPR	LBYTE CRLF M,B HILOX ••II	GET BAD BYTE BACK PRINT IT REPLACE BYTE RANGE TEST
	; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;	HIS COMMAND ROM <1> THRU I <3>. THIS OME CAUTION, ARELESSLY IM	MOVES MAS <2> TO 1 ROUTINE AS IT CO PLEMENTED	S AMOUNTS OF MEMORY THE ADDRESS STARTING SHOULD BE USED WITH DULD SMASH MEMORY IF D.
	;	M<1>,<2	>,<3>	
00C5* FE 00C7* 20 00C9* CD 00CC* 7E 00CD* 02 00CE* 03 00CF* CD 00D2* 18	4D MOV 00B 00288* M 0028D* F8	E: CPI JRNZ CALL : MOV STAX INX CALL JMPR	M READ EXPR3 A.M B B HILOX.	SEE IF MOVE GET 3 PARAMETERS PICK UP PUT DOWN MOVE UP CHECK IF DONE
	: I F R B B I I V S L T L	HIS COMMAND I OR BOTH THE I ELOCATING FOI E ADDED, WHIC E PLACED IN NTENDED EXEC HAT WOULD HAY OCATION, AND DADING ANY PI	READS THE NORMAL IN RMAT. ON CH WILL C A LOCATIO JTION LOC VE BEEN I WILL WRA ROGRAM AN	CHECK-SUMMED HEX FILES TEL FORMAT AND THE TOL BOTH FILES, A 'BIAS' MAY AUSE THE OBJECT CODE TO N OTHER THAN ITS ATION. THE BIAS IS ADDED TO HE NORMAL LOADING P AROUND TO ENABLE YWHERE IN MEMORY.
	# W # P # A # B	HEN LOADING ARAMETER MAY CTUAL EXECUT E ANY LOCATIO	A RELOCAT BE ADUED ION ADDRE DN IN MEM	ABLE FILE, AN ADDITIONAL , WHICH REPRESENTS THE SS DESIRED. THIS ALSO MAY ORY.
	; E	XAMPLES:		
	; R ; R ; R ; R	[CR] =0 BIAS, <addr1>[CR] = ,<addr1>[CR] <addr1>,<addr< td=""><td>, O EXECU =&lt;1&gt;BIAS, =O BIAS, R2&gt;[CR] =</td><td>TION ADDR. O EXECUTION ADDR. &lt;1&gt; EXECUTION ADDR. &lt;1&gt;BIAS, &lt;2&gt; EXECUTION ADDR.</td></addr<></addr1></addr1></addr1>	, O EXECU =<1>BIAS, =O BIAS, R2>[CR] =	TION ADDR. O EXECUTION ADDR. <1> EXECUTION ADDR. <1>BIAS, <2> EXECUTION ADDR.
00 D4* FE 00 D6* C2 00 D9* CD 00 DC* 78 00 DD* D60 00 DF* 47 00 E0* 4F 00 E1* D1 00 E2* 280	52 READ 017C* 0296* 0D	CPI JNZ CALL MOV SUI MOV MOV POP JRZ	R SUBS EXPRI A,B CR B,A C,A D RO	SEE IF 'READ' COMMAND GET BIAS, IF ANY LOOK AT DELIMITER ALL DONE? SET UP RELOCATION OF O IF CR ENTERED BIAS AMOUNT CR ENTERED

,

00E4/ 00E7/	CD 0296* C1		CALL Pop	EXPR1 B	GET RELOCATION
00 E8	EB	RO:	XCHG		HIZEBIAS, BCZERELOCATION
OOEA	CD 0278		CALL	CRLF	
OOED'	CD 020C/	LODO:		RIFF 764	FGEL A CHARACIER
00F0 <sup>-</sup>			SUI	121	ABSOLUTE FILE CUE?
00F4	47		моч	B,A	SAVE CUE CLUE
00F51	E6FE		ANI	OFEH	KILL BIT O
00 F7*	20F4		JRNZ	LODO	TEPS OF OKSING
00-54	57				CET FILE LENGTH
OOFA'	5F		MOV	E.A	SAVE IN E REG.
00 FE1	CD 0162		CALL	SBYTE	IGET LOAD MSB
01017	F5		PUSH	PSW	SAVE IT
0102	CD 0162		CALL	SBY IE	CHANGE GEARS
0105	נס		POP	D	RECOVER MSB
01074	5F		MOV	Ē, A	FULL LOAD ADDR
1081	C5		PUSH	В	;BC/=RELOCATION
01091	D5		PUSH	D	
010A	E2 10			л D	: BIAS+LUAD
01001	E3	,	XTHL	2	RESTORE HL'
010D*	DDEI		POP	Х	; X=BIAS+LOAD
010F/	D9		EXX	11	
01112			CATI	SBYTE	GET FILE TYPE
0114	3D		DCR	A	; 1=REL. FILE, O=ABS.
01151	78		MOV	А, В	SAVE CUE BIT
0116	CI		POP	В	+BC=RELOCATION
0110	2003			••A B	FISE RELOCATE
0.114	DD09		DADX	B .	BOTH X & HL
01104	10	••A*	INR	E	TEST LENGTH
011D*	1D		DCR	Ε	10=DONE
OTIE	C8 ·			۵	TEST CUE
01201	2810		JRZ	LODR	RELATIVE
01221	CD 0162*	••L1=	CALL	SBY TE	;NEXT
01251	CD 0175			SIGRE	STURE II
0128	2018		CALL	SBYTE	IGET CHECKSUM
012D	28BE		JRZ	LODO	GOOD CHECKSUM
012F1	C3 001E'		JMP	ERROR	BAD, ABORT
01321	2E01	LODR	MVI	L.I	SET-UP BIT COUNTER
0134	CD 0152	••••••		LUDCB	TOUBLE BIT
01301	3807 CD 01754		CALL	STORE	WRITE IT
01301	20F6		JRNZ	••L1	
013E*	18EA		JMPR	LOD4	TEST CHECKSUM
0140		₹ئيل،،	MUV CALT	C, A LODCB	INFXT CONTROL BIT
0144	47		MOV	B,A	SAVE HIGH BYTE

.

0145'	D9 C5		EXX PUSH	В	GET RELOCATION
0147 0148 0149 0148 0148 0148 0148 0148 0145 0150 0152	D9 E3 O9 7D CD 0175* 7C E1 18E7 2D	LODCB:	E XX XTHL DAD MOV CALL MOV POP JMPR DCR	B A.L SIORE A.H H L5 L	INTO HL RELOCATE LOW BYTE STORE IT HIGH BYTE RESTORE HL DO THIS AGAIN COUNT BITS
0155/ 0155/ 0158/ 0159/ 015A/	2007 CD 0162* 1D 67 2E08	1.01.	CALL DCR MOV MVI	SBYTE E H, A L, 8 SBYTE	GET NEXT COUNT BYTES SAVE THE BITS BITS/BYTE
015F*	CB24	••••••	SLAR	H	TEST NEXT BIT
0162* 0163* 0166* 0167*	C5 CD 0333* 07 07	SBYTE:	PUSH CALL RLC RLC	B RIBBLE	PRESERVE BC GET A CONVERTED ASCII CHAR.
0168 0169 016A 016E 016E 016F 016F 0170 0171 0172 0173 0174	07 07 4F CD 0333* B1 4F 82 57 79 C1 C9		RLC RLC MOV CALL ORA MOV ADD MOV MOV POP RE T	C,A RIBBLE C,A D,A A,C B	#MOVE IT TO HIGH NIBBLE #SAVE IT #GET OTHER HALF #MAKE WHOLE #SAVE AGAIN IN C #UPDATE CHECKSUM #NEW CHECKSUM #CONVERTED BY TE
0175* 0178* 0178* 0178*	DD7700 DD23 1D C9	S.TORE *	MOV INX DCR RET	0(X),A X E	WRITE TO MEMORY ADVANCE POINTER COUNT DOWN
		THIS F MODIF BASIS FOLLOW LOCAT DESIRE ENTERE THE NE WILL ADDS XXXO PRESEN EACH O VP THE PRE VIC	ROUTINE ICATION O IT TAKE VED BY A ION WILL D TO CH. ED. A FO EXT BYTE IERMINATE A CRLF A DR XXX8. IT ADDRES CRLF. A FOINTEE DUS LOCAT	ALLOWS BO DF MEMORY ES ONE AD SPACE. BE DISPL ANGE II, DLLOWING A CARR THE COM I LOCATIO TO AID I SS, IT IS BACKARRO R AND DIS TION.	OTH INSPECTION OF & ON A BYTE BY BYTE DDRESS PARAMETER, THE DATA AT THAT AYED. IF IT IS THE VALUE IS THEN SPACE WILL DISPLAY IAGE RETURN [CR] MAND. THE SYSTEM ONS ENDING WITH EITHER N DETERMINING THE PRINTED AFTER W [_] WILL BACK PLAY THE

017C* 017E* 0180* 0183* 0184* 0185* 0185* 0188* 0188* 0188* 018E* 018E*	FE53 202E CD 0296* E1 7E CD 02E3* CD 0360* D8 2814 FE5F 2819	SUBS:	CP I JRNZ CALL POP MOV CALL CALL RC JRZ CP I JRZ CP I JRZ	WRITE EXPRI H A.M LBYTE COPCK S1 S2	<pre>;SEE IF 'SUBSTITUIE' ;GET STARTING ADDR. ;DISPLAY THE BYTE ;MODIFY? ; NO, ALL DONE ;DON'T MODIFY ;BACKUP? ;SAVE DOINTED</pre>
0192' 0193' 0195' 0198' 0198' 019C' 019C' 019E' 019F'	ED 0E01 21 0000 CD 029E* D1 E1 73 78 FE0D		MVI LXI CALL POP POP MOV MOV CPI	C, 1 H, 0 E 31 D H M, E A, B CR	GET NEW VALUE VALUE IN E MODIFY TEST DELIMITER
01A1 01A2 01A3 01A4 01A6	C8 23 7D E607 CC 021A*	5]: 53:	RZ INX MOV ANI CZ	H A.L 7 LFADR	DONE SEE IF TIME TO CRLF TIME TO CRLF
OI AB' OI AC'	18 <i>D</i> 9 2B 18F5	52: ;		H ••\$3	;DECREMENT POINTER ;AND PRINT DATA THERE.
		; THIS I ; INTEL ; PARAME ; OF THE ; GENER.	ROUTINE D HEX-FILE ETER IS R E DUMP, A ATED WITH	DUMPS MEN FORMAI. REQUIRED. N "END C H THE "E"	ORY IN THE STANDARD A START & END AT THE CONCLUSION F FILE" SHOULD BE COMMAND.
01 AE* 01B0*	FE57 2061	* WRITE*	CPI JRNZ	SIZE	SEE IF 'WRITE' COMMAND
0182* 0185* 0188* 0188* 0188* 0188* 0188*	CD 0273* CD 0374* CD 022C* 01 003A CD 0233* D5	••WO*	CALL CALL CALL LXI CALL PUSH	EXLF CI PEOL B,':' PO D	IGET IWU PARAMETERS IPAUSE FOR PUNCH-ON ICRLF TO PUNCH ISTART-OF-FILE CUE IPUNCH IT ISAVE POINTERS
01C2 01C3 01C4 01C7 01C9 01CB	04 CD 02C3* 3824 3E18 90 20F5	Wî≭	INR CALL JRC MVI SUB JRNZ	B HILO •.W4 A,24 B •.W1	SHORT FILE SHORT FILE 24 BYTES PER FILE ENOUGH YET? NO.
01CF 01D2 01D3	CD 01D5* D1 18E3		CALL POP JMPR	W2 D WO	SEND THE BLOCK RESTORE END OF FILE POINTER KEEP GOING

01D5 01D6 01D7 01DA 01DD 01DE 01E2 01E5 01E6 01E8 01E8 01E8 01EA 01ED 01EF 01EF	57 78 CD 034D* CD 0348* AF CD 034D* 7E CD 034D* 23 10F9 AF 92 C3 034D* E1 D1 AF 18E3	W2: W3: W4:	MOV MOV CALL CALL XRA CALL MOV CALL INX DJNZ XRA SUB JMP POP POP XRA JMP R	D. A A.B PBY TE PADR A PBY TE A.M PBY TE H W3 A D PBY TE H D D A W2	<pre># INITIAL IZE CHECKSUM #FILE LENGTH #PUNCH IT #PUNCH ADDRESS #FILE TYPE=0 #PUNCH IT #GET A DATA BYTE #PUNCH IT #POINT TO NEXT BYTE #DECREMENT FILE COUNT #CALCULATE CHECKSUM #PUNCH IT, RETURN #CLEAR STACK # OF POINTERS #SET-UP A #FINISH UP &amp; RETURN</pre>
		THIS IT IS POINT TOMI)	IS A MES USED B' ER IS II AND LEM	SSAGE OUT Y THE SIG N HL (WHE NGTH IN B	PUT ROUTINE. N-ON AND CRLF. N ENTERED A.T REG.
01F2* 01F5* 01F6* 01F7* 01F7* 01FC* 01FF* 0200*	21 0029' 4E 23 CD 0222' 10F9 CD 0282' B7 C8	TOM: TOM: TOM:	LXI MOV INX CALL DJNZ CALL ORA RZ	H, MSG C, M H CU TOM I CS TS A	GET A CHARACTER MOVE POINTER OUTPUT II KEEP GOING TILL B=0 SEE IF AN ABORT REQUEST WAITING. NO.
		; SEE I ; ABORI	F CONTRO IF SO.	DL-C IS W	AITING
0201* 0204* 0206* 0208*	CD 0374* E67F FE03 CO	•	CALL AN I CP I RNZ	CI 7FH 3	<pre>#KILL PARITY BIT #CONTROL-C?</pre>
02091	C3 001E*	FRRX:	JMP	ERROR	
·		THIS THIS AND C IT AB CONDI	GETS A F OMAPRES ORTS ON IION.	READER CH. IT WITH ( AN. 1001-0	ARACTER, 'D' REG. DF-DATA'
020C* 020F* 0211* 0212*	CD 037D* 38F8 BA C9	RIFF:	CALL JRC CMP RE T	RI ERRX D	GET READER CHARACTER SABORT ON CARRY STEST D
		THIS	ROUTINE	WILL RETU	JRN THE

TDI	2 Z80	RELOCATING <zap mon:<br="">Copyright 19</zap>	ASSEMBLE itor, Ve 977 by T	R VERSIO rsion 2. ECHNICAL	N 1.2 O, Jan. DESIGN	16 1977: LABS, II	> NC.		
			CURRE READ/ IS AV IS AV IT WI SIARI AND G IS FO	NT VALUE WRITE ME AILABLE LL "SEAR ING AI T O UPWARD UND.	OF THE MORY LOC ON THE S CH" FOR HE BOTTO S UNTIL	HIGHEST ATION T YSTEM. MEMORY M OF MEN NON-R/W	HAT MORY MEMORY	ł	
	02 13* 02 15* 02 17*	FE5A 2026 CD 0313'	S IZE:	CPI JRNZ CALL	VZV UNLD MEMSIZ	SEE II	F <b>/</b> SIZE HE VALU	JE COMM	AND
			; CRLF	BEFORE H	LSP ROUT	INE			
	02 I A-	CD 0278	‡ LFADR‡	CALL	CRLF				
		. /	; PRINT ; AND A	THE CUR SPACE.	RENT VALU	UE OF Ha	aL.		
	021D*	CD 02DE*	HLSP:	CALL	LADR				
			PRINT	A SPACE	ON THE C	CONSOLE			
	0220*	0E20	BLK:	NVI	C, * *				
			THIS OUTPU TELEP I/O D	IS THE M T ROUTIN RINTER CO RIVER.	AIN CONSU E. ONFIGURAT	DLE FION			
	0222* 0224* 0226* 0228* 0229* 0229*	DB00 E680 20FA 79 D301 C9	CO:	IN ANI JRNZ MOV OUT RET	TIS TIYBE CO A.C TIO				-
			SEND (	CRLF TO P	PUNCH DEV	/ICE			
	022C* 022E* 0231*	OEOD CD 0233' OEOA	FEOL:	MVI CALL MVI	C,CR PO C,LF				
			THIS DRIVER TIY PO FOR AN SEP AR AND RE	IS THE 'P R. IT IS DRTS, BU' NOTHER PO ATION OF EADER/PUN	PUNCH OU SET UP F I MAY BE DRT, FOR THE CONS NCH DEVIC	TPUT FOR THE MODIFIE TRUE SOLE CES.		ГС )	
	02224		; (I.E. ; D∏:	- PURI (	TTS	CADDE I	DODT	<b>U</b> .)	
	02351	E680		ANI	TIYBE	TRANSM	ITTER	BUFFER	EMP TY 7

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PAGE 1

1

0237* 0239* 023A* 023C*	20FA 79 D301 C9		JRNZ MOV OUT RET	PO A.C TTO	FIF NOT, LOOP. GET CHARACTER TO OUTPUIT TO DATA PORT DONE
		THIS USED SYSTE AND I FROM FILE USINC FOR F	IS A B IN WITH BOJ MS. IT HEN PUNC MEMORY. MARKER. THE "L" AST LOAD	IARY DUMP TH PAPER- PUNCHES HES IN FU IT IS FU IHESE DU COMMAND ING.	ROUTINE THAT MAY BE TAPE AND/OR CASSETTE A START-OF-FILE MARK ULL 8-BITS DIRECTLY OLLOWED BY AN END-OF- MPS MAY BE LOADED . THEY ARE USEFUL
		; U <a ; PUNCH</a 	1>, <a2>( IES FROM</a2>	CRI <ai> THR</ai>	U <a2></a2>
023D 023F 0241 0244 0247 024A 024D 024E 0251 0251 0256 0259	FE55 201A CD 0273' CD 0374' CD 02F6' CD 02F1' 4E CD 0233' CD 02C3' 30F7 CD 02F1' 1804	UNLD: U:	CP I JRNZ CALL CALL CALL CALL CALL CALL JRNC CALL JMPR	VU NULLX EXLF CI LEAD MARK C.M PO HILO .U MARK NULL	SEE IF 'UNLOAD' COMMAND GET TWO PARAMETERS PAUSE FOR PUNCH-ON (ITY) PUNCH LEADER PUNCH FILE MARKER GET MEMORY BY IE PUNCH IT SEE IF DONE PUNCH END FILE MARKER
		: THIS : II RE	PUNCHES TURNS "Q	NULLS (LE UIET"	EADER/TRAILER).
025B 025D 025F 0262	FE4E 206E CD 02F6* C3 004A*,	NULLX: NULL:	CPI JRNZ CALL JMP	'N' HEXN LEAD SIARO	SEE IF - NULL PUNCH NULLS RETURN QUIET
		CONVE	RT HEX T	O ASCII	
0265* 0266* 0267* 0268*	OF OF OF OF	CBYTE:	RRC RRC RRC RRC	-	
0269 0268 0260 026E 0270 0271 0271	E60F C690 27 CE40 27 4F C9		AN I ADI DAA ACI DAA MOV RET	OFH 90H 40H C,A	;LOW NIBBLE ONLY
		; THEM	IN DE &	HL, AND I	THEN

	; CRLF.	•				
0273' CD 029 0276' D1 0277' E1	8' EXLF:	CALL POP POP	E XP R D H			
	CONSC LINE	DLE CARR FEED RO	IAGE REIU UTINE.	RN &		
	THE MAY E MAY E VALUE VALUE IS FI	NUMBER O BE ADJUS PLACED FOR "B IVE (5).	FFILL CH TED TO O- IN THE B IS TWO	ARACTERS 3 BY THE REG. MINIMUM (2). MAXIMUM		
0278' E5 0279' C5 027A' 0604 027C' CD 01F 027F' C1 0280' E1 0281' C9	CRLF:	PUSH PUSH MVI CALL POP POP RET	Н В,4 Том В Н	SAVE HL & BC CRLF LENGTH SEND CRLF	(SETFOR 2 F	FILLS)
	; TEST ; KEYBC ; RETUF ; IF TH ; WAITI	THE CON JARD FOR IN TRUE IERE IS ING.	SOLE'S A KEY-PR (OFFH IN A CHARACI	ESS. A REG) ER		
0282* DB00 0284* E601 0286* 3E00 0288* C0 0289* 2F 028A* C9	¢ CS TS =	IN ANI MVI RNZ CMA RET	TIS TTYDA A, FALSE	;MAY NEED PAT ;IF DIFFERENT	CHING*** I/O USED	
	; GET I ; CRLF.	HREE PA	RAMETERS	AND		
0288' OC 028C' CD 029 028F' CD 027 0292' C1 0293' D1 0294' E1 0295' C9	EXPR3:	INR CALL CALL POP POP POP RET	C EXPR CRLF B D H			
	GET C ND CR	NE PARA	METER.			
0296* 0E01	÷ EXPR1:	MVI	C,1			
	; THIS ; THIS ; IT TA	IS THE P ROUTINE KES THE	MAIN "PAR. WILL ABOI MOST RECI	AMETER-GETTING RT ON A NON-HE ENTLY TYPED FO	" ROUTINE. X CHARACTER. NUR VALID	

TDL	<b>Z8</b> 0	RELOCATING	ASSEMBLE	ER VERSIO	N 1.2		
		<zap mon<="" td=""><td>itor, Ve</td><td>ersion 2.0</td><td>O, Jan.</td><td>16 197</td><td>17&gt;</td></zap>	itor, Ve	ersion 2.0	O, Jan.	16 197	17>
		Copyright 1	977 by 1	TECHN ICAL	DES IGN	LABS,	INC.

		; HEX C ; (AS D ; 8-BIT ; IT WI	HARACTER NE 16 BI BYTES.) LL PLACE	S, AND PI 1 VALUE, IF A C THE VALU	LACES THEM UP ON THE STACK. CONTAINED IN TWO ARRIAGE RETURN IS ENTERED, JE OF "0000" IN THE STACK.
0298 0298 0298 0297 0242 0242 0245 0245	21 0000 CD 03DC' 47 CD 0338' 3808 29 29 29	E XPR: E XO: EX:	L XI CALL MOV CALL JRC DAD DAD DAD	H,O TI B,A NIBBLE EX2 H H H	INITIALIZE HL TO ZERO GET SOMETHING FROM CONSOLE SAVE IT CONVERT ASCII TO HEX. ILLEGAL CHARACTER DETECTED MULTIPLY BY 16
02 A7* 02 A8* 02 A9* 02 A4* 02 AC*	29 85 6F 18EF F3	EX2:	DAD ORA MOV JMPR XTHL	H L L,A E 30	OR IN THE SINGLE NIBBLE
02 AD' 02 AE' 02 AE' 02 B2' 02 B2'	E5 78 CD 0368* 3002 0D	• • tap ( ) ta	PUSH MOV CALL JRNC DCR	H A,B QCHK .EX3 C	REPLACE THE RETURN TEST THE DELIMITER DELIMITER ENTERED? CR. SHOULD GO TO ZERO
0285* 0286* 0289* 0284* 028C*	C8 C2 001E* 0D 20DC C9	EX3:	RZ JNZ DCR JRNZ RET	ERROR C E XP.R	<pre># RETURN IF IT DOES #SOMETHING WRONG #DO THIS AGAIN? # YES. #ELSE RETURN</pre>
		RANGE CARRY	TESTING. SET IND	ROUTINES ICATES RA	S. NGE EXCEEDED.
02BD* 02C0* 02C1* 02C2*	CD 02C3*. D0 D1 C9	HILOX:	CALL RNC POP RET	HILO D	OK RETURN ONE LEVEL BACK
02C3* 02C4* 02C5* 02C6* 02C7* 02C8*	23 7C 85 37 C8 7B	¥ HILO≇	INX MOV ORA SIC RZ MOV	H A,H L	: INCREMENT HL :TEST FOR CROSSING 64K BORDER :CARRY SET=STOP :YES, BORDER CROSSED :NOW, TEST HL VS, DE
02C9 02CA 02CB 02CC	95 7A 9C C9	ţ	SUB MOV SBB RET	L A, D H	IF CARRY WAS SET, THEN SIDP
		; ;	HE XADEC :	IMAL MATH	ROUTINE
		; THIS.R ; DETERM ; OFFSET ; & DIFF ;	OUTINE I IINING RE S. IT R ERENCE C	IS USEFUL ELATIVE J RETURNS I DF IWO PA	. FOR UMP THE SUM RAMETERS.

	; H< }	>, <y></y>		
	X+Y	X-Y		
02CD' FE48 02CF' C2 039C' 02D2' CD 0273' 02D5' E5 02D6' 19 02D7' CD 021D' 02DA' E1 02DB' B7 02DC' ED52	HEXN:	CP I JNZ CALL PUSH DAD CALL POP ORA DSBC.	ΥΗΥ LOAD E >LF H D HLSP H A D	SEE IF HEX MATH SAVE HL FOR LATER GET SUM PRINT IT THIS IS LATER CLEAR CARRY GET DIFFERENCE & PRINT IT
	; PRINT	H&L ON	CONSOLE	
02 DE* 7C 02 DF* CD 02E3* 02E2* 7D 02E3* F5 02E4* CD 0265* 02E7* CD 0265* 02E7* CD 0222* 02EA* F1 02EB* CD 0269* 02EE* C3 0222*	LADR: LBY TE:	MOV CALL MOV PUSH CALL CALL POP CALL JMP	A,H LBYTE A,L PSW CBYTE CO PSW CONV CO	
	THIS I	ROUTINE E PUNCH	SÉNDS ELC DEVICE.	GHT RUBOUTS
02F1' 01 08FF 02F4' 1803	MARK:	LXI JMPR	B,08FFH LEO	SET-UP B&C
•	THIS I	ROUTINE DEVICE.	SENDS BLA	NKS TO THE
02F6' 01 4800 02F9' CD 0233' 02FC' 10FB 02FE' C9	LEAD LEO:	L XI C ALL D JNZ RE T	B,4800H PO LEO	PRESET FOR SOME NULLS
	THIS F PROGRA MEMORY	ROUTINE AM THE C ( VALUE JSED BY	RETURNS I URRENT IC MINUS WOR IHE MONIT	TO A USER DP OF RKSPACE TOR.
02FF* E5 0300* CD 0313* 0303* 44 0304* 3EC0 0306* E1 0307* C9	MEMCK :	PUSH CALL MOV MVI POP RET	H MEMSIZ B,H A,OCOH H	LEAVE SOME ROOM FOR STACK

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PAGE

	:					
	÷ .	WE BEGI	N IN THE	MIDDLE.	• • • • •	
0308' 3E00 030A' ED47 030C' AF 030D' D303	BEG IN:	MVI STAI XRA OUT	A, I A RCP	<pre># INITIAL #NEEDED # CLEAR L # PORT.</pre>	L 'I' REG. V IF USING IN READER CONTR	/ ALUE ITERUP T. ROL
030F* 31 00	341	LXI	SP, STACE	<	SET UP A F	AKE STACK
0312* 06	,	. BY TE	(MVI)		SKIP OVER	PUSH
•	; THIS ; TO CA ; START ; MEMOR ; FIRSI ; CONTI ; MEMOR ; AND I ; HAS B ; IT IS ; RESET	IS A CALI LCULATE ING FROM Y, AND SI R/W MEMU NUING UN Y. THIS NSURES A EEN FOUNI USED BY THE STAC	LED ROUT THE TOP O THE BOI EARCHING DRY IS FO TIL THE E ALLOWS R. CONTINUE C. THE ERRO CK POINTE	INE USED DF MEMORY IDM OF UPWARD U DUND, AND END OF TH O.M. AT DUS MEMOR DR ROUTIN ER.	INTIL D THEN HE R/W ZERG, RY BLOCK NE TO	
0313' C5 0314' 01 000 0317' 21 FFF 031A' 24 031B' 7E 031C' 2F	MEMSIZ: F	PUSH LXI LXI INR MOV CMA	B B,ZAP H,-1 H A,M	POINT T RAM SEA FIRST F	TO START OF ARCH STARTIN FIND R/W MEM	MONITOR IG PT1 IORY
031D' 77 031E' BE 031F' 2F 0320' 77 0321' 20F7 0323' 24 0324' 7E 0325' 2F 0326' 77 0327' BE 0328' 2F 0328' 2F 0329' 77 032A' 2004 032A' 2004	••M1*	MUV CMP CMA MUV JRNZ INR MUV CMA MUV CMP CMA MUV JRNZ	M • A M • A • • MO H A • M M • A M • A M • A • • M2 A • H	R/W FOU	IND, NOW FIN	
032C* 7C 032D* B8 032E* 20F3 0330* 25 0331* C1 0332* C9	M2:	MOV CMP JRNZ DCR POP RET	A,H B ••M1 H B	; IESI FL ;NOIT THE ;BACK UP ;VALUE I	REYET	URDER
	THIS CONVE	GETS A RE RTS IT FI	EADER CHA ROM ASCII	RACTER, TO HEX.	AND	
0333' CD 020 0336' E67F	C RIBBLE:	CALL AN I	R IFF 7FH			

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0338' 033A' 033B' 033D' 033E' 0341' 0342' 0343' 0345'	D630 D8 FE17 3F D8 FEOA 3F D0 D607 FEOA	N IBBLE 3	SUI RC CPI CMC RC CPI CMC RNC SUI * A* CPI	•0• •G•-•0• 10 -•9•-1 10	; QUALIFY & CONVERT ;<0 ;>F? ;PERVERT CARRY ;NMBR? ;PERVERT AGAIN ;RETURN CLEAN ; ADJUST ;FILTER ":" THRU "@"
0347 •	C9	Ŧ	RET		
		; SEND	HAL VALUI	E TO PUN	CH DEVICE
0348' 0349' 034C'	7C CD 034D* 7D	PADR:	MOV CALL MOV	A.H PBYTE A.L	
		PUNCH	A SINGLE	EBYTE	
034D 034E 0351 0355 0355 0355 0355 0355 0355 0355	F5 CD 0265 CD 0233 F1 F5 CD 0269 CD 0233 F1 82 57 C9	FBYTE:	PUSH CALL POP PUSH CALL CALL POP ADD MOV RET	PSW CBYTE PO PSW PSW CONV PO PSW D D,A	NIBBLE AT A TIME NEXT NIBBLE SAVE FOR CHECKSUM ORIGINAL BYTE HERE ADDED TO CHECKSUM UPDATE CHECKSUM
		; :			
0360* 0362* 0365*	0E2D CD 0222* CD 03DC*	COPCK:	MV I CALL CALL	C, CO TI	
		TEST F	OR DELIM	ITERS	
0368' 036A' 036B'	FE20 C8 FE2C	GCHK:	CPI RZ CPI	1.1 1.1	RETURN ZERO IF DELIMITER
036E <sup>2</sup> 0370 <sup>2</sup>	FEOD 37		CP I STC	CR	RETURN W/CARRY SET IF CR
0372* 0373*	3F C9		CMC RET		ELSE NON-ZERO, NO CARRY
		MAIN C	CONSOLE 1	INPUT ROU	TINE
0374 0376 0378 0378	DB00 E601 20FA DB01	CI:	IN AN I JRNZ IN	TTS TTYDA CI TII	

03701	C9	•	RET		
		READE TIME PULSI TO IN READE	R INPUT OUT DELA NG OF HA DICATE R R DATA.	ROUTINE, Y. INCLU RDWARE PO EQUEST FO	WITH DES DRT DR
		<pre># THIS # I∕O P # SEPAR</pre>	MAY BE A ORT CONF ATE READ	LTERED 10 IGURATION ER/PUNCH	D ANY N TO ENABLE DEVICE.
037D* 037E* 0380* 0382* 0383* 0385* 0386* 0388* 0388* 0388* 038C* 038D* 038F* 0390* 0391* 0393*	E5 3EFF D303 AF D303 67 DB00 E601 280C C5 C5 C5 C5 C5 C5 C5 C6FF E3 E3 10FC C1	RI: RIO: DLO:	PUSH MVI OUT XRA OUT MOV IN ANI JRZ PUSH MVI XTHL XTHL DJNZ POP	H A,OFFH RCP A RCP H,A TIS TTYDA RI2 B B,OFFH DLO B	<pre>;MAY BE ALTERED TO SUIT ;PULSE READER CONTROL PORT ;CLEAR IT ;CLEAR FOR TIME-OUT TEST ;MAY BE MODIFIED *** ;BUT ALWAYS USE 'ANI' ;TO CLEAR CARRY ;SHORTEN FOR HIGH-SPEED DEVICE ;WASTE TIME ;FOR DELAY</pre>
0395* 0395* 0397*	25 20EF 37	R.11 *	JRNZ STC	H RIO	**NOTE: CARRY SET TO INDICATE
0398* 039 A* 039B*	DB01 E1 C9	R 12 = R ID=	IN POP RET	TII H	¥ NU DAIA.
		; THIS ; IMAGE ; THE ; ONE P ; ADORE ; THE L ; CONSO	ROUTINE IN THE U" (UNLO) ARAMETER SS OF TH AST ADDR LE DEVICI	READS A E FORM AS AD) COMMA , WHICH I E LOAD, A ESS(+1) L E.	BINARY FILE PUNCHED IN AND. II TAKES IS THE STARTING AND WILL PRINT OADED ON THE
039C' 039E'	FE4C 205F	LOAD	CPI JRNZ	'L' NEXT	SEE IF 'LOAD' COMMAND
03 AO- 03 A3-	CD 0296* E1		CALL POP	EXPRI H	; INITIAL LOAD ADDRESS
03A7' 03A9' 03A8' 03AE' 03AE'	16FF 0604 CD 020C* 20F9	LO: LI:	MVI MVI CALL JRNZ	D, OFFH B, 4 RIFF ••LO	START-OF-FILE TAG FIND AT LEAST FOUR OFFH'S
03B2 03B5	CD 020C	L2:	CALL JRZ	RIFF	\$4 FOUND, NOW WALT FOR NON-OFFH

03B7' 77 03B8' 3E07 03BA' D301 03BC' 23 03BD' CD 020C' 03C0' 2803 03C2' 77 03C3' 18F7 03C5' 0601 03C7' CD 020C' 03C5' 0601 03C7' CD 020C' 03CA' 2009 03CC' 04 03CD' 3E07 03CF' B8 03D0' 20F5 03D2' C3 02DE' 03D5' 72 03D5' 72 03D6' 23 03D7' 10FC 03D9' 77 03DA' 18E0	EL: ELO: EL1:	MOV MVI OUT INX CALL JRZ MOV JMPR MVI CALL JRNZ JRNZ JRNZ JRNZ JRNZ JMP MOV INX DJNZ MOV JMPR	M,A A,BELL TTO H RIFF •EL M,A •L3 B,1 RIFF •EL1 B A,MAX B •ELO LADR M,D H •EL1 M,A •L3	<pre>;FIRST REAL DATA BYTE ;TELL TTY :POSS IBLE END OF FILE :INITIALIZE :COUNT QUES :LOOK FOR EOF :FOUND MAX? :NOPE :YEP, PRINT END ADOR :REAL BYTE</pre>
	THIS HANDL RUBOU AND I (NO N II CC CASE O THER ARE R	IS THE I ING ROUT ITS (OF FH IT WILL N I'S FOR I I'S FOR I NVERTS L FOR THE CHARACT RECIE VED.	NTERNAL INE. II OT ECHO THE "NULL OWER CAS LOOK-UP ERS ARE	KEYBOARD WILL IGNORE ANKS (OO), CR'S & N'S. " COMMAND). E TO UPPER OF COMMANDS. ECHOED AS THEY
03DC* CD 0374* 03DF* E67F 03E1* 3C 03E2* F8 03E3* 3D 03E4* C8 03E5* FE4E 03E7* C8 03E5* FE6E 03E8* FE6E 03E8* 2810 03EC* FE0D 03EC* FE0D 03EC* C8 03EF* C5 03F0* 4F 03F1* CD 0222* 03F4* 79 03F4* 79 03F5* C1 03F6* FE40 03F8* D8 03F9* FE7B 03F8* D0	; TI:	CALL ANI INR RM DCR RZ CPI RZ CPI JRZ CPI RZ PUSH MOV CALL MOV POP CPI RC CPI RC CPI RC CPI RC	CI 7FH A A ^N ^ CR B C,A CD A,C B ^ A,-1 'z*+1	<pre>:KILL PARITY BIT :IGNORE RUBOUTS :IGNORE NULLS :IGNORE N'S FOR NULL CMND :IGNORE CR'S :CONVERT TO UPPER CASE</pre>

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03FC* 03FE*	E65F C9	T: ; ;	AN I RE T	05F.H	
03FF'	C9	NEXT:	RET		ADDITIONAL COMMANDS MAY BE TESTED FROM HERE, AND THE MONITOR EXTENDED FROM BEYOND THIS POINT.
0400*		; ; ;	Z:		\$END OF PROGRAM
•0000		. END	ZAP		

## +++++ SYMBOL TABLE +++++

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AHE AD	0038*	BEGIN	03081	BELL	0007	BLK	0220-
CBY TE	0265*	CI	0374/	CO	02221	CONV	02694
COPCK	03604	CR	000D	CRLF	0278*	CSTS	02821
D ISP	0057 •	DLO	038F1	EOF	006E*	ERROR	001E*
ERRX	02091	EXO	029B1	EXI	029E1	EXLF	02731
EXPR	0298/	EXPRI	02961	EXP.R.3	028B*	FALSE	0000
FIL	0000	FILL	008C/	GOTO	00901	HEXN	02CD*
HILO	02031	HILOX	02BD*	HLSP	02101	I	0000
IOSET	00171	LADR	02DE /	LBY TE	02E31	LEO	02F9/
LEAD	02F61	LENGTH	04001	LF	000 A	LFADR	02141
LOAD	03904	LODO	00ED1	LOD4	0124	LODCB	01521
LODR	01321	MARK	02F1/	MAX	0007	MEMCK	02FF /
MEMSIZ	03131	MOVE	00051	MSG .	00291	MSGL	000D
NEXT	03FF	NIBBLE	0338/	NULL	025F	NULLX	025B/
PADR	0348	PBYTE	034D*	PEOL	.022C*	PO	02331
QCHK	03681	RCP	0003	READ	00 D4 1	RI	037D'
R IO	03861	RII	0397/	R I2	0398*	RIBBLE	03331
RID	039A *	RIFF	02001	RUB	OOFF	SBYTE	01621
SIZE	02131	STACK	00341	STARO	004 A-	START	003E1
STORE	01751	SUBS	0170/	IES T	00 46'	TI	03DC1
TOM	01F2	TOMI	01F51	IRUE	FFFF	TTI	0001
TIO	0001	TTS	0000	TTYBE	0080	ITYDA	0001
UNLD	02.3D*	WRITE	OIAE ·	Z	0400*	ZAP	0000

NO PROGRAM ERRORS

PAGE 19

## GENERAL INFORMATION

### A. Customer Service

Customer service falls into two broad categories:

- 1. Equipment troubleshooting
- 2. User applications counseling.

In the case of Equipment troubleshooting when you wish to return the unit for factory service, the following procedure should be adhered to whether the unit is under warranty or not.

- Write up the exact symptoms of the problem. Give exact details of what you observed, what you noticed, what you were doing when the problem was first noticed, etc.
- Describe the system you had in operation when the problem developed. Note kind of mainframe, accessory boards in use, program being run, etc. Also note if the other boards are still working correctly.
- 3. Describe what you have done to try and handle the problem. Please be as specific as possible.
- 4. Pack the unit well (You would be wise to keep the shipping carton and materials this unit came in for this possibility.) and return it <u>postpaid</u> to TDL.
- 5. If the unit is NOT under warranty, enclose an authorization to repair and bill to whatever dollar limit beyond which you would want to be informed before we continue.
- 6. If the unit is under warranty, it will be treated as per the conditions as laid out in the warranty.

In the case of user applications counseling, the service is generally free of charge. This service is designed to aid you in applications where your own ability or experience is not sufficient to provide the answer. This is not intended to provide a broad educational service of a general nature. Rather it is designed to answer specific applications problems where a "how to" may not be clear to a less than very experienced computerist. If your questions are specific, you will receive an answer as fast as is possible.

For questions of a more general nature, such as those that might repeat from many users, or for items which we feel would be of interest to a broader public, such will be printed up and distributed as part of the Z-80 User's group Newsletter which is currently being established. The newsletter will publish any information, program development, novel computer applications etc. which are either submitted to us by you, the user's, or by our engineers and programmers. Please feel free to contribute to this effort in any way.

As our development progresses, and as your programming ideas come in, a software library will be established for your use.

### TDL WARRANTY

TECHNICAL DESIGN LABS INC., in recognition of its responsibility to provide quality components and adequate instructions for their proper assembly, warrants its products as follows:

All components sold by Technical Design Labs Inc., (hereinafter referred to as TDL) are first quality prime and are procured from reputable distributors and/or factories and their representatives, and any part which fails because of defects in manufacture or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled products following the date of purchase as shown on the customer's invoice. For replacement, the defective part must be returned to TDL postpaid within the warranty period.

Any malfunctioning unit or subunit, purchased as a kit and returned to TDL within the 3 month warranty period, which in the judgement of TDL has been constructed with care, and has not been subject to electrical or mechanical abuse, will be restored to proper operating condition or replaced at TDL's discretion and returned, with a minimal charge to cover postage.

Any units or subunits purchased as a kit and returned to TDL within the 3 month warranty period, which in the opinion of TDL is not covered by the above conditions will be repaired and returned at a cost sommensurate with the work required. In no case will this charge exceed \$30.00 without prior notification and approval of the owner.

Any unit or subunit, purchased as assembled units are guaranteed to meet the specifications in effect at the time of manufacture for a period of at least one year following purchase. These units are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to TDL postpaid will be repaired and returned without charge providing only that no evidence of electrical or mechanical abuse exists.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the unit or subunit involved.



## TDL ZPU CARD BUS SIGNAL LIST

# (For explanation of asterisks (\*) see next page.)

1	+8v
2	+16v
3	XRDY
4	VIØ
5	VI 1
6	VI 2
7	<u>VT 3</u>
<u><u>é</u></u>	VT 4
<u> </u>	
<u> </u>	<u><u>v</u><u></u><u>v</u><u></u><u>v</u><u></u><u>v</u><u></u><u>v</u><u></u><u>v</u><u></u><u>v</u><u></u><u>v</u></u>
<del>+</del>	VI /
12	
<u> </u>	
<u>16</u>	·
17	
· <u>18</u>	STATUS DSBL
19	CCDSBL
20	****
21	SS
22	ADDR DSBL
23	DO DSBL
24	Ø2
25	Øl
26	PHLDA
27	PWAIT
28	PINTE
29	A5
30	<u>а</u> д
	<u> </u>
	<u></u> <u><u></u><u></u></u>
	<u>AQ</u>
	<u></u>
- 30	
40	
41	
42	D1. 3
43	DI 7
43	DI 7 SMI
43 44 45	DI 7 SMI SOUT
43 44 45 46	DI 7 SMI SOUT SINP
43 44 45 46 47	DI 7 SMI SOUT SINP SMEMR
$     \begin{array}{r}             43 \\             44 \\           $	DI 7 SMI SOUT SINP SMEMR SHLTA
$     \begin{array}{r}             43 \\             44 \\           $	DI 7 SMI SOUT SINP SMEMR SHLTA CLOCK (2MHz)

	<del>،</del>
51	+8v
52	-16v
53	SSW DSB
54	EXT CLR
55	*
56	**
	**
	**
<u> </u>	
<u> </u>	
62	
53	
64	
65	
66	
67	***
68	MWRITE
69	****
70	****
71	RUN
72	PRDY
73	PINT
74	PHOLI
	PRESEI
	PSINC
	PWR
/8	PDBIN
	<u>AØ</u>
80	<u>A1</u>
81	A2
82	A6
83	A7
84	A8
85	A13
86	Al4
87	All
88	DO 2
89	DO 3
90	DO 7
	DI 4
92	DT 5
	DT 6
	STN1X
<u> </u>	SWU DROUV(antidated)
<u> </u>	KFSH(OPTIONAL)
99	<u>+0C</u>
100	GND

*	reserved	for	chassis ground
* *	reserved	for	Altair 8800B
* * *	reserved	for	PTCO PHANTOM
***	reserved	for	protect status
****	reserved	for	memory unprotect
* * * * * *	reserved	for	memory protect

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 CMW reserved for Conditional Memory Write, which is a system protect signal on TDL's Memory Management Board.

