**TDL D-32 32K DRAM Board**

(From www.s100computers.com)

This was TDL's last board. It was advertised once in the July 1978 issue of Interface Age. It is now a very rare board.

The board had the following features:-

The D-32's high speed was based upon precise control of timing and conservative design. It operated in S-100 bus systems with cycle timing independent of the bus.  
  
Memory cycle timing was derived from a precision digital delay line, which was four times more accurate than other techniques at the time. Power consumption was minimized by the performance of dynamic refresh cycles only when required and by timing them with a 35khz oscillator. During normal program execution, refresh cycles occur following instruction fetch (MI) cycles, and were fully transparent.   
  
The D-32 was, they claimed, as reliable as static memory boards, since close attention was paid to the proper engineering discipline to maximize reliability. These details included: the use of molded ceramic bypass capacitors for superior noise immunity, keeping trace lines to the edge connector to a minimum to suppress noise spikes on the bus. Precisely-controlled timing and a multi-layer PC board with internal power and ground planes for superior noise immunity.   
  
The D-32 had a fully-transparent, dynamic refresh. Each 4096 byte block was addressable at any 4K page boundary. Extended address selection allows expandability to one megabyte co-resident in the system.   
  
Main Features:-  
Static board reliability   
32K byte memory   
Fastest S-100 board available  
Independently addressable 4-K blocks extended address selection for expansion to one megabyte   
5 megahertz typical performance, 4 megahertz worst-case   
Cycle timing independent of S-100 bus   
Precision digital delay line for highest speed   
Fully-transparent dynamic refresh   
Lowest power consumption   
Internal ground plane to increase noise immunity