OPERATIONS
MANUAL

SBC-100

Single Board Computer

SD SYSTEMS

REWORK/ERRATA SHEET DATE 3-1-80

PRODUCT SBC-100 MFG. LEVEL 5

APPROVAL [signature] SHEET 1

ERRATA (MANUAL REVISION 0)
SECTION VIII

8-2 ASSEMBLY PROCEDURE

1. Should read:

Install and solder the IC sockets in their proper locations.

Add: 14 Pin at U1-U3,U6-U10,U12,U14,U15,U21-U24,U26,U28,U32
16 Pin at U11,U13,U25,U27,U29
18 Pin at U19,U20
20 Pin at U4,U5,U30,U31,U33-U35
24 Pin at U36-U39
28 Pin at U16,U17
40 Pin at U18

2. Should read: Install and solder the resistors as follows:

APPENDIX C

Replace old Parts Placement Drawing with new Assembly Drawing.

ADD: Install two PCB ejectors using pins (See Assembly Drawing).

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OPERATIONS
MANUAL

SBC-100

SINGLE BOARD COMPUTER

JULY, 1980

REVISION A
MAY, 1980

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APPENDICES

SECTION I

INTRODUCTION

1-1 GENERAL

SBC-100 is an S-100 single board microcomputer containing the powerful Z80 microprocessor, 1024 bytes of RAM, 4K/8K bytes of ROM/PROM, synchronous/asynchronous serial I/O with RS-232 and current loop interfaces, and software programmable baud rate (up to 9600 BAUD), a parallel input port, a parallel output port, a four channel counter/timer, four maskable, vectored interrupt inputs and a non-maskable interrupt.

The SBC-100 provides enough on board memory and I/O for many control applications and also provides a low cost means to a disk based computer system when used with the EXPANDORAM AND VERSAFLOPPY boards.

1-2 FUNCTIONAL DESCRIPTION

Figure 1-1 is a block diagram describing the functional blocks contained on the SBC-100. The following sections describe each of the blocks in Figure 1-1.

1-3 Z80 CPU

At the heart of SBC-100 is the powerful Z80 microprocessor chip which provides the major control signals required to read and write to memory and I/O ports. The Z80 also generates a 16 bit address bus and an 8-bit bi-directional data bus.

1-4 CTC

The CTC (Counter/Timer Circuit) is a device which contains four independent 16 bit counters which may be used as "divide by" blocks for time delays or as event counters. The four event count inputs may optionally be used as vectored interrupt inputs from the S-100 bus. This allows use of the powerful Z80 mode 2 interrupt processing. Normally, channel 0 is used for generating the 16 x baud rate clock for the serial I/O channel.

1-5 OSCILLATOR

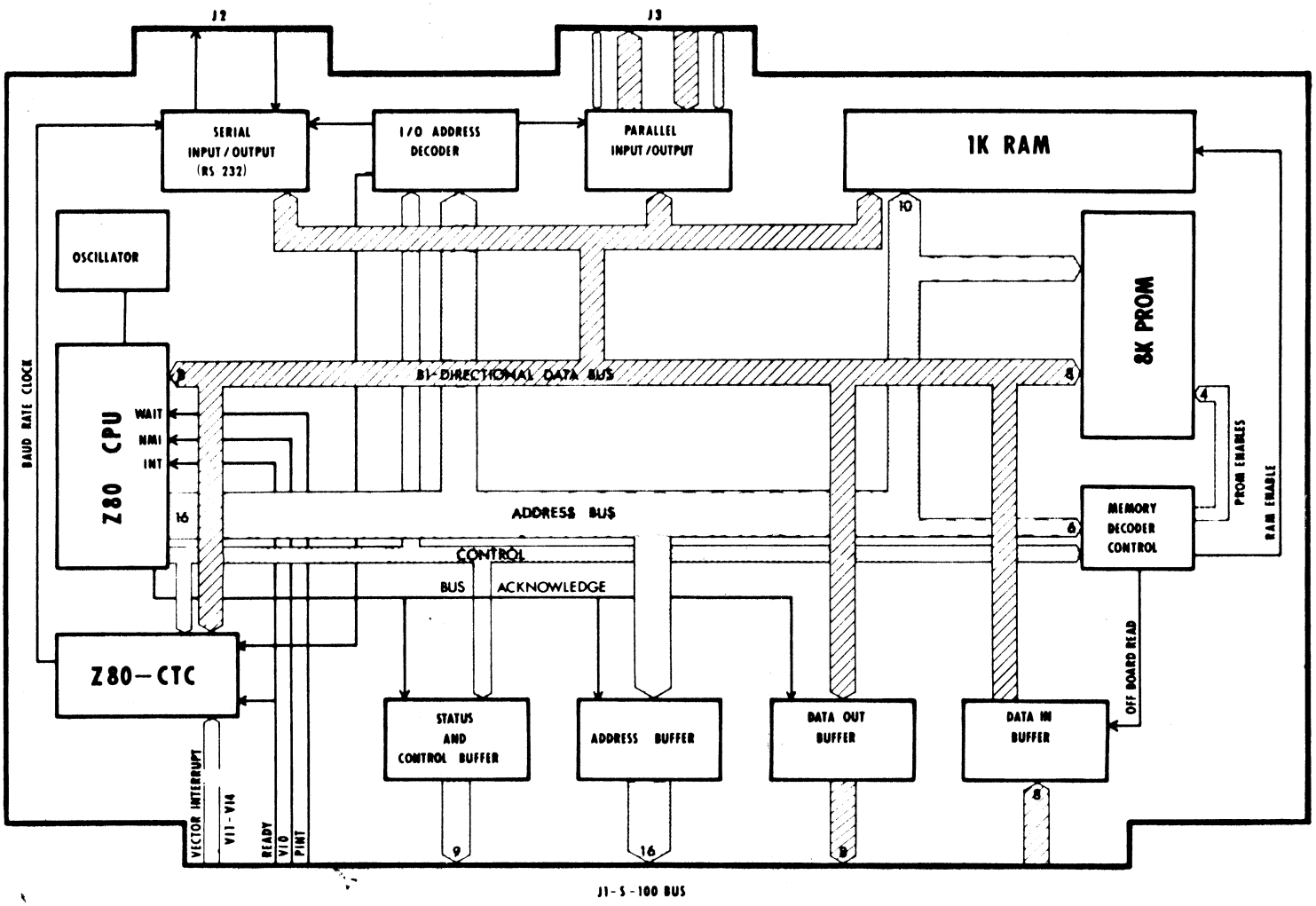
The oscillator is a crystal controlled circuit which generates the Ø clock for the system.

1-6 STATUS AND CONTROL BUFFER

The status and control buffer provides drive for the various S-100 bus status and control signals. During a DMA (BUSAK=1) the status and control BUFFER is turned off allowing the DMA device to control the S-100 bus.

1-7 ADDRESS BUFFER

The address buffer is actually a 16 bit latch/buffer. The latch is gated by MREQ=0, eliminating address changes during MREQ. The ADDRESS BUFFER is turned off during BUSAK=1.



BLOCK DIAGRAM

FIGURE 1.1

1-8 DATA OUT BUFFER

The Data Out Buffer is turned on at all times except during BUSAK=1. (DMA)

1-9 DATA IN BUFFER

The DATA IN BUFFER only turns on during off board memory or I/O reads or interrupt acknowledge cycles to off board devices.

1-10 MEMORY DECODE AND CONTROL

The Memory Decode and Control decodes the high order address bits and selects the RAM or PROM which is being addressed. This block also generates the Offboard signal used in controlling the DATA IN BUFFER.

1-11 ROM/PROM SOCKETS

The ROM/PROM sockets can hold up to four ROMS or PROMS each containing 1K, 2K, 4K or 8K bytes. The ROM and PROM may be strapped for any area of memory.

1-12 1K RAM

The 1K RAM is a static scratch pad RAM area. This RAM may also be strapped to occupy any area of memory.

1-13 PARALLEL I/O

There is one parallel input port and one parallel output port on SBC-100, each having two handshake lines.

1-14 I/O ADDRESS DECODE

This block decodes the low order 8 bits of address to determine which ports are being accessed during I/O instructions.

1-15 SERIAL I/O

The serial I/O provides synchronous and asynchronous serial I/O via RS-232 and current loop interfaces.

SECTION II

MEMORY

2-1 INTRODUCTION

The SBC-100 contains 1024 bytes of static RAM and sockets for 4 ROMS or PROMS. Each socket may contain a 1K, 2K, 4K or 8K byte ROM or PROM. Jumpers on SBC-100 allow mapping the RAM and ROM to reside at any location in memory and the auto-start circuit allows reset starting on any 4K boundary. The memory on the SBC-100 takes priority over any memory on another board which might occupy the same memory addresses.

2-2 COMPATIBLE ROMS AND PROMS

There are a number of ROMS and PROMS which can be used in the SBC-100. The following is a list of some of the known compatible devices:

INTEL	2758	1K x 8	EPROM	or EQUIVALENT
INTEL	2716	2K x 8	EPROM	"
INTEL	2732	4K x 8	EPROM	"
INTEL	2308	1K x 8	ROM	"
INTEL	2316	2K x 8	ROM	"
INTEL	2332	4K x 8	ROM	"
MOSTEK	34000	2K x 8	ROM	"
MOSTEK	32000	4K x 8	ROM	"
MOSTEK	36000	8K x 8	ROM	"
FAIRCHILD	93451	1K x 8	BIPOLAR PROM	"

2-3 ROM TYPE SELECTION JUMPERS

There are several jumpers which must be set up to determine the type of ROMS/PROMS to be used. These jumpers are on header X2. Figure 2-1 shows the physical pin arrangement of X2.

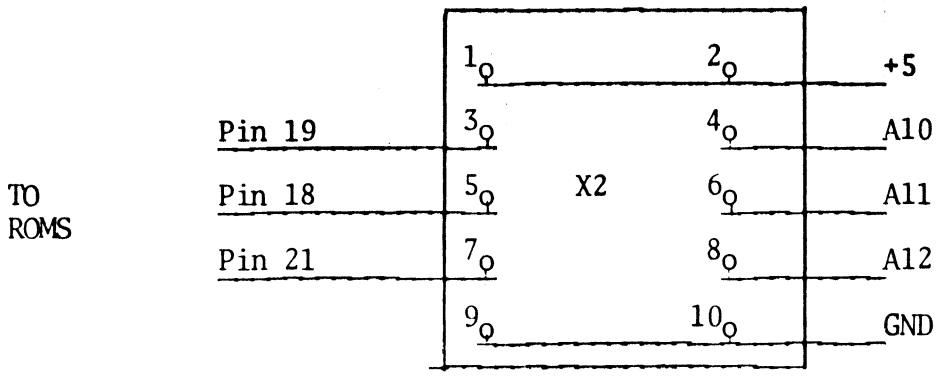


Figure 2-1

Table 2-1 contains a list of jumpers for each of the previously listed ROMS and PROMS. Note that Rev B boards are etch jumpered for 2716 EPROMS.

PART #	DESCRIPTION	JUMPERS
I 2758	1K x 8 EPROM	X2-3,X2-9,X2-5 to X2-10,X2-7 to X2-1
I 2716	2K x 8 EPROM	X2-3 to X2-4,X2-5 to X2-10,X2-7 to X2-1
I 2732	4K x 8 EPROM	X2-3 to X2-4,X2-5 to X2-10,X2-7 to X2-6
I 2308	1K x 8 ROM	Same as 2758
I 2316	2K x 8 ROM	Same as 2716
I 2332	4K x 8 ROM	Same as 2732
MK 34000	2K x 8 ROM	Same as 2716 (custom CS options)
MK 32000	4K x 8 ROM	Same as 2732 (custom CS options)
MK 36000	8K x 8 ROM	X2-3 to X2-4,X2-5 to X2-6,X2-7 to X2-9
FAIRCHILD	1K x 8 BIPOLAR PROM	X2-3 to X2-1,X2-5 to X2-2,X2-7 to X2-9

TABLE 2-1

2-4 MEMORY MAPPING

There are several selections which must be made when setting up the memory map. The first is selecting the bank of memory to be occupied by the RAM and ROM/PROM on SBC-100. Header X1 contains these jumpers as shown in Figure 2-2.

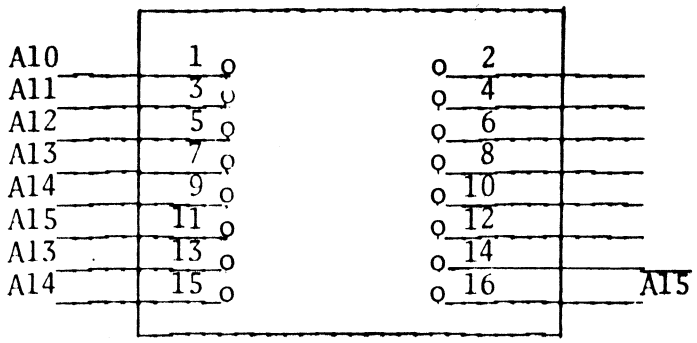


Figure 2-2

Two types of jumpers are on X1. The first type determines the number of bytes contained in each ROM/PROM socket. The second type determines the particular bank or area of memory the SBC-100 memory (RAM and ROM) will occupy. These jumpers are detailed in Tables 2-2 and 2-3. Rev B boards are etch-jumpered for 2K Byte ROMS to reside in the top (Bank #3) of memory.

ROM/PROM SIZE (PER CHIP)	JUMPERS
1K BYTES	X1-1 to X1-2, X1-3 to X1-4, X1-5 to X1-6
2K BYTES	X1-2 to X1-3, X1-4 to X1-5, X1-6 to X1-7, X1-8 to X1-10
4K BYTES	X1-2 to X1-5, X1-4 to X1-7, X1-6 to X1-9, X1-8 to X1-10, X1-10 to X1-12
8K BYTES	X1-2 to X1-7, X1-4 to X1-9, X1-6 to X1-11

TABLE 2-2
Rom Size Selection

ROM/PROM CHIP SIZE	JUMPERS	BANK SELECTION	BANK #
1K BYTES	X1-8 to X1-13, X1-10 to X1-15, X1-12 to X1-16	0000-1FFF	0
	X1-8 to X1-7, X1-10 to X1-15, X1-12 to X1-16	2000-3FFF	1
	X1-8 to X1-13, X1-10 to X1-9, X1-12 to X1-16	4000-5FFF	2
	X1-8 to X1-7, X1-10 to X1-9, X1-12 to X1-16	6000-7FFF	3
	X1-8 to X1-13, X1-10 to X1-15, X1-12 to X1-11	8000-9FFF	4
	X1-8 to X1-7, X1-10 to X1-15, X1-12 to X1-11	A000-BFFF	5
	X1-8 to X1-13, X1-10 to X1-9, X1-12 to X1-11	C000-DFFF	6
	X1-8 to X1-7, X1-10 to X1-9, X1-12 to X1-11	E000-FFFF	7
2K BYTES	X1-10 to X1-15, X1-12 to X1-16	0000- FFF	0
	X1-10 to X1-9, X1-12 to X1-16	4000-7FFF	1
	X1-10 to X1-15, X1-12 to X1-11	8000-BFFF	2
	X1-9 to X1-10, X1-11 to X1-12	C000-FFFF	3
4K BYTES	X1-12 to X1-16	0000-7FFF	0
	X1-12 to X1-11	8000-FFFF	1
8K BYTES	NONE	0000-FFFF	0

TABLE 2-3
MEMORY BANK SELECTION

Now that the memory bank has been selected, it is necessary to select the specific addresses each ROM/PROM socket will occupy as well as the 1K bytes of RAM. Header X3 is used to select these options as shown in Figure 2-3.

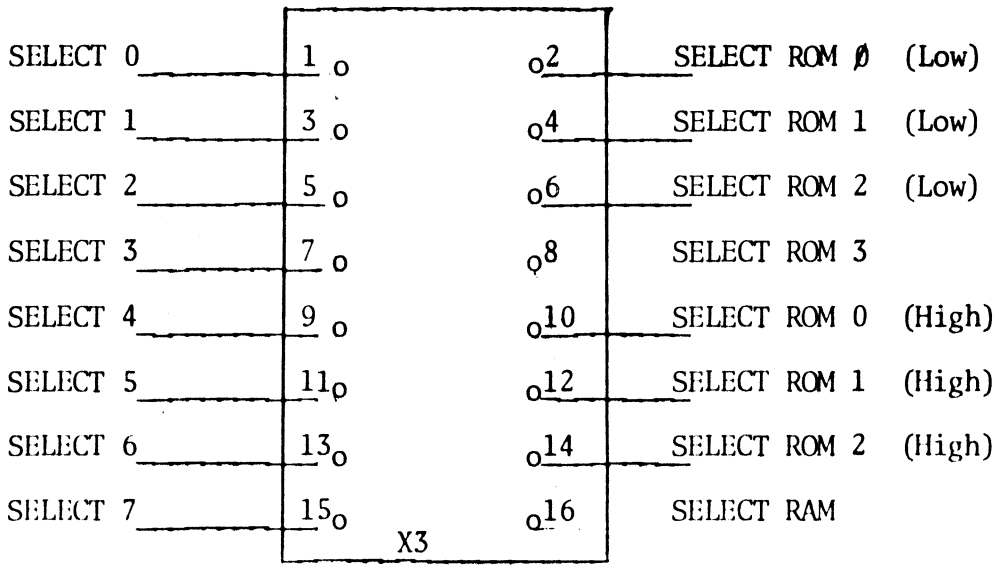


Figure 2-3

Note that ROMS 0, 1 and 2 may occupy one of two possible locations within the bank specified by the X1 jumpers in Table 2-3 while ROM 3 may occupy only one location. The RAM will occupy a portion of the specified memory bank; usually the last section of a bank. Two things are important to understand at this point. The first is that the only sections of the memory map occupied by the SBC-100 are those jumpered in on X3. If only one PROM is needed in the system, only install the X3 jumper for that socket. This allows use of a 64K EXPANDORAM with the SBC-100 only occupying 1K.

The second important point is that when the on board 1K Static Ram is used, it will occupy the same amount of memory as each of the ROM/PROM sockets. (Table 2-2) For example, if 2K ROM/PROMS are used, the 1K RAM will occupy two contiguous 1K blocks, redundantly. Table 2-4 contains the jumpers required to select the memory space for each ROM socket and the RAM.

1K ROM/PROM

NAME	LOCATION	JUMPER	BANK 0	BANK 1	BANK 2	BANK 3	BANK 4	BANK 5	BANK 6	BANK 7
ROM 0	U36	X3-1 to X3-2	0000-03FF	2000-23FF	4000-43FF	6000-63FF	8000-83FF	A000-A3FF	C000-C3FF	E000-E3FF
ROM 1	U37	X3-3 to X3-4	0400-07FF	2400-27FF	4400-47FF	6400-67FF	8400-87FF	A400-A7FF	C400-C7FF	E400-E7FF
ROM 2	U38	X3-5 to X3-6	0800-0BFF	2800-2BFF	4800-4BFF	6800-6BFF	8800-8BFF	A800-ABFF	C800-CBFF	E800-EBFF
ROM 3	U39	X3-7 to X3-8	0C00-0FFF	2C00-2FFF	4C00-4FFF	6C00-6FFF	8C00-8FFF	AC00-AFFF	CC00-CFFF	EC00-EFFF
ROM 0	U36	X3-9 to X3-10	1000-13FF	3000-33FF	5000-53FF	7000-73FF	9000-93FF	B000-B3FF	D000-D3FF	F000-F3FF
ROM 1	U37	X3-11 to X3-12	1400-17FF	3400-37FF	5400-57FF	7400-77FF	9400-97FF	B400-B7FF	D400-D7FF	F400-F7FF
ROM 2	U38	X3-13 to X3-14	1800-1BFF	3800-3BFF	5800-5BFF	7800-7BFF	9800-9BFF	B800-BBFF	D800-DBFF	F800-FBFF
RAM	U19,U20	X3-15 to X3-16	1C00-1FFF	3C00-3FFF	5C00-5FFF	7C00-7FFF	9C00-9FFF	BC00-BFFF	DC00-DFFF	FC00-FFFF

2K ROM/PROM

NAME	LOCATION	JUMPER	BANK 0	BANK 1	BANK 2	BANK 3
ROM 0	U36	X3-1 to X3-2	0000-07FF	4000-47FF	8000-87FF	C000-C7FF
ROM 1	U37	X3-3 to X3-4	0800-0FFF	4800-4FFF	8800-8FFF	C800-CFFF
ROM 2	U38	X3-5 to X3-6	1000-17FF	5000-57FF	9000-97FF	D000-D7FF
ROM 3	U39	X3-7 to X3-8	1800-1FFF	5800-5FFF	9800-9FFF	D800-DFFF
ROM 0	U36	X3-9 to X3-10	2000-27FF	6000-67FF	A000-A7FF	E000-E7FF
ROM 1	U37	X3-11 to X3-12	2800-2FFF	6800-6FFF	A800-AFFF	E800-EFFF
ROM 2	U38	X3-13 to X3-14	3000-37FF	7000-77FF	B000-B7FF	E000-F7FF
RAM	U19,U20	X3-15 to X3-16	3800-3FFF	7800-7FFF	B800-BFFF	F800-FFFF

			8K ROM	4K ROM	
NAME	LOCATION	JUMPER	BANK 0	BANK 0	BANK 1
ROM 0	U36	X3-1 to X3-2	0000-1FFF	0000-0FFF	8000-8FFF
ROM 1	U37	X3-3 to X3-4	2000-3FFF	1000-1FFF	9000-9FFF
ROM 2	U38	X3-5 to X3-6	4000-5FFF	2000-2FFF	A000-AFFF
ROM 3	U39	X3-7 to X3-8	6000-7FFF	3000-3FFF	B000-BFFF
ROM 0	U36	X3-9 to X3-10	8000-9FFF	4000-4FFF	C000-CFFF
ROM 1	U37	X3-11 to X3-12	A000-BFFF	5000-5FFF	D000-DFFF
ROM 2	U38	X3-13 to X3-14	C000-DFFF	6000-6FFF	E000-EFFF
RAM	U19,U20	X3-15 to X3-16	E000-FFFF	7000-7FFF	F000-FFFF

TABLE 2-4

SECTION III

AUTO START

3-1

Since many systems require RAM starting at address 0, the SBC-100 has the capability of automatically causing control to begin on any 4K boundary upon resetting the board. Table 3-1 contains the jumpers required to start on each of the possible 4K boundaries.

START ADDRESS (HEX)	JUMPERS
0000	X17-2 to X17-3, X18-5 to X18-6, X16-2 to X16-3, X18-2 to X18-3
1000	X17-2 to X17-3, X18-5 to X18-6, X16-2 to X16-3, X18-1 to X18-2
2000	X17-2 to X17-3, X18-5 to X18-6, X16-1 to X16-2, X18-2 to X18-3
3000	X17-2 to X17-3, X18-5 to X18-6, X16-1 to X16-2, X18-1 to X18-2
4000	X17-2 to X17-3, X18-4 to X18-5, X16-2 to X16-3, X18-2 to X18-3
5000	X17-2 to X17-3, X18-4 to X18-5, X16-2 to X16-3, X18-1 to X18-2
6000	X17-2 to X17-3, X18-4 to X18-5, X16-1 to X16-2, X18-2 to X18-3
7000	X17-2 to X17-3, X18-4 to X18-5, X16-1 to X16-2, X18-1 to X18-2
8000	X17-1 to X17-2, X18-5 to X18-6, X16-2 to X16-3, X18-2 to X18-3
9000	X17-1 to X17-2, X18-5 to X18-6, X16-2 to X16-3, X18-1 to X18-2
A000	X17-1 to X17-2, X18-5 to X18-6, X16-1 to X16-2, X18-2 to X18-3
B000	X17-1 to X17-2, X18-5 to X18-6, X16-1 to X16-2, X18-1 to X18-2
C000	X17-1 to X17-2, X18-4 to X18-5, X16-2 to X16-3, X18-2 to X18-3
D000	X17-1 to X17-2, X18-4 to X18-5, X16-2 to X16-3, X18-1 to X18-2
E000	X17-1 to X17-2, X18-4 to X18-5, X16-1 to X16-2, X18-2 to X18-3
F000	X17-1 to X17-2, X18-4 to X18-5, X16-1 to X16-2, X18-1 to X18-2

TABLE 3-1

When writing software which will be entered upon reset, two instructions must be executed immediately following reset:

ADDRESS	SOURCE CODE	OBJECT CODE
X000	JP X003	C3 03 X0
X003	IN Z,(7FH)	DB 7F

This resets the hardware which caused execution to occur at X000 instead of 0000. The only case where these instructions are not needed is when X=0 i.e. when resetting to 0000.

The S.D. Monitor resides at EØØØ and requires that the jumpers be set to cause an auto start to that address. When resetting to the disk controller prom (BIOS). Set the auto start for FØØØ.

The P.C. Board is etch-jumpered for auto starting at E000 or F000. Only the last jumper (X18-2) must be connected to select between the two start-up addresses.

SECTION IV

SERIAL I/O

4-1 INTRODUCTION

The SBC-100 contains one serial I/O port with RS-232 and current loop interfaces. The hardware allows both asynchronous and synchronous data communications with BAUD rates from 110 to 9600. The standard S. D. Monitor utilizes the serial I/O port for console interaction in the async mode.

4-2 BAUD RATE GENERATOR

The CTC (Counter-Timer Circuit MK3880) is a four channel counter/timer and one channel is used for generating the 16X BAUD RATE CLOCK required by the SERIAL I/O.

The standard S.D. Monitor waits for the first keyboard entry after being reset, measures the pulse width of the start bit, and sets up the CTC to match the BAUD rate. Table 4-1 lists the CTC counts required for each of the standard BAUD rates from 110-9600.

BAUD RATE CONSTANTS

SYSTEM CLOCK RATE	BAUD RATE	DIVIDED BY	CTC CONSTANT
2.4576 MHZ	110	1392	57_H
	300	512	20_H
	600	256	10_H
	1200	128	08_H
	2400	64	04_H
	4800	32	02_H
	9600	16	01_H

TABLE 4-1

4-3 USART

The serial communications are controlled by a 8251 USART (Universal Synchronous/Asynchronous Transmitter/Receiver). This device controls the serial to parallel and parallel to serial data conversions, synchronizing with data in both asychronous and synchronous modes, error checking and generating the key RS-232 signals. For complete details of this device see the Intel data sheet.

The USART resides at port address $7C_H$ and $7D_H$, with 7C being data and 7D status/control.

The standard S.D. MONITOR sets the USART up as follows:

```
LD      A,4EH
OUT     (7DH),A
LD      A,37H
OUT     (7DH),A
```

The baud rate is then set up by outputting 05H followed by the appropriate constant from Table 4-1 to CTC port 78H:

```
LD      A,05H
OUT     (78H),A
LD      A,1             9600 BAUD
OUT     (78H),A
```

The following routines may then be used to input and output to the serial I/O channel.

```
SERIN   IN      A, (7DH)    Input Status
        AND     2
        JP      Z,SERIN     Wait for RX data ready
        IN      A, (7CH)    Read Data
        AND     7FH         Strip off parity
        RET
```

```
SEROUT      IN      A, (7DH)      Input Status
            AND     1
            JP      Z,SEROUT      Wait for TX ready
            LD      A,C,          Data in C
            OUT     (7CH,) A      Output H
            RET
```

4-4 SERIAL I/O CABLE

The J2 card edge connector contains the RS-232 and current loop signals from the serial I/O port. This connector is pinned out so that when a 26 pin flat cable (mass terminated) is used with a D-25 connector, the SBC-100 looks a MODEM to a device being connected. This allows pin to pin connection to most CRT terminals and serial printers. 20MA current loop signals are also provided. Table 4-2 is a list of the J2 pinout.

J2	D-25 CONNECTOR RS-232 TYPE		SIGNAL NAME
3	2	INPUT	RECEIVED DATA ($\overline{RX}$)
4	15	INPUT	RECEIVER CLOCK (OPTIONAL)
5	3	OUTPUT	TRANSMITTED DATA ($\overline{TX}$)
7	4	INPUT	REQUEST TO SEND (RTS)
8	17	OUTPUT	TRANSMITTER CLOCK (OPTIONAL)
9	5	OUTPUT	CLEAR TO SEND (CTS)
11	6	OUTPUT	DATA SET READY (DSR)
13	7		LOGIC GROUND
14	20	INPUT	DATA TERMINAL READY (DTS)
15	8	OUTPUT	CARRIER DETECT (CD)
22	24		RX + CURRENT LOOP
23	12		RX - CURRENT LOOP
24	25		TX - CURRENT LOOP
25	13		TX + CURRENT LOOP

TABLE 4-2

4-5 SERIAL I/O JUMPER OPTIONS

Several options must be selected when using the serial I/O channel. Install the jumpers specified in Table 4-3 to select the required serial I/O configuration. When the SBC-100 is to be connected to a MODEM, the RS-232 signal pins must be reversed. (TX & RX, RTS & CTS, DSR & DTR).

OPTION	JUMPERS
Standard Asynchronous Operation (Etch jumpered on P.C. Board.	X9-1 to X9-2 X10-2 to X10-3 X11-1 to X11-2 X6-2 to X6-3
Synchronous Mode with External RX Clock	X10-1 to X10-2 X4-2 to X4-3 X6-1 to X6-2 X11-2 to X11-3
External Baud Rate Clock	X9-1 to X9-3
Other options may be selected for specific user requirements. See SBC-100 Schematic, Sheet 3 for details.	

TABLE 4-3

SECTION V

PARALLEL INPUT/OUTPUT

5-1 INTRODUCTION

SBC-100 contains one parallel input port and one output port with two handshake lines each. Table 5-1 contains the pin out for J3, the parallel I/O connector:

J3 PINOUT		
PIN NUMBER	DIRECTION	DESCRIPTION
1		Logic Ground
3	OUTPUT	PDOØ, Parallel Data Out Bit Ø
5	OUTPUT	PDO1, Parallel Data Out Bit 1
7	OUTPUT	PDO2, Parallel Data Out Bit 2
9	OUTPUT	PDO3, Parallel Data Out Bit 3
11	OUTPUT	PDO4, Parallel Data Out Bit 4
13	OUTPUT	PDO5, Parallel Data Out Bit 5
15	OUTPUT	PDO6, Parallel Data Out Bit 6
17	OUTPUT	PDO7, Parallel Data Out Bit 7
19	INPUT	ORPLY, Output Reply
21	OUTPUT	OSTB, Output Strobe
23		+5 Volts
4	INPUT	PDI0, Parallel Data In Bit 0
6	INPUT	PDI1, Parallel Data In Bit 1
8	INPUT	PDI2, Parallel Data In Bit 2
10	INPUT	PDI3, Parallel Data In Bit 3
12	INPUT	PDI4, Parallel Data In Bit 4
14	INPUT	PDI5, Parallel Data In Bit 5
16	INPUT	PDI6, Parallel Data In Bit 6
18	INPUT	PDI7, Parallel Data In Bit 7
20	OUTPUT	IRPLY, Input Reply
22	INPUT	ISTRB, Input Strobe

TABLE 5-1

5-2 PARALLEL OUTPUT PORT

The parallel output port is composed of an eight bit latch and two handshake lines. The latch is addressed at $7E_H$ and the handshake lines at $7F_H$. The outputs of the latch are tri-state and may optionally be disabled by the ORPLY handshake input. The ORPLY is read via port $7F_H$, bit Ø. This line may be used to let the SBC-100 know when the output device (such as a printer) is ready to receive data. The other handshake line (OSTB) is used to strobe the data to the output device. This line may be jumpered for positive or negative pulses and may optionally be reset by the $\overline{\text{ORPLY}}$ line. The OSTB line is controlled by a one bit latch addressed at output port $7F_H$, bit Ø. See Table 5-2 for option selection details.

5-3 PARALLEL INPUT PORT

The parallel input port is composed of an 8 bit latch and two handshake lines. The 8 bit latch is addressed at $7E_H$ while the handshake lines are addressed at $7F_H$.

The ISTRB handshake line sets a flip-flop when a positive transition occurs. The output of this flop is read at port address 7F, bit 1, and indicates that data is available from the input device. (When bit 1=0, data is available). The flop is cleared when data is input from port $7E_H$. The $\overline{Q}$ of the flop is the $\overline{\text{IRPLY}}$ line which indicates to the input device that the data has been received. Table 5-2 contains the details of options on the parallel input port.

PARALLEL INPUT/OUTPUT PORT OPTIONS

PARAMETER	OPTIONS	JUMPERS
1. Parallel out data Enabled:	a. Always b. Only during $\overline{\text{ORPLY}}$	X4-7 to X4-8 X4-8 to X4-9
2. Output Strobe Polarity (OSTB)	a. Positive true b. Negative true	X4-4 to X4-5 X4-5 to X4-6
3. Output Strobe Cleared by:	a. Output Reply (ORPLY) b. Software Control	X5-1 to X5-2 None
4. Input Port Latch Gated:	a. Always b. By Input Strobe (ISTRB)	X7-2 to X7-3 X7-1 to X7-2

TABLE 5-2

SECTION VI

THE COUNTER/TIMER CIRCUIT (CTC)

6-1 INTRODUCTION

The counter/timer circuit utilizes the MK3882 CTC chip which features four independent channels which may be configured to operate in various modes as required. See the Mostek MK3882 data sheet for details of programming the CTC. (Normally on the SBC-100, channel 0 is used to generate the BAUD rate clock.) CTC channels 0, 1, 2 and 3 are addressed at 78_H, 79_H, 7A and $7B_H$ respectively.

6-2 CTC AS INTERRUPT CONTROLLER

The SBC-100 allows using the CTC as a vectored interrupt controller. For this, the channels to be used as vector interrupt inputs must be jumpered to the S-100 pins as shown in Table 6-1. Additionally, if other external interrupts must be prioritized with the CTC interrupts, pins 14 and 64 may optionally be used to create an interrupt daisy chain between boards.

CTC VECTORED INTERRUPT INPUTS		
INTERRUPT CHANNEL	SOURCE	JUMPER
0	VI1	X14-1 to X14-2
1	VI2 SYNDET	X14-3 to X14-4 X14-3 to X12-3
2	VI3 SERIAL RX READY	X13-2 to X13-3 X13-1 to X13-2
3	VI4 SERIAL TX READY	X12-4 to X12-5 X12-5 to X12-6

TABLE 6-1

To use interrupt priority daisy chain, connect: X14-1 to X14-2 and X15-3 to X15-4.

SECTION VII

SYSTEM CLOCK SELECTION

7-1 INTRODUCTION

The standard version of the SBC-100 utilizes a 4.9152 MHZ system clock (Ø). This frequency was selected to allow for precise baud rate generation by the CTC.

7-2 CLOCK JUMPER

X8 provides a means of selecting the system clock on the SBC-100. The standard configuration uses the divide-by-two circuit. However, the user may wish to use another crystal value and bypass the divide-by-two. Table 7-1 describes the X8 jumpers.

DESCRIPTION	JUMPER
Divide By Two (Standard)	X8-1 to X8-2
No Divide by Two	X8-2 to X8-3

TABLE 7-1

7-3 HIGHER CLOCK RATES

The SBC-100 may be operated at higher clock rates with several device changes. The user should realize that if the serial interface is to be used it is impossible to go to 9600 baud accurately using the CTC baud rate generator unless the standard crystal is used. However, an external baud rate generator may be used if higher system clock rates are required.

The following devices are required to allow 4 MHZ operation:

1.	Z80A (MK3880-4)		
2.	CTCA (MK3882-4)		
3.	8251A		
4.	2114-3	300 nsec	Access Time
5.	ROM/PROM	350 nsec	Access Time

SECTION VIII

CONSTRUCTION

8-1 INTRODUCTION

The Single Board Computer kit is intended for those people who have had some prior experience with kit building and digital electronics. If you do not fall into this category, it is highly recommended that you find an experienced person to help you in assembly and check out the board.

Appendix B shows the parts list for the Single Board Computer. Double check all the parts against this parts list.

8-2 ASSEMBLY PROCEDURE

1. Install and solder the IC sockets in their proper locations.

   A. 14-Pin-U1-U3, U6-U10, U12, U14, U15, U21-U24, U26, U28, U32
   B. 16-Pin-U11, U13, U25, U27, U29
   C. 18-Pin-U19, U20
   D. 20-Pin-U4, U5, U30, U31, U33-U35
   E. 24-Pin-U36-U39
   F. 28-Pin-U16, U17
   G. 40-Pin-U18

2. Install and solder the resistors as follows:

   A. R1,4,6,8,12,18 220 Ohm, 1/4W 10% (RED,RED,BROWN)
   B. R2,3,5,10 2.4K Ohm, 1/4W 10% (RED,YELLOW,RED)
   C. R7,22 Ohm, 1/4W 10% (RED,RED,BLACK)
   D. R9,1.2 Ohm, 1/4W 10% (BROWN,RED,RED)
   E. R11, 4.7K Ohm, 1/4W 10% (YELLOW,VIOLET,RED)
   F. R13,14 820 Ohm, 1/4W 10% (GRAY,RED,BROWN)
   G. R15,19 10K Ohm, 1/4W 10% (BROWN,BLACK,ORANGE)
   H. R16,17 150 Ohm, 1/2W 10% (BROWN,GREEN,BROWN)
   I. RP1,2,3 Resistor Pack 4.7K Ohm 6 pin SIP
   J. RP4 Resistor Pack 10K Ohm 10 pin SIP

   NOTE: Pin 1 of the SIP is designated by a notch or dot on the end of this package.

3. Install diodes CR1, Cr2 and CR3 with the banded end as shown on the PC Board.

   A. CR1 Zener diode 1N751 -5V
   B. CR2, 3 Zener diodes 1N4742A -12V

4. Install the capacitors as follows:

   A. C1,2,3,18,25V tantalum (Note: Proper Polarity)
   B. C4-6, C8-12,17,19-24,26 0,1 MF 50V
   C. C7 100 Pf
   D. C13 33 Pf
   E. C14 10 Pf
   F. C15 .01 MF
   G. C16 470 Pf

5. Install the voltage regulator with the heat sink, using the 6-32 hardware supplies.

   Heatsink TO-3
   VR1 323 +5V

6. Install BERG PIN HEADERS (on top side of board with long portion of Pin up).

   A. X3 2 by 8 65610-416
   B. X18 1 by 6 65599-406

   NOTE: All X-numbers with Pin 1 are marked on the PC board. Double check all the pin headers and their pin configuration before any wire wrapping.

7. Install transistors Q1 and Q2.

8. Install crystal Y1 (XTAL 4.915MHZ)

9. Double check all solder connections for cold solder joints. Unsoldered connections or shorted connections.

8-3 VOLTAGE CHECK

1. Install the board into Bus-100 connector and measure the output of +5V regulator VR1, +12V and -12V Of CR2 and CR3 respectively.

   A. VR1 = +5V (Right side pin, looking from front of PCB)
   B. CR2 = -12V (Anode)
   C. CR3 = +12V (Anode)

2. Measure the power supply voltages in the Single Board Computer chips. (Any of the IC socket can be used).

NOTE: Do not proceed with board checkout until all power supply voltages are correct. The TTL and MOS logic can Be permanently damaged if improper voltages are applied.

3. Install the IC's in their sockets observing the pin 1 designation on each socket marked on the PC Board.

A.	U1	75188/MC1488
B.	U2	75189/MC1489
C.	U3, 22, 23	74LS74
D.	U4, 5, 30, 31	74LS373
E.	U6, 14, 26, 32	74LS32
F.	U7, 8	74LS02
G.	U9, U21	74LS04
H.	U10	74LS20
I.	U11	74LS138
J.	U12	74LS30
K.	U13	74LS368
L.	U15	74LS122
M.	U16	USART 8251
N.	U17	MK3882 CTC
O.	U18	MK3880 Z80 CPU
P.	U19, U20	2114/4114
Q.	U28	74LS14
R.	U24	74LS08
S.	U25, 27	74LS367
T.	U29	74LS139
U.	U33, 34	74LS244
V.	U35	74LS240
W.	U36, 37, 38, 39	ROM 0-3

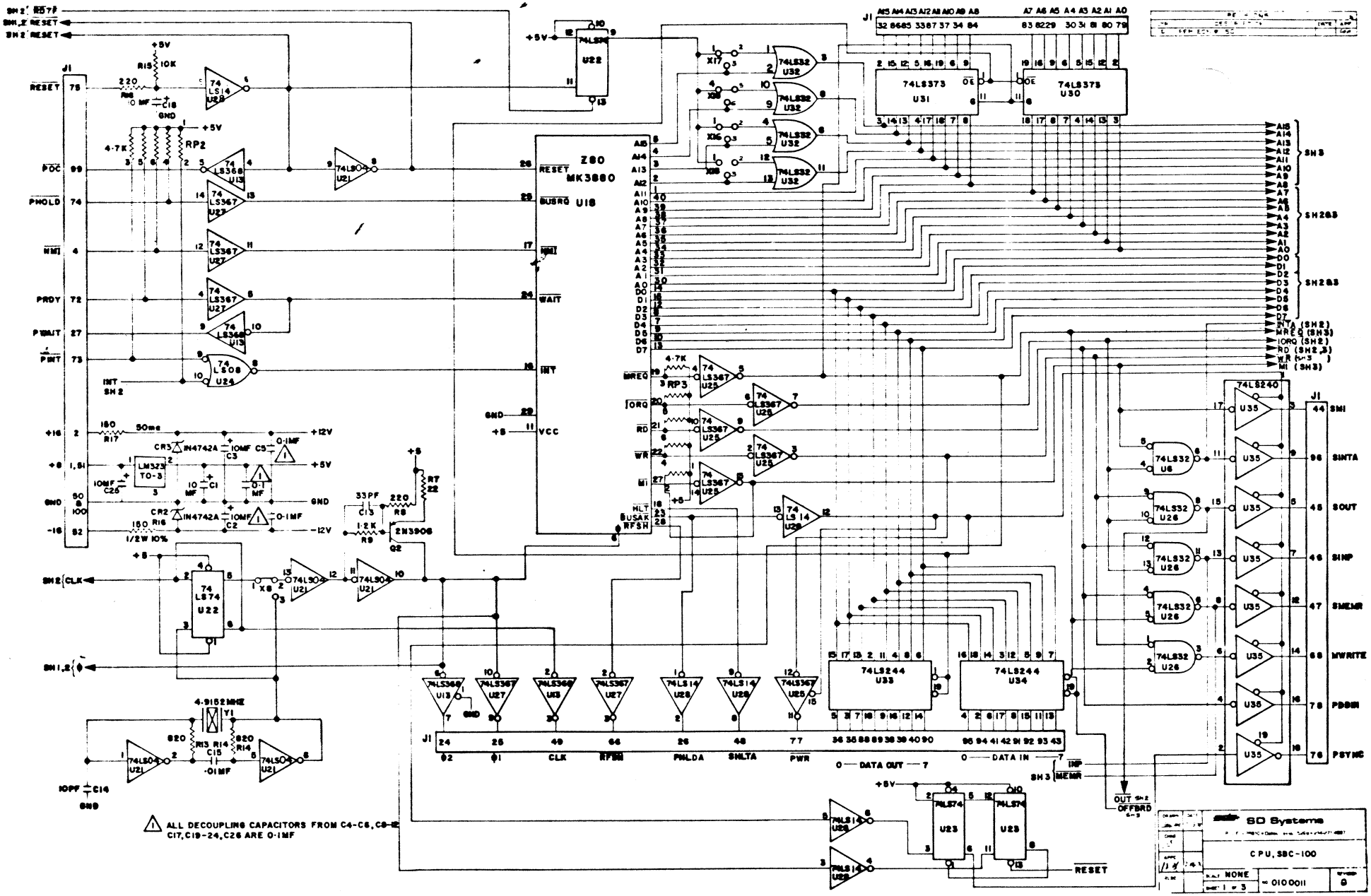
4. Double check all IC's for proper orientation and location.

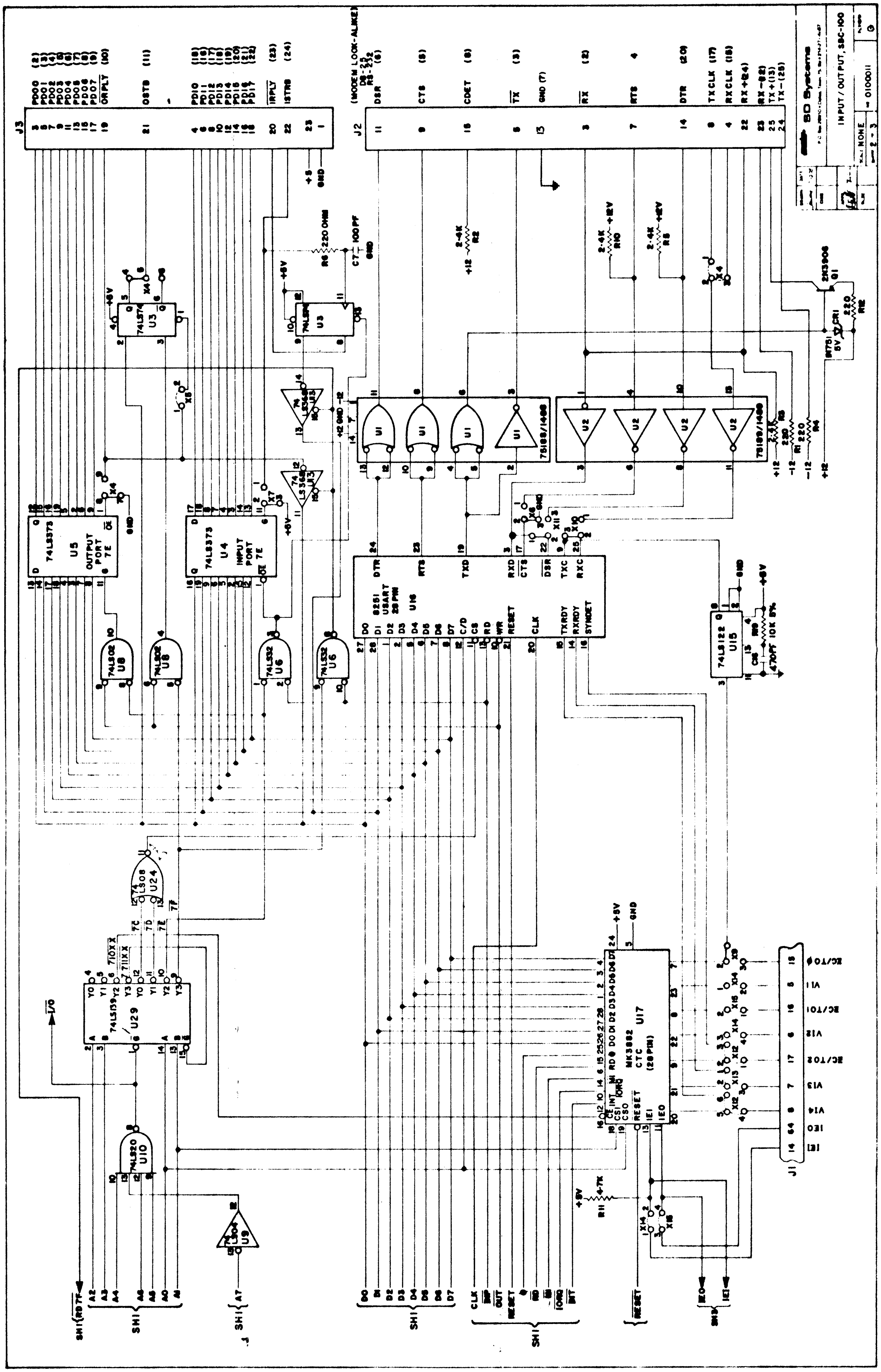
5. Refer to other Sections for proper configuration of jumper options and connect jumpers as required.

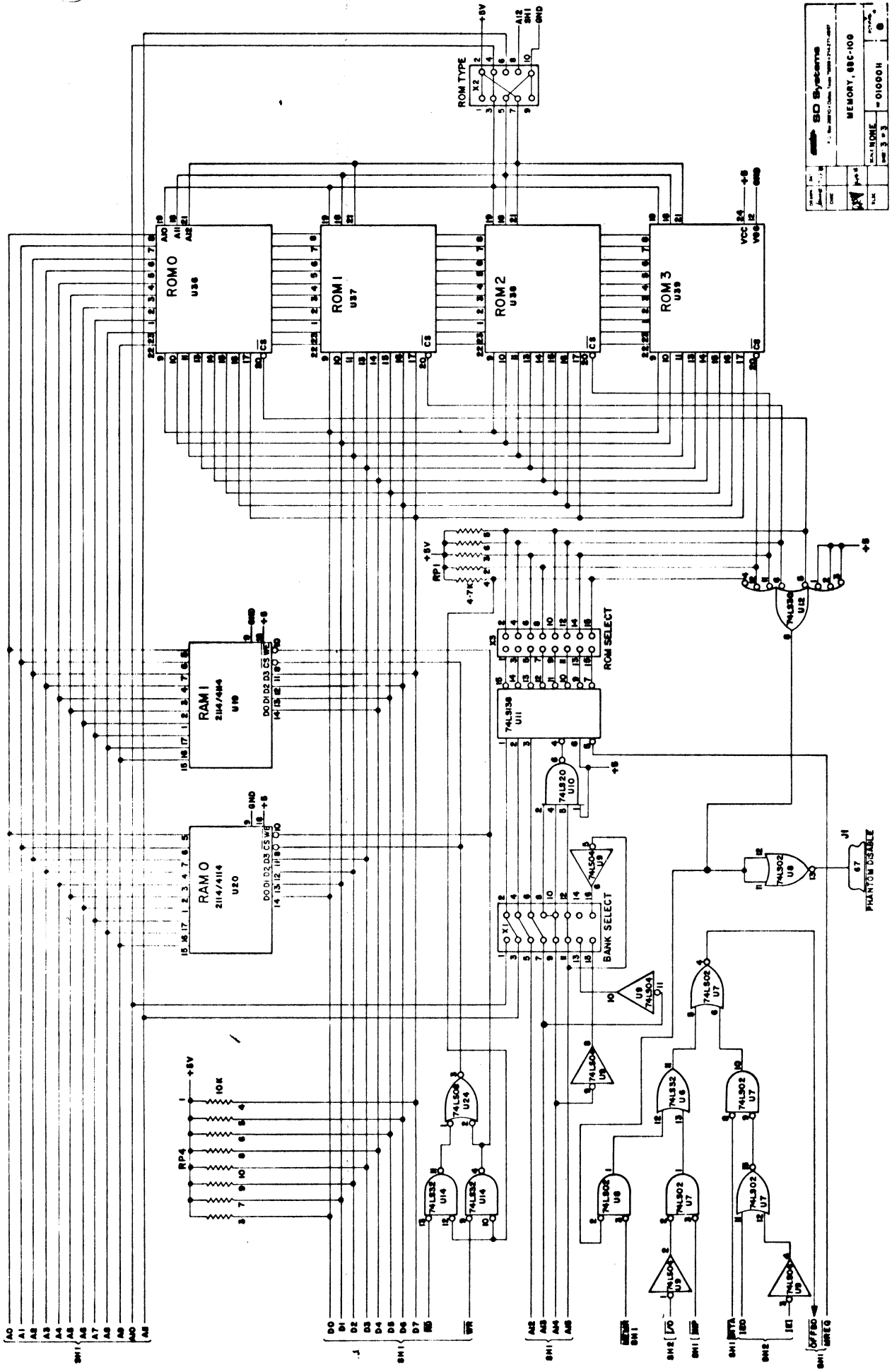
6. Install two PCB ejectors using pins (see Assembly Drawing).

APPENDIX A

SBC-100 SCHEMATIC


Z80 MK3880
CPU, SBC-100
SD Systems
ALL DECOUPLING CAPACITORS FROM C4-C6, C8-12 C17, C19-24, C26 ARE 0-1MF
4.9152 MHz
DATA OUT
DATA IN
RESET


SD Systems
INPUT / OUTPUT, SBC-100


SD Systems
MEMORY, 68C-100
ROM TYPE
ROM 0
U36
ROM 1
U37
ROM 2
U38
ROM 3
U39
RAM 1
2114/4044
U19
RAM 0
2114/4114
U20
ROM SELECT
BANK SELECT
PHANTOM DISABLE
RP1
4.7K
RP4
10K
74LS138 U11
74LS20 U10
74LS04 U9
74LS08 U24
74LS32 U14
74LS02 U8
74LS02 U7
74LS00 U12
74LS04 U9
74LS32 U6
74LS02 U7
74LS04 U9
74LS02 U7
74LS04 U9
74LS02 U8
J1
67

APPENDIX B

SBC-100 PARTS LIST

SD Systems

P.O. Box 28810 • Dallas, Texas 75228 214-271-4687

BILL OF MATERIALS

Title:	PL No.	Rev.
SBC-100 SINGLE BOARD COMPUTER	0100010	K

Date Released:	Approved:	Sheet 1 Of 3
May 25, 1978	DDH CLF	

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
1	1	7000003	P. C. Board 0100012		
2	1	7010318	Z-80 CPU, U18		
3	1	7010320	CTC, MK3882, U17		
4	2	7010321	RAM 2114, U19, 20		
5	1	7010341	USART, 8251, U16		
6	1	7080003	XTAL 4.9152 MHZ, Y1		
7	2	7010162	74LS02, U7, 8		
8	2	7010164	74LS04, U9, 21		
9	1	7010166	74LS08, U24		
10	1	7010172	74LS14, U28		
11	1	7010174	74LS20, U10		
12	1	7010180	74LS30, U12		
13	4	7010181	74LS32, U6, 14, 26, 32		
14	3	7010195	74LS74, U3, 22, 23		
15	1	7010213	74LS122, U15		
16	1	7010219	74LS138, U11		
17	1	7010220	74LS139, U29		
18	1	7010260	74LS240, U35		
19	2	7010264	74LS244, U33, 34		
20	2	7010302	74LS367, U25, 27		
21	1	7010303	74LS368, U13		
22	4	7010304	74LS373, U4, 5, 30, 31		
23	1	7010332	75188/MC1488, U1		
24	1	7010333	75189/MC1489, U2		

SD Systems

P.O. Box 28810 • Dallas, Texas 75228 214-271-4887

BILL OF MATERIALS

Title: SBC-100 SINGLE BOARD COMPUTER	PL No. 0100010	Rev. K
Date Released: May 25, 1978	Approved: DDH	Sheet 2 Of 3

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
25	18	7060002	Socket, 14 Pin U1, U2, U3, U6, U7, U8, U9, U10, U12, U14, U15, U21, U21, U22, U23, U24, U26, U28 & U32		
26	5	7060003	Socket, 16 Pin U11, U13, U25, U27 & U29		
27	2	7060004	Socket, 18 Pin U19 & U20		
28	7	7060005	Socket, 20 Pin U4, U5, U30, U31, U33, U34 & U35		
29	4	7060007	Socket, 24 Pin U36 THRU U39		
30	2	7060008	Socket, 28 Pin U16 & U17		
31	1	7060009	Socket, 40 Pin U18		
32	1	7160002	Voltage Reg., 5V 3A VR1		
33	5	7030009	Capacitor, 10MFD, 25V, C1-3, C18, C25		
34	16	7030045	Capacitor, .1 MFD, 50V, C4-6, C8-12, C17, C19-24,		
			C26		
35	1	7030008	Capacitor, .01 MFD 50V, C15		
36	1	7030015	Capacitor, 470 PFD, 50V, C16		
37	1	7030048	Capacitor, 10 PFD, 50V, C14		
38	1	7030047	Capacitor, 33 PFD, 50V, C13		
39	1	7030049	Capacitor, 100 PF, 50V, C7		
40	1	7010347	Resistor SIP, 10K 10 Pin, RP4		
41	3	7010348	Resistor SIP, 4.7K, 6 Pin RP1, 2, 3		
42	6	7020057	Resistor, 220 Ohm, ¼W, 10%, R1,4,6,8, 12,18		
43	2	7020171	Resistor, 150 Ohm, ½W, 10%, R16, 17		
44	2	7020071	Resistor, 820 Ohm, ¼W, 10%, R13, 14		
45	1	7020089	Resistor, 4.7K, ¼W, 10%, R11		
46	1	7020075	Resistor, 1.2K, ¼W, 10%, R9		
47	1	7020033	Resistor, 22 Ohm, ¼W, 10%, R7		

SD Systems

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BILL OF MATERIALS

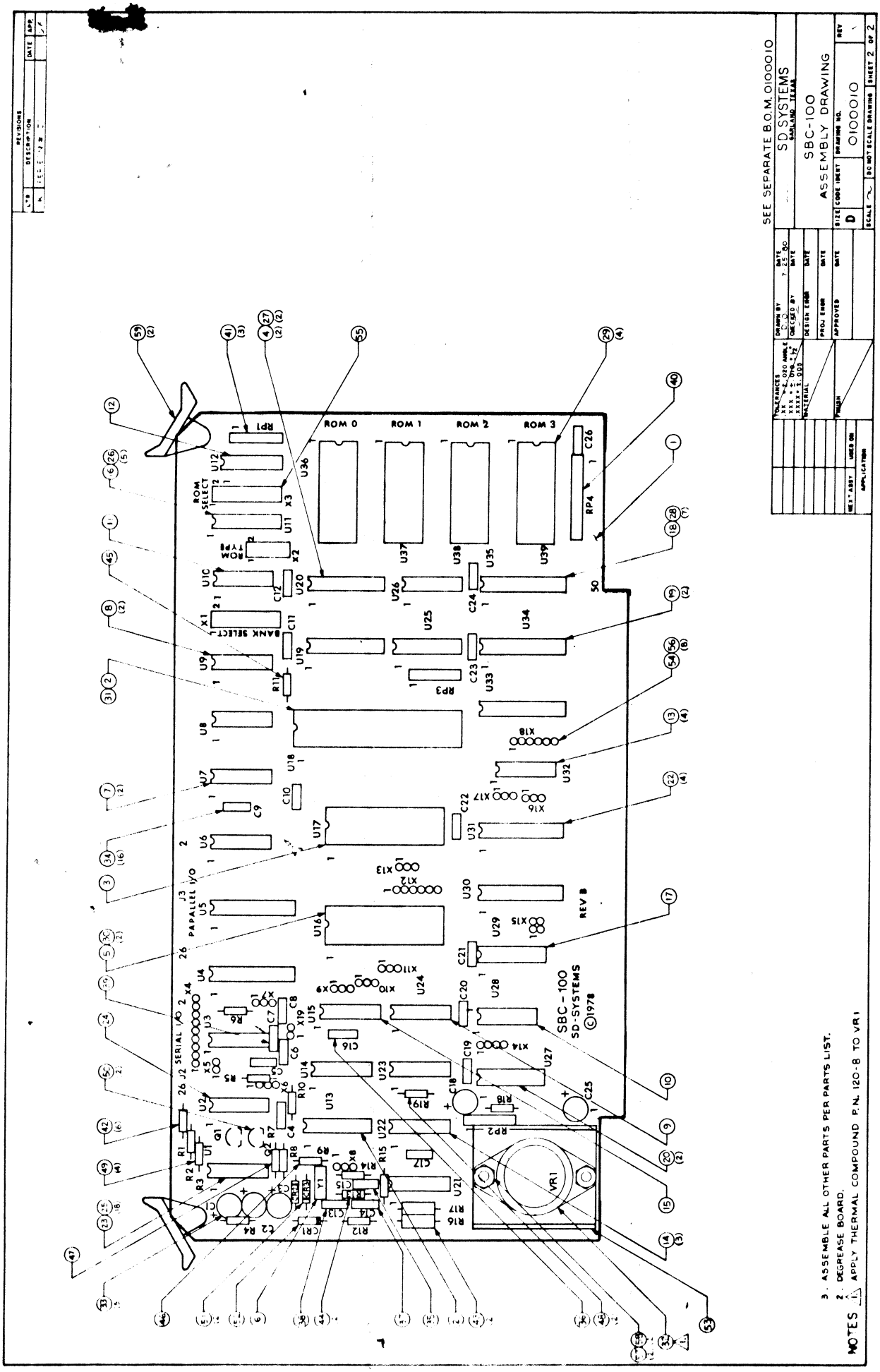
Title:	PL No.	Rev.
SBC-100 SINGLE BOARD COMPUTER	0100010	K

Date Released:	Approved:	Sheet 3 Of 3
May 25, 1978	DDH	

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
48	2	7020097	Resistor, 10K, ¼W, 10%, R15, R19		
49	4	7020082	Resistor, 2.4K, ¼W, R2,3,5,10		
50	2	7040006	Transistor, Q1, Q2		
51	2	7040004	Diode, Zener 12V, 5% CR2, CR3		
52	1	7040003	Diode, Zener 5V1N751, CR1		
53	1	7130004	Heat Sink		
54	1	7170002	Berg Straight Header (1x6), X18		
55	1	7170003	Berg Straight Header (2x8) X3		
56	8	7170004	Berg PV Jumpers		
57	2	7130006	Screw, 6-32 X 3/8		
58	2	7130007	Nut, 6-32		
59	2	7130072	EJECTOR P.C.B.		

APPENDIX C

SBC-100 ASSEMBLY DRAWING


SEE SEPARATE B.O.M. 0100010
SD SYSTEMS
SBC-100
ASSEMBLY DRAWING
0100010
SIZE D
SHEET 2 OF 2
ROM 0
ROM 1
ROM 2
ROM 3
SBC-100
SD-SYSTEMS
©1978
REV B
PARALLEL I/O
SERIAL I/O
BANK SELECT
ROM SELECT
NOTES
1. APPLY THERMAL COMPOUND P.N. 120-8 TO VR1
2. DEGREASE BOARD.
3. ASSEMBLE ALL OTHER PARTS PER PARTS LIST.