Decision 1 Alteration Guide for the Oasis Operating System

Preliminary Edition
Rev. Ø - 4/82

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MODIFICATIONS

The Oasis operating system requires that the first 16K of user memory be global, that is, shared by all the users. For this reason, a non-extended address board (i.e., Morrow Designs Super-ram 16) is is addressed at XXØØØØh - XX3FFFh, where the operating system will reside. This memory will be common to all tasks running. In addition to this memory, each user will have 48K of memory at his disposal. In order to minimize the changes to Oasis, the MPZ8Ø will control the upper four address lines (A2Ø - A23) to simulate a bank select type of system with the extended addressing. This requires that the user memory be extended address memory (a Morrow Designs MM65KS16 static memory de-populated to 48K or with two 16K banks overlapping each other). The operating system allows only 16 users and the memory must be addressed to take into account the switching of the upper four address lines when users swap in and out. This would mean the users' memory maps would be as follows:

User Memory Maps

User	Extended Memory Address
Ø	ØØ4ØØØ - ØØFFFFH
1	1Ø4ØØØ - 1ØFFFFH
2	2Ø4ØØØ - 2ØFFFFH
3	3Ø4ØØØ - 3ØFFFFH
4	4Ø4ØØØ - 4ØFFFFH
5	5Ø4ØØØ - 5ØFFFFH
6	6Ø4ØØØ - 6ØFFFFH
7	7Ø4ØØØ - 7ØFFFFH
8	8Ø4ØØØ - 8ØFFFFH
9	9Ø4ØØØ - 9ØFFFFH
1Ø	AØ4ØØØ - AØFFFFH
11	BØ4ØØØ - BØFFFFH
12	CØ4ØØØ - CØFFFFH
13	DØ4ØØØ - DØFFFFH
14	EØ4ØØØ - EØFFFFH
15	FØ4ØØØ - FØFFFFH

Global Memory

The global memory part of the system may be composed of any board which does not respond to extended address. This can be any of the following Morrow Design products:

16K Superram
16K Memory Master
24K Memory Master
32K Superram
MM65KS16Memory Board (setup for bank select)

Switch settings for 16K Superram:

Far Left Switch

Paddle	State
1	ON
2	ON
3	ON
4	ON
5	ON
6	ON
7	ON
8	OFF

Middle Switch

Paddle	State
1	ON
2	ON
3	OFF
4	ON
5	ON
6	ON
7	OFF
8	OFF

Right Switch

Paddle	State
1	ON
2	ON
3	ON
4	ON
5	ON
6	ON
7	ON
8	ON

Switch settings for 16K Memory Master:

Switch 6A

Paddle	State
1	ON
2	ON
3	ON
4	ON
5	ON
6	ON
7	ON
8	ON

Switch 7A

Paddle	State
1	OFF
2	OFF
3	OFF
4	OFF
5	OFF
6	OFF
7	OFF
8	ON

Switch 8A

Paddle	State
1	OFF
2	OFF
3	ON
4	OFF
5	OFF
6	OFF
7	ON
8	ON

Switch 8D

Paddle	State
1	ON
2	ON
3	ON
4	ON
5	ON
6	ON
7	ON
8	OFF

Switch 7E

Paddle	State
1	ON
2	ON
3	ON
4	ON
5	ON
6	ON
7	ON
8	ON

Switch 7F

Paddle	State
1	ON
2	ON
3	ON
4	ON
5	ON
6	ON
7	ON
8	ON

Extended Address Memory
(MM65KS16 Addressing/Jumpering)

The following procedures set up the MM65KS16 memory board for the Oasis operating system.

I. Depopulate board to 48K. Remove RAM chips at board locations:

1A, 2A, 3A, 4A, 1B, 2B, 1C, 2C

The board now has 48K of RAM.

II. Addressing the board:

The following are the switch settings for MM65KS16 for a multi-user Oasis system:

MM65KS16 USER Ø

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	ON	OFF
6	ON	ON
7	ON	OFF
8	ON	OFF

MM65KS16 USER 1

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	OFF	OFF
6	ON	ON
7	ON	OFF
8	ON	OFF

MM65KS16 USER 2

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	ON	OFF
6	OFF	ON
7	ON	OFF
8	ON	OFF

MM65KS16 USER 3

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	OFF	OFF
6	OFF	ON
7	ON	OFF
8	ON	OFF

MM65KS16 USER 4

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	ON	OFF
6	ON	ON
7	OFF	OFF
8	ON	OFF

MM65KS16 USER 5

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	OFF	OFF
6	ON	ON
7	OFF	OFF
8	ON	OFF

MM65KS16 USER 6

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	ON	OFF
6	OFF	ON
7	OFF	OFF
8	ON	OFF

MM65KS16 USER 7

Paddle	S1	S2
1	ON	ON
2	ON	OFF
3	ON	ON
4	ON	OFF
5	OFF	OFF
6	OFF	ON
7	OFF	OFF
8	ON	OFF

Note the progression of the extended address switch: S1 paddles 5 through 8 form a binary progression. By incrementing these four bits, you will increment the upper four bits of the extended address to which the memory will respond and thus increment users.

The memory board should be set as extended address (not bank select) meaning a 25LS2521 should be installed in location 1D and no chip should be installed in location 2D.

MM65KS16 Jumpers

J1	-	In
J2	-	In
J3	-	Out
J4	-	In
J5	-	Out
J6	-	In
J7	-	Out

No jumpers in area 17D (bank select jumpers).

MPZ8Ø Hardware Modifications

Normally the Decision 1 is designed to trap on a 'Halt' instruction (system calls from UNIX) but the Oasis operating system will trap on a 'RST 6' instruction instead. At present, this requires a hardware modification to the MPZ8Ø board. The modification requires four jumpers and is performed as follows:

1. Lift pins 9 and 1Ø of IC 8D.
2. Connect pin 9 of chip 8D to pin 1 of chip 6D.
3. Connect pin 1Ø of chip 8D to pin 13 of chip 6D.
4. Connect pin 9 on the socket of 8D to pins 2 and 3 of chip 6D.
5. Connect pin 1Ø on the socket of 8D to pins 11 and 12 of chip 6D.

MPZ8Ø Firmware Modifications

The firmware on the MPZ8Ø CPU board has also been changed to accommodate this hardware change and the operating system. Whenever a 'RST 6' instruction is executed in the first 4K of memory of any task, it is assumed to be an Oasis system call. The EPROM code on the MPZ8Ø will then latch the contents of the upper 4 bits of the 'A' register onto the S-1ØØ address line A19 - A23. The lower 4 bits of the 'A' register are masked off. Operation then resumes at the instruction immediately following the 'RST 6' instruction with all registers preserved.

If a 'RST 6' is executed above the first 4K by any user, it is assumed to be a user wishing to use a 'RST6' instruction and the program will continue execution at location 3Ø in the global memory as though it were actually executing the 'RST 6'. It is in fact interpreting this instruction for the user. Users are warned that the memory location of all the Restart vectors is common to all users and should use care when using these areas.

The switches on the MPZ8Ø are the same as for the standard EPROM:

Switches 1 - 5 control the power on jump address. Normally these switches are all off to boot up a DJ 2D/B at F8ØØh. If these switches are all on, the Morrow Designs BOOTHD program is executed to boot up a HDCA hard sectored hard disk. If all switches are on except for 5, the HDC/DMA boot routine is executed.

When ON, switch 6 causes the monitor to be invoked, OFF allows power on jump to the address determined by S1 - S5. See MPZ8Ø manual for details on the monitor commands.

Switch 7 is unused.

Switch 8 must always be on in systems requiring MWRITE (with DJ 2D/B for instance).

Mult I/O **Switches and Jumpers**
(Revision 3 and 4)

Mult I/O Switches

Switch 2D
(Address ØFØØØØh)

Paddle	State
1	ON
2	ON
3	ON
4	ON
5	OFF
6	OFF
7	OFF
8	OFF

Switch 7B

Paddle	State
1	ON
2	ON
3	OFF
4	ON
5	ON
6	OFF
7	OFF
8	OFF

Switch 10B

Paddle	State
1	OFF
2	ON
3	ON
4	ON
5	ON
6	ON
7	OFF
8	OFF

Mult I/O Jumpers

Jumper	Location	State
J1	1A	A to H
	1A	B to I
J2	5A	A to H
	5A	B to I
J3	8A	A to H
	8A	B to I
J4	11C	B to C
J5	3D	B to PINT
J6	7A	Installed (Rev. 4 only)
P5	11A	Not installed
P6	14D	Clock battery back-up

WB I/O Switches and Jumpers

Switch 7C

Paddle	State
1	ON
2	ON
3	OFF
4	ON
5	ON
6	OFF
7	OFF
8	OFF

Switch 10A (9600 Baud)

Paddle	State
1	ON
2	OFF
3	ON
4	OFF
5	OFF
6	OFF
7	OFF
8	OFF

Jumper	Location	State
J1	8A	not installed
J2	8C	Jumper A to B
J3	8C	Installed
J4	2C	No jumpers
J5	13A	Battery back-up for clock
J6	8E	Reset switch input

DJ 2D/B Floppy Controller Settings

Switch 5D

Paddle	State
1	OFF
2	OFF
3	OFF
4	OFF
5	OFF
6	OFF
7	OFF
8	OFF

Switch 13C
(9600 Baud)

Paddle	State
1	OFF
2	OFF
3	OFF
4	ON
5	OFF
6	OFF
7	OFF
8	OFF

DJ 2D/B Jumpers

Jumper	Location	State
J1A	3D	Not installed
J2	4D	Installed
J3A	11C	J3A to Data Ø
J4	4A	A to B

HDCA Winchester Controller Jumpers and Settings
(Revisions 3 and 4)

Switch 8C
(Port 50 - 53h)

Paddle	State
1	OFF
2	OFF
3	ON
4	OFF
5	ON
6	ON
7	ON
8	ON

HDCA Jumpers

Jumper	Location	State
J1	6C	Not installed
J2	6C	Not installed
A	ØC	Not installed
B	ØC	Not installed

Oasis EPROM Installation

Parts list:

(1) Decision 1 CPU, MPZ80 rev 2

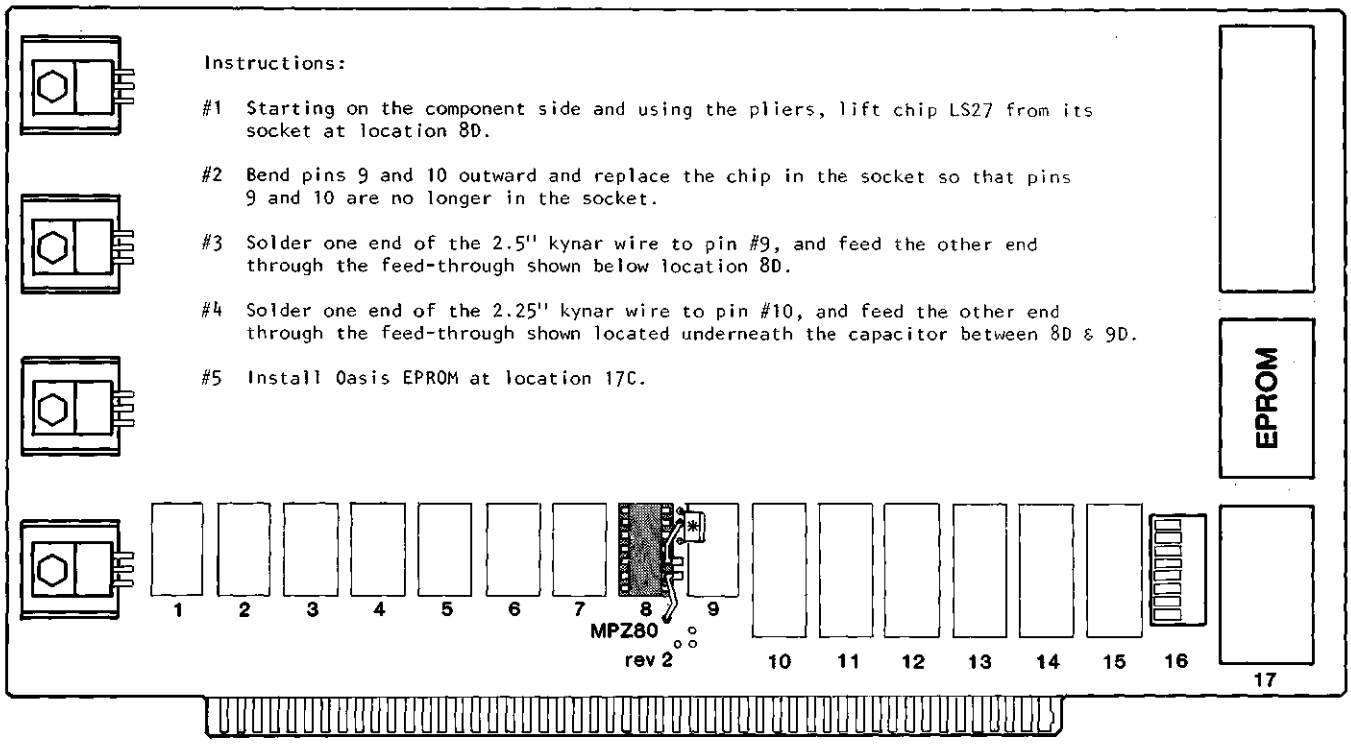
(1) Oasis EPROM (to be located at 17C)

(4) pieces of 30 gauge insulated (Kynar) wire: 2.5", 2.25", 2" & 1.5"

(1) 6" length of solder (60/40 recommended)

(1) solder iron

(1) pair of pliers



Instructions:

#1 Starting on the component side and using the pliers, lift chip LS27 from its socket at location 8D.

#2 Bend pins 9 and 10 outward and replace the chip in the socket so that pins 9 and 10 are no longer in the socket.

#3 Solder one end of the 2.5" kynar wire to pin #9, and feed the other end through the feed-through shown below location 8D.

#4 Solder one end of the 2.25" kynar wire to pin #10, and feed the other end through the feed-through shown located underneath the capacitor between 8D & 9D.

#5 Install Oasis EPROM at location 17C.

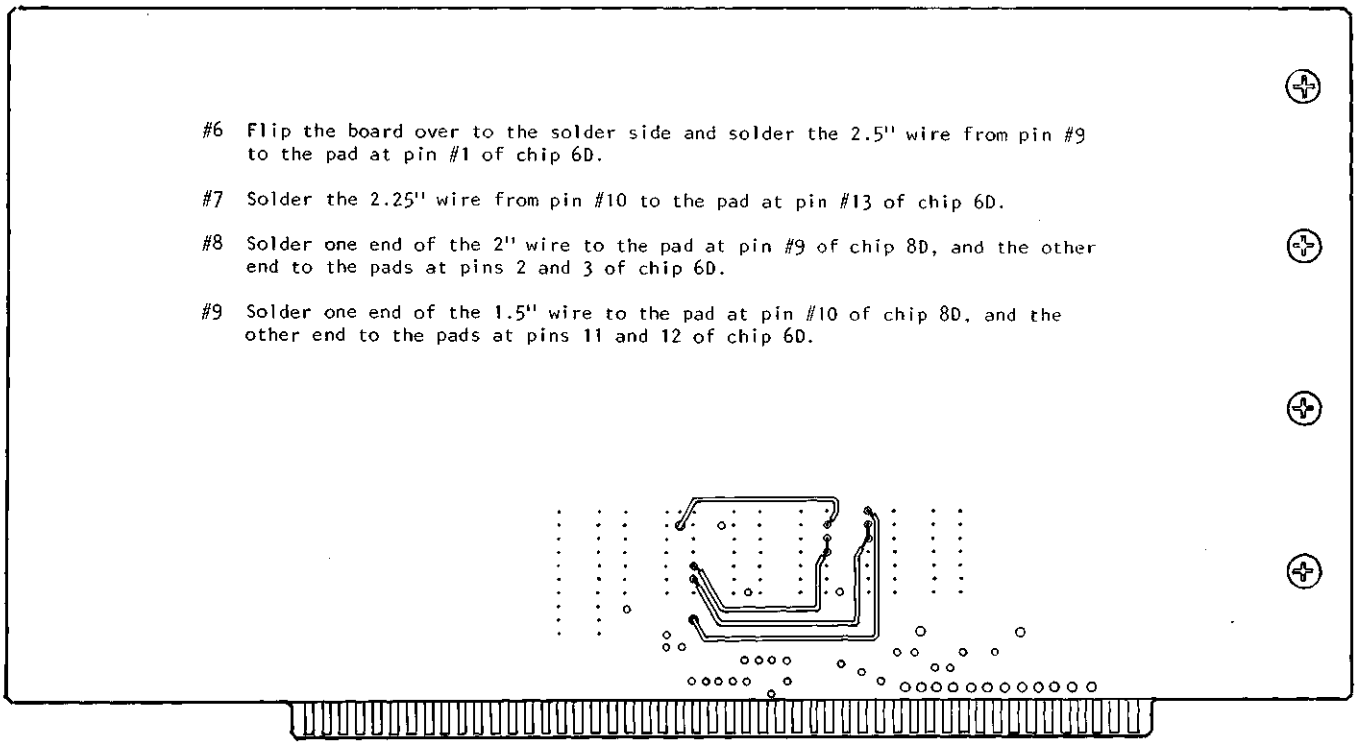
#1 Component Side

#6 Flip the board over to the solder side and solder the 2.5" wire from pin #9 to the pad at pin #1 of chip 6D.

#7 Solder the 2.25" wire from pin #10 to the pad at pin #13 of chip 6D.

#8 Solder one end of the 2" wire to the pad at pin #9 of chip 8D, and the other end to the pads at pins 2 and 3 of chip 6D.

#9 Solder one end of the 1.5" wire to the pad at pin #10 of chip 8D, and the other end to the pads at pins 11 and 12 of chip 6D.



#2 Solder Side