User's Manual

Econoram III*

SYNCHROFRESH VIII™

S-100 Buss Compatible

8K Random Access Memory

Thinker Toys™ 1201 10th. Berkeley, Calif. 94710

Synchrofresh™ VIII Memory Systems

INTRODUCTION

Dynamic memory has two very attractive features: It is less expensive to manufacture than static and it consumes significantly less power. Both of these attributes stem from the extremely simple cell design of a dynamic device. Typical static memory cells require four transistors as opposed to one for the dynamic part. This simplicity of design results in much smaller devices. And, small devices require less power. They also result in higher yields which mean a lower cost per bit.

There are, however, certain penalities which accrue from low cost and low power consumption: dynamic memorys require periodic refreshing. Thus a memory product which uses dynamic devices must include extra control logic to produce the required refresh cycles. This usually results in complicated designs with more parts and, therefore, more power and reduced reliability.

Until now, most of the memory designers in the small computer market have stayed with static devices for design simplicity. Those who attempted to use dynamic parts have been plagued with troublesome units (most notable MITS of Altair fame) or have had extremely complicated circuit boards. One unit has over thirty-five control circuits plus a delay line, and another is made with a five layer board to accomodate all the needed signal traces.

What has been missing from past designs is a scheme to make the refresh control logic both simple and reliable. Synchrofresh™ is just that. Synchrofresh stands for synchronized refresh -- a refresh scheme which derives its timing directly from the S-100 buss just as static memory boards do. This eliminates the possibility of a conflict. Both memory access and refresh timing are woven into the same clock signals which eminate from the CPU. The natural timing from the buss insures a reliable memory refresh. But these same buss signals also simplify the control logic necessary to perform this refresh. The result is a memory which behaves just as if it were static but with two big differences: the cost is lower ($100 cheaper than some 8K static boards) and the power consumption is drastically cut (typically by a third).

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OPERATION

GENERAL

The Synchrofresh 8K memory unit is an S-100 compatible product. It contains two completely independent 4K blocks. Each of these two 4K blocks may be placed on any 4K address boundary -- the addressing details are presented below.

The physical design allows stacking on 3/4" centers (this is the spacing used in most of the S-100 buss boards such as the 20-slot WunderBuss). A hardwired write enable switch is included on the board to provide a foolproof method of protecting data stored in the memory.

In the paragraphs which follow, reference will be made to positions of different parts on the circuit board. In all cases, the orientation of the circuit board is that the gold fingered edge connector is at the bottom of the board. This places the voltage regulators on the left side of the board while the memory array is toward the right and to the top.

MAINTENANCE

Assembled Synchrofresh memories carry a one year warranty against defects. The only required maintenance is to run the memory test included with this manual or a reasonable substitute if you suspect that the unit is not functioning properly. If the memory should fail to operate properly and has not been damaged or subjected to abuse (as determined by us), it will be repaired or replaced at no charge during the warranty period.

WRITE PROTECTION

At the top of the circuit board just above position 2A, there is a three-position slide switch. The left and middle positions are both write enable states while the right position is the write protect state.

When the board is to be used as read/write memory, the slide switch should be to the left or in the center. In these positions, the CPU can write into or read from either 4K memory block.

When the unit is to be used as "read only" memory, the slide switch should be in the right most position. In this position, write commands issued to the memory by the CPU or DMA devices are ignored.

The write protect mode is especially useful when it is necessary to prevent a program or data from being accidently destroyed by another program or from the front panel.

ADDRESSING

The 8,192 byte memory array on the Synchrofresh board is divided into two 4,096 byte sections. The addressing of these two sections is controlled by an eight position dip switch located at position 1F toward the bottom and to the left of the board.

The left four switches (1 through 4) are dedicated to one 4K block while the right four switches (5 through 8) control the other 4K block.

Block Ø occupies positions 4C (bit Ø), 5C (bit 1), 6C (bit 2), 7C (bit 3), 4B (bit 4), 5B (bit 5), 6B (bit 6), and 7B (bit 7).

Block 1 occupies positions 4D (bit Ø), 5D (bit 1), 6D (bit 2), 7D (bit 3), 4A (bit 4), 5A (bit 6), 6A (bit 6), and 7A (bit 7).

4K address boundaries have a hexidecimal expression of the form XØØØ where X is some hexidecimal digit between Ø and F. Thus, one four bit hexidecimal digit is sufficient to determine the addressing of a 4K block of memory which resides between 4K address boundaries. Since each switch position corresponds to a bit position within a hex digit, you can see how an eight position dip switch can control the addressing of two 4K blocks of memory.

The relative positions of the switches correspond to the relative bit positions within a hex digit. That is, the left most switch of each group of four (switch #1 or #5) has the highest numeric weight while the right most switch of each group (switch #4 or #8) has the lowest numerical weight. A switch in the "on" position or to the top signifies a zero bit while a one bit is obtained by pulling the switch down.

Consider a practical example in the use of the address selecting dip switch. The two 4K blocks are designated block Ø and block 1. The left four switches control block Ø and the right four switches control block 1. Suppose block Ø is to be located at $(AØØØ)_{16}$ and block 1 at $(7ØØØ)_{16}$. The left four switches must then express 1010 which is the binary for the hex digit A while the right four switches must show 0111 which the binary equivalent of 7. Since an "on" or "up" position corresponds to a Ø while an "off" or "down" position corresponds to a 1, the switches should be arranged as follows:

SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8
off	on	off	on	on	off	off	off
down	up	down	up	up	down	down	down
1	0	1	0	0	1	1	1
		A				7	

Below is a table of possible starting addresses along with switch pattern corresponding to these addresses.

			Switch No.			
Block A			1	2	3	4
Block B			5	6	7	8
Starting Address:						
Hex	Octal					
0000	000:000		on	on	on	on
1000	020:000		on	on	on	off
2000	040:000		on	on	off	on
3000	060:000		on	on	off	off
4000	100:000		on	off	on	on
5000	120:000		on	off	on	off
6000	140:000		on	off	off	on
7000	160:000		on	off	off	off
8000	200:000		off	on	on	on
9000	220:000		off	on	on	off
A000	240:000		off	on	off	on
B000	260:000		off	on	off	off
C000	300:000		off	off	on	on
D000	320:000		off	off	on	off
E000	340:000		off	off	off	on
F000	360:000		off	off	off	off

THEORY OF OPERATION

GENERAL

Synchrofresh was designed with two primary objectives -- that it be reliable and foolproof. Ideally, dynamic memory should be reliable, low in cost, and with power consumption well below comparable static memory units. The user should be able to purchase dynamic memory with the same confidence he has shown in the static.

The objectives of low cost and low power consumption have been met in Synchrofresh. Although extensive tests have been performed, true reliability cannot be measured until the memories have been used in varying applications in the field over a length of time. Unquestionably, the design innovation of this memory is a break through. It dispenses with the usual complicated timing mechanisms -- the one shots and crystal oscillator have been eliminated and replaced with simple timing derived from the ϕ_2 and PSYNC signals on the S-100 buss.

DATA BUFFERS

A peculiarity of the 2107B type part is that the input and output data have the opposite polarity. The input data to the array from the S-100 buss is buffered by two 74LSØ4/14 inverters at positions 3B and 3C to accomodate the polarity problem. The output data from the memory array to the S-100 buss is latched and buffered by a 74LS373/S373. This is one of the newer twenty-pin octal parts being introduced by Texas Instruments and other vendors. This part is both a transparent latch and a tri-state* buffer. Moreover, it is a full eight bits wide making it a very desirable part for microprocessor applications.

The input buffers are active at all times while the output buffer is active only when the board has been selected and the data input strobe PDBIN is active.

ADDRESS BUFFERS/MULTIPLEXORS

Addresses to the memory from the S-100 buss and the refresh address counter are buffered and selected through three 74LS157/158/257/258 quad two-input multiplexors. The control input to the multiplexors comes from a D- flip-flop at 3A which switches data and refresh addresses to the array at the proper times. A careful examination of the timing of this flip-flop will reveal that addresses are switched in the middle of a memory cycle. This would be unacceptable were we using static RAMs. The situation with dynamic RAMs is somewhat different. The address inputs of a dynamic RAM chip are not only buffered but also latched. This latching occurs with the rising edge of CENBL, the signal which initiates a cycle for the memory chip. The main concern with the address signals to the 2107B is that they are stable at the rising edge of CENBL and remain so for approximately 150 ns. In the present case, the MUX CNTL signal does

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not change for 250 ns after the rising edge of CENBL, giving a margin of 100 ns.

REFRESH ADDRESS COUNTER

The refresh address for the array are generated by the 74393 at 3E which is a dual hex counter. This counter advances at the falling edge of its clock inputs (pins 1 and 13). The signal REFRESH drives the primary clock input at pin 1. This signal is high during memory refresh cycles. Thus, the refresh addresses change upon termination of a refresh cycle and are stable throughout memory refreshes. This is a desirable state of affairs in view of the preceeding discussion concerning address signal stability requirements for the 2107B.

ADDRESS SELECTION LOGIC

Block starting addresses are determined using four of the DIP switches and a 74LS266. This device is a quad 2 input comparator with open collector outputs. This is an example of an extremely efficient use of open collector logic. The standard methods for selecting addresses are with a 4 or 6 bit comparator or using a pair of 1 of 4 decoders in series. The former uses parts costing from four to eight times that of the 74LS266 and the latter uses twice as many switches and a part which costs twice as much as the 74LS266.

During the late sixties and early seventies, logic designers used far too much open collector logic. The cause of this was their inability to avoid habits acquired when designing with DTL (diode-transistor logic). One of the characteristics of DTL is that all the outputs have either an open collector or a collector with an internal pull-up resistor. Either structure facilitates the use of so called "wired OR" logic. This is exactly the way the outputs of the 74LS266 are connected (see page 1 of the schmatics). The only way the connected outputs can be high is when each pair of inputs is individually at the same logic state, ie, the switch positions correspond one for one with the address A15, A14, A13, and A12.

The major disadvantage of open collector logic is that the transition time from the logic zero state to the logic one state is slow (the resistor has to do the work charging a collector which looks like a capacitor when the device is off). In our case, the slow rise times are of no consequence since the 8080A puts its addresses on the buss very early. TTL and more recently tri-state LS TTL have replaced most of the old DTL open collector designs. However, keep in mind that though the active outputs of TTL are usually superior, the older open collector structures still have their uses.

THEORY OF OPERATION

BOARD SELECTION LOGIC

The 74LSØ2 at position 3D performs most of the board selection logic using the outputs of the two 74LS266 along with the buss signals SINTA, SINP, and SOUT. If SOUT is zero and SINP is zero and SINTA is zero and ENBL A or ENBL B is true, the board is selected at the rising edge of ϕ_2 when PSYNC is active. As a practical matter, this is the earliest time when all the status signals and address signals are stable. The rising edge of ϕ_2 during the active state of PSYNC also starts a memory access cycle assuming that the board selection logic permits it.

CHIP ENABLE CIRCUITRY

The chip enable input pin of the 2107B memory chip is the only pin that is not TTL compatible. This input must swing between zero and twelve volts. Moreover, these swings in voltage cannot take more than 40 ns. This is the signal which initiates a memory cycle for the 2107B and the rising edge of this signal activates the data buffers, the many internal sense amplifiers and the address buffers and latches. This activation period is the major source of noise on the various voltage lines since so much circuitry within the memory chips abruptly begins to use power and current. The large number of ceramic and tantalum capacitors in and around the memory array is used to absorb this noise and insure adequate signal-to-noise ratios. Transistors Q_1 and Q_2 are driven with a classical "boot strap" circuit. While the transistors are off, capacitors C75 and C76 are charged through the diode resistor pairs CR3, R4 and CR5, R6 to approximately 11 volts.

When the 7406s turn off, C75 begins discharging through R4 and R5 and the base of Q_1. But the emitter of Q_1 cannot be more than .7 volts less than the base. Thus, the emitter begins to rise. But, as the emitter rises, so does the emitter side of C75. And, since the voltage across C75 cannot change instantaneously, the R4 side of C75 is forced to rise above 11 volts. In fact, for a short period of time, the voltage difference across C75 will remain approximately 11 volts. The fact that the voltage across a capacitor cannot change instantaneously causes the emitters of Q_1 and Q_2 to snap up to within 11.6 volts very rapidly. Typically, in 25 ns. When the 7406s turn on again, the bases of Q_1 and Q_2 are pulled down by one pair of 7406s to turn the transistors off while the other pair of 7406s insure that the emitters are pulled below .4 volts.

This circuit is very fast with almost no over shoot at either 12 volts or ground.

TIMING AND CONTROL LOGIC

The heart of the timing and control circuitry is the 74LS161 hex counter. This counter goes through two types of cycles depending on the length of the buss memory cycle and implements a so called "finite state" machine. During buss memory cycles consisting of T_1, T_2, and T_3 states, the counter counts from zero to two synchronous with PSYNC. During buss memory cycles which have four or more T states between one PSYNC and another, the counter counts from zero to three and back to zero again. This counter directs all the other control circuitry on the board. Each state of the counter consists of two phases: when $\phi 2$ is a logic zero (which we label phase A) and when $\phi 2$ is a logic one (which we call phase B). The counter advances on the falling edge of $\phi 2$. To better understand the control circuitry, we shall discuss what happens with the memory at each phase of each state of the counter. For simplicity, we will assume that the zero state is simultaneous with PSYNC.

1. Zero - Phase A
   Memory chip precharge time (CE low). The address multiplexors are switched to the S-100 address buss lines and away from the refresh counter addresses. Chip select lines conditionally enabled.

2. Zero - Phase B
   Memory cycle is started and data latch is enabled.

3. One - Phase A
   Memory cycle continues; latch is still enabled.

4. One - Phase B
   Address multiplexors are switched from S-100 address buss to refresh counter outputs and chip select lines disabled.

5. Two - Phase A
   Memory cycle terminated; data latch disabled.

6. Two - Phase B
   Memory chip precharge time (CE low).

7. Three - Phase A
   Refresh cycle started.

8. Three - Phase B
   Refresh cycle continues.

MEMORY DIAGNOSTIC

The memory test described below was designed by Phil Meads of William Brobeck Associates to exercise the most sensitive circuitry of 22 pin NMOS 4k dynamic memory chips: the address buffers and latches. The test starts from the middle and works its way outward alternately to the top and bottom of memory. This type of test inverts the address lines more often than sequential ones. This continual inversion process punishes and eventually breaks down weak or faulty address buffers in the device.

USING THE TEST

The test itself must be placed in an area which is different than the location of the board(s) to be tested. The test starts on a page boundary to make the task of relocating the binary code easier.

There are two parameters in the test to be set by the user:

(1) The number of 4k blocks to be tested -- keep in mind that there are two 4k blocks per board. This constant is called BLKCNT and is located at the eleventh byte of the test.

(2) The starting page number of the lowest 4k block to be tested is called PAGENO and is located at the ninth byte of the test.

When testing more than one 4k block of memory, be sure that they occupy contiguous memory.

The page number of the position of the test itself must be entered wherever a $(YYY)_8$ or $(YY)_{16}$ occurs in the test listing. This is necessary because JMP and CALL need both the page number and the location within the page to execute correctly.

The only other thing to remember when loading the test is that it must be placed at the starting address of a page.

Start the test at the first instruction. Once started, the test will run continuously unless an error is detected. If the test encounters an error, all the data pertinent to this error is stored in the last ten locations of the test. After storing this data, the test comes to a dynamic halt at the label STALL. The test may be restarted by stopping the computer and restarting it at the POP PSW instruction following JMP STALL. The user may also restart the test from the beginning. If errors indicate the board is malfunctioning, return it as soon as possible for warranty service.

For $4.95 a cassette tape of both the source and binary of the memory test recorded in the Kansas City Standard 300 baud format is available. It auto loads into the RAM of the Speakeasy I/O board which is also available from Thinker Toys.

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Octal)

```
YYY 000 061 175 YYY     START   LXI     SP,STACK    INITIALIZE STACK POINTER
    003 001 000 000             LXI     B,0         INITIALIZE CYCLE COUNT
    006 305             NEWCYL  PUSH    B           UPDATE CYCLE COUNT
    007 006 100                 MVI     B,PAGENO    STARTING ADDR OF TEST MEM
    011 016 002                 MVI     C,BLKCNT    NO. OF 4K BLOCKS TO TEST
    013 041 377 007     LOOP    LXI     H,7:377Q    HALF SIZE OF MEMORY -1
    016 170                     MOV     A,B
    017 204                     ADD     H           CALCULATE MIDDLE
    020 147                     MOV     H,A           OF CURRENT BLOCK
    021 345                     PUSH    H           SAVE INITIAL ADDRESS
    022 315 114 YYY     WRITE   CALL    TWORD       GET TEST WORD
    025 167                     MOV     M,A         STORE
    026 315 123 YYY             CALL    COMP        COMPLIMENT ADDRESS
    031 315 114 YYY             CALL    TWORD       GET TEST WORD
    034 167                     MOV     M,A         STORE
    035 315 134 YYY             CALL    INCR        COMPLEMENT AND DECREMENT
    040 302 022 YYY             JNZ     WRITE         ADDRESS
    043 341                     POP     H           RECOVER INITIAL ADDRESS

YYY 044 315 114 YYY     READ    CALL    TWORD       GET TEST WORD
    047 256                     XRA     M           COMPARE
    050 304 145 YYY             CNZ     ERROR
    053 315 123 YYY             CALL    COMP        COMPLEMENT ADDRESS
    056 315 114 YYY             CALL    TWORD       GET TEST WORD
    061 256                     XRA     M           COMPARE
    062 304 145 YYY             CNZ     ERROR
    065 315 134 YYY             CALL    INCR        COMPLIMENT AND DEC
    070 302 044 YYY             JNZ     READ          ADDRESS
YYY 073 076 020                 MVI     A,20Q       ADVANCE
    075 200                     ADD     B             THE
    076 107                     MOV     B,A           BLOCK
    077 015                     DCR     C           DECREMENT BLOCK COUNT
    100 302 013 YYY             JNZ     LOOP
    103 173                     MOV     A,E         CALCULATE NEW
    104 306 207                 ADI     135           BASE FOR
    106 137                     MOV     E,A           TEST WORD
    107 301                     POP     B
    110 003                     INX     B           INCREMENT CYCLE COUNT
    111 303 006 YYY             JMP     NEWCYL

    114 175             TWORD   MOV     A,L         GET LOWER BYTE OF ADDRESS
    115 007                     RLC                 ROTATE
    116 207                     ADD     A           SHIFT
    117 204                     ADD     H           ADD HIGHER BYTE OF ADDR
    120 203                     ADD     E           ADD BASE
    121 127                     MOV     D,A         SAVE TEST WORD
    122 311                     RET
```

```
YYY 123 174             COMP    MOV     A,H     COMPLIMENT THE UPPER
    124 356 017                 XRI     17Q       BYTE ADDRESS
    126 147                     MOV     H,A       WITH RESPECT TO MEM SIZE
    127 175                     MOV     A,L     COMPLIMENT THE LOWER
    130 356 377                 XRI     377Q      BYTE OF THE
    132 157                     MOV     L,A       ADDRESS
    133 311                     RET

YYY 134 315 123 YYY     INCR    CALL    COMP    RESTORE ADDRESS TO NORMAL STATE
    137 053                     DCX     H       DECREMENT
    140 300                     RNZ             TEST IF LOWER BYTE ZERO
    141 170                     MOV     A,B     TEST UPPER BYTE EQUAL
    142 075                     DCR     A         TO BLOCK
    143 274                     CMP     H         BOUNDARY
    144 311                     RET

YYY 145 345             ERROR   PUSH    H       SAVE ERROR ADDRESS
    146 305                     PUSH    B       SAVE CURRENT BLOCK
    147 325                     PUSH    D       SAVE TEST WORD
    150 365                     PUSH    PSW     SAVE ERROR BITS
    151 303 151 YYY     STALL   JMP     STALL   DYNAMIC HALT
    154 361                     POP     PSW     RESTORE
    155 321                     POP     D         THE
    156 301                     POP     B         STATE OF
    157 341                     POP     H         THE CPU
    160 311                     RET

YYY 161 000             TABLE   DB      0       FLAGS
    162 000                     DB      0       ACC - 1S ARE ERROR BITS
    163 000                     DB      0       E - CURRENT RANDOM OFFSET
    164 000                     DB      0       D - CURRENT TEST WORD
    165 000                     DB      0       C - CURRENT BLOCK COUNT
    166 000                     DB      0       B - CURRENT BLOCK PAGE
    167 000 000                 DW      0       HL - ERROR ADDRESS
    171 000 000                 DW      0       RETURN ADDRESS
    173 000 000                 DW      0       CYCLE COUNT
    175 000 000         STACK   DW      0
```

MEMORY TEST PROGRAM FOR 4K NMOS RAMS
(Hex)

```
YY 00   31 7D YY     START    LXI     SP,STACK
   03   01 00 00              LXI     B,0
   06   C5           NEWCYL   PUSH    B
   07   06 40                 MVI     B,PAGENO
   09   0E 02                 MVI     C,BLKCNT
   0B   21 FF 07     LOOP     LXI     H,7:377Q
   0E   78                    MOV     A,B
   0F   84                    ADD     H
   10   67                    MOV     H,A
   11   E5                    PUSH    H
   12   CD 4C YY     WRITE    CALL    TWORD
   15   77                    MOV     M,A
   16   CD 53 YY              CALL    COMP
   19   CD 4C YY              CALL    TWORD
   1C   77                    MOV     M,A
   1D   CD 5C YY              CALL    INCR
   20   C2 12 YY              JNZ     WRITE
   23   E1                    POP     H

YY 24   CD 4C YY     READ     CALL    TWORD
   27   AE                    XRA     M
   28   C4 65 YY              CNZ     ERROR
   2B   CD 53 YY              CALL    COMP
   2E   CD 4C YY              CALL    TWORD
   31   AE                    XRA     M
   32   C4 65 YY              CNZ     ERROR
   35   CD 5C YY              CALL    INCR
   38   C2 24 YY              JNZ     READ

YY 3B   3E 10                 MVI     A,20Q
   3D   80                    ADD     B
   3E   47                    MOV     B,A
   3F   0D                    DCR     C
   40   C2 0B YY              JNZ     LOOP
   43   7B                    MOV     A,E
   44   C6 87                 ADI     135
   46   5F                    MOV     E,A
   47   C1                    POP     B
   48   03                    INX     B
   49   C3 06 YY              JMP     NEWCYL

YY 4C   7D           TWORD    MOV     A,L
   4D   07                    RLC
   4E   87                    ADD     A
   4F   84                    ADD     H
   50   83                    ADD     E
   51   57                    MOV     D,A
   52   C9                    RET
```

```
YY 53  7C          COMP    MOV     A,H
   54  EE 0F               XRI     17Q
   56  67                  MOV     H,A
   57  7D                  MOV     A,L
   58  EE FF               XRI     377Q
   5A  6F                  MOV     L,A
   5B  C9                  RET

YY 5C  CD 53 YY    INCR    CALL    COMP
   5F  2B                  DCX     H
   60  C0                  RNZ
   61  78                  MOV     A,B
   62  3D                  DCR     A
   63  BC                  CMP     H
   64  C9                  RET

YY 65  E5          ERROR   PUSH    H
   66  C5                  PUSH    B
   67  D5                  PUSH    D
   68  F5                  PUSH    PSW
   69  C3 69 YY    STALL   JMP     STALL
   6C  F1                  POP     PSW
   6D  D1                  POP     D
   6E  C1                  POP     B
   6F  E1                  POP     H
   70  C9                  RET

YY 71  00          TABLE   DB      0       FLAGS
   72  00                  DB      0       ACC - 1S ARE ERROR BITS
   73  00                  DB      0       E - CURRENT RANDOM OFFSET
   74  00                  DB      0       D - CURRENT TEST WORD
   75  00                  DB      0       C - BLOCKS LEFT TO TEST
   76  00                  DB      0       B - CURRENT BLOCK PAGE
   77  00 00               DW      0       HL - ERROR ADDRESS
   79  00 00               DW      0       RETURN ADDRESS
   7B  00 00               DW      0       CYCLE COUNT
   7D  00 00      STACK    DW      0
```

KIT PARTS LIST

_____	1	8" x 10" glossy photograph of assembled board	
_____	1	5" x 10" circuit board with solder mask	
_____	2	.027 µfd capacitors	
_____	46	.01 - .1 µfd disk capacitors*	
_____	24	2.7 µfd tantalum capacitors	
_____	14	39 µfd tantalum capacitors	
_____	2	2N3904 transistors	
_____	4	1N914/4820-0201 signal diodes	
_____	1	1N751/1N5231 5-volt zener diode	
_____	1	7805/LM340-5 +5-volt regulator	
_____	1	78M12/7812/LM340-12 +12-volt regulator	
_____	14	14-pin low profile sockets	
_____	4	16-pin low profile sockets	
_____	1	20-pin low profile socket	
_____	16	22-pin low profile sockets	
_____	1	double-pole single throw PC mount slide switch	
_____	1	8 position DIP switch	
_____	1	750Ω ½ watt resistor	purple-green-brown
_____	2	200Ω ¼ watt resistors	red-black-brown
_____	4	510Ω ¼ watt resistors	green-brown-brown
_____	2	910Ω ¼ watt resistors	white-brown-brown
_____	9	3.3kΩ ¼ watt resistors	orange-orange-red
_____	1	74LS00 quad 2 input NAND gate	
_____	1	74LS02 quad 2 input NOR gate	

*by-pass capacitors - value will vary from .01 µfd to .1 µfd depending on current supply.

_____	1	7406 hex inverter/buffer
_____	2	74LS08 quad 2 input AND gate
_____	1	74LS10 triple 3 input NAND gate
_____	3	74LS14/74LS04 hex inverter/Schmidt trigger
_____	2	74LS74 dual D- flip-flop
_____	3	74LS158/74LS258 quad 2 input inverting multiplexor
_____	1	74LS160/74LS161/74LS162/74LS163 hex/decade counter
_____	2	74LS266 quad 2 input EXCLUSIVE NOR gates
_____	1	74LS373/74S373 octal latch/tri-state* buffer
_____	1	74LS393/74393 dual hex counter
_____	16	2107B/RM1701/MM5280 4096 x 1 dynamic memory
_____	2	sets machine screws and nuts

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ASSEMBLY INSTRUCTIONS

DO NOT INSTALL OR SOLDER ANY PARTS UNTIL YOU HAVE READ THE INSTRUCTIONS SEVERAL TIMES AND HAVE FULLY DIGESTED THE INFORMATION!

CAUTION - DO NOT SOLDER OR CLIP COMPONENT LEADS WITHOUT USING SAFETY GLASSES!

INSPECTION

Use the Parts List to make sure that there are no missing items in your kit. Please notify us of any shortages. Be sure that you check for missing parts before you start to assemble the kit.

COMPONENT LEAD WIDTHS

Bend the leads on the resistors, axial capacitors and diodes to their proper widths before insertion so that they will insert easily, solder cleanly, and give the assembled board a professional appearance. If you do not have a bending block, you can make one easily by driving small finishing nails into a block of wood at intervals 4/10 inches apart for 1/2 inch, 4.5/10 inches for .55 inch and 1/2 inch for 6/10 inches. The component leads can be bent over the nails.

All resistors in this kit should have a lead width of 1/2 inch. This is also true for the diodes.

There are a total of twelve 2.7 µfd tantalum capacitors located within the memory array. These have a lead length of 1/2 inch. There are eight 2.7 µfd tantalum capacitors located at the top of the memory array -- four of these have lead lengths of 1/2 inch while the other four have lead lengths of 6/10 inches. The four 39 µfd tantalum capacitors at the top of the memory array have lead lengths of 6/10 inches. There are eight 39 µfd tantalum capacitors at the bottom of the memory array. The four vertical pieces have 5.5/10 inch lead lengths while the four horizontal have 6/10 inches.

The two 39 µfd tantalum capacitors near the 7805 +5 volt regulator have lead lengths of 6/10 inches as do the four 2.7 µfd tantalum capacitors on the side and below the 78M12 +12 volt regulator.

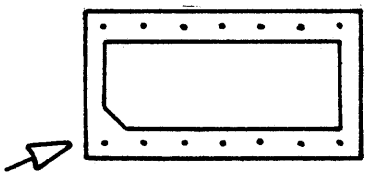
The transistors and disk capacitors have partially formed leads and may be inserted without preparation.

SOCKETS

A socket is furnished for every integrated circuit. It is important that you use these sockets, otherwise a defective part will be extremely difficult to replace. NO REPAIR OR SERVICE WILL BE PERFORMED ON A KIT WHICH HAS HAD INTEGRATED CIRCUITS SOLDERED TO THE CIRCUIT BOARD.

PARTS ORIENTATION

In all references throughout the instructions, the convention used is that the gold edge connector is the bottom of the board. Orientation identification is molded into the plastic of the sockets and is illustrated below.



This orientation marks identifies where pin #1 of the integrated circuit is to be positioned when it is plugged into the socket. The sockets should be inserted in the board so that the orientation mark is in the lower left hand corner.

Orientation of the transistors, tantalum capacitors, diodes and voltage regulators is specified in the component layout drawing. Be sure to study this drawing and the 8x10 glossy photograph carefully before building the kit. Refer to both during parts installation.

The DIP switch occupies position 1F on the circuit board and should be oriented so that switch #1 is on the left. The "off" position for all switches is then in the down direction while the "on" position is toward the top.

SOLDERING AND SOLDER IRONS

A minature style 18 watt iron with a fine tip is ideal for constructing this kit. Do not use an iron of more than 25 watts under any circumstance. In any event, the tip should be small. If too much heat is applied to the board, the copper traces will lift. The most desirable soldering iron for complex electronic kits is a constant temperature tool. These are somewhat more expensive but will make a good investment for the serious kit builder.

As a general rule, bend the component leads and socket pins only enough to hold the part to the board until it is soldered. Even though a protective solder mask has been applied to the circuit board, excessive solder can still cause bridges where leads are close together. It is important to economize on solder. Use only enough to cover the joint and leave the iron on the pad just long enough to cause the solder to flow throughout the joint.

The ground and power pads of the voltage regulators and tantalum capacitors adjacent to the regulators are designed so that these components will solder to their pads without absorbing too much heat from the iron. The 18 watt iron will supply enough heat without burning up components or lifting solder pads.

DO NOT INSTALL OR SOLDER ANY PARTS UNTIL YOU HAVE READ THESE INSTRUCTIONS CAREFULLY!

CAUTION - DO NOT SOLDER CLIP COMPONENT LEADS WITHOUT USING SAFETY GLASSES!

PARTS INSTALLATION

Before installing parts, bend the leads of the resistors, diodes and tantalum capacitors to their proper lengths. After a series of parts have been installed in the board, bend the leads slightly to hold them in place. Solder the leads and trim the excess lead length before proceeding to the next series.

Install

_____ C4, C7, C10, C13 (top of board) Check for orientation!

_____ C5, C8, C11, C14 (top of board) Check for orientation!

_____ C22, C25, C28, C31 (upper) Check for orientation!

_____ C33, C34 (middle left) Check for orientation!

_____ C39, C42, C45, C48 (middle) Check for orientation!

_____ C54, C57, C60, C63 (middle) Check for orientation!

_____ C65, C66 (left) Check for orientation!

_____ R1 (top)

_____ R2, R3 (middle)

_____ R4, R5, R6, R7 (left)

_____ R8, R9, R10 (left)

_____ R11 - R18 (lower left)

_____ CR1 (left) Check for orientation!

_____ CR2 - CR5 (lower left) Check for orientation!

_____ Sockets 3A, 1B, 2B, 3B, 1C, 2C, 3C, 1D, 2D, 3D, 1E, 2E, 3E, 2F, 3F Check for orientation!

_____ Sockets 4A, 5A, 6A, 7A, 4B, 5B, 6B, 7B, 4C, 5C, 6C, 7C, 4D, 5D, 6D, 7D Check for orientation!

_____ Sockets 4E, 5E, 6E, 7E Check for orientation!

_____ C6, C9, C12, C15 (top) Check for orientation!

_____ C16, C17 (left) Check for orientation!

_____ C67, C69, C71, C73 (bottom) Check for orientation!

_____ C68, C70, C72, C74 (bottom) Check for orientation!

_____ Slide switch

_____ C1, C2, C3, C18, C19, C20, C35, C36, C37, C50, C51, C52, C75, C76, C77, C78, C79, C80, C84, C85, C86

_____ C21, C24, C27, C30, C38, C41, C44, C47, C53, C56, C59, C62

_____ C23, C26, C29, C32, C40, C43, C46, C49, C55, C58, C61, C64, C81, C82, C83

_____ Q1, Q2 (left) Check for orientation!

_____ Install the +5 volt and +12 volt regulators by bending leads, inserting and hand tightening the nut and bolt through the regulators and circuit board. Finally, solder the leads.

_____ Install the 8 position DIP switch (lower left) Check for orientation!

POWER-UP AND SYSTEM CHECK OUT

POWER SUPPLY/VOLTAGE REGULATOR CHECK OUT

Voltage requirements: (reference to ground connector pins 50 and 100)

Pins 1 and 51	not less than 7 volts not more than 10 volts	approx. 260 ma
Pin 2	not less than 14 volts not more than 22 volts	approx. 80 ma
Pin 52	not less than -22 volts not more than -7 volts	approx. 20 ma

Before installing any of the integrated circuits, apply power to pins 1 and 51, pin 2, and pin 52 (ground pins 50 and 100) of the edge connector as specified above. Perform the following measurements with a volt meter.

(1)	Pin 18 of 4D	+12 volts
(2)	Pin 18 of 7D	+12 volts
(3)	Pin 1 of 4A	-5 volts
(4)	Pin 1 of 7A	-5 volts
(5)	Pin 11 of 4D	+5 volts
(6)	Pin 11 of 7D	+5 volts
(7)	Pin 20 of 7E	+5 volts
(8)	Pin 16 of 4D	+5 volts
(9)	Pin 24 of 3F	+5 volts
(10)	Pin 14 of 1E	+5 volts

If the voltage at any of the check points differs from the required value, return the board for trouble shooting and repair.

POWER-UP CHECK OUT

Install the integrated circuits as per the layout sheet. When inserting these parts, be careful about bending pins under the package -- a pin which is bent under the integrated circuit may appear to be inserted in the socket. Many of the units will be shipped with memorys which are housed in ceramic packages with pins brazed to the side of the device. These pins are slightly wider than the pins of plastic parts and as a result are somewhat harder to

insert into new IC sockets. The best way to handle this problem is to tilt the part slightly so that one end goes into the socket slightly before the other.

After all parts have been installed, voltages checked and integrated circuits installed, configure the address selection switches to a convenient address block, insert the board and power up your computer. Through either the front panel or system monitor, do several examines and deposits in block A and block B. Be sure the write protect switch is in the write enabled position. If any problem occurs when data is written into either block, return the board for trouble shooting and repair.

Next, read the memory test section of this manual carefully. Load and initialize the memory test program and then start it. If errors occur, return the board. Most of the problems with malfunctioning boards are either errors in construction or faulty parts. However, the operation of dynamic memory units is somewhat more complex than static boards and therefore more difficult to trouble shoot. So, if the board has been properly assembled but does not work, it will save time and be less frustrating if the memory is returned for check out, repair and testing.

WARRANTY

Parts are warranted to be free from defects in material and workmanship. Defective parts returned postpaid will be exchanged free of charge. ThinkerToy products purchased in kit form are warranted for six months from date of invoice. ThinkerToy products purchased as assembled units are warranted for one year from invoice date. Malfunctioning units whether purchased in kit form or pre-assembled will be repaired, tested, and returned with a minimal charge for postage/handling if in the opinion of Morrow's Micro-Stuff or ThinkerToys care has been exercised in their assembly and/or use. If on inspection by Morrow's, it is found that the product has been subject to improper assembly or abuse, charges will be assessed accordingly for repair parts and labor. Repair fees will not exceed $25.00 unless prior approval has been obtained from purchaser.

The foregoing warranty is in lieu of all other warranties expressed or implied and in any event is limited to product repair or replacement.

COMPATIBILITY

The Synchrofresh memory design is very simple. It requires no delay lines, one shots, or on-board crystal oscillators. This simplicity results in lower cost and higher reliability; however, this simplicity has a trade off. Synchrofresh design requires that the timing relationships on the S-100 buss be well defined so that invisible refresh can be woven into normal memory cycles. Specifically, the timing relations between ϕ_2, PSYNC, PDBIN and $\overline{\text{PWR}}$ must closely resemble the natural sequencing of the 8080A. Unfortunately, there are a number of processor boards and DMA units which plug into the S-100 buss whose timing is considerably different from the classic 8080A signals. The devices which are known not to work with the Synchrofresh 8K memory are:

1. TDL Z-80 CPU board
2. SD Sales Z-80 CPU board
3. Mini-term DMA video board
4. Digital Systems DMA disk controller
5. Cromenco Dazzler DMA video board.

Care should be exercised whenever the memory is used with a DMA device or a Z80 CPU board. If the timing signals of these devices are reasonably close to those of the classic 8080A signals, the memory should perform flawlessly. If the differences are too great, the memory may fail. In such an event, we ask that the customer return the memory so that the purchase price can be refunded.