altair 680b
UNIVERSAL I/O BOARD DOCUMENTATION

First Printing, December, 1976

mits INC.
2450 Alamo S.E./Albuquerque, New Mexico 87106

Altair 680b Universal I/O Board

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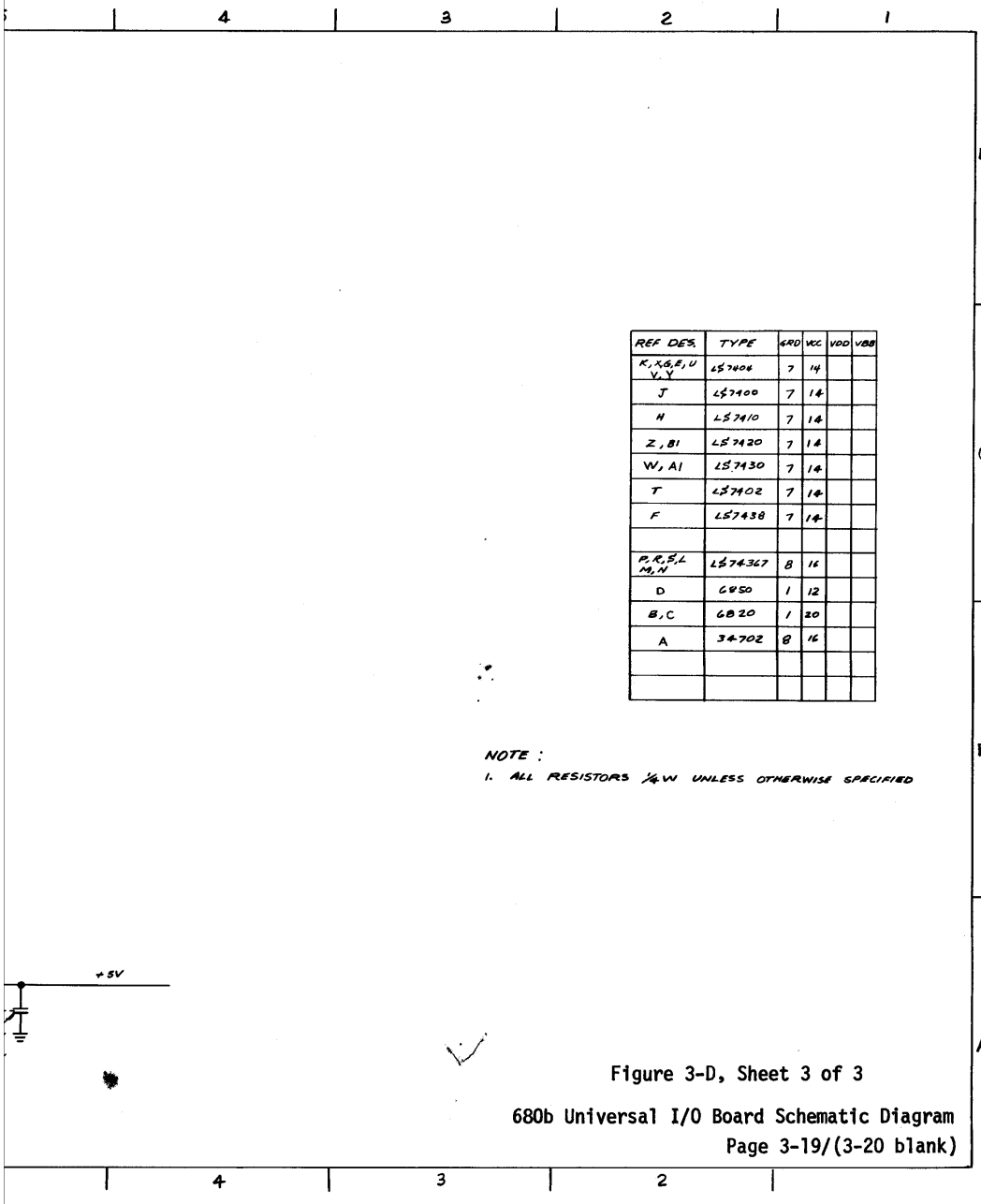
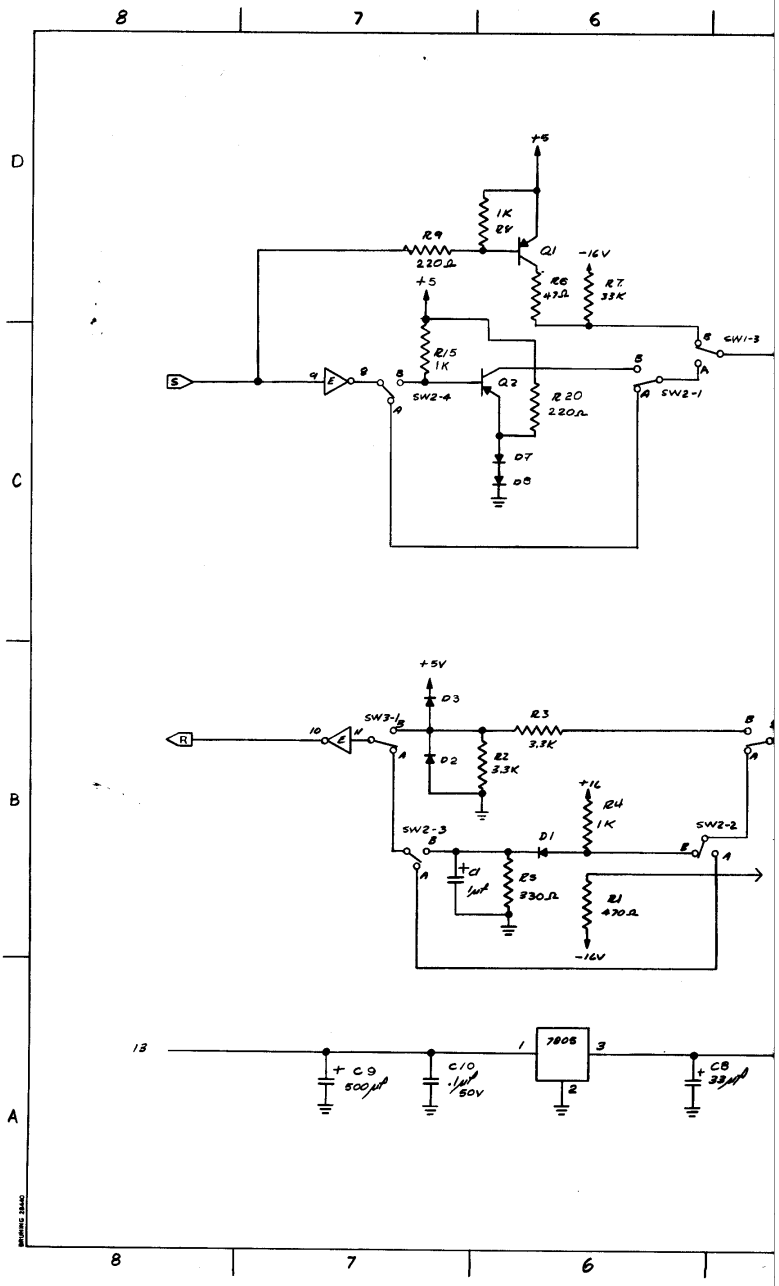


Figure 3-D, Sheet 3 of 3

680b Universal I/O Board Schematic Diagram

LIST OF ILLUSTRATIONS

LIST OF PROGRAMS


8
7
6
D
C
B
A
+5
1K
R9
220Ω
Q1
-16V
R6
47Ω
R7
33K
+5
R15
1K
Q2
R20
220Ω
SW2-4
SW2-1
SW1-3
D7
D9
S
E
+5V
D3
SW3-1
R3
3.3K
10
R
D2
R2
3.3K
+16
R4
1K
SW2-3
D1
SW2-2
+C1
1μF
R5
330Ω
R1
470Ω
-16V
13
7805
1
3
2
+C9
500μF
C10
.1μF
50V
+C8
33μF

1-1. SCOPE AND ARRANGEMENT

The Altair 680b Universal I/O Board Documentation provides a general description of the printed circuit board and detailed theory of its operation. The manual contains five sections as follows:

1. Section I contains a general description of the Altair 680b Universal I/O Board.
2. An explanation of parallel (PIA) and serial (ACIA) port selection, including the port structure and operation, is presented in Section II.
3. Section III includes a detailed theory explanation of the 680b Universal I/O circuit operation.
4. Section IV contains instructions for installing the Universal I/O Board into the Altair 680b computer.
5. Troubleshooting information for the 680b Universal I/O Board is found in Section V.

1-2. DESCRIPTION

The 680b Universal I/O Board provides two parallel ports and one serial port while occupying only one slot on the 680b expander card. The design of the parallel and serial ports is based upon two peripheral ICs, the 6820 Parallel Interface Adapter (PIA) and the 6850 Asynchronous Communication Interface Adapter (ACIA), respectively.

The PIA contains all Control and Data Registers, thus most options are software selectable. These options include data direction (each data line can act as an input or an output) and interrupt/control structure. The Universal I/O Board can be expanded up to two parallel ports. With only one PIA parallel port, the board can handle two inputs (such as a paper tape reader or keyboard) or two output devices (such as a paper tape punch and printer) or any combination of custom applications. A Universal I/O with two PIA parallel ports has 32 data lines (each group of eight is individually selectable) and all data lines are fully TTL compatable. When utilized as outputs, eight of the 16 data lines are capable of directly driving the base of a transistor switch (1.5v at 1ma). The Universal I/O is also provided with a parallel 8-bit non-latched output at TTL levels.

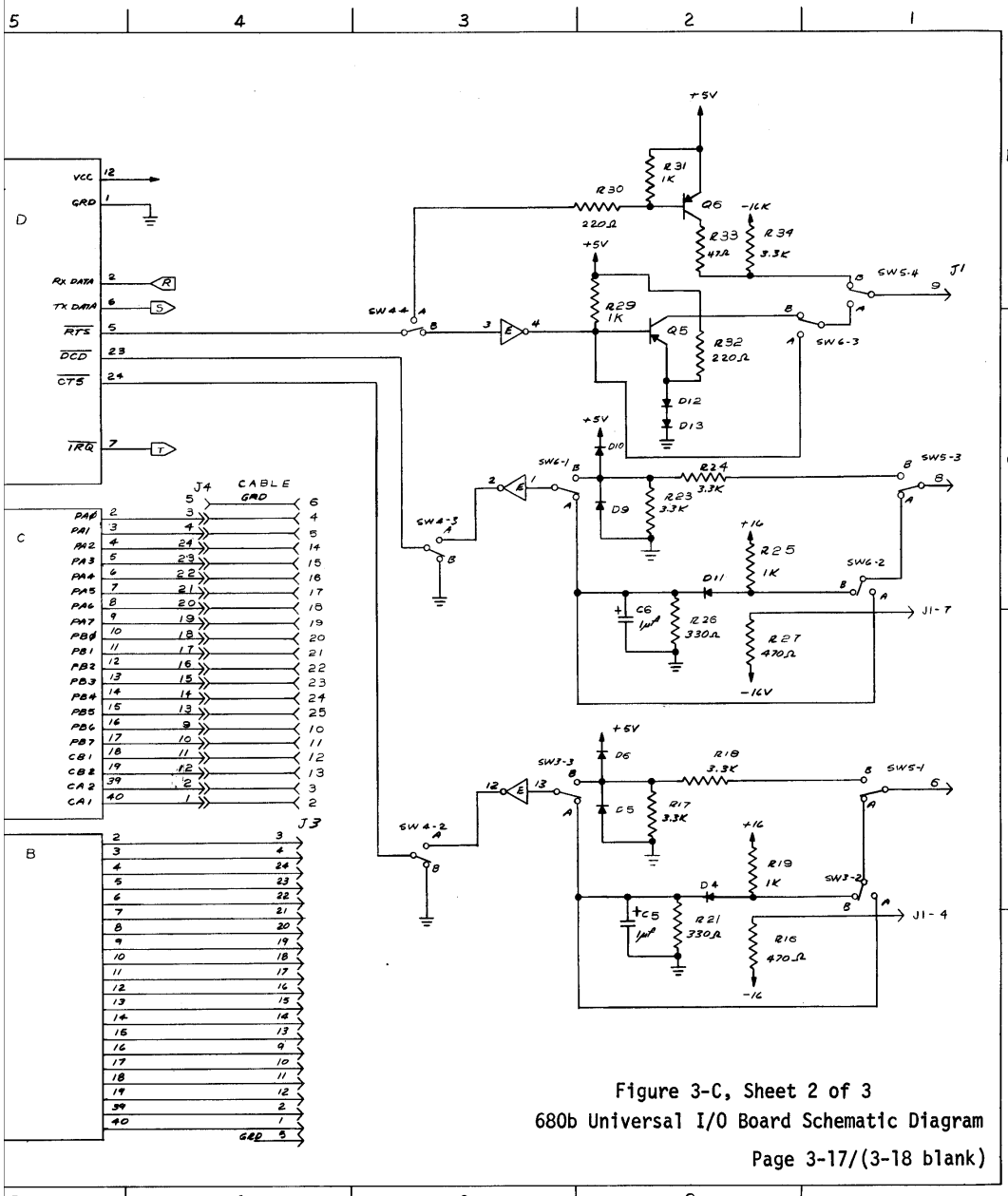
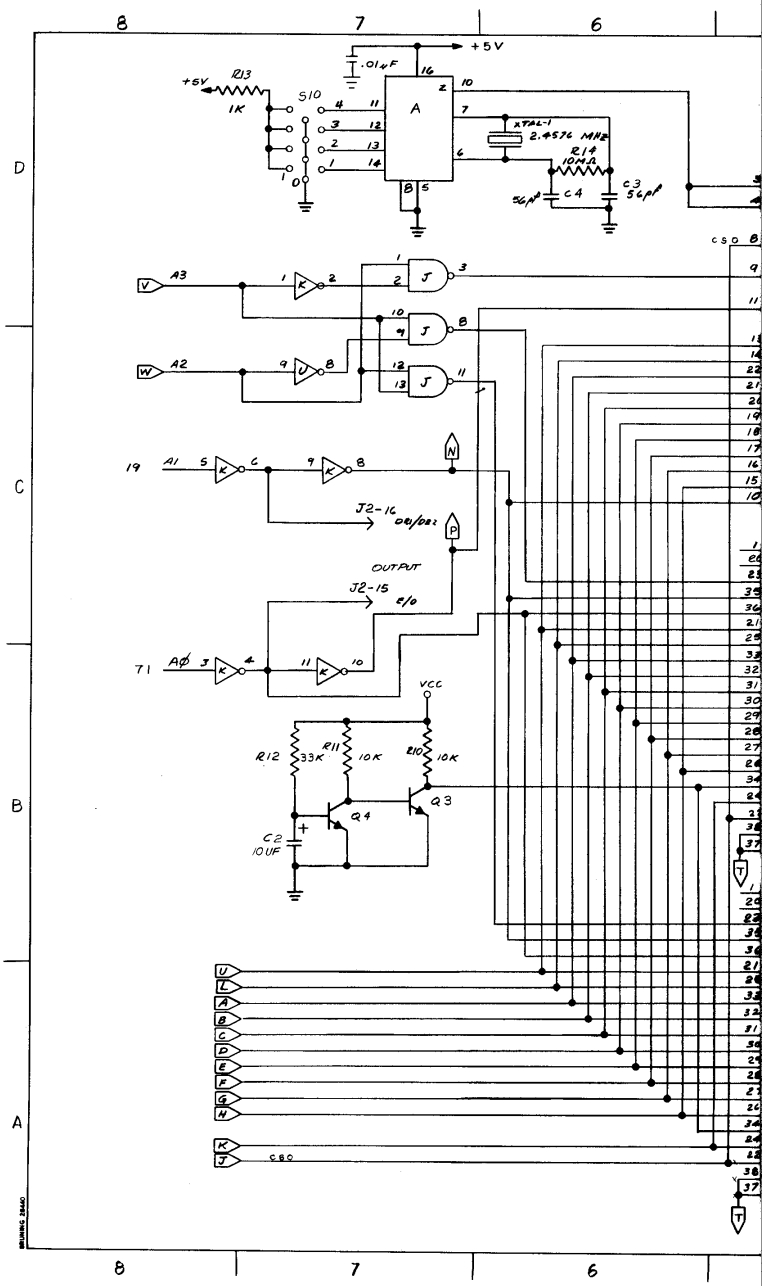


Figure 3-C, Sheet 2 of 3
680b Universal I/O Board Schematic Diagram

SECTION II

altair 680b UNIVERSAL I/O
THEORY OF OPERATION
PORT SELECTION


8
7
6
D
C
B
A
+5V
.01uF
+5V
R13
1K
S10
A
XTAL-1
2.4576 MHz
R14
10MΩ
C4
56pF
C3
56pF
A3
A2
A1
A0
J2-16
OUTPUT
J2-15
I/O
VCC
R12
33K
R11
10K
R10
10K
Q3
Q4
C2
10UF
CSO
CSO
BRUNING 2840

2-1. GENERAL

Section II contains a detailed description of the MITS Altair 680b Universal I/O Board parallel (PIA) and serial (ACIA) port selection. Tables are provided to aid in understanding the PIA and ACIA structure and operation.

2-2. PARALLEL PORT (PIA) SELECTION

The Altair 680b reserves 256 address locations for I/O interfacing and each I/O card requires 16 address lines. Hardware sets the upper address lines, A15 through A8, to F0 for all I/O ports. These addresses are F0XX (XX = user selectable). Address lines A7 through A4 and their complements, $\overline{A7}$ through $\overline{A4}$, are also user selectable. With these addresses, there are 16 different address locations for the Universal I/O. Address lines A3 and A2 select between three ports. A3 addresses the parallel ports or the serial port and A2 selects between the parallel ports.

Each PIA contains two sections, A and B, and each section has two channels, Control/Status and Data-Data Direction. Address lines AØ and A1 enable the selection of the port section and the channel. If the two parallel ports are addressed at F008 and F00C, the port, section, and channel addresses would appear as in Table 2-1, assuming the board is strapped at the lowest possible position.

Table 2-1. PIA Address Selection

ADDRESS	IC	SECTION	CHANNEL
F008	C	A	CONTROL/STATUS
F009			DATA - DDR
F00A		B	CONTROL/STATUS
F00B			DATA - DDR
F00C	B	A	CONTROL/STATUS
F00D			DATA - DDR
F00E		B	CONTROL/STATUS
F00F			DATA - DDR

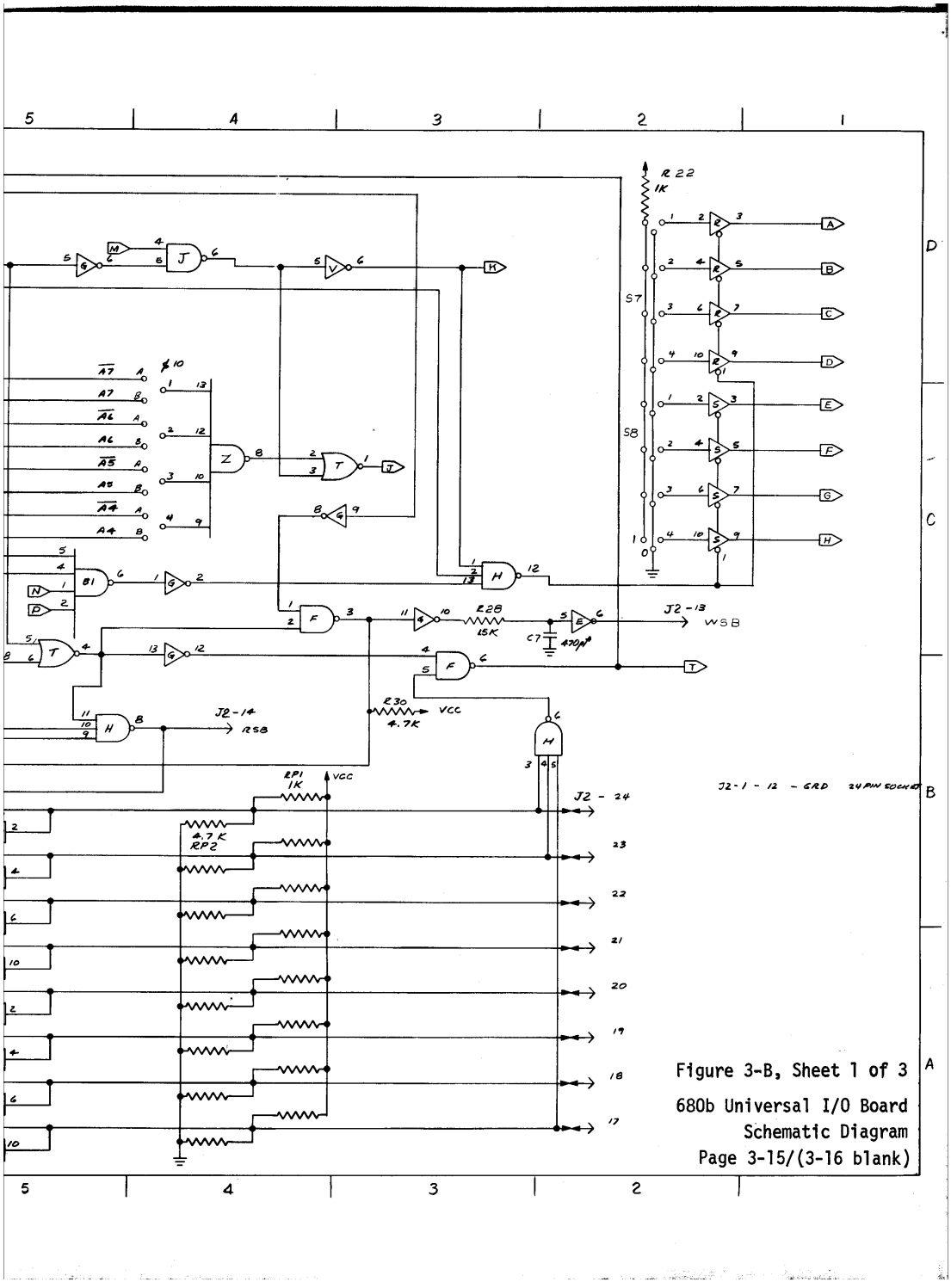


Figure 3-B, Sheet 1 of 3

680b Universal I/O Board
Schematic Diagram
Page 3-15/(3-16 blank)

Control bits 1 and Ø affect the operation of the external control line, C1. C1 is used as an input control line from the I/O device. Status bit 7 and the interrupt request output to the system bus, $\overline{IRQ}$, are then affected by the activity of C1 as shown in Table 2-3. Bit 7 and $\overline{IRQ}$ are reset (bit 7 goes LOW, $\overline{IRQ}$ goes HIGH) when the Data Register is read by the MPU. Control bit 1 determines whether C1 is active with a LOW going transition (bit 1 = 0) or active with a HIGH going transition (bit 1 = 1). The $\overline{IRQ}$ is dependant on how bit Ø is set in the Control Register. For example, if bit Ø = 1 and C1 is active, the $\overline{IRQ}$ output will be LOW, interrupting the system.

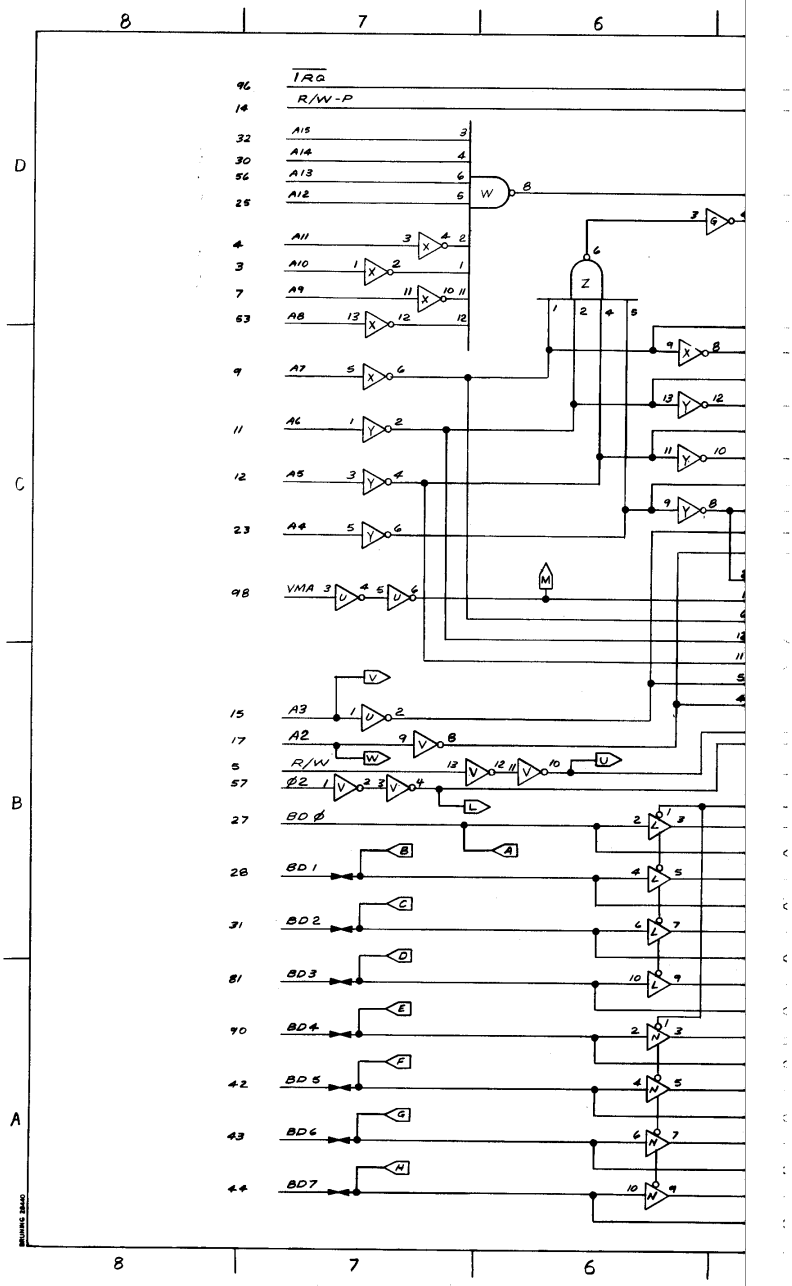
Table 2-3. Control of Interrupt Inputs, C1 (CA1 and CB1)

CONTROL BITS 1	0	C1 INPUT	STATUS BIT 7	$\overline{IRQ}$ OUTPUT
0	0	Active LOW	Set HIGH when C1 is active	Disabled -- remains HIGH
0	1	Active LOW	Set HIGH when C1 is active	Goes LOW when Bit 7 is HIGH
1	0	Active HIGH	Set HIGH when C1 is active	Disabled -- remains HIGH
1	1	Active HIGH	Set HIGH when C1 is active	Goes LOW when Bit 7 is HIGH

The C2 control line can function as either an input or an output for the I/O device. When C2 functions as an input (control bit 5 LOW), its mode of operation is determined by control bits 5, 4, and 3 as shown in Table 2-4. Sections A and B operate identically when C2 functions as an input.

Table 2-4. Control of Interrupt Inputs, C2 (CA2 and CB2)

CONTROL BITS 5	4	3	C2 INPUT	STATUS BIT 6	$\overline{IRQ}$ OUTPUT
0	0	0	Active LOW	Set HIGH when C2 is active	Disabled -- remains HIGH
0	0	1	Active LOW	Set HIGH when C2 is active	Goes LOW when Bit 6 is HIGH
0	1	0	Active HIGH	Set HIGH when C2 is active	Disabled -- remains HIGH
0	1	1	Active HIGH	Set HIGH when C2 is active	Goes LOW when Bit 6 is HIGH


8
7
6
D
C
B
A
96 IRQ
14 R/W-P
32 A15
30 A14
56 A13
25 A12
4 A11
3 A10
7 A9
63 A8
9 A7
11 A6
12 A5
23 A4
98 VMA
15 A3
17 A2
5 R/W
57 Ø2
27 BD Ø
28 BD 1
31 BD 2
81 BD 3
90 BD 4
42 BD 5
43 BD 6
44 BD 7
W
Z
M
BROWNING 28A40

Data channel address permits access to either the Data Register or the Data Direction Register (DDR). The status bit 2 in the Control Register determines whether the Data Register or the DDR is accessed. If bit 2 is a logic Ø, the DDR is accessed. If bit 2 is logic 1, the Data Register is accessed. Writing a logic Ø into any bit of the DDR will cause the corresponding data line to act as an output. Thus, there can be any combination of inputs or outputs on the data lines (PAØ through PA7 and PBØ through PB7).

2-3. PIA Initialization

Program 2-I illustrates the initialization procedure for a parallel port. The initialization sets up communication between the MPU and the 680b Universal I/O Board. In this example, PIA-C is utilized and the Universal I/O is addressed at its lowest location, F008 through F00B. If a second parallel port is used, the lowest address location would be F00C through F00F.

The addresses function as follows: F008 = section A Control/Status Register; F009 = section A Data-Direction (when accessed) and Data Channel Register; F00A = section B Control/Status Register; F00B = section B Data-Direction (when accessed) and Data Channel Register.

Section A functions as an input and section B functions as an output.

INPUT

1. If the I/O device has valid data, a strobe signal from the I/O device pulls the input CA1 line LOW. Bit 7 of section A Control/Status Register goes HIGH. CA2 goes LOW following a Read of section A Data Channel, then returns HIGH after the next ENABLE pulse. CA2 is telling the I/O device that data has been read and to send more data.
2. With additional programming, the MPU can be instructed to periodically check the section A Control/Status Register to interpret the status of bit 7. When bit 7 is HIGH, Step 3 will be entered.
3. Data Channel Register is input to the accumulator. This, in turn, resets bit 7 of the Control/Status Register and CA2 becomes active. CA2 returns HIGH after the next E pulse. CA2 tells the I/O device that new data may be entered.

5	"	Pin 13 of H should be HIGH	If pin 13 is LOW, monitor output pin 6 of B1 (sheet 1 of 3, zone C5). If pin 6 is LOW, replace IC-G (zone C4). If pin 6 is HIGH, check input pins 5, 4, 2, and 1 of B1 (zone C5). All input pins of B1 should be HIGH. If one pin is LOW, the inverter on the pin is probably defective or the address lines are open or shorted.

2-4. SERIAL PORT (ACIA) SELECTION

The 680b Universal I/O Board utilizes a 6850 Asynchronous Communications Interface Adapter (ACIA). The ACIA allows serial data to be taken in on its receive line and transfers the data onto the data bus, or data can be entered from the data bus into the ACIA and sent out the transmit data line in serial form.

The ACIA has three chip select inputs, CSØ, CS1, and $\overline{CS2}$, which are used in the selection of the ACIA. It also has a Register Select (RS) input, controlled by address line AØ, that can select between the different internal registers. The ENABLE signal is used for internal interrupt control and the timing of Control/Status changes. Since all data transfers take place during Ø2 of the system clock, it is used as the ENABLE signal. The R/W signal determines the direction of data flow.

2-5. ACIA Control Register

The ACIA has an 8-bit Control Register that allows port configuration under software control. Each bit is defined in Table 2-7.

7	6	5	4	3	2	1	0
In Interrupt	Out Interrupt		Transmission Bits			Clock Divide And Reset	

NOTE: Data Bit LOW = 0
Data Bit HIGH = 1

Table 2-7. ACIA Control Register

The first two data bits, Ø and 1, control the internal clock divide circuit and the Master Reset as shown in Table 2-8.

BIT 1	BIT Ø	FUNCTION
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Table 2-8. Control Bits for Internal Clock Divide and Master Reset

		RSØ = Logic 1	If RSØ = Logic Ø, IC-K pins 3 and 4 (sheet 2 of 3, zone C7) are probably defective or address line AØ is HIGH. If AØ switch is toggled, RSØ will be LOW when AØ is HIGH and HIGH when AØ is LOW.
3	Check ENABLE pins 25 of IC-B and IC-C	Ø2 clock (500KHz)	If missing, IC-V pins 1 and 2 and 3 and 4 (sheet 1 of 3, zone B7) are probably defective.
4	Check R/W line pins 21 of IC-B and IC-C	Normally HIGH until deposit switch is actuated and then it drops LOW. (See 680b manual for R/W timing)	If always LOW or always HIGH, IC-V pins 11, 10, and 13, 12 (sheet 1 of 3, zone B6) are probably defective.
5	Check Reset pins 34 of IC-B and IC-C	Should be +5 volts	If LOW, Q3 or Q4 (sheet 2 of 3, zone B7) are probably defective.
6	Deposit various bit patterns in memory	Data lines DØ through D7 (pins 33 through 26) should have the same bit pattern as shown on the Data LEDs	If pattern differs, check the lines for shorts or opens.

In order to choose any one of 5 additional baud rates, select the baud rate from Table 2-10 and set S10, using the ÷ 64 mode (data bits 1 and Ø are equal to 1 and Ø, respectively). Note that the selected baud rate is four times larger than the desired baud rate. Due to the internal structure of the ACIA, it is not possible to use the ÷ 1 clock because some means of external synchronization must be used.

DESIRED BAUD RATE	SELECTED BAUD RATE
27.5	110
37.5	150
75.0	300
450	1800
600	2400

Table 2-10. Additional Baud Rate Selection

The next three bits of the Control Register determine word length, parity, and the number of stop bits. Consult the I/O device manual for the configuration required and set the bits according to Table 2-11.

DATA BIT			FUNCTION		
4	3	2	# of Data Bits	# of Stop Bits	Parity
0	0	0	7	2	Even
0	0	1	7	2	Odd
0	1	0	7	1	Even
0	1	1	7	1	Odd
1	0	0	8	2	None
1	0	1	8	1	None
1	1	0	8	1	Even
1	1	1	8	1	Odd

Table 2-11. Transmission Control Bits

5	Toggle address switch AØ	RS (pin 11 of ACIA-D) should toggle along with AØ. AØ = RS	If RS (zone D5) does not toggle or toggles but is inverted from AØ, then IC-K (zone B7) is probably defective.
6	"	ENABLE pin 14 should be Ø2 clock (500 KHz). If it is correct, proceed to Step 7.	If Ø2 is missing, IC-V (sheet 1 of 3, zone B7) is probably defective.
7	"	R/W pin 13 (sheet 2 of 3, zone C5) is normally HIGH until deposit switch is actuated. Then it drops LOW for approximately 2.5 msecs. If correct, proceed to Step 8.	If signal is missing or inverted, IC-V (sheet 1 of 3, zone B6) is probably defective.
8	Deposit various bit patterns in memory	Data lines on ACIA-D (pins 22 through 15) should have the same pattern on them as the Data LEDs. If correct, proceed to Step 9.	If pattern differs, check the lines for shorts or opens.
9	Check pin 10 of IC-A	Baud Rate Clock frequency will be 16 times higher than the selected baud rate.	If clock is missing, IC-A (sheet 2 of 3, zone D7) or associated components are probably defective. If baud rate is incorrect, double check baud rate selected.

2-6. ACIA Status Register*

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when Register Select (RS) is LOW and R/W is HIGH. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit Ø - RDRF indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. $\overline{\text{Data Carrier Detect}}$ being HIGH also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 - The TDRE bit being set HIGH indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The LOW state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

$\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), Bit 2 - The $\overline{\text{DCD}}$ bit will be HIGH when the $\overline{\text{DCD}}$ input from a modem has gone HIGH to indicate that a carrier is not present. This bit going HIGH causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains HIGH after the $\overline{\text{DCD}}$ input is returned LOW until cleared by first reading the Status Register and then the Data Register or until a Master Reset occurs. If the $\overline{\text{DCD}}$ input remains HIGH after Read Status and Read Data or Master Reset have occurred, the $\overline{\text{DCD}}$ status bit remains HIGH and will follow the $\overline{\text{DCD}}$ input.

$\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$), Bit 3 - The $\overline{\text{CTS}}$ bit indicates the state of the $\overline{\text{CTS}}$ input from a modem. A LOW $\overline{\text{CTS}}$ indicates that there is a $\overline{\text{Clear To Send}}$ from the modem. In the HIGH state, the Transmit Data Register Empty bit is inhibited and the $\overline{\text{Clear To Send}}$ status bit will be HIGH. Master Reset does not affect the $\overline{\text{Clear To Send}}$ status bit.

Table 5-1. POWER SUPPLY CHECK

Step	Settings and Instructions	Correct Readings	If Incorrect
1	Check +9v UNREG at bus pin 13, +16v at bus pin 76, -16v UNREG at bus pin 72	Should be about +9v; +16v and -16v, respectively	Problem probably with input tramsformer (refer to 680b manual or 680b-MB)
2	Check +5v REG at output side of VR1 or check VCC on various ICs (pin 14 for 14-pin ICs and pin 16 for 16-pin ICs)	Should be a constant +5v with a ±5% tolerance	Check VR1 or check for possible shorts

SECTION III

altair 680b UNIVERSAL I/O
THEORY OF OPERATION
CIRCUITRY

b. With these connections made, th PA data lines are shorted to the PB data lines. CA1 is tied to CB2 and CA2 is tied to CB1. The connections allow the parallel port echo program (Program 5-II) to be run by outputting data on the PB data lines and inputting data on the PA data lines.

c. Using the 680b monitor M and N commands, enter all underlined characters in Program 5-II.

Program 5-II. PIA Parallel Port Echo

```
.M ØØØØ 4F
.N ØØØ1 B7
.N ØØØ2 F0
.N ØØØ3 08 or 0C
.N ØØØ4 B7
.N ØØØ5 F0
.N ØØØ6 09 or 0D
.N ØØØ7 B7
.N ØØØ8 F0
.N ØØØ9 0A or 0E
.N ØØØA 43
.N ØØØB B7
.N ØØØC F0
.N ØØØD 0B or 0F
.N ØØØE 86
.N ØØØF 04
.N ØØ1Ø B7
.N ØØ11 F0
.N ØØ12 08 or 0C
.N ØØ13 B7
.N ØØ14 F0
.N ØØ15 0A or 0E
.N ØØ16 BD
.N ØØ17 FF
.N ØØ18 00
.N ØØ19 F7
.N ØØ1A F0
.N ØØ1B 0B or 0F
.N ØØ1C F1
.N ØØ1D F0
.N ØØ1E 09 or 0D
.N ØØ1F 27
.N ØØ2Ø F5
.N ØØ21 7E
.N ØØ22 FF
.N ØØ23 AB
.J ØØØØ
```

d. The program should echo any character entered through the 680b Main Board ACIA. If there is an error whenever a character is entered, the program will jump back to the system monitor and print out a dot.

e. Halt the machine and follow the instructions in Table 5-3 (page 5-12). The table assumes the board is strapped at the lowest location. The VMA must be jumpered HIGH at pin 3 of IC-U.

3-1. GENERAL

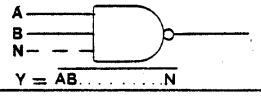
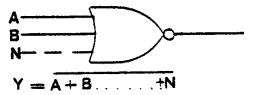
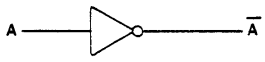
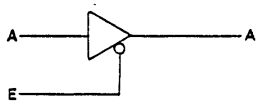
Section III provides a detailed theory explanation of the 680b Universal I/O Board circuitry, including a basic description of the logic symbols used in the Universal I/O schematics.

3-2. LOGIC CIRCUITS

The detailed schematics of the 680b Universal I/O Board (sheets 1 of 3, 2 of 3, and 3 of 3) are drawn to aid in determining signal direction and tracing. A solid arrow (→) on the signal line indicates direction.

The logic circuits used in the Universal I/O schematics are presented in Table 3-1. The table provides the functional name, symbolic representation, and brief description of each logic circuit. Where applicable, a truth table is furnished to aid in understanding circuit operation. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

Table 3-1. Symbol Definitions

NAME	LOGIC SYMBOL	DESCRIPTION
NAND gate		The NAND gate performs one of the common logic functions. All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output.
NOR gate		The NOR gate performs one of the common logic functions. Any of the inputs needs to be enabled (HIGH) to produce the desired (LOW) output.
Inverter		The inverter is an amplifier whose output is the opposite state of the input.
Non-Inverting Bus Driver		The non-inverting bus driver is an amplifier whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input.

the probable cause is a defective input at one of the elements that the output feeds. Isolate each input in turn by disconnecting it from the external circuitry.

c. If an input is between .8 volts and 2 volts, check continuity back to the driving output.

5-6. ACIA TROUBLESHOOTING

1. Since the 680b Universal I/O Board is mainly software controlled, possible failures may be due to software bugs. Program 5-I is for ACIA serial port echo.
   a. Be sure the board is strapped at the lowest position.
   b. Program 5-I may be changed for the particular terminal being used (refer to terminal manual). The program also works with TTY.
   c. Using the 680b monitor M and N commands, enter all underlined characters in Program 5-I.

Program 5-I. ACIA Serial Port Echo

.M	ØØØØ	86	.N	ØØØB	FØ	.N	ØØ16	57
.N	ØØØ1	03	.N	ØØØC	Ø6	.N	ØØ17	57
.N	ØØØ2	B7	.N	ØØØD	47	.N	ØØ18	24
.N	ØØØ3	FØ	.N	ØØØE	24	.N	ØØ19	F9
.N	ØØØ4	Ø6	.N	ØØØF	FA	.N	ØØ1A	B7
.N	ØØØ5	86	.N	ØØ1Ø	B6	.N	ØØ1B	FØ
.N	ØØØ6	B1*	.N	ØØ11	FØ	.N	ØØ1C	Ø7
.N	ØØØ7	B7	.N	ØØ12	Ø7	.N	ØØ1D	2Ø
.N	ØØØ8	FØ	.N	ØØ13	F6	.N	ØØ1E	EB
.N	ØØØ9	Ø6	.N	ØØ14	FØ	.J	ØØØØ	
.N	ØØØA	B6	.N	ØØ15	Ø6			

*NOTE: B1 sets up 8 data bits, 2 stop bits, Receive-Transmit interrupts enabled, and ÷ 16 mode.

Table 3-2. S9 Address Selection

PIA - B	PIA - C	ACIA - D	S9 Positions A7	A6	A5	A4
F00C - F00F	F008 - F00B	F006 - F007	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
F01C - F01F	F018 - F01B	F016 - F017	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4
F02C - F02F	F028 - F02B	F026 - F027	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$
F03C - F03F	F038 - F03B	F036 - F037	$\overline{A7}$	$\overline{A6}$	A5	A4
F04C - F04F	F048 - F04B	F046 - F047	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$
F05C - F05F	F058 - F05B	F056 - F057	$\overline{A7}$	A6	$\overline{A5}$	A4
F06C - F06F	F068 - F06B	F066 - F067	$\overline{A7}$	A6	A5	$\overline{A4}$
F07C - F07F	F078 - F07B	F076 - F077	$\overline{A7}$	A6	A5	A4
F08C - F08F	F088 - F08B	F086 - F087	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
F09C - F09F	F098 - F09B	F096 - F097	A7	$\overline{A6}$	$\overline{A5}$	A4
F0AC - F0AF	F0A8 - F0AB	F0A6 - F0A7	A7	$\overline{A6}$	A5	$\overline{A4}$
F0BC - F0BF	F0B8 - F0BB	F0B6 - F0B7	A7	$\overline{A6}$	A5	A4
F0CC - F0CF	F0C8 - F0CB	F0C6 - F0C7	A7	A6	$\overline{A5}$	$\overline{A4}$
F0DC - F0DF	F0D8 - F0DB	F0D6 - F0D7	A7	A6	$\overline{A5}$	A4
F0EC - F0EF	F0E8 - F0EB	F0E6 - F0E7	A7	A6	A5	$\overline{A4}$
F0FC - F0FF	F0F8 - F0FB	F0F6 - F0F7	A7	A6	A5	A4

3. Address Switch Settings

   Check to see that all the switch settings are set according to needs.

   a. Refer to Table 3-2, S9 Address Selection (page 3-3), to insure that the board is strapped to the proper locations for the ACIA and the PIAs.
   b. Make sure that your program uses the correct addresses.
   c. If the ACIA serial interface is used, insure that the proper interface is selected on S1 through S6. Refer to Table 3-3, ACIA-D Interface Selection (page 3-10).

5-3. POWER SUPPLY CHECK

After installation of the Universal I/O Board, a power supply check is necessary to insure that the proper voltage levels are being supplied to the various ICs. Follow the instructions in Table 5-1 (page 5-9), Power Supply Check.

5-4. PRELIMINARY CHECK

Upon completion of the power supply check, leave the machine on and place it in the Halt mode to check the address and data lines for shorts and opens.

1. The 16 address switches on the 680b front panel should be in the down position initially. Place all the switches in the up position and observe that all the address LEDs are on. Return all the switches to the down position and observe that all the LEDs go off.
2. Next, place each switch in the up position individually. Observe that the corresponding LED is on. After all the switches are up, return them individually to the down position and each LED should go off.
3. Another way of checking each address line is by toggling each address switch individually and checking the signal toggle while tracing it through the logic.

When FO for the upper address lines is selected, a LOW signal is presented to the input of NOR gate T pin 5 (sheet 1 of 3, zone C5). A LOW signal also goes to pin 6 from the output of NAND gate A1 pin 8 (zone B5). For A1 to have a LOW output, all the inputs must be HIGH. Address lines A7, A6, A5, A3, and A2 are LOW and inverted HIGH to the inputs of A1 pins 6, 12, 11, 5, and 4. A4 is double inverted to the input of A1 pin 2 and must be HIGH for the proper condition to exist. VMA is tied to pin 1 of A1. With VMA valid and the other input pins of A1 HIGH, the output pin 8 will be LOW.

The LOW signals at the input pins 5 and 6 (zone C5) enable pin 4 of NOR gate T HIGH. This signal goes to NAND gate H pin 11 (zone B5), enabling the gate for double inverted R/W and Ø clock signals. A LOW going pulse, 1 microsecond wide with a 20 microsecond period, occurs at the output pin 8 when data or status is being read from the device. This LOW going pulse is the READ STROBE and goes to J2 which is a 24-pin socket. A flat cable assembly plugs into this socket. The 25-pin plug on the other side of the assembly is used for the interface. The READ STROBE signal enables pins 1 (zone B5 and A5) of Tri-State drivers M and P, allowing data to be transferred from the device to the data bus.

The HIGH signal from NOR gate T pin 4 is also present at the input of NAND gate F pin 2 (zone C4) and inverted to F pin 4 (zone B3). R/W-P (zone D7) is inverted HIGH to F pin 1, enabling the output of F pin 3 (zone C3) LOW. There is a delay on this line and it is used to insure that Write data is valid when it is written into the device. The WRITE STROBE occurs at the output of E pin 6 (zone C2) and is a LOW going pulse with an approximate width of 1 microsecond and a period of 3 milliseconds. This signal goes directly to socket J2. Write data becomes valid 200 nanoseconds (maximum) after Data Bus Enable (DBE), which is tied directly to Ø2 of the system clock, is active HIGH.

5-1. INTRODUCTION

Section V is designed to aid in the location of malfunctions that could be encountered after the Altair 680b Universal I/O Board is installed in the 680b computer. Before installation of the board, it should be visually inspected according to the visual inspection check list. A power supply check, preliminary check, and general procedures for troubleshooting TTL logic are included to insure that the board is functioning properly. Since the board is mainly software controlled, programs for troubleshooting the ACIA, PIAs and sense switches are presented to assist in the location of possible failures.

> **WARNING**
> Always disconnect power when removing the board, cutting or resoldering PC lands, and removing or installing ICs.

5-2. VISUAL INSPECTION CHECK LIST

Before the 680b Universal I/O Board is installed, it is important to check the component assembly, etching of lands, and switch settings. Although the board should be assembled correctly, an extensive inspection may eliminate possible malfunctions.

1. General

   Carefully examine the board for the following:

   a. leads that have not been soldered
   b. solder bridges
   c. cold solder connections
   d. errors such as hairline opens in lands

2. Component Check

   Using the silkscreen diagram (Figure 5-A, page 5-2) as a guide, check the following:

   a. proper polarity of capacitors
   b. proper polarity of diodes
   c. correct color codes on all resistors
   d. proper pin placement and good solder connections
   e. proper placement of all components

The CS1 signal line for ACIA-D pin 10 (sheet 2 of 3, zone C5) is controlled by address line A1. A1 must be HIGH for ACIA-D to be selected since the signal is double inverted to the input pin 10. Line K is tied to CS1 of both parallel ports at pins 24 and must be HIGH at the same time CSØ is HIGH. This signal was derived earlier.

Addresses A3 (zone D8) and A2 (zone C8) are the inputs for a $\overline{CS2}$ decoding circuit. Only one of the outputs of NAND gate J (zone D7 and C7) should be LOW, enabling the particular port being used. The remaining two outputs of J should be HIGH, disabling the other ports. If the output of J pin 3 (zone D7) is LOW (ACIA-D selected), the input pins 1 and 2 are HIGH. Address line 2 is HIGH and this signal is presented to pin 1. Address line 3 is inverted HIGH and goes to pin 2. These two input signals give the desired LOW at the output of NAND gate J. If A3 is LOW, this signal goes directly to the inputs of NAND gates J pins 10 and 13, disabling both gates. If PIA-C (location FOO8) is selected, the output of J pin 8 (zone C7) is LOW. Input pins 10 and 9 must be HIGH for pin 8 to be LOW. This is assuming that S9 is positioned to $\overline{A7}$, $\overline{A6}$, $\overline{A5}$, and $\overline{A4}$. A HIGH signal from A3 goes directly to pin 10. A2 is LOW and inverted to present a HIGH to the input pin 9. The LOW signal from A2 goes directly to the input pins 1 and 12 of J, disabling ACIA-D and PIA-B. If PIA-B is to be enabled (location FOOC), pin 11 (zone C7) should be LOW, and the other two output pins 3 and 8 should be HIGH. A HIGH signal goes directly to input pins 12 and 13 from A2 and A3, respectively, resulting in a LOW output. The HIGH signals from A2 and A3 are inverted to present LOWs at input pins 1 and 2, disabling ACIA-D and PIA-C.

SECTION V

altair 680b UNIVERSAL I/O TROUBLESHOOTING

To control the rate of data flow in and out of ACIA-D, a baud rate generator is used. IC-A (zone D7) is a Programmable Bit Rate Generator, implementing a 2.4576 MHz crystal. The output of A pin 10 drives the Receive (RX) and Transmit (TX) clock inputs of ACIA-D pins 3 and 4 (zone D5).

The $\overline{IRQ}$ output of the ACIA, pin 7 (zone C5), and the PIAs, pins 37 and 38, are tied directly to the $\overline{IRQ}$ input of the MPU. The $\overline{IRQ}$ output of each port is an active LOW and is used to interrupt the MPU. This signal remains LOW as long as the cause of the interrupt is present and the appropriate interrupt ENABLE is set within the I/O ports.

The parallel data lines (PAØ through PA7 and PBØ through PB7) and control lines (CA1, CA2 and CB1, CB2) for PIAs C and B go directly to two 24-pin sockets, J3 and J4. Flat cable assemblies plug into these sockets and the 25-pin plug on the other side of the assembly is used for the I/O device.

ACIA-D has a Receive data (RX Data) input pin 2 (zone D5) and a Transmit data (TX Data) output pin 6 (zone C5). It also has Request To Send (RTS) output pin 5 (zone C5), $\overline{\text{Data Carrier Detect}}$ ($\overline{DCD}$) input pin 23 (zone C5), and $\overline{\text{Clear To Send}}$ ($\overline{CTS}$) input pin 24 (zone C5). These inputs and outputs can be configured for TTY 20 milliamp current loop, RS-232, or TTL. These configurations are determined by the switch settings S1 and S6. Refer to Table 3-3, ACIA-D Interface Selection (page 3-10), for the desired configuration.

3. With the cable sockets properly inserted, fold the excess flat cable once against the back panel slot. Secure the cable(s) with the metal plate supplied with the 680b back panel and the two #4-40 x 5/8" screws supplied with the Universal I/O Board as shown in Figure 4-E.

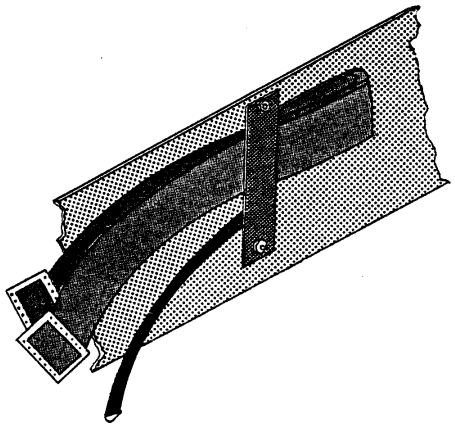


Figure 4-E. Final Cable Assembly Installation

3-5. SERIAL I/O INTERFACE OPERATION

The following two circuit descriptions apply to all TTY interface circuits.

The transmit distributor contacts inside the Teletype input to J1 (10-pin miniature plug) pins 2 and 1 (sheet 3 of 3, zone B5). These contacts are normally closed and allow current flow through R4 and R1 (zone B6). A negative voltage results at the anode of diode D1 (zone B6), and D1 will not conduct. The input pin 11 of E (zone B7) goes LOW via resistor R5. The output of E pin 10 is HIGH, providing an off condition or "marking" state to the port. When the contacts open due to data transmission, the anode of diode D1 is pulled to +16 volts, and D1 conducts. The input of E pin 11 goes to approximately +4 volts via the divider resistors, R1 and R4. Capacitor C1 is used for contact debounce. Thus, the output of E pin 10 is LOW and represents a transmitted data bit to the RX Data line pin 2 of ACIA-D (sheet 2 of 3, zone D5).

The ACIA port output line, TX Data (sheet 2 of 3, zone D5, pin 6), is normally HIGH, causing a LOW at the base of Q2 (sheet 3 of 3, zone C6). The emitter of Q2 is pulled to approximately 1.2 volts through diodes D7 and D8 (zone C6). This forward biases Q2 to cause current flow through resistor R20, Q2, and the device. This is the "marking" state. When a data bit is transmitted, the base of Q2 goes HIGH via resistor R15 (zone C7), turning Q2 off. This provides a very high impedance at the device and represents a valid data bit. The signal connections from the 10-pin miniature plug (J1) to the TTY device are shown in Table 3-4.

	1	2	3	4	5	6	7	8	9	10
TTY	Receive (No Polarity)		* Transmit(+)	Clear To Send (No Polarity)	Blank	Clear To Send (No Polarity)	$\overline{\text{DCD}}$ (No Polarity)		* Request To Send (+)	Ground

* The (+) side of Transmit and Request To Send is the collector of corresponding transistors.

Table 3-4.
Signal Connections
10-Pin Plug (J1) to TTY Device

4-5. Installation of More Than One Board (Figure 4-C)

1. If this board is being installed in the second or third position above the 680b Main Board, follow the same procedure for installation of the 100-pin edge connector onto the expander card (Paragraph 4-2).
2. After installation of the 100-pin connector, reinstall the expander card and the lower board(s) into the 680b Main Board.
3. Replace both #6-32 x 7/8" screws and #6 lockwashers that previously secured the lower board with a #6-32 x 7/8" threaded standoff and a #6 lockwasher.
4. Insert the card stab connector of the Universal I/O Board (silk-screen side up) into the 100-pin edge connector.
5. Secure the Universal I/O Board in place with a #6-32 x 3/8" screw and a #6 lockwasher into the top of each of the threaded standoffs.

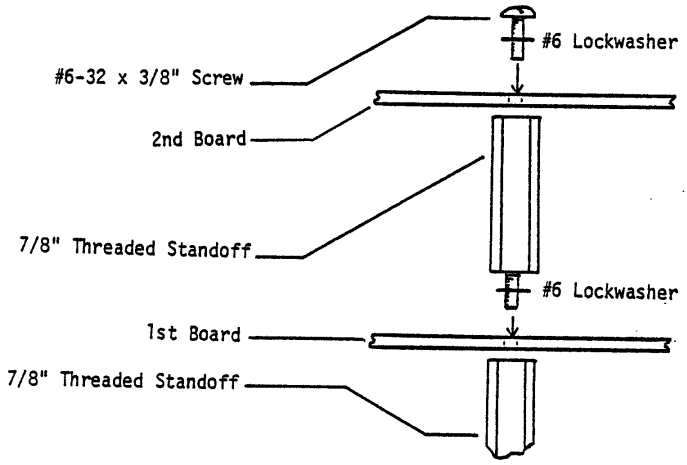


Figure 4-C. Installation of More Than One Board

The following circuit description apply to all RS-232 input and output circuits.

Whenever a logic one (approximately +16 volts) is received from the RS-232 device at the input of the ACIA, RX Data (sheet 2 of 3, zone D5, pin 2), R3 limits the current. D2 (sheet 3 of 3, zone B7) keeps the input of E pin 11 LOW and a TTL HIGH is present at the output of E pin 10 (zone B7). If a logic Ø (approximately +5 volts) is received from the RS-232 device, R3 again limits the current and D2 is reversed biased. The input of E pin 11 is HIGH and the output pin 10 is LOW.

Whenever a logic one is transmitted, transistor Q1 (zone D6) is reversed biased and a -16 volt level appears on the output line. If a logic Ø is transmitted, Q1 will conduct and approximately +5 volts is present on the output. Table 3-5 contains the signal connections for the 10-pin miniature plug (J1) to the RS-232 or TTL device.

	1	2	3	4	5	6	7	8	9	10
RS-232 and TTL		Receive	Transmit		Blank	Clear To Send		$\overline{\text{DCD}}$	Request To Send	Ground
Wire Color		orange	red			green		brown	yellow	black

Table 3-5.
Signal Connections
10-Pin Plug (J1) to RS-232 or TTL Device

4-1. INTRODUCTION

Before installing the 680b Universal I/O Board, refer to Section V, paragraph 5-2, and perform the visual checks. Make sure the 680-MB Expander Card is correctly installed according to the instructions enclosed with the card. The Universal I/O Board is connected to the expander card by means of a 100-pin edge connector and is installed horizontally above the 680b Main Board with two threaded standoffs. Install the 680b Universal I/O Board according to the following instructions.

4-2. Installation of 100-pin Edge Connector onto Expander Card (Figure 4-A)

1. Remove the expander card from the socket on the 680b Main Board.
2. Orient the 100-pin edge connector over the two rows of holes at the lowest unused position on the expander card.
3. Insert the connector pins into their respective holes. It may be necessary to guide some of the pins with the tip of a small screwdriver. Insure that the 100-pin connector is tight against the board and that all 100 pins are in their respective holes.
4. Secure the connector to the board with two #4-40 x 1/2" screws and two 4-40 nuts.
5. Solder each pin to the foil (bottom) side of the board. Insure that solder bridges are not formed.

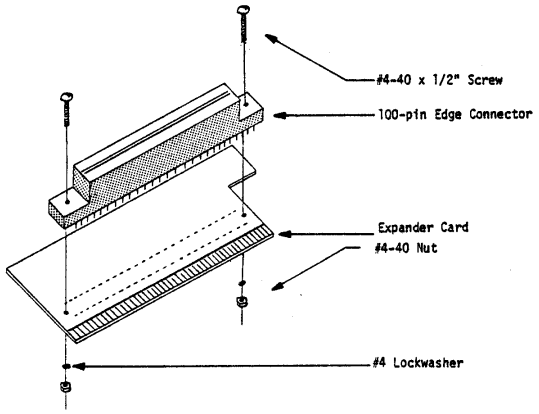


Figure 4-A. Installation of 100-pin Edge Connector onto Expander Card

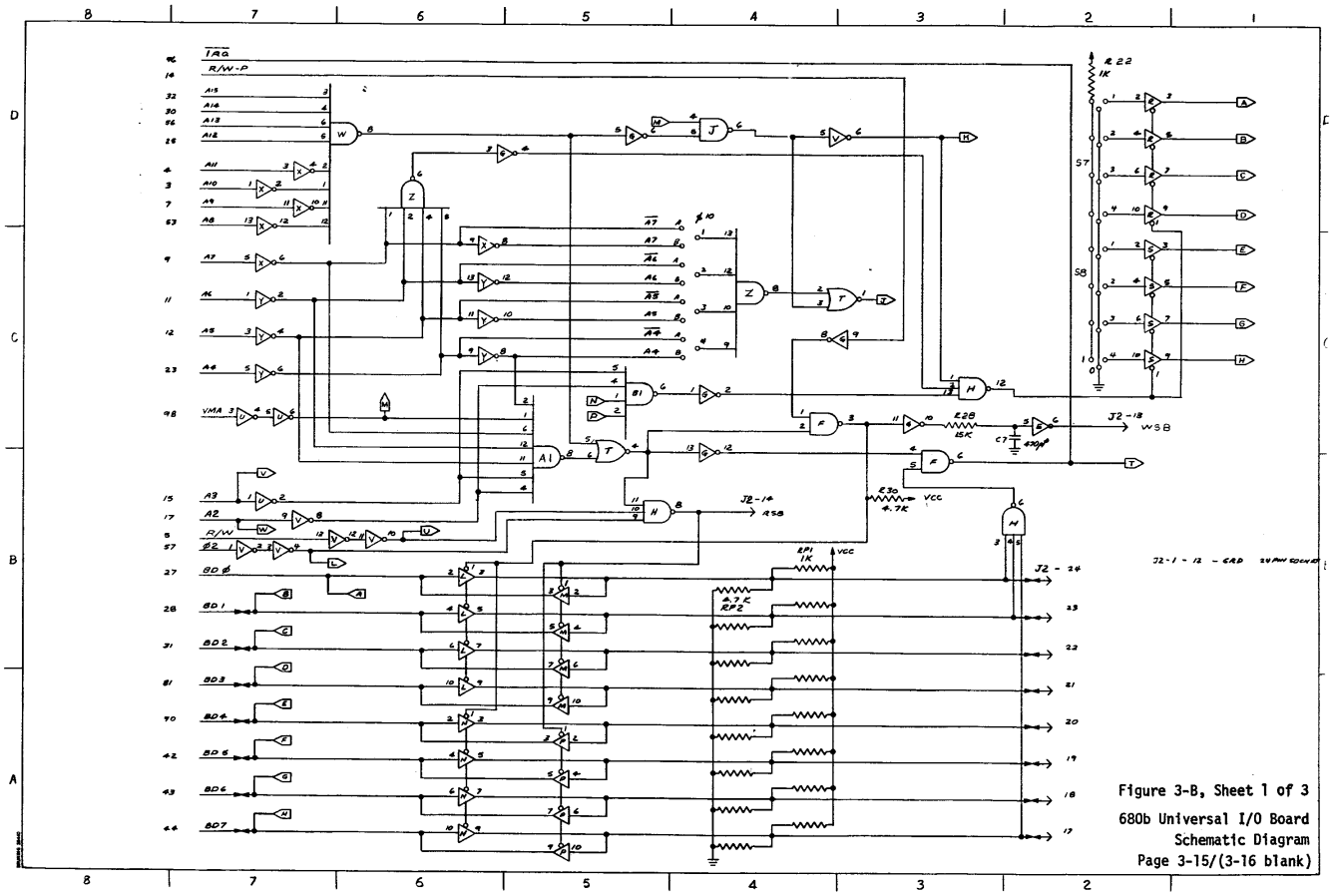


Figure 3-B, Sheet 1 of 3

680b Universal I/O Board
Schematic Diagram
Page 3-15/(3-16 blank)

SECTION IV

altair 680b UNIVERSAL I/O INSTALLATION

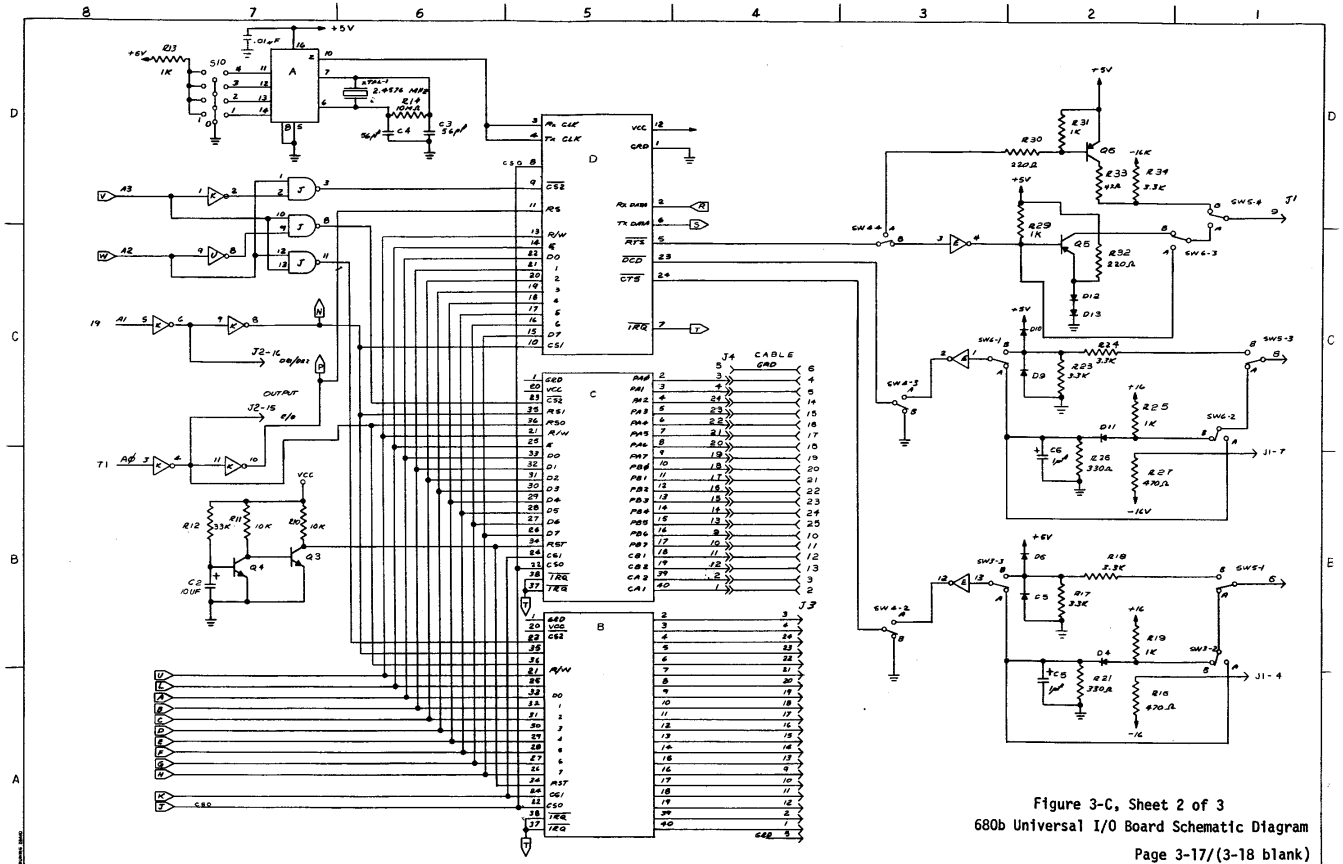
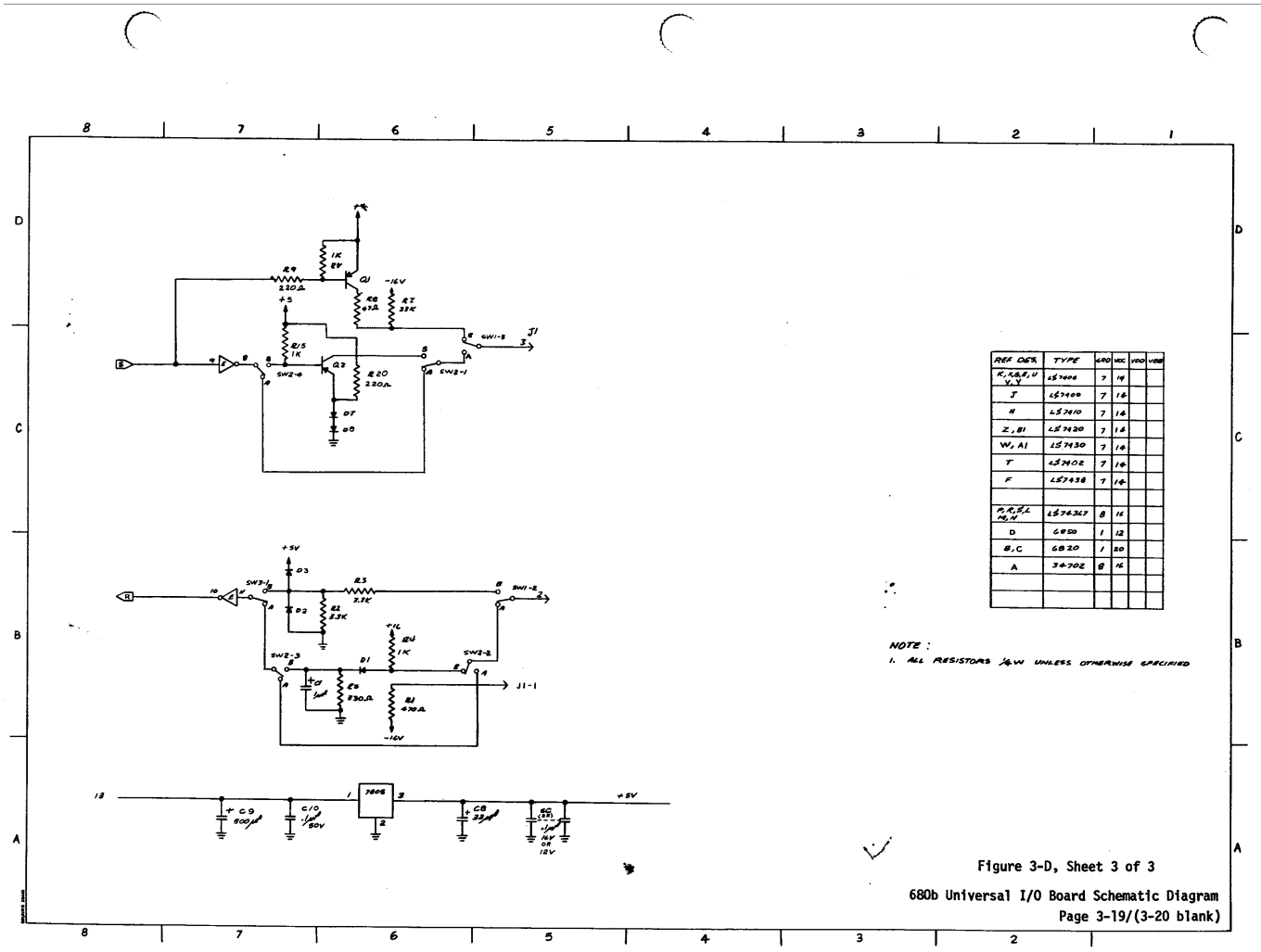


Figure 3-C, Sheet 2 of 3
680b Universal I/O Board Schematic Diagram

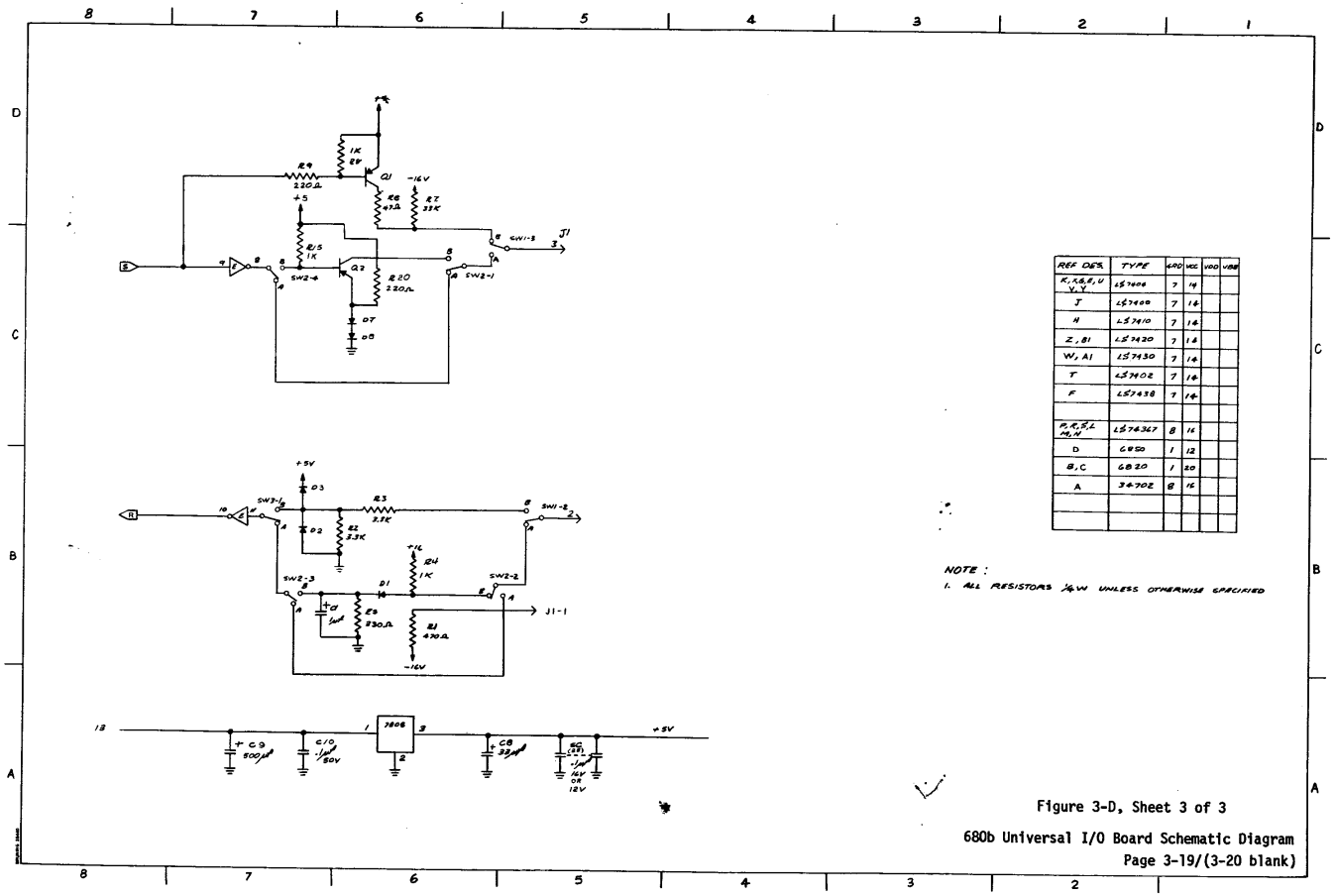


REF DES.	TYPE	GND	VCC	VDD	VBB
K,X&P,U V,Y	LS7008	7	14		
J	LS7400	7	14		
H	LS7410	7	14		
Z, B1	LS7420	7	14		
W, A1	LS7430	7	14		
T	LS7402	7	14		
F	LS7438	7	14		
R,S,L N5,N	LS74367	8	16		
D	6850	1	12		
B,C	6820	1	20		
A	34702	8	16		

NOTE:
1. ALL RESISTORS ¼W UNLESS OTHERWISE SPECIFIED

Figure 3-D, Sheet 3 of 3

680b Universal I/O Board Schematic Diagram



REF DES	TYPE	GND	VCC	VDD	VBB
K,K6,K,U V,Y	LS7408	7	14		
J	LS7400	7	14		
H	LS7410	7	14		
Z, B1	LS7420	7	14		
W, A1	LS7430	7	14		
T	LS7402	7	14		
F	LS7438	7	14		
P,R,S,L M,N	LS74367	8	16		
D	6850	1	12		
B,C	6820	1	20		
A	34702	8	16		

NOTE :
1. ALL RESISTORS ¼W UNLESS OTHERWISE SPECIFIED

Figure 3-D, Sheet 3 of 3

680b Universal I/O Board Schematic Diagram

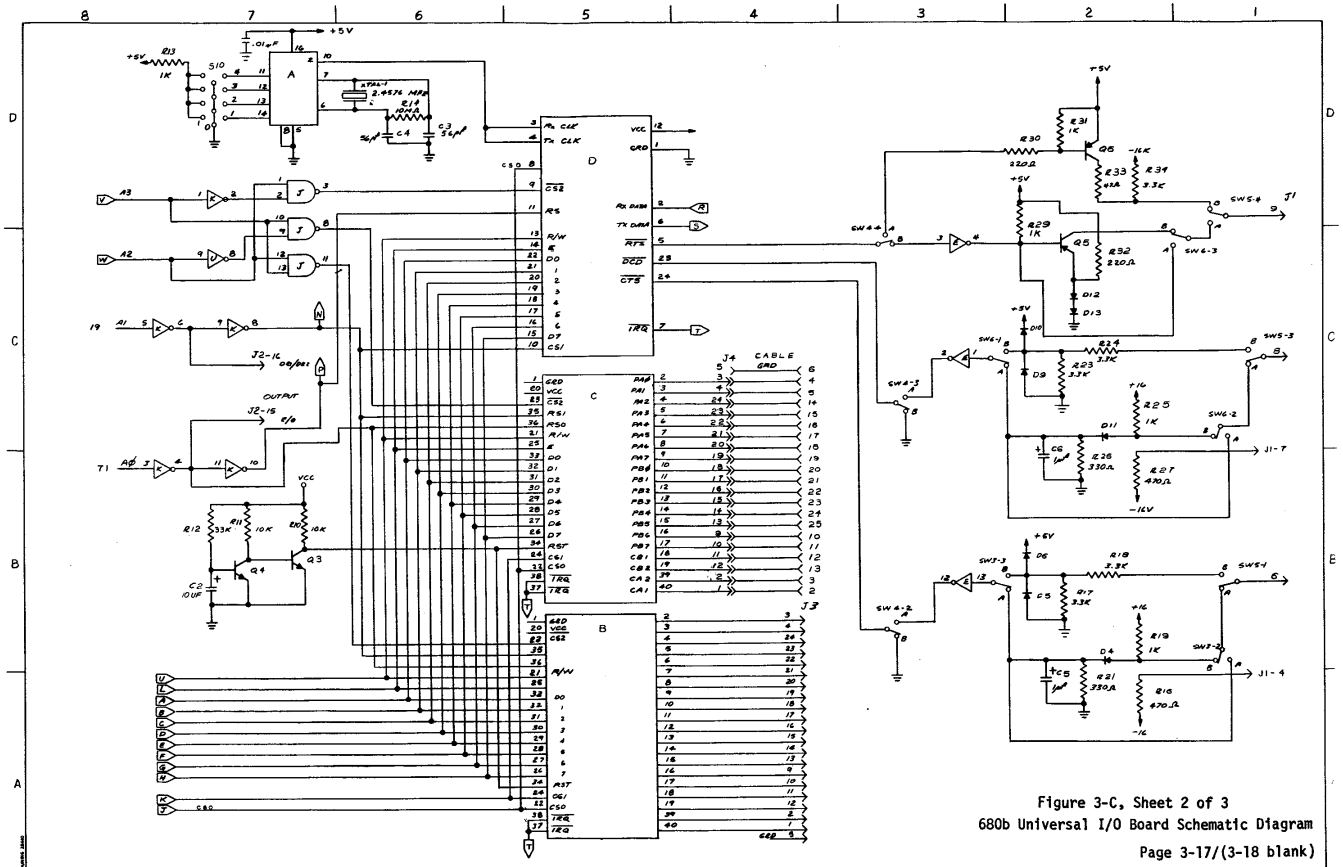


Figure 3-C, Sheet 2 of 3
680b Universal I/O Board Schematic Diagram

SECTION IV

altair 680b UNIVERSAL I/O INSTALLATION

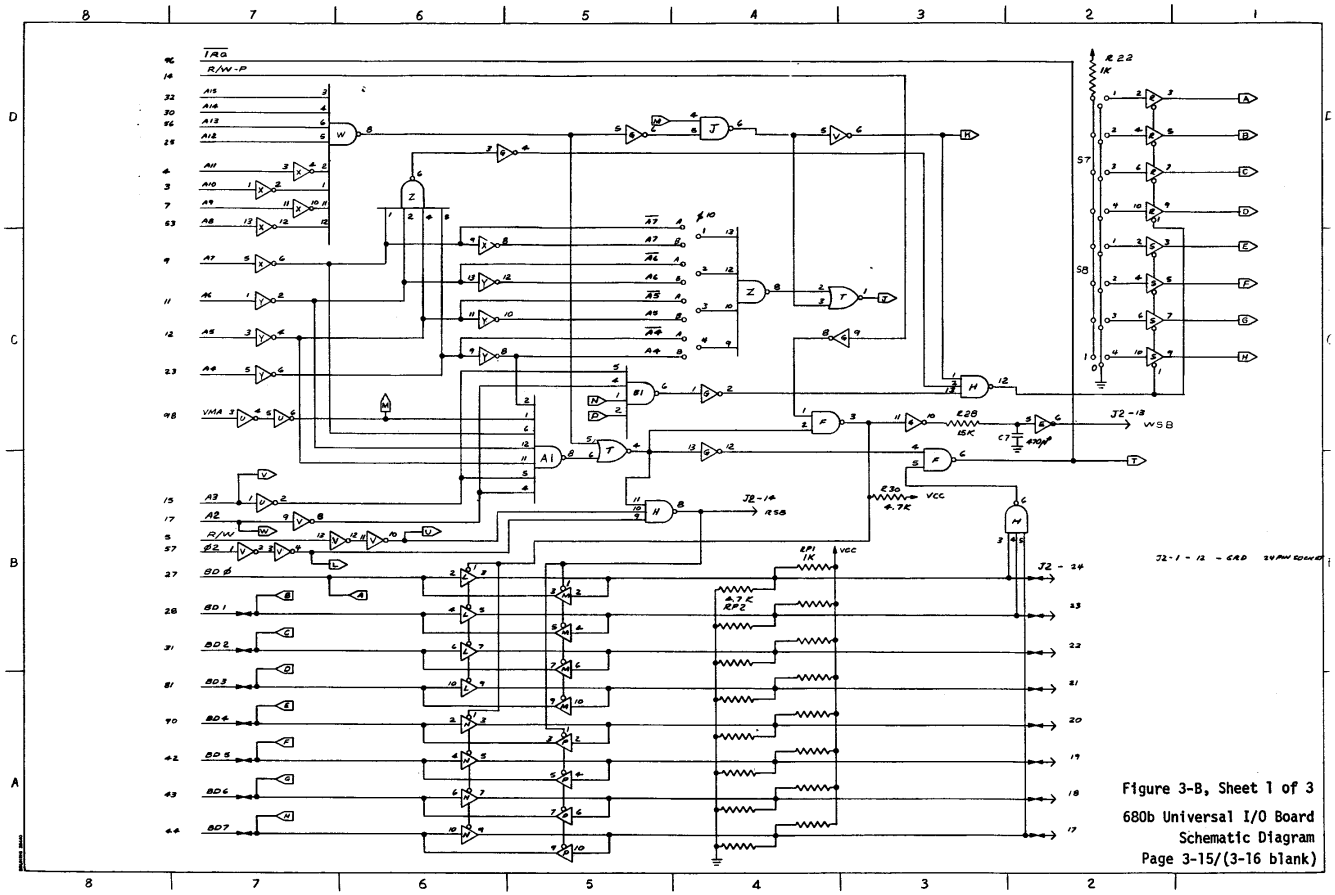


Figure 3-B, Sheet 1 of 3

680b Universal I/O Board
Schematic Diagram
Page 3-15/(3-16 blank)

4-1. INTRODUCTION

Before installing the 680b Universal I/O Board, refer to Section V, paragraph 5-2, and perform the visual checks. Make sure the 680-MB Expander Card is correctly installed according to the instructions enclosed with the card. The Universal I/O Board is connected to the expander card by means of a 100-pin edge connector and is installed horizontally above the 680b Main Board with two threaded standoffs. Install the 680b Universal I/O Board according to the following instructions.

4-2. Installation of 100-pin Edge Connector onto Expander Card (Figure 4-A)

1. Remove the expander card from the socket on the 680b Main Board.
2. Orient the 100-pin edge connector over the two rows of holes at the lowest unused position on the expander card.
3. Insert the connector pins into their respective holes. It may be necessary to guide some of the pins with the tip of a small screwdriver. Insure that the 100-pin connector is tight against the board and that all 100 pins are in their respective holes.
4. Secure the connector to the board with two #4-40 x 1/2" screws and two 4-40 nuts.
5. Solder each pin to the foil (bottom) side of the board. Insure that solder bridges are not formed.

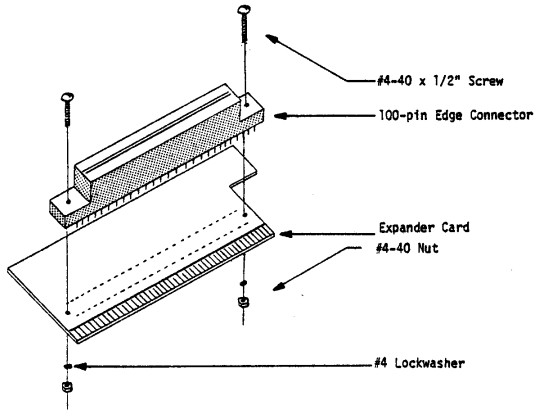


Figure 4-A. Installation of 100-pin Edge Connector onto Expander Card

The following circuit description apply to all RS-232 input and output circuits.

Whenever a logic one (approximately +16 volts) is received from the RS-232 device at the input of the ACIA, RX Data (sheet 2 of 3, zone D5, pin 2), R3 limits the current. D2 (sheet 3 of 3, zone B7) keeps the input of E pin 11 LOW and a TTL HIGH is present at the output of E pin 10 (zone B7). If a logic Ø (approximately +5 volts) is received from the RS-232 device, R3 again limits the current and D2 is reversed biased. The input of E pin 11 is HIGH and the output pin 10 is LOW.

Whenever a logic one is transmitted, transistor Q1 (zone D6) is reversed biased and a -16 volt level appears on the output line. If a logic Ø is transmitted, Q1 will conduct and approximately +5 volts is present on the output. Table 3-5 contains the signal connections for the 10-pin miniature plug (J1) to the RS-232 or TTL device.

	1	2	3	4	5	6	7	8	9	10
RS-232 and TTL		Receive	Transmit		Blank	Clear To Send		$\overline{\text{DCD}}$	Request To Send	Ground
Wire Color		orange	red			green		brown	yellow	black

Table 3-5.
Signal Connections
10-Pin Plug (J1) to RS-232 or TTL Device

4-5. Installation of More Than One Board (Figure 4-C)

1. If this board is being installed in the second or third position above the 680b Main Board, follow the same procedure for installation of the 100-pin edge connector onto the expander card (Paragraph 4-2).
2. After installation of the 100-pin connector, reinstall the expander card and the lower board(s) into the 680b Main Board.
3. Replace both #6-32 x 7/8" screws and #6 lockwashers that previously secured the lower board with a #6-32 x 7/8" threaded standoff and a #6 lockwasher.
4. Insert the card stab connector of the Universal I/O Board (silk-screen side up) into the 100-pin edge connector.
5. Secure the Universal I/O Board in place with a #6-32 x 3/8" screw and a #6 lockwasher into the top of each of the threaded standoffs.

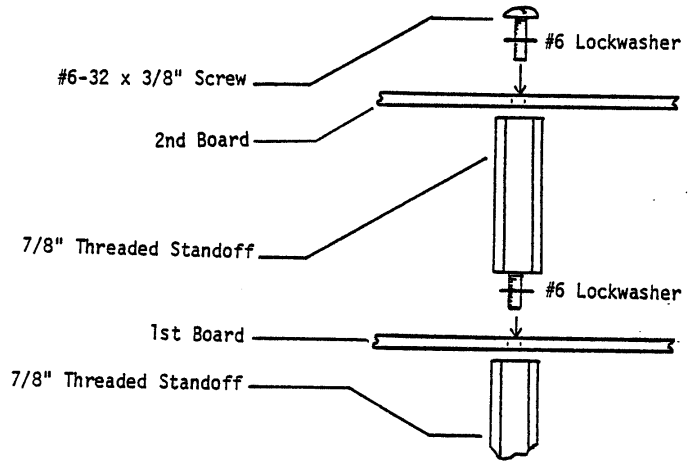


Figure 4-C. Installation of More Than One Board

3-5. SERIAL I/O INTERFACE OPERATION

The following two circuit descriptions apply to all TTY interface circuits.

The transmit distributor contacts inside the Teletype input to J1 (10-pin miniature plug) pins 2 and 1 (sheet 3 of 3, zone B5). These contacts are normally closed and allow current flow through R4 and R1 (zone B6). A negative voltage results at the anode of diode D1 (zone B6), and D1 will not conduct. The input pin 11 of E (zone B7) goes LOW via resistor R5. The output of E pin 10 is HIGH, providing an off condition or "marking" state to the port. When the contacts open due to data transmission, the anode of diode D1 is pulled to +16 volts, and D1 conducts. The input of E pin 11 goes to approximately +4 volts via the divider resistors, R1 and R4. Capacitor C1 is used for contact debounce. Thus, the output of E pin 10 is LOW and represents a transmitted data bit to the RX Data line pin 2 of ACIA-D (sheet 2 of 3, zone D5).

The ACIA port output line, TX Data (sheet 2 of 3, zone D5, pin 6), is normally HIGH, causing a LOW at the base of Q2 (sheet 3 of 3, zone C6). The emitter of Q2 is pulled to approximately 1.2 volts through diodes D7 and D8 (zone C6). This forward biases Q2 to cause current flow through resistor R20, Q2, and the device. This is the "marking" state. When a data bit is transmitted, the base of Q2 goes HIGH via resistor R15 (zone C7), turning Q2 off. This provides a very high impedance at the device and represents a valid data bit. The signal connections from the 10-pin miniature plug (J1) to the TTY device are shown in Table 3-4.

	1 2	3	4	5	6	7 8	9	10
TTY	Receive (No Polarity)	* Transmit(+)	Clear To Send (No Polarity)	Blank	Clear To Send (No Polarity)	$\overline{\text{DCD}}$ (No Polarity)	* Request To Send (+)	Ground

* The (+) side of Transmit and Request To Send is the collector of corresponding transistors.

Table 3-4.
Signal Connections
10-Pin Plug (J1) to TTY Device

3. With the cable sockets properly inserted, fold the excess flat cable once against the back panel slot. Secure the cable(s) with the metal plate supplied with the 680b back panel and the two #4-40 x 5/8" screws supplied with the Universal I/O Board as shown in Figure 4-E.

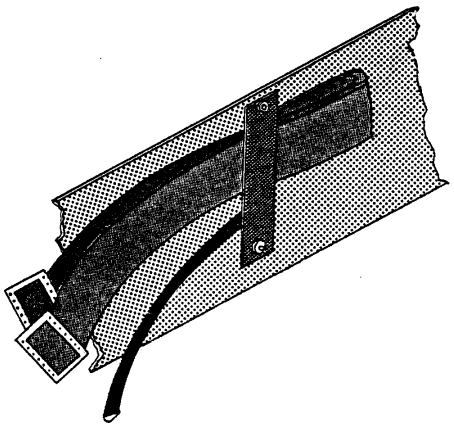


Figure 4-E. Final Cable Assembly Installation

To control the rate of data flow in and out of ACIA-D, a baud rate generator is used. IC-A (zone D7) is a Programmable Bit Rate Generator, implementing a 2.4576 MHz crystal. The output of A pin 10 drives the Receive (RX) and Transmit (TX) clock inputs of ACIA-D pins 3 and 4 (zone D5).

The $\overline{IRQ}$ output of the ACIA, pin 7 (zone C5), and the PIAs, pins 37 and 38, are tied directly to the $\overline{IRQ}$ input of the MPU. The $\overline{IRQ}$ output of each port is an active LOW and is used to interrupt the MPU. This signal remains LOW as long as the cause of the interrupt is present and the appropriate interrupt ENABLE is set within the I/O ports.

The parallel data lines (PAØ through PA7 and PBØ through PB7) and control lines (CA1, CA2 and CB1, CB2) for PIAs C and B go directly to two 24-pin sockets, J3 and J4. Flat cable assemblies plug into these sockets and the 25-pin plug on the other side of the assembly is used for the I/O device.

ACIA-D has a Receive data (RX Data) input pin 2 (zone D5) and a Transmit data (TX Data) output pin 6 (zone C5). It also has Request To Send (RTS) output pin 5 (zone C5), $\overline{\text{Data Carrier Detect}}$ ($\overline{DCD}$) input pin 23 (zone C5), and $\overline{\text{Clear To Send}}$ ($\overline{CTS}$) input pin 24 (zone C5). These inputs and outputs can be configured for TTY 20 milliamp current loop, RS-232, or TTL. These configurations are determined by the switch settings S1 and S6. Refer to Table 3-3, ACIA-D Interface Selection (page 3-10), for the desired configuration.

SECTION V

altair 680b UNIVERSAL I/O TROUBLESHOOTING

The CS1 signal line for ACIA-D pin 10 (sheet 2 of 3, zone C5) is controlled by address line A1. A1 must be HIGH for ACIA-D to be selected since the signal is double inverted to the input pin 10. Line K is tied to CS1 of both parallel ports at pins 24 and must be HIGH at the same time CSØ is HIGH. This signal was derived earlier.

Addresses A3 (zone D8) and A2 (zone C8) are the inputs for a $\overline{CS2}$ decoding circuit. Only one of the outputs of NAND gate J (zone D7 and C7) should be LOW, enabling the particular port being used. The remaining two outputs of J should be HIGH, disabling the other ports. If the output of J pin 3 (zone D7) is LOW (ACIA-D selected), the input pins 1 and 2 are HIGH. Address line 2 is HIGH and this signal is presented to pin 1. Address line 3 is inverted HIGH and goes to pin 2. These two input signals give the desired LOW at the output of NAND gate J. If A3 is LOW, this signal goes directly to the inputs of NAND gates J pins 10 and 13, disabling both gates. If PIA-C (location FOO8) is selected, the output of J pin 8 (zone C7) is LOW. Input pins 10 and 9 must be HIGH for pin 8 to be LOW. This is assuming that S9 is positioned to $\overline{A7}$, $\overline{A6}$, $\overline{A5}$, and $\overline{A4}$. A HIGH signal from A3 goes directly to pin 10. A2 is LOW and inverted to present a HIGH to the input pin 9. The LOW signal from A2 goes directly to the input pins 1 and 12 of J, disabling ACIA-D and PIA-B. If PIA-B is to be enabled (location FOOC), pin 11 (zone C7) should be LOW, and the other two output pins 3 and 8 should be HIGH. A HIGH signal goes directly to input pins 12 and 13 from A2 and A3, respectively, resulting in a LOW output. The HIGH signals from A2 and A3 are inverted to present LOWs at input pins 1 and 2, disabling ACIA-D and PIA-C.

5-1. INTRODUCTION

Section V is designed to aid in the location of malfunctions that could be encountered after the Altair 680b Universal I/O Board is installed in the 680b computer. Before installation of the board, it should be visually inspected according to the visual inspection check list. A power supply check, preliminary check, and general procedures for troubleshooting TTL logic are included to insure that the board is functioning properly. Since the board is mainly software controlled, programs for troubleshooting the ACIA, PIAs and sense switches are presented to assist in the location of possible failures.

> **WARNING**
> Always disconnect power when removing the board, cutting or resoldering PC lands, and removing or installing ICs.

5-2. VISUAL INSPECTION CHECK LIST

Before the 680b Universal I/O Board is installed, it is important to check the component assembly, etching of lands, and switch settings. Although the board should be assembled correctly, an extensive inspection may eliminate possible malfunctions.

1. General

   Carefully examine the board for the following:

   a. leads that have not been soldered
   b. solder bridges
   c. cold solder connections
   d. errors such as hairline opens in lands

2. Component Check

   Using the silkscreen diagram (Figure 5-A, page 5-2) as a guide, check the following:

   a. proper polarity of capacitors
   b. proper polarity of diodes
   c. correct color codes on all resistors
   d. proper pin placement and good solder connections
   e. proper placement of all components

When FO for the upper address lines is selected, a LOW signal is presented to the input of NOR gate T pin 5 (sheet 1 of 3, zone C5). A LOW signal also goes to pin 6 from the output of NAND gate A1 pin 8 (zone B5). For A1 to have a LOW output, all the inputs must be HIGH. Address lines A7, A6, A5, A3, and A2 are LOW and inverted HIGH to the inputs of A1 pins 6, 12, 11, 5, and 4. A4 is double inverted to the input of A1 pin 2 and must be HIGH for the proper condition to exist. VMA is tied to pin 1 of A1. With VMA valid and the other input pins of A1 HIGH, the output pin 8 will be LOW.

The LOW signals at the input pins 5 and 6 (zone C5) enable pin 4 of NOR gate T HIGH. This signal goes to NAND gate H pin 11 (zone B5), enabling the gate for double inverted R/W and Ø clock signals. A LOW going pulse, 1 microsecond wide with a 20 microsecond period, occurs at the output pin 8 when data or status is being read from the device. This LOW going pulse is the READ STROBE and goes to J2 which is a 24-pin socket. A flat cable assembly plugs into this socket. The 25-pin plug on the other side of the assembly is used for the interface. The READ STROBE signal enables pins 1 (zone B5 and A5) of Tri-State drivers M and P, allowing data to be transferred from the device to the data bus.

The HIGH signal from NOR gate T pin 4 is also present at the input of NAND gate F pin 2 (zone C4) and inverted to F pin 4 (zone B3). R/W-P (zone D7) is inverted HIGH to F pin 1, enabling the output of F pin 3 (zone C3) LOW. There is a delay on this line and it is used to insure that Write data is valid when it is written into the device. The WRITE STROBE occurs at the output of E pin 6 (zone C2) and is a LOW going pulse with an approximate width of 1 microsecond and a period of 3 milliseconds. This signal goes directly to socket J2. Write data becomes valid 200 nanoseconds (maximum) after Data Bus Enable (DBE), which is tied directly to Ø2 of the system clock, is active HIGH.

3. Address Switch Settings

   Check to see that all the switch settings are set according to needs.

   a. Refer to Table 3-2, S9 Address Selection (page 3-3), to insure that the board is strapped to the proper locations for the ACIA and the PIAs.
   b. Make sure that your program uses the correct addresses.
   c. If the ACIA serial interface is used, insure that the proper interface is selected on S1 through S6. Refer to Table 3-3, ACIA-D Interface Selection (page 3-10).

5-3. POWER SUPPLY CHECK

After installation of the Universal I/O Board, a power supply check is necessary to insure that the proper voltage levels are being supplied to the various ICs. Follow the instructions in Table 5-1 (page 5-9), Power Supply Check.

5-4. PRELIMINARY CHECK

Upon completion of the power supply check, leave the machine on and place it in the Halt mode to check the address and data lines for shorts and opens.

1. The 16 address switches on the 680b front panel should be in the down position initially. Place all the switches in the up position and observe that all the address LEDs are on. Return all the switches to the down position and observe that all the LEDs go off.
2. Next, place each switch in the up position individually. Observe that the corresponding LED is on. After all the switches are up, return them individually to the down position and each LED should go off.
3. Another way of checking each address line is by toggling each address switch individually and checking the signal toggle while tracing it through the logic.

Table 3-2. S9 Address Selection

PIA - B	PIA - C	ACIA - D	S9 Positions A7	A6	A5	A4
F00C - F00F	F008 - F00B	F006 - F007	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
F01C - F01F	F018 - F01B	F016 - F017	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4
F02C - F02F	F028 - F02B	F026 - F027	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$
F03C - F03F	F038 - F03B	F036 - F037	$\overline{A7}$	$\overline{A6}$	A5	A4
F04C - F04F	F048 - F04B	F046 - F047	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$
F05C - F05F	F058 - F05B	F056 - F057	$\overline{A7}$	A6	$\overline{A5}$	A4
F06C - F06F	F068 - F06B	F066 - F067	$\overline{A7}$	A6	A5	$\overline{A4}$
F07C - F07F	F078 - F07B	F076 - F077	$\overline{A7}$	A6	A5	A4
F08C - F08F	F088 - F08B	F086 - F087	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
F09C - F09F	F098 - F09B	F096 - F097	A7	$\overline{A6}$	$\overline{A5}$	A4
F0AC - F0AF	F0A8 - F0AB	F0A6 - F0A7	A7	$\overline{A6}$	A5	$\overline{A4}$
F0BC - F0BF	F0B8 - F0BB	F0B6 - F0B7	A7	$\overline{A6}$	A5	A4
F0CC - F0CF	F0C8 - F0CB	F0C6 - F0C7	A7	A6	$\overline{A5}$	$\overline{A4}$
F0DC - F0DF	F0D8 - F0DB	F0D6 - F0D7	A7	A6	$\overline{A5}$	A4
F0EC - F0EF	F0E8 - F0EB	F0E6 - F0E7	A7	A6	A5	$\overline{A4}$
F0FC - F0FF	F0F8 - F0FB	F0F6 - F0F7	A7	A6	A5	A4

the probable cause is a defective input at one of the elements that the output feeds. Isolate each input in turn by disconnecting it from the external circuitry.

c. If an input is between .8 volts and 2 volts, check continuity back to the driving output.

5-6. ACIA TROUBLESHOOTING

1. Since the 680b Universal I/O Board is mainly software controlled, possible failures may be due to software bugs. Program 5-I is for ACIA serial port echo.
   a. Be sure the board is strapped at the lowest position.
   b. Program 5-I may be changed for the particular terminal being used (refer to terminal manual). The program also works with TTY.
   c. Using the 680b monitor M and N commands, enter all underlined characters in Program 5-I.

Program 5-I. ACIA Serial Port Echo

.M	ØØØØ	86	.N	ØØØB	FØ	.N	ØØ16	57
.N	ØØØ1	03	.N	ØØØC	Ø6	.N	ØØ17	57
.N	ØØØ2	B7	.N	ØØØD	47	.N	ØØ18	24
.N	ØØØ3	FØ	.N	ØØØE	24	.N	ØØ19	F9
.N	ØØØ4	Ø6	.N	ØØØF	FA	.N	ØØ1A	B7
.N	ØØØ5	86	.N	ØØ1Ø	B6	.N	ØØ1B	FØ
.N	ØØØ6	B1*	.N	ØØ11	FØ	.N	ØØ1C	Ø7
.N	ØØØ7	B7	.N	ØØ12	Ø7	.N	ØØ1D	2Ø
.N	ØØØ8	FØ	.N	ØØ13	F6	.N	ØØ1E	EB
.N	ØØØ9	Ø6	.N	ØØ14	FØ	.J	ØØØØ	
.N	ØØØA	B6	.N	ØØ15	Ø6			

*NOTE: B1 sets up 8 data bits, 2 stop bits, Receive-Transmit interrupts enabled, and ÷ 16 mode.

3-1. GENERAL

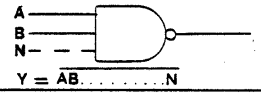
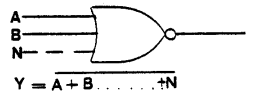
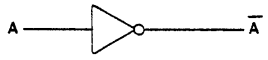
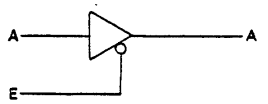
Section III provides a detailed theory explanation of the 680b Universal I/O Board circuitry, including a basic description of the logic symbols used in the Universal I/O schematics.

3-2. LOGIC CIRCUITS

The detailed schematics of the 680b Universal I/O Board (sheets 1 of 3, 2 of 3, and 3 of 3) are drawn to aid in determining signal direction and tracing. A solid arrow (→) on the signal line indicates direction.

The logic circuits used in the Universal I/O schematics are presented in Table 3-1. The table provides the functional name, symbolic representation, and brief description of each logic circuit. Where applicable, a truth table is furnished to aid in understanding circuit operation. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

Table 3-1. Symbol Definitions

NAME	LOGIC SYMBOL	DESCRIPTION
NAND gate		The NAND gate performs one of the common logic functions. All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output.
NOR gate		The NOR gate performs one of the common logic functions. Any of the inputs needs to be enabled (HIGH) to produce the desired (LOW) output.
Inverter		The inverter is an amplifier whose output is the opposite state of the input.
Non-Inverting Bus Driver		The non-inverting bus driver is an amplifier whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input.

b. With these connections made, th PA data lines are shorted to the PB data lines. CA1 is tied to CB2 and CA2 is tied to CB1. The connections allow the parallel port echo program (Program 5-II) to be run by outputting data on the PB data lines and inputting data on the PA data lines.

c. Using the 680b monitor M and N commands, enter all underlined characters in Program 5-II.

Program 5-II. PIA Parallel Port Echo

.M	ØØØØ	4F	.N	ØØØD	0B or 0F	.N	ØØ1A	F0
.N	ØØØ1	B7	.N	ØØØE	86	.N	ØØ1B	0B or 0F
.N	ØØØ2	F0	.N	ØØØF	04	.N	ØØ1C	F1
.N	ØØØ3	08 or 0C	.N	ØØ1Ø	B7	.N	ØØ1D	F0
.N	ØØØ4	B7	.N	ØØ11	F0	.N	ØØ1E	09 or 0D
.N	ØØØ5	F0	.N	ØØ12	08 or 0C	.N	ØØ1F	27
.N	ØØØ6	09 or 0D	.N	ØØ13	B7	.N	ØØ2Ø	F5
.N	ØØØ7	B7	.N	ØØ14	F0	.N	ØØ21	7E
.N	ØØØ8	F0	.N	ØØ15	0A or 0E	.N	ØØ22	FF
.N	ØØØ9	0A or 0E	.N	ØØ16	BD	.N	ØØ23	AB
.N	ØØØA	43	.N	ØØ17	FF	.J	ØØØØ	
.N	ØØØB	B7	.N	ØØ18	00			
.N	ØØØC	F0	.N	ØØ19	F7			

d. The program should echo any character entered through the 680b Main Board ACIA. If there is an error whenever a character is entered, the program will jump back to the system monitor and print out a dot.

e. Halt the machine and follow the instructions in Table 5-3 (page 5-12). The table assumes the board is strapped at the lowest location. The VMA must be jumpered HIGH at pin 3 of IC-U.

SECTION III

altair 680b UNIVERSAL I/O THEORY OF OPERATION CIRCUITRY

Table 5-1. POWER SUPPLY CHECK

Step	Settings and Instructions	Correct Readings	If Incorrect
1	Check +9v UNREG at bus pin 13, +16v at bus pin 76, -16v UNREG at bus pin 72	Should be about +9v; +16v and -16v, respectively	Problem probably with input tramsformer (refer to 680b manual or 680b-MB)
2	Check +5v REG at output side of VR1 or check VCC on various ICs (pin 14 for 14-pin ICs and pin 16 for 16-pin ICs)	Should be a constant +5v with a ±5% tolerance	Check VR1 or check for possible shorts

2-6. ACIA Status Register*

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when Register Select (RS) is LOW and R/W is HIGH. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit Ø - RDRF indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. $\overline{\text{Data Carrier Detect}}$ being HIGH also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 - The TDRE bit being set HIGH indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The LOW state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

$\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), Bit 2 - The $\overline{\text{DCD}}$ bit will be HIGH when the $\overline{\text{DCD}}$ input from a modem has gone HIGH to indicate that a carrier is not present. This bit going HIGH causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains HIGH after the $\overline{\text{DCD}}$ input is returned LOW until cleared by first reading the Status Register and then the Data Register or until a Master Reset occurs. If the $\overline{\text{DCD}}$ input remains HIGH after Read Status and Read Data or Master Reset have occurred, the $\overline{\text{DCD}}$ status bit remains HIGH and will follow the $\overline{\text{DCD}}$ input.

$\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$), Bit 3 - The $\overline{\text{CTS}}$ bit indicates the state of the $\overline{\text{CTS}}$ input from a modem. A LOW $\overline{\text{CTS}}$ indicates that there is a $\overline{\text{Clear To Send}}$ from the modem. In the HIGH state, the Transmit Data Register Empty bit is inhibited and the $\overline{\text{Clear To Send}}$ status bit will be HIGH. Master Reset does not affect the $\overline{\text{Clear To Send}}$ status bit.

5	Toggle address switch AØ	RS (pin 11 of ACIA-D) should toggle along with AØ. AØ = RS	If RS (zone D5) does not toggle or toggles but is inverted from AØ, then IC-K (zone B7) is probably defective.
6	"	ENABLE pin 14 should be Ø2 clock (500 KHz). If it is correct, proceed to Step 7.	If Ø2 is missing, IC-V (sheet 1 of 3, zone B7) is probably defective.
7	"	R/W pin 13 (sheet 2 of 3, zone C5) is normally HIGH until deposit switch is actuated. Then it drops LOW for approximately 2.5 msecs. If correct, proceed to Step 8.	If signal is missing or inverted, IC-V (sheet 1 of 3, zone B6) is probably defective.
8	Deposit various bit patterns in memory	Data lines on ACIA-D (pins 22 through 15) should have the same pattern on them as the Data LEDs. If correct, proceed to Step 9.	If pattern differs, check the lines for shorts or opens.
9	Check pin 10 of IC-A	Baud Rate Clock frequency will be 16 times higher than the selected baud rate.	If clock is missing, IC-A (sheet 2 of 3, zone D7) or associated components are probably defective. If baud rate is incorrect, double check baud rate selected.

In order to choose any one of 5 additional baud rates, select the baud rate from Table 2-10 and set S10, using the ÷ 64 mode (data bits 1 and Ø are equal to 1 and Ø, respectively). Note that the selected baud rate is four times larger than the desired baud rate. Due to the internal structure of the ACIA, it is not possible to use the ÷ 1 clock because some means of external synchronization must be used.

DESIRED BAUD RATE	SELECTED BAUD RATE
27.5	110
37.5	150
75.0	300
450	1800
600	2400

Table 2-10. Additional Baud Rate Selection

The next three bits of the Control Register determine word length, parity, and the number of stop bits. Consult the I/O device manual for the configuration required and set the bits according to Table 2-11.

DATA BIT			FUNCTION		
4	3	2	# of Data Bits	# of Stop Bits	Parity
0	0	0	7	2	Even
0	0	1	7	2	Odd
0	1	0	7	1	Even
0	1	1	7	1	Odd
1	0	0	8	2	None
1	0	1	8	1	None
1	1	0	8	1	Even
1	1	1	8	1	Odd

Table 2-11. Transmission Control Bits

		RSØ = Logic 1	If RSØ = Logic Ø, IC-K pins 3 and 4 (sheet 2 of 3, zone C7) are probably defective or address line AØ is HIGH. If AØ switch is toggled, RSØ will be LOW when AØ is HIGH and HIGH when AØ is LOW.
3	Check ENABLE pins 25 of IC-B and IC-C	Ø2 clock (500KHz)	If missing, IC-V pins 1 and 2 and 3 and 4 (sheet 1 of 3, zone B7) are probably defective.
4	Check R/W line pins 21 of IC-B and IC-C	Normally HIGH until deposit switch is actuated and then it drops LOW. (See 680b manual for R/W timing)	If always LOW or always HIGH, IC-V pins 11, 10, and 13, 12 (sheet 1 of 3, zone B6) are probably defective.
5	Check Reset pins 34 of IC-B and IC-C	Should be +5 volts	If LOW, Q3 or Q4 (sheet 2 of 3, zone B7) are probably defective.
6	Deposit various bit patterns in memory	Data lines DØ through D7 (pins 33 through 26) should have the same bit pattern as shown on the Data LEDs	If pattern differs, check the lines for shorts or opens.

2-4. SERIAL PORT (ACIA) SELECTION

The 680b Universal I/O Board utilizes a 6850 Asynchronous Communications Interface Adapter (ACIA). The ACIA allows serial data to be taken in on its receive line and transfers the data onto the data bus, or data can be entered from the data bus into the ACIA and sent out the transmit data line in serial form.

The ACIA has three chip select inputs, CSØ, CS1, and $\overline{CS2}$, which are used in the selection of the ACIA. It also has a Register Select (RS) input, controlled by address line AØ, that can select between the different internal registers. The ENABLE signal is used for internal interrupt control and the timing of Control/Status changes. Since all data transfers take place during Ø2 of the system clock, it is used as the ENABLE signal. The R/W signal determines the direction of data flow.

2-5. ACIA Control Register

The ACIA has an 8-bit Control Register that allows port configuration under software control. Each bit is defined in Table 2-7.

7	6	5	4	3	2	1	0
In Interrupt	Out Interrupt		Transmission Bits			Clock Divide And Reset	

NOTE: Data Bit LOW = 0
Data Bit HIGH = 1

Table 2-7. ACIA Control Register

The first two data bits, Ø and 1, control the internal clock divide circuit and the Master Reset as shown in Table 2-8.

BIT 1	BIT Ø	FUNCTION
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Table 2-8. Control Bits for Internal Clock Divide and Master Reset

5	"	Pin 13 of H should be HIGH	If pin 13 is LOW, monitor output pin 6 of B1 (sheet 1 of 3, zone C5). If pin 6 is LOW, replace IC-G (zone C4). If pin 6 is HIGH, check input pins 5, 4, 2, and 1 of B1 (zone C5). All input pins of B1 should be HIGH. If one pin is LOW, the inverter on the pin is probably defective or the address lines are open or shorted.

Data channel address permits access to either the Data Register or the Data Direction Register (DDR). The status bit 2 in the Control Register determines whether the Data Register or the DDR is accessed. If bit 2 is a logic Ø, the DDR is accessed. If bit 2 is logic 1, the Data Register is accessed. Writing a logic Ø into any bit of the DDR will cause the corresponding data line to act as an output. Thus, there can be any combination of inputs or outputs on the data lines (PAØ through PA7 and PBØ through PB7).

2-3. PIA Initialization

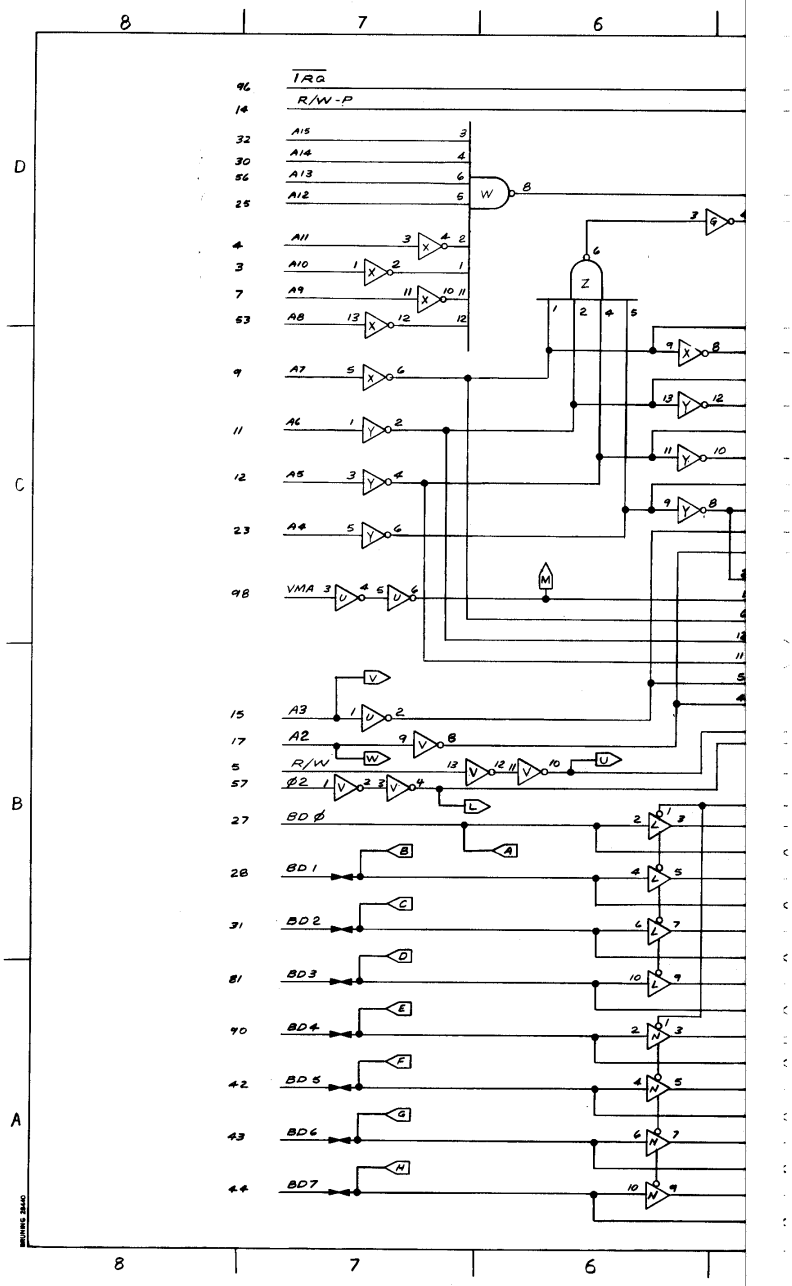
Program 2-I illustrates the initialization procedure for a parallel port. The initialization sets up communication between the MPU and the 680b Universal I/O Board. In this example, PIA-C is utilized and the Universal I/O is addressed at its lowest location, F008 through F00B. If a second parallel port is used, the lowest address location would be F00C through F00F.

The addresses function as follows: F008 = section A Control/Status Register; F009 = section A Data-Direction (when accessed) and Data Channel Register; F00A = section B Control/Status Register; F00B = section B Data-Direction (when accessed) and Data Channel Register.

Section A functions as an input and section B functions as an output.

INPUT

1. If the I/O device has valid data, a strobe signal from the I/O device pulls the input CA1 line LOW. Bit 7 of section A Control/Status Register goes HIGH. CA2 goes LOW following a Read of section A Data Channel, then returns HIGH after the next ENABLE pulse. CA2 is telling the I/O device that data has been read and to send more data.
2. With additional programming, the MPU can be instructed to periodically check the section A Control/Status Register to interpret the status of bit 7. When bit 7 is HIGH, Step 3 will be entered.
3. Data Channel Register is input to the accumulator. This, in turn, resets bit 7 of the Control/Status Register and CA2 becomes active. CA2 returns HIGH after the next E pulse. CA2 tells the I/O device that new data may be entered.


8
7
6
D
C
B
A
IRQ
R/W-P
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
VMA
A3
A2
R/W
Ø2
BD Ø
BD 1
BD 2
BD 3
BD 4
BD 5
BD 6
BD 7
W
Z
M
BRUNING 2440

Control bits 1 and Ø affect the operation of the external control line, C1. C1 is used as an input control line from the I/O device. Status bit 7 and the interrupt request output to the system bus, $\overline{IRQ}$, are then affected by the activity of C1 as shown in Table 2-3. Bit 7 and $\overline{IRQ}$ are reset (bit 7 goes LOW, $\overline{IRQ}$ goes HIGH) when the Data Register is read by the MPU. Control bit 1 determines whether C1 is active with a LOW going transition (bit 1 = 0) or active with a HIGH going transition (bit 1 = 1). The $\overline{IRQ}$ is dependant on how bit Ø is set in the Control Register. For example, if bit Ø = 1 and C1 is active, the $\overline{IRQ}$ output will be LOW, interrupting the system.

Table 2-3. Control of Interrupt Inputs, C1 (CA1 and CB1)

CONTROL BITS 1	0	C1 INPUT	STATUS BIT 7	$\overline{IRQ}$ OUTPUT
0	0	Active LOW	Set HIGH when C1 is active	Disabled -- remains HIGH
0	1	Active LOW	Set HIGH when C1 is active	Goes LOW when Bit 7 is HIGH
1	0	Active HIGH	Set HIGH when C1 is active	Disabled -- remains HIGH
1	1	Active HIGH	Set HIGH when C1 is active	Goes LOW when Bit 7 is HIGH

The C2 control line can function as either an input or an output for the I/O device. When C2 functions as an input (control bit 5 LOW), its mode of operation is determined by control bits 5, 4, and 3 as shown in Table 2-4. Sections A and B operate identically when C2 functions as an input.

Table 2-4. Control of Interrupt Inputs, C2 (CA2 and CB2)

CONTROL BITS 5	4	3	C2 INPUT	STATUS BIT 6	$\overline{IRQ}$ OUTPUT
0	0	0	Active LOW	Set HIGH when C2 is active	Disabled -- remains HIGH
0	0	1	Active LOW	Set HIGH when C2 is active	Goes LOW when Bit 6 is HIGH
0	1	0	Active HIGH	Set HIGH when C2 is active	Disabled -- remains HIGH
0	1	1	Active HIGH	Set HIGH when C2 is active	Goes LOW when Bit 6 is HIGH

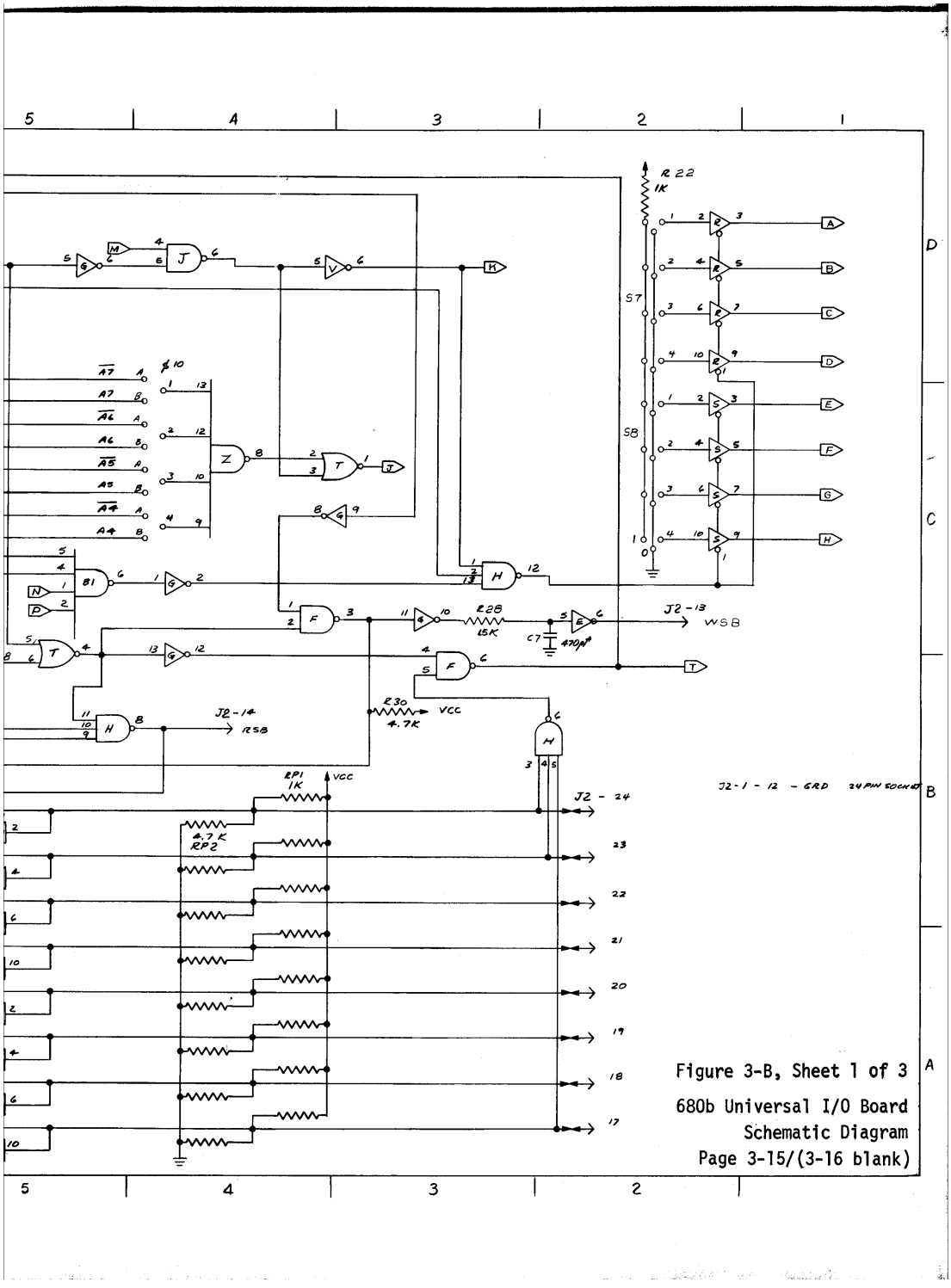


Figure 3-B, Sheet 1 of 3

680b Universal I/O Board
Schematic Diagram
Page 3-15/(3-16 blank)

2-1. GENERAL

Section II contains a detailed description of the MITS Altair 680b Universal I/O Board parallel (PIA) and serial (ACIA) port selection. Tables are provided to aid in understanding the PIA and ACIA structure and operation.

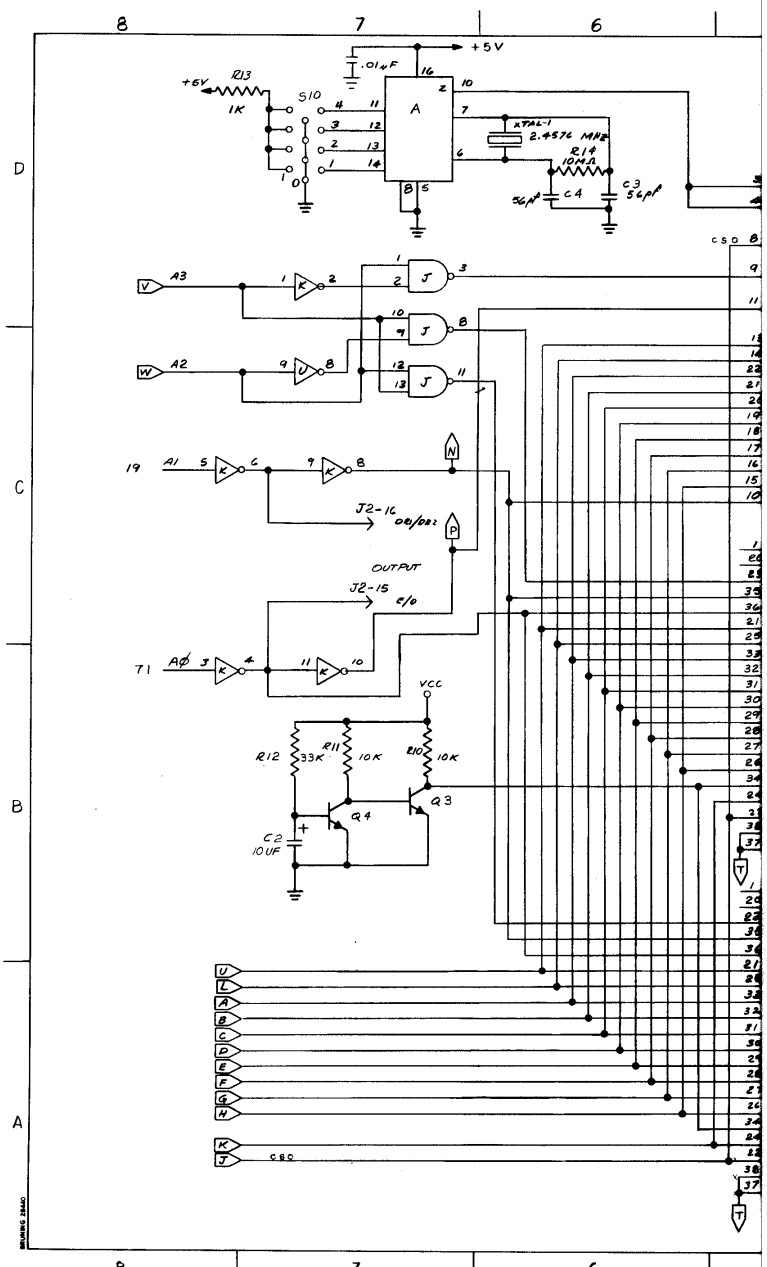
2-2. PARALLEL PORT (PIA) SELECTION

The Altair 680b reserves 256 address locations for I/O interfacing and each I/O card requires 16 address lines. Hardware sets the upper address lines, A15 through A8, to F0 for all I/O ports. These addresses are F0XX (XX = user selectable). Address lines A7 through A4 and their complements, $\overline{A7}$ through $\overline{A4}$, are also user selectable. With these addresses, there are 16 different address locations for the Universal I/O. Address lines A3 and A2 select between three ports. A3 addresses the parallel ports or the serial port and A2 selects between the parallel ports.

Each PIA contains two sections, A and B, and each section has two channels, Control/Status and Data-Data Direction. Address lines AØ and A1 enable the selection of the port section and the channel. If the two parallel ports are addressed at F008 and F00C, the port, section, and channel addresses would appear as in Table 2-1, assuming the board is strapped at the lowest possible position.

Table 2-1. PIA Address Selection

ADDRESS	IC	SECTION	CHANNEL
F008	C	A	CONTROL/STATUS
F009			DATA - DDR
F00A		B	CONTROL/STATUS
F00B			DATA - DDR
F00C	B	A	CONTROL/STATUS
F00D			DATA - DDR
F00E		B	CONTROL/STATUS
F00F			DATA - DDR


8
7
6
D
C
B
A
+5V
.01uF
+5V
R13
1K
S10
A
XTAL-1
2.4576 MHz
R14
10MΩ
C3
56pF
C4
56pF
A3
A2
A1
A0
J2-16
OE/DE2
OUTPUT
J2-15
E/O
VCC
R12
33K
R11
10K
R10
10K
Q3
Q4
C2
10UF
CSO
BRUNING 2840

SECTION II

altair 680b UNIVERSAL I/O
THEORY OF OPERATION
PORT SELECTION

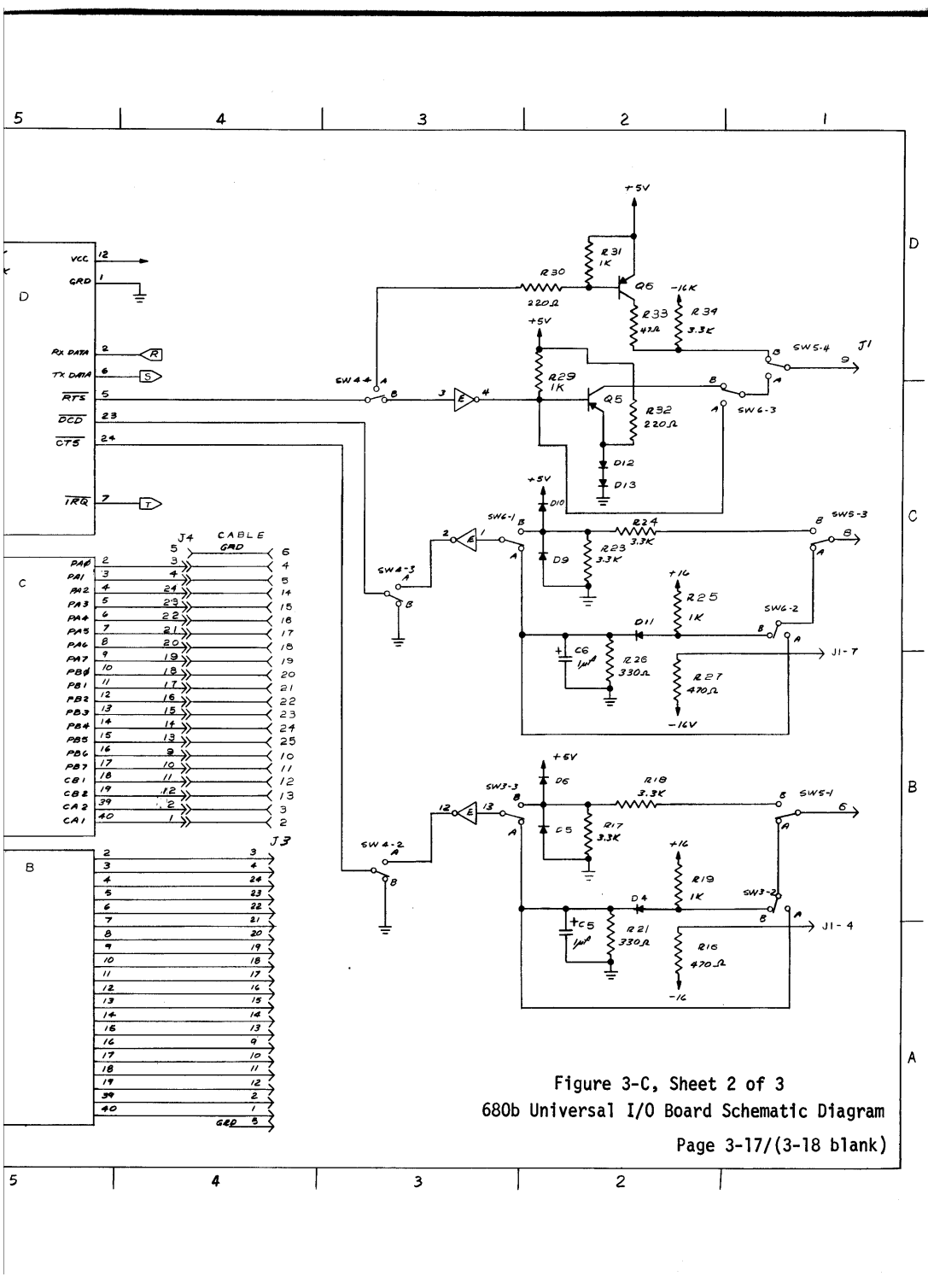


Figure 3-C, Sheet 2 of 3
680b Universal I/O Board Schematic Diagram

1-1. SCOPE AND ARRANGEMENT

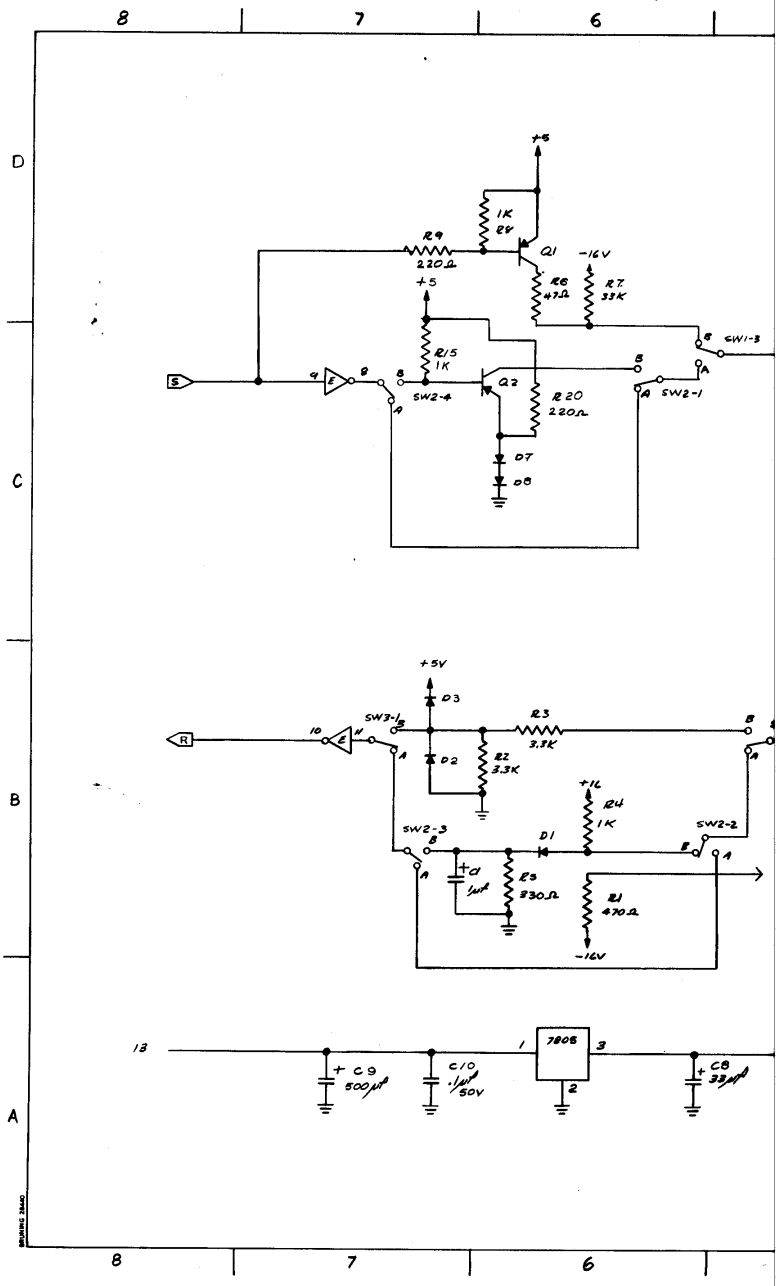
The Altair 680b Universal I/O Board Documentation provides a general description of the printed circuit board and detailed theory of its operation. The manual contains five sections as follows:

1. Section I contains a general description of the Altair 680b Universal I/O Board.
2. An explanation of parallel (PIA) and serial (ACIA) port selection, including the port structure and operation, is presented in Section II.
3. Section III includes a detailed theory explanation of the 680b Universal I/O circuit operation.
4. Section IV contains instructions for installing the Universal I/O Board into the Altair 680b computer.
5. Troubleshooting information for the 680b Universal I/O Board is found in Section V.

1-2. DESCRIPTION

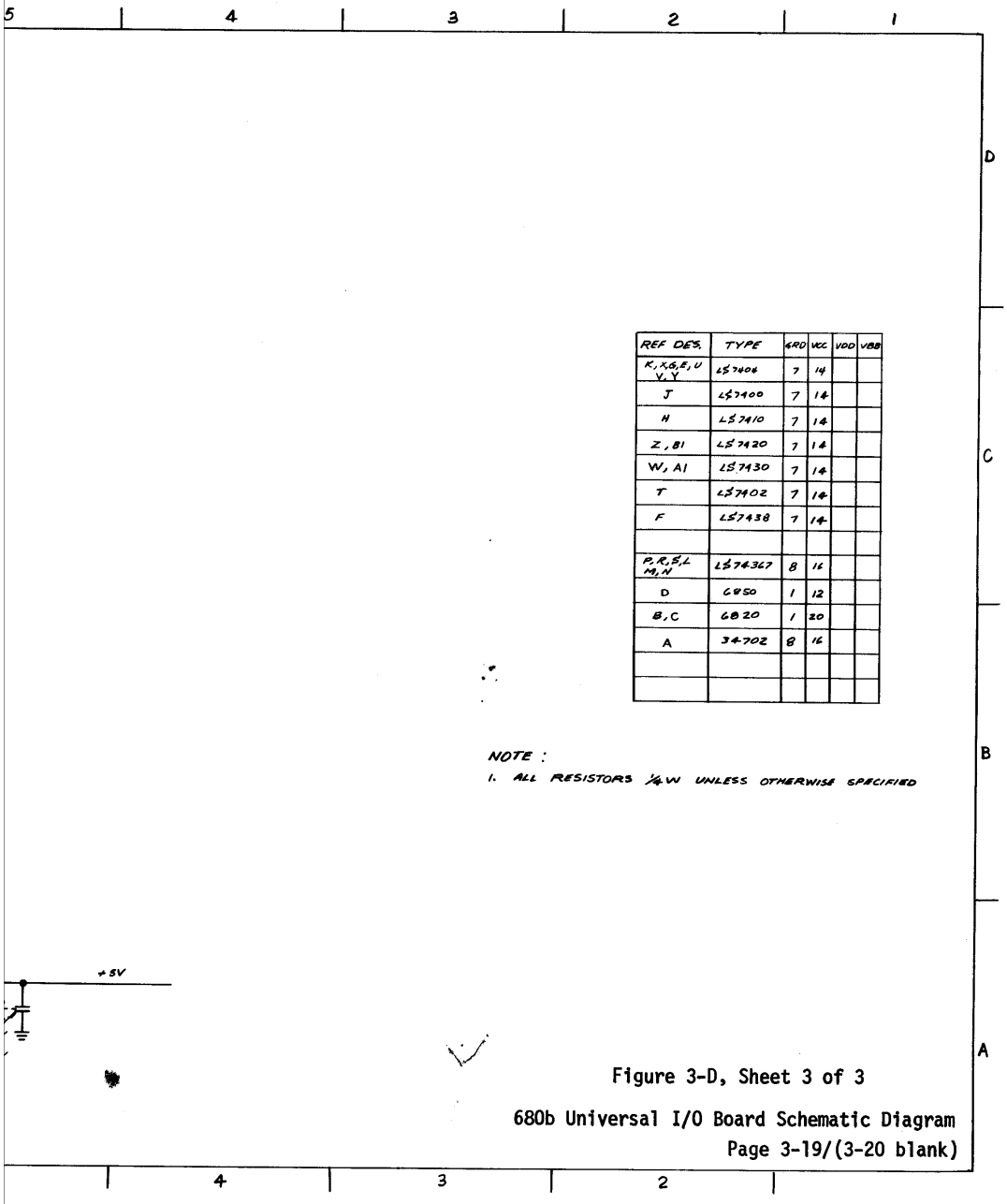
The 680b Universal I/O Board provides two parallel ports and one serial port while occupying only one slot on the 680b expander card. The design of the parallel and serial ports is based upon two peripheral ICs, the 6820 Parallel Interface Adapter (PIA) and the 6850 Asynchronous Communication Interface Adapter (ACIA), respectively.

The PIA contains all Control and Data Registers, thus most options are software selectable. These options include data direction (each data line can act as an input or an output) and interrupt/control structure. The Universal I/O Board can be expanded up to two parallel ports. With only one PIA parallel port, the board can handle two inputs (such as a paper tape reader or keyboard) or two output devices (such as a paper tape punch and printer) or any combination of custom applications. A Universal I/O with two PIA parallel ports has 32 data lines (each group of eight is individually selectable) and all data lines are fully TTL compatable. When utilized as outputs, eight of the 16 data lines are capable of directly driving the base of a transistor switch (1.5v at 1ma). The Universal I/O is also provided with a parallel 8-bit non-latched output at TTL levels.


8
7
6
D
C
B
A
+5
1K
R4
R9
220Ω
Q1
-16V
R6
47Ω
R7
33K
+5
R15
1K
SW1-3
S
SW2-4
Q2
R20
220Ω
SW2-1
D7
D8
+5V
D3
SW3-1
R
10
R3
3.3K
D2
R2
3.3K
+16
R4
1K
SW2-3
SW2-2
D1
C1
1μf
R5
330Ω
R1
470Ω
-16V
13
7806
1
3
2
+ C9
500μf
C10
.1μf
50V
+ C8
33μf

LIST OF ILLUSTRATIONS

LIST OF PROGRAMS



REF DES.	TYPE	GRD	VCC	VDD	VBB
K, X, G, E, U V, Y	LS7404	7	14		
J	LS7400	7	14		
H	LS7410	7	14		
Z, B1	LS7420	7	14		
W, A1	LS7430	7	14		
T	LS7402	7	14		
F	LS7438	7	14		
P, R, S, L M, N	LS74367	8	16		
D	6850	1	12		
B, C	6820	1	20		
A	34702	8	16		

Figure 3-D, Sheet 3 of 3

680b Universal I/O Board Schematic Diagram

Altair 680b Universal I/O Board

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altair 680b
UNIVERSAL I/O BOARD DOCUMENTATION

First Printing, December, 1976

mits, INC.
2450 Alamo S.E./Albuquerque, New Mexico 87106