

## 88-HSR

### Power and I/O Description

#### GENERAL

#### Power Supply

AC line voltage is applied to the primaries of T1 & T2 through switch S1 and fuse F1. The secondary of T2 is rectified by diodes D6 & D7 and regulated to +5 volts by VR1. R8 is a current bypass resistor and C4 is a filter capacitor. The regulated +5 volts supplies the Reader logic/Driver board.

The secondary of T1 is rectified to provide 35 volts DC at C2 and 17 volts DC at C3. Pad "1" (at R7) is a TTL input. This input is brought in at pin 22 of the 25 DB connector to pin A of the 15 pin edge connector and then jumpered to pin o of the 5-pin molex at the top of the Reader board. A wire connects pin 1 of the molex to a pad on the power supply board. When this input is a logic "1" (2 volts - 5 volts), Q1 conducts causing Q2 and Q3 to conduct which provides approx. 30 volts at V+. This voltage supplies the drivers of the stepping motor. When the run command is given, tapes will be read at a rate of approx. 300 cps.

When the input to Q1 is low (0 volts - .5 volts), Q1, Q2, and Q3 are turned off. This is the 'standby' mode and V+ becomes approx. 10 volts, supplied by the secondary of T1 through Diode D1. Although tapes will run at a speed of approx. 30 cps, this mode is normally used to decrease motor power during periods of inactivity. The Light-Emitting Diode on the front panel provides a different brightness for each mode: When dim, the reader is on but is in the standby mode. When bright, the reader is on in the normal mode. When not lit, the reader is off.

## I/O SIGNAL INTERCONNECT

FUNCTION	88-4PIO 25 PIN CONNECTOR	SIGNAL NAME	READER 15 PIN CONNECTOR
DATA	4	Data Bit 0	1
	5	1	2
	14	2	3
	15	3	4
	16	4	5
	17	5	6
	18	6	7
19	7	8	
STATUS	3	CA2 (Data RDY)	9
GROUND	6	GND	12 10  JUMPER
CONTROL	22	PB2 (STBY)	A
	20	PB0 (RUN)	F

### Theory of Operation

The 88-HSR is directly plug-compatible with the 88-4PIO parallel interface board.

88-4PIO Initialization (assume 4PIO is at address 20 octal)

One port of a 4PIO is used to interface the Reader. The 'A' section provides data input and status while the 'B' section provides Reader Control.

The 'A' section initialization sets PA0 - PA7 as data inputs and CA2 as the Data Available input. These inputs are all high active.

The 'B' section uses 2 bits as outputs to control the Reader:

Bit 0    when low, Reader runs

Bit 2    when low, Reader is in standby mode

Shown below is the full initialization procedure:

257		Make 'A' data lines inputs and 'B' data lines outputs
323		
020		
323		
021		
323		
022		
057		
323		
023		

076		Make DDR bit (bit 2) high and CA2 high active with interrupts enabled for 'A' section
034		
323		
020		
076		Make DDR bit (bit 2) high for 'B' section
004		
323		
022		

After initialization, the Reader is controllable via the 'B' data channel (address 023) as shown below:

<u>Bit 0</u>	<u>Bit 1</u> (Don't Care)	<u>Bit 2</u>	<u>Octal Equiv</u>
0	0	0	0
1	0	0	1
0	0	1	4
1	0	1	5

Normally, the Reader would first be stopped and in the standby mode:

```
076
001
323
023
```

Then the power switch is turned on. The Reader lamp will light, but the tape will be stopped. Then an output of 4 will start the tape.

### Loading Basic

The following boot-strap loader is entered in lower memory beginning at location 0. Once entered, load the BASIC paper tape in the middle of the "276" leader and turn the Reader on. Then start the program.

NOTE: The Reader should be in the "STANDBY" mode during the periods of inactivity and should be turned off when not in use.

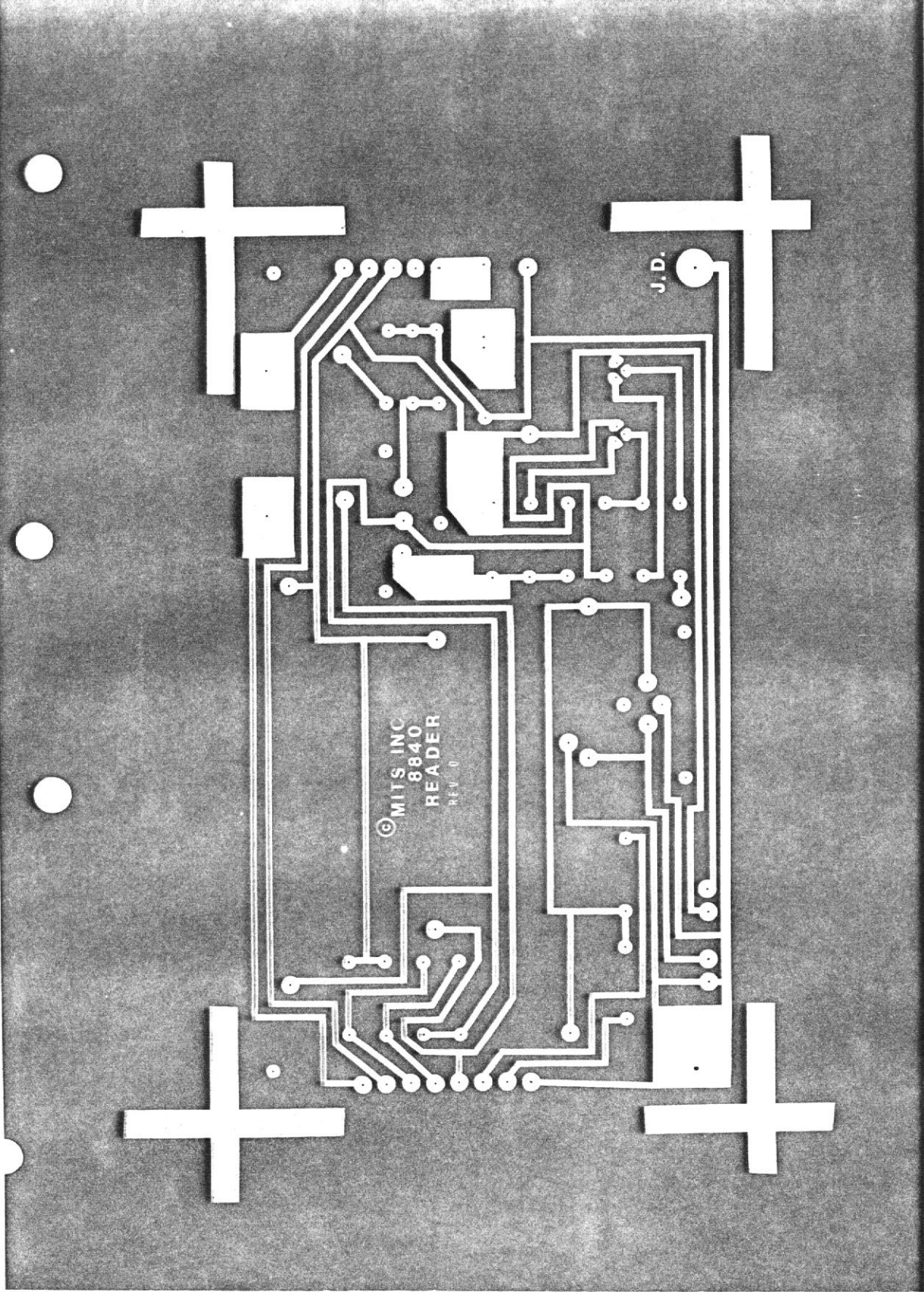
HSR BOOTSTRAP LOADER

<u>Location</u>	<u>Instruction</u>
000	257
001	323
002	020
003	323
004	021
005	323
006	022
007	057
010	323
011	023
012	076
013	014
014	323
015	020
016	076
017	004
020	323
021	022
022	076
023	004
024	323
025	023
026	041
027	256
030	XXX
031	061
032	051
033	000
034	333
035	020
036	346
037	100
040	310
041	333
042	021
043	275
044	310
045	055
046	167
047	300
050	351
051	031
052	000

17 for 4K, 37 for 8K, 57 for Ext.

NOTE: Front panel switch A12 should be raised before starting the bootstrap loader.






© MITSUMI INC  
8840  
READER  
REV. 0

J.D.

2)  $\textcircled{8}$   $\overset{10}{[2.5V PP]}$   $\textcircled{8}$   $\overset{9}{}$   
 $R_{pp}$  now down  
 to 7V  
 $\textcircled{8}$  (9.5) (7.6) (9.1) (0.4)

If then put CPU BD IN RIPP ON  
 OUTPUT (EZ) 

IS GETTING BELOW 7 (SAY DOWN TO 6.5)  
 YOU CAN JUST BARELY SEE IT ON T5 OUT  
 OF CPU REG

ANY MORE RIP ON INPUT STARTS TO  
 GO RIGHT THRU REG (MOTOROLA REG  
 ON CPU BD)

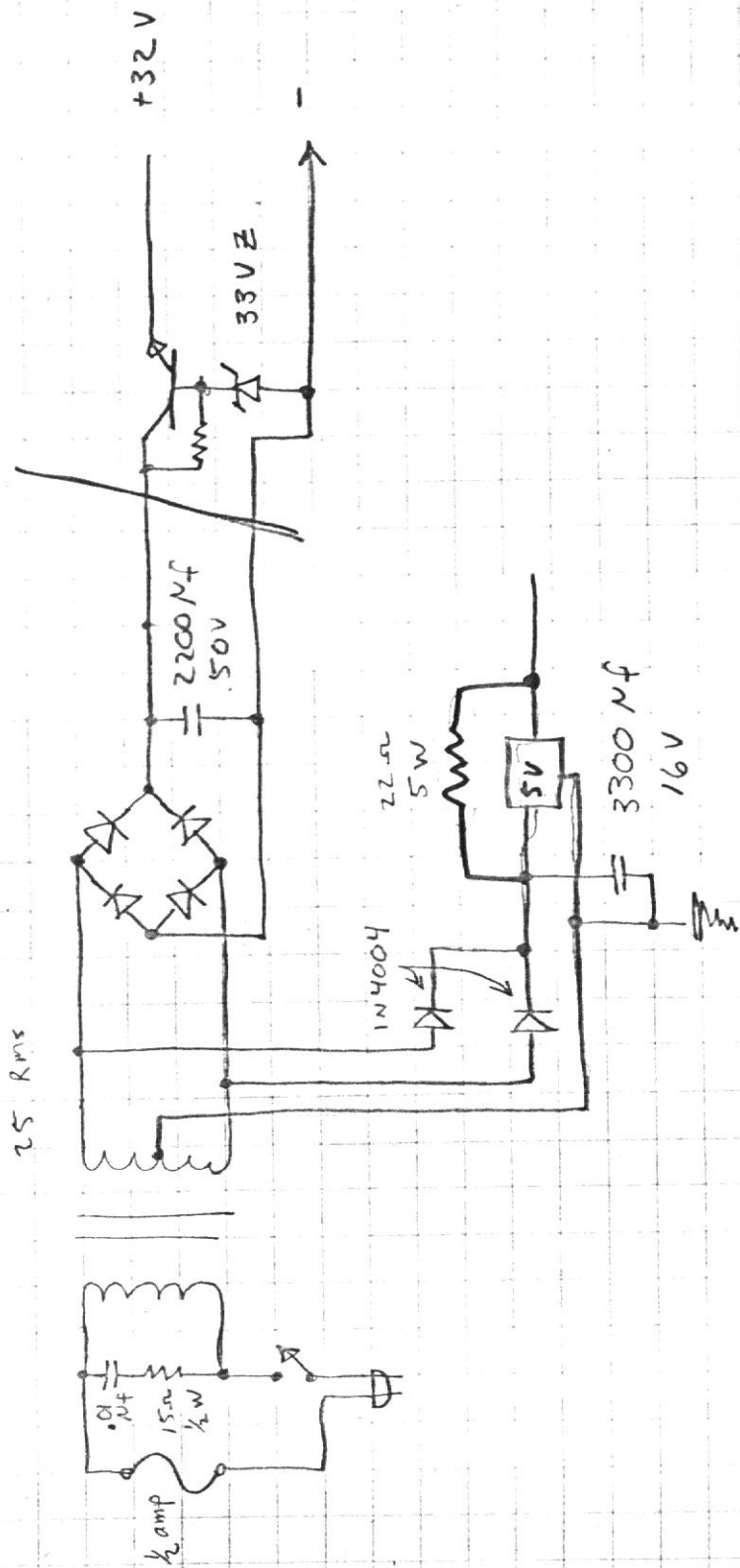
RDR

3 Mar 76

- 1) CR on X-former
- 2) 5 pin STRAIGHT molex
- 3) Case & tooling
- 4) Incoming Remex

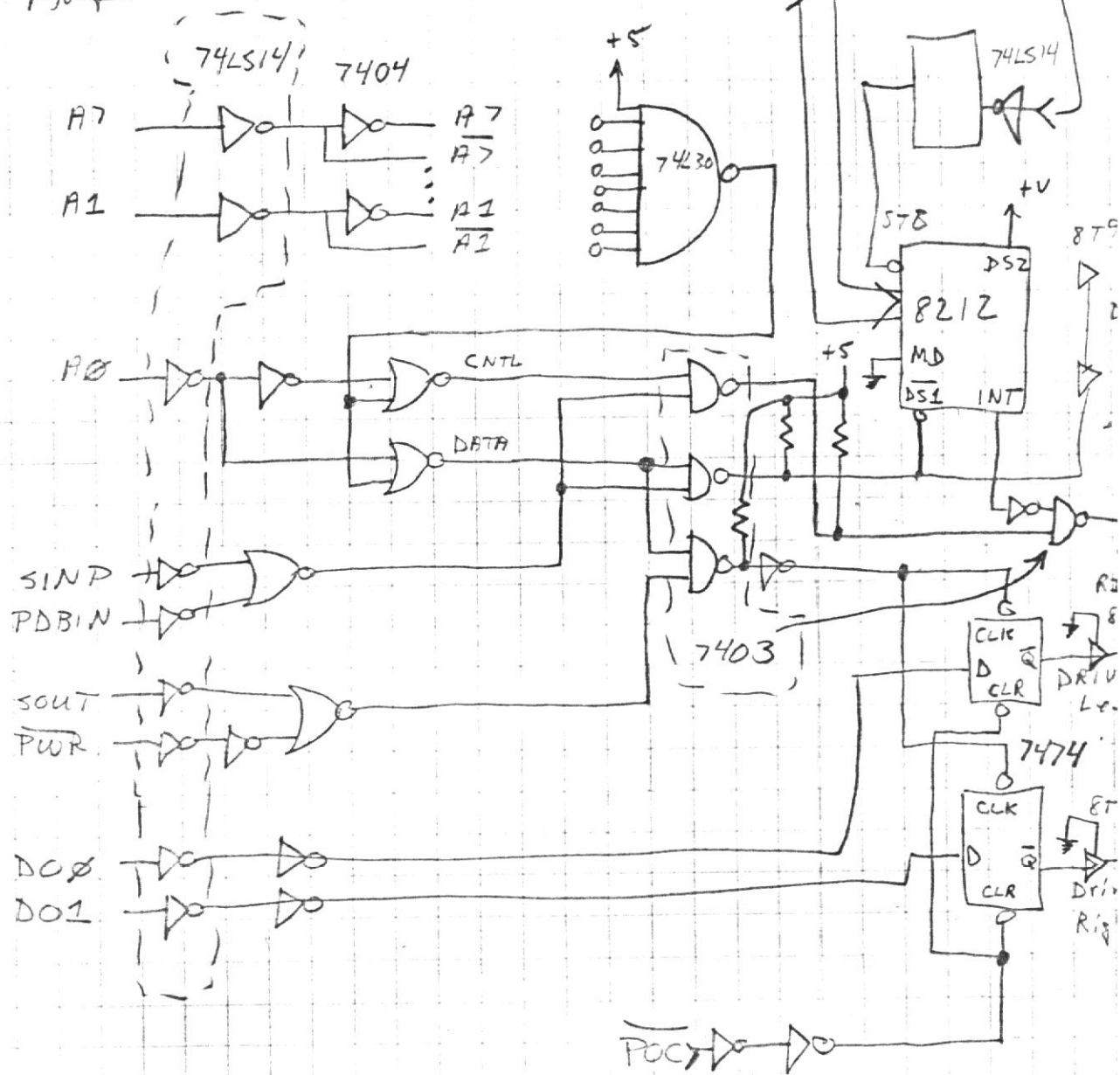
April 7 (P.O. Date 4 Mar 76)



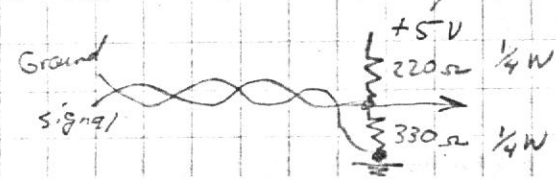


4.00  
 2.00  
7.75  
 5.00

6 Jan 74  
PNA



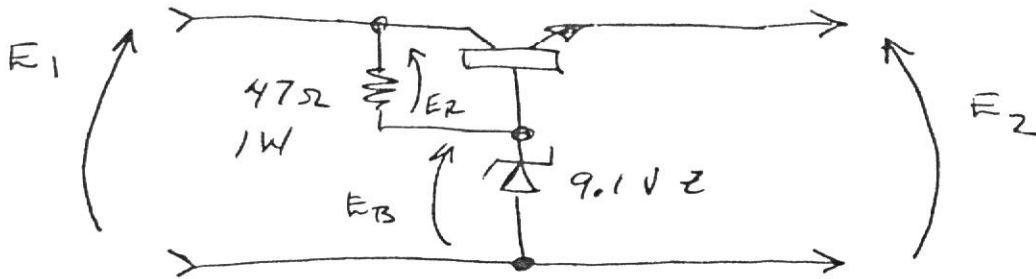
All signals from reader come into mini molex (~~25 pin~~ <sup>25 pin</sup> = 10 pins). There's 11 signals + eleven grounds. The inputs (8 data lines + Data Ready) are terminated as below



resistors should be as close as possible to IC that the signal goes to

# 7/S MEAS. (31 AUG 75)

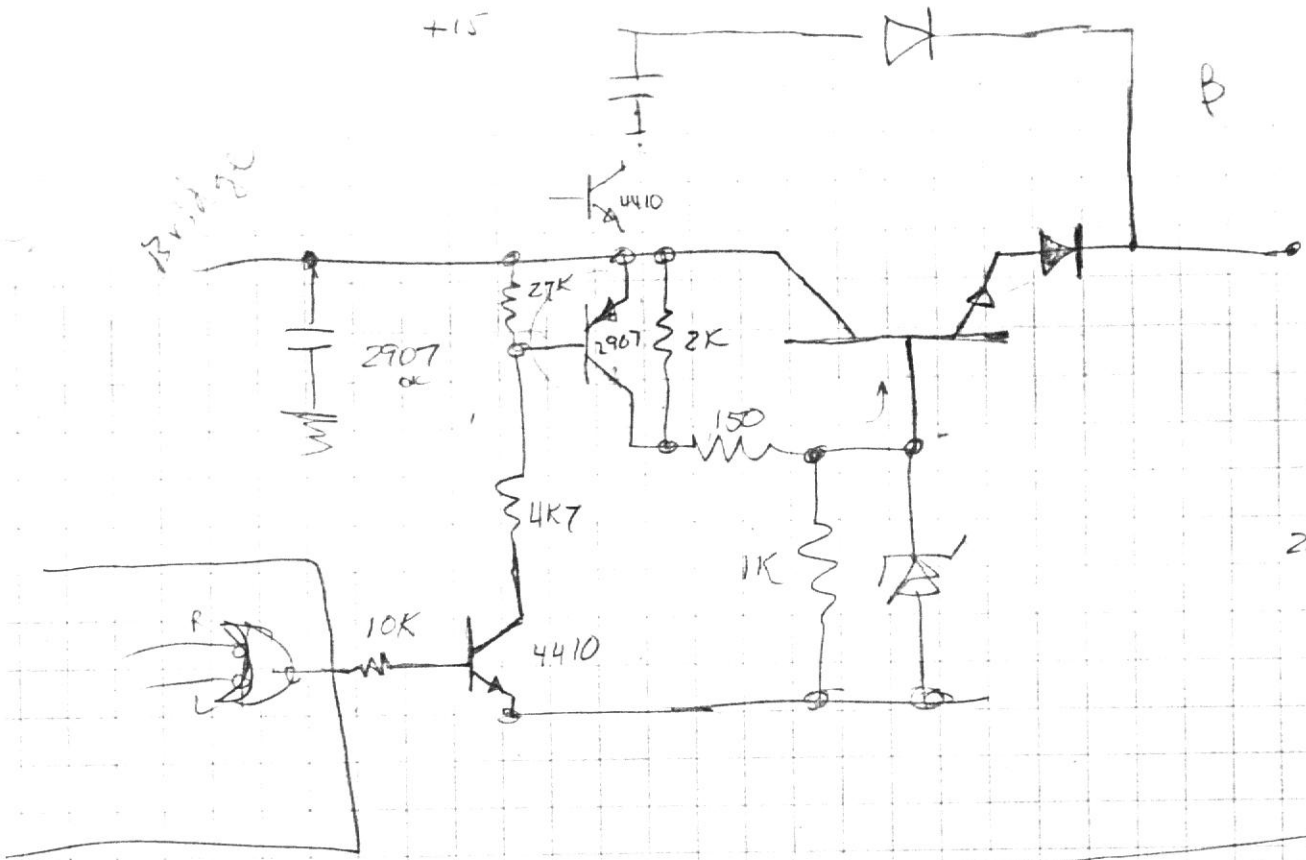
## ③ PRE-REG



LOAD	$E_1$	$E_2$	$E_Z$	$E_R$
a) 0	14 (13.8)	10.0 (10.0)	10.2 (10.1)	3.65
b) 0.6A	13 [RIP 1V PP] (13)	9.0 (8.8)	10. (9.9)	3 (3.0)
c) * 2.6A	12 [1V PP] (11.9)	8.5 (8.5)	9.8 (9.7)	2 [ ] (2.1)
d) 4A	11.5 [2V PP] (11.3)	8.5 (8.4)	9.8 (9.6)	[ ] (1.6)
e) 6.8	10.1 [2V PP] (10.1)	8.0 Start to get slight r. reg loss the .25V (7.9)	9.5 Same reg (9.3)	[ ] (.74)

(CPU 3D IN)

used



.7 A

NPN  
 2N3117  $N_f = 1.0$   
 $V_{CE0} = 30$   
 $V_{CB0} = 60$   
 $HFE = 250 - 500$   
 $f_T$  MHz 60  
 70-18

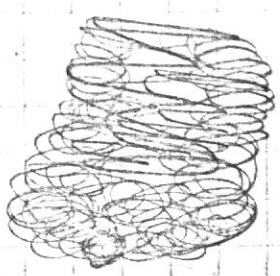
C E B  $n + V_{CE}$   
 36.4 4.6 4.5 7.6 11.8

$I = \frac{V}{R}$       $15V \cdot .7A = 10.5$

$175A @ 16V = 12W$

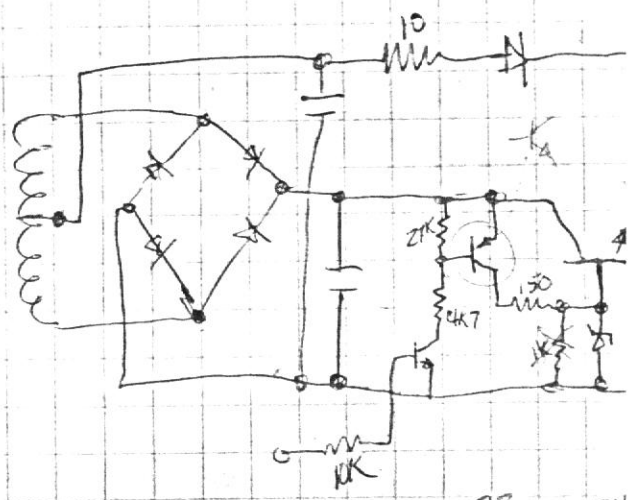
$21.33 \Omega$

$+10 \text{ series} \Rightarrow .52 A$



$\mu$

$\alpha \lambda \mu$   
 $\beta \gamma \theta$



- 1 = 5
- 11 = +5
- 18 = +12
- 22 = 1

- 22
- 74
- 66
- 50

HSR boot

377/000

77/0	257	40	257
1 1	323	41	323
1 2	020	42	022
3	000	43	076
4	323	44	377
5	021	45	323
6	076	46	023
7	014	47	000
10	323	50	323
11	020	51	022
12	041	52	076
13	256	53	002
14	037	54	323
15	061	55	023
16	035	56	333
17	377	57	020
20	333	60	000
21	020	61	333
22	346	62	021
23	100	63	303
24	310	64	000
25	333	65	377
26	021		
27	275		
30	310		
31	055		
32	167		
33	300		
34	351		

035 000

## MITS HIGH SPEED READER BOOT

000	257	
001	323	
002	020	
003	323	
004	021	
005	323	
006	022	
007	057	
010	323	
011	023	
012	076	
013	014	
014	323	
015	020	
016	076	
017	004	
020	323	
021	022	
022	076	
023	<del>016</del> 12	
024	323	
025	<del>023</del>	
026	041	
027	256	
030	017	
031	061	LXI SP
032	051	B1
033	000	B2
034	333	
035	020	
036	346	
037	100	
040	310	R2
041	333	
042	021	
043	275	CMP L, A
044	310	R2
045	055	DEC L
046	167	MOV M, A
047	300	RNZ
050	351	PCHL
051	031	
052	000	

1 0 1 0

So, to load the Bootstrap Loader:

- 4) Put switches 0-15 in the Down position.
- 5) Raise EXAMINE.
- 6) Put 041 (the data for address 000) in switches 0-7.

9, 12

~~100306 1 4" @ 250V~~  
~~100378 2 220V @ 50V~~  
~~100376~~

100908	2	4-40 x 3/8
100932	2	4-40 nut
100941	2	#4 lock washer
100925	5	6-32 x 3/8
100919	4	6-32 x 1
100933	17	6-32 nut
100942	17	6-32 lock washer
101822	4	.4 spacer
100929	4	8-32 Nut
103021	1	Cable clamp 1/4"
103061	1	3' orange 20 ga
103062	1	6' black 20 ga

# HSR - PWR SUP Bd

## Transistors

EN2907 (PNP)	1	102304
4410 (NPN)	1	102306
TIP 141 (NPN-HP)	1	102317
7805 (Voltage Reg)	1	101074

## DIODES

1N4004	11	100718
1N4751A (30VZ)	1	100729
1N4737 (7.5VZ)	1	100719
RL-21 (LED)	1	100702

## Transformers

9-[8388]	(25.2V @ 28a)	1	102305
<del>8130</del> NO	8V (12.6V @ 2a)	1	

## Resistors

150 $\Omega$ , $\frac{1}{2}$ W	<del>1</del>	1	<del>101715</del> order
1.5 K $\Omega$ , $\frac{1}{2}$ W		1	101946
4.7 K $\Omega$ , $\frac{1}{2}$ W		1	101930
10 K $\Omega$ , $\frac{1}{2}$ W		2	101932
27 K $\Omega$ , $\frac{1}{2}$ W		1	101939
<hr/>			
10 $\Omega$ , 5 W		1	<del>101903</del> (20W) 1
15 $\Omega$ , 2 W		1	101901



HSR - PWR SUP Bd (cont.)

Capacitors

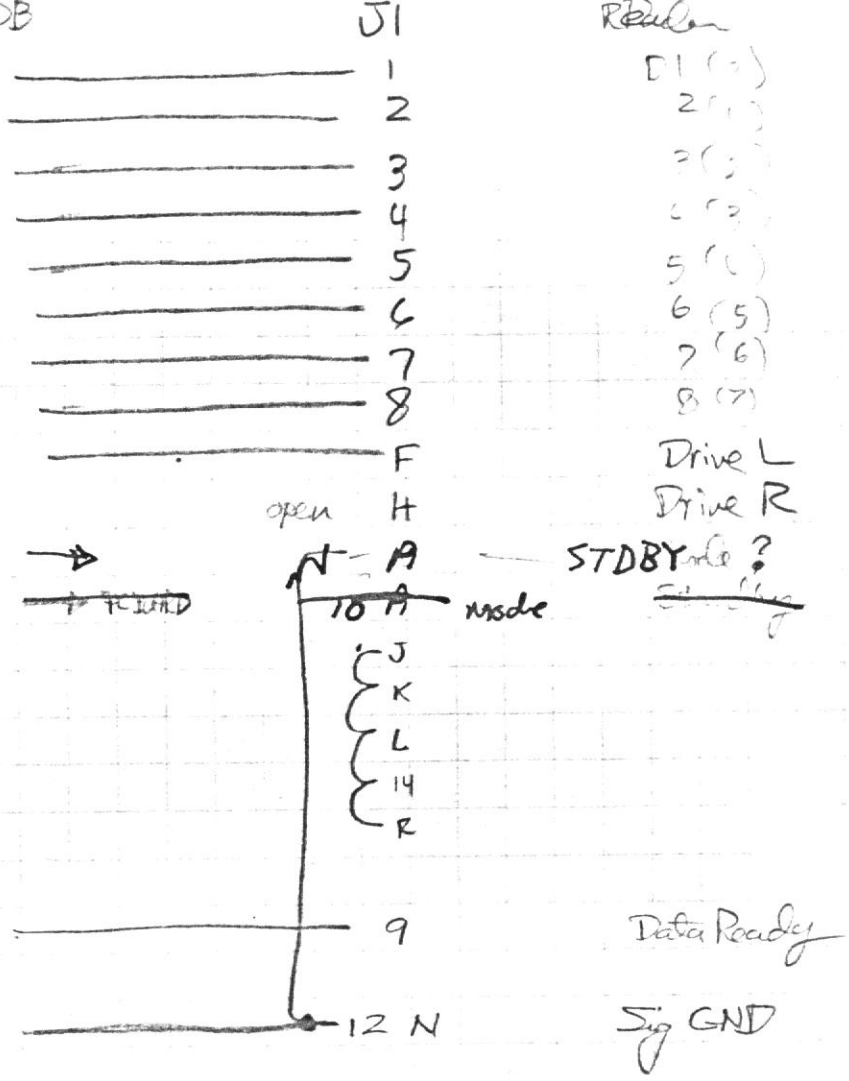
1Mf @ 50V	1	1002006
2200Mf @ 25V	2	1002115
2200Mf @ 50V	1	1002116

General

Thermal # 6030 B

Terminal Strip ( <del>6</del> <sup>5</sup> position)	1	<del>101712</del> 101713	<del>NO!</del>
AC Pwr. Cord	1	3 wire 101742	
Hotsink (stand up - large)	2	<del>101673</del> 101673	NO!
Bezel (for RL20 LED)	1	1002116	
Fuse 1A SB	1	101777	
Fuse clips	2	1017006	
25DB connector (female)	1	102112	
" P " (male)	2	102111	
flack <del>Molex</del> Ring Headers (2x)	1	101757 ?	
AC Pwr. Switch	1	1023106	
Case	1		
AC Pwr. cord grommet	1	1017116	
Molex Plug (10-pin)	1	<del>101812</del> 101812	
Molex Plug (5-pin)	2	101812	
Molex Recep. (10-pin)	1	101768	
Molex Recep (5-pin)	2	101812	
Molex terminals	20	101769	
PC Bd. (HSR - Ps)	1		
88-94PIO Kit (w/ 1 port)	1		
Twisted Pair Cable	7	1020100 ?	
Reader	1		

chip	2 chip	25 pin DB
PAD	2	3
1	3	4
2	4	24
3	5	23
4	6	22
5	7	21
6	8	20
7	9	19
PBO	10	18
1	11	17
2	12	16
3	13	15
4	14	14
5	15	13
6	16	9
7	17	10
CB	18	11
2	19	12
CA	39	2
1	40	1
<del>GND</del>	→ 5	6

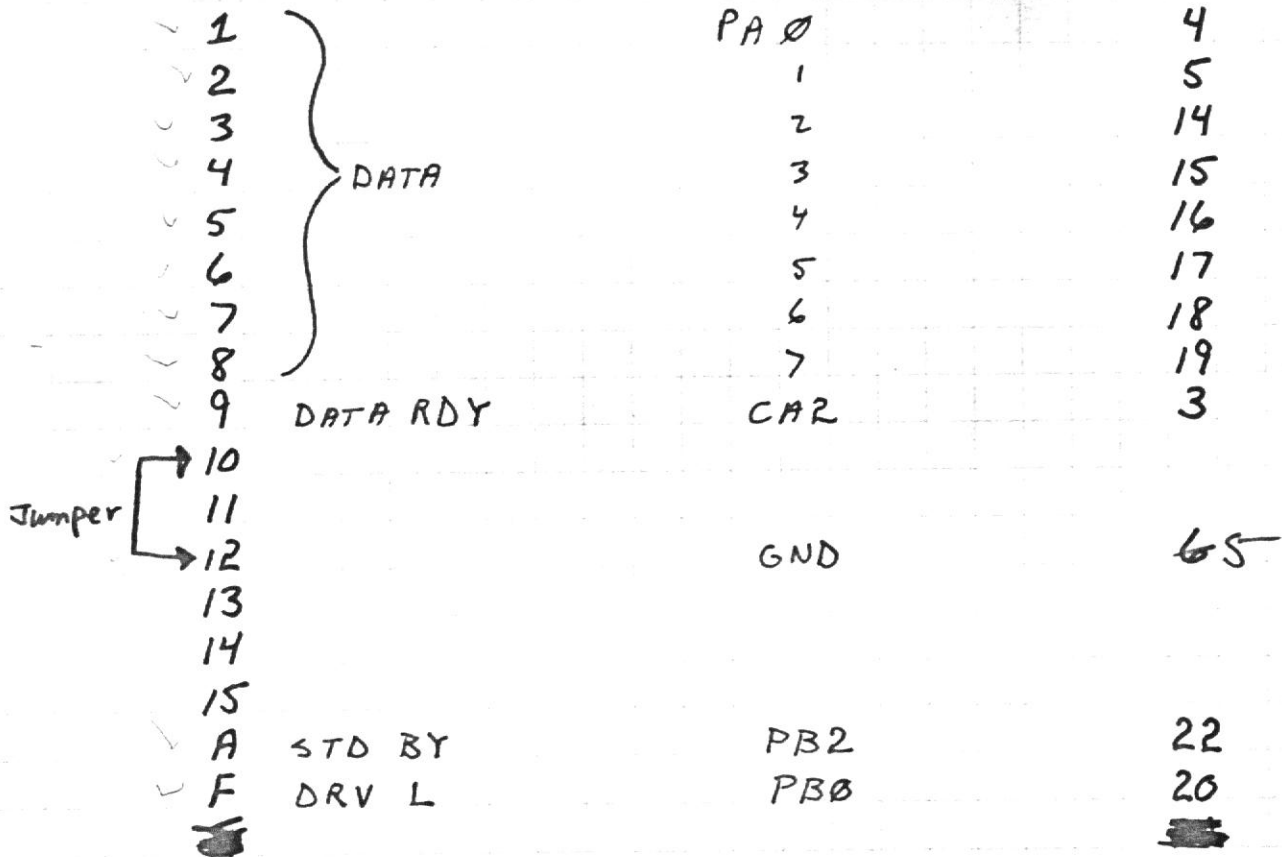


# From Reader to Back Panel

15 pin Edge Connector

12 Conductor Cable (1 foot)

25 DBS (Female)



# From Reader Back Panel to Computer Back Panel

25 DBP

12 cond. (6 feet)

25 DBP

4  
5  
14  
15  
16  
17  
18  
19  
3  
6  
10

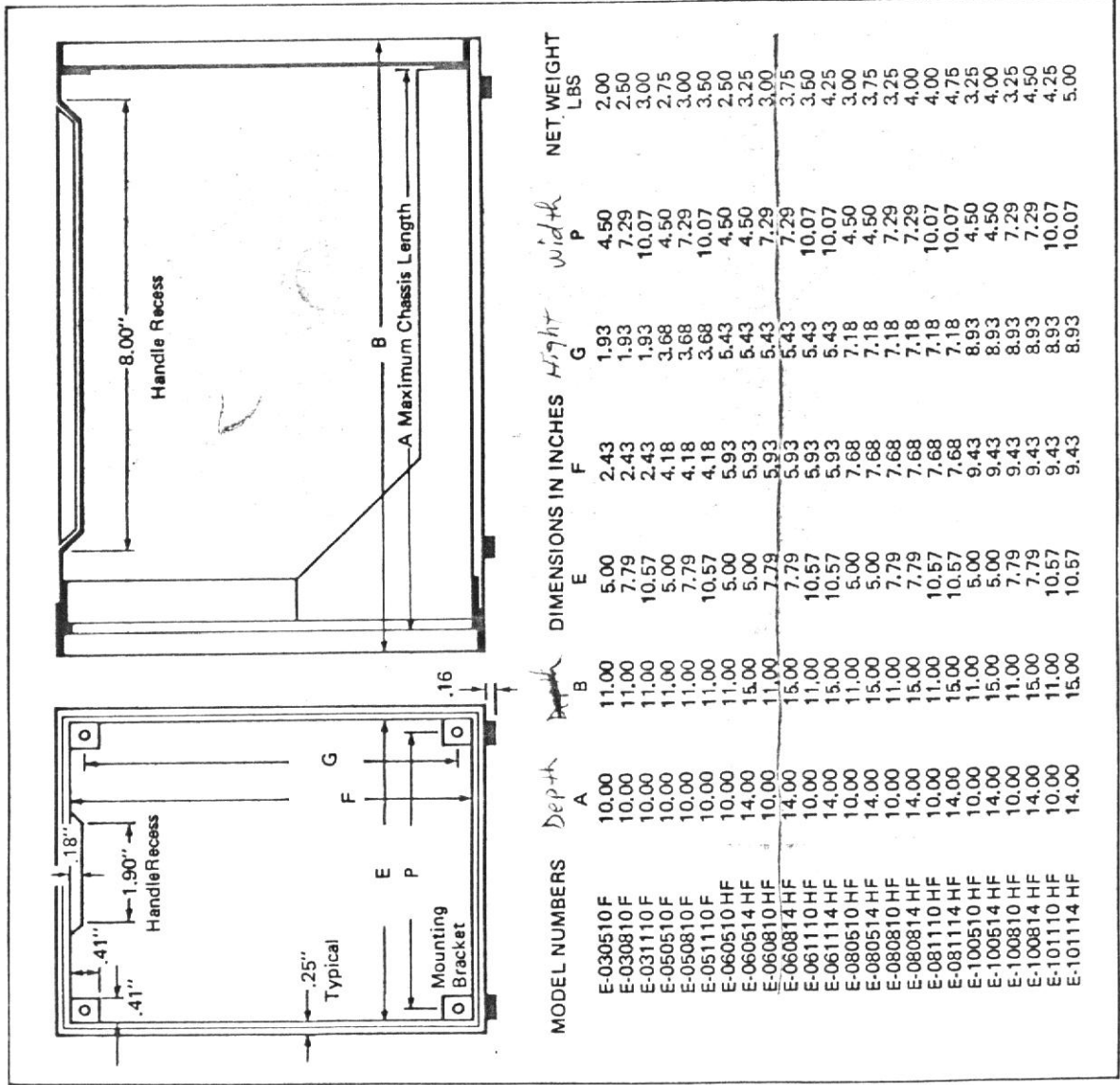
4  
5  
14  
15  
16  
17  
18  
19  
3  
6  
10

# RDR CASE

13 MAY 76

- 1) cut Front pannel on inside (marks)
- 2) PC bd. mtg. back & to right
- 3) Big X-former left
- 4) lower notch for pow. cord

# dimension data



Optima has 24 standard-size small cases available, in a wide variety of colors, color combinations, and textures. Our Color and Finish brochure will tell you all about them. Overall depth is 11" or 15".

Optima small case covers are easily removable for total instrument servicing via two screws. Optional tiltstands and flush carrying handles add to the versatility and convenience of these lightweight aluminum enclosures. With the optional rack adapters, many combinations of two or three complete cases can be installed in a standard 19" wide enclosure. (We'll show you some possibilities a little later.) Front panel mounting hardware can be eliminated by fastening the front panel and chassis assembly to the rear of the case.

Optima's basic small instrument case consists of two major elements: the one-piece cover and the bezel-and-bottom-pan assembly. The suffix "F" in the model number (model numbers are covered in the size-and-weight chart immediately following this section) designates front-panel mounting hardware. The suffix "H" specifies the optional flush self-retracting handle. Nonstaining celcon plastic feet are included.

Panel and chassis are loaded from the front. Front-panel mounting hardware (suffix "F") may be omitted if the panel-and-chassis assembly is attached to the rear of the case. The chassis and cover are fastened to two sets of holes at the rear and can therefore be removed independently.

For Detail Information Refer to Engineering Drawing E-36699



Table 3-1. Interface Signal Descriptions, RRK 7000

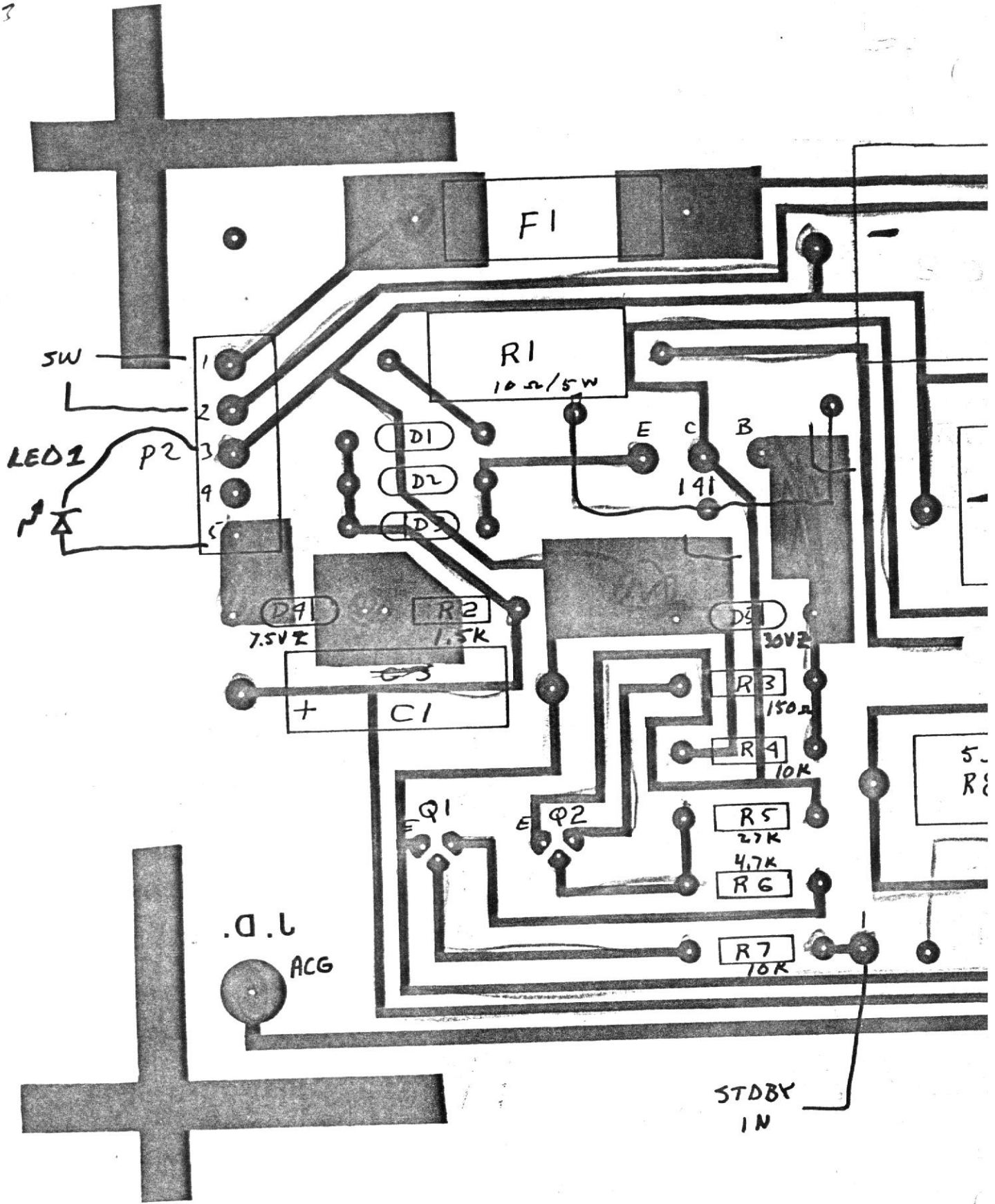
Connector Pin	Description	Interface IC Type	Signal Levels	
			Active	Inactive
J1-1 thru J1-8	Data Tracks 1-8 Output. Active signal indicates data track hole and inactive condition indicates no hole condition. Output mode 5 or 6 selectable (see J1-10).	SN7486N	Operates in mode 5 or 6: Mode 5: $+2.4 < V < +5 @ 0.2 \text{ mA}$ (source); Hole (or Data Ready)	Operates in mode 5 or 6: Mode 5: $0 < V < +0.4 @ 16 \text{ mA}$ (sink); No hole (or Data Not Ready).
J1-9	Data Ready Output. Active signal indicates data track outputs are in "On Character" condition. Signal active with leading edge of feed hole and remains active until next drive signal is accepted. Output mode 5 or 6 selectable (see J1-10)		Mode 6: $0 < V < +0.4 @ 16 \text{ mA}$ (sink); Hole (or Data Ready).	
J1-10	Data Mode Select Input. Active signal places Data Outputs and Data Ready output in Mode 6. Inactive signal places these signals in Mode 5.	SN7486N	$+2.4 < V < +5.0$ (or open circuit) Data Track and Data Ready signals in Mode 6.	$0 < V < +0.4 @ 17 \text{ mA max.}$ Data Track and Data Ready signals in Mode 5.
J1-12, J1-N	Signal Ground (0Vdc), +5V return. Isolated from J1-14 and J1-R.			
J1-13, J1-P	$+5 \pm 0.2 \text{ Vdc} @ 1.3 \text{ mA}$ logic and lamp supply.			
J1-14, J1-R, J1-J, J1-K, J1-L	Signal Ground (0Vdc), +32V motor supply return (VMR)			
J1-15, J1-S	$+32 \pm 10\% \text{ Vdc} @ 1.5 \text{ amps}$ motor supply (VMOT)			
J1-F	(Drive Left)* Input. Active signal drives tape to left. Pulse or DC level input drives tape at 300 characters second. Signal must be maintained until the Data Ready signal becomes inactive (typically less than 0.5 $\mu\text{sec}$ ) and must be removed within 50 $\mu\text{sec}$ . after the leading edge of the active Data Ready signal to stop on that character. The next pulse or DC level may be applied any time after the Data Ready signal becomes active. See Timing Diagram, page 3.	SN7400N	$0 < V < +0.4 @ 5.0 \text{ mA, max.}$ Reader drives tape.	$+2.4 < V < +5.0$ (or open circuit). Tape is not being driven.
J1-H	(Drive Right)* Input. Same as drive left except drives tape to right.			
J1-11, J1-D, J1-E, J1-M	Not Connected.			
J1-A, J1-B, J1-C	Reserved.			

Table 3-2. Interface Signal Descriptions, RRT 7000

Connector Pin	Signal and Definition and/or Usage
P1-1 thru P1-4	Step Motor phases 1 thru 4, respectively. The motor is a four phase stepper motor with a mechanical damper attached to the rear of the motor shaft. To drive tape it is required that two motor phases at a time be energized in the following sequence which drives tape to the right: 1 and 2, 2 and 3, 3 and 4 and then 4 and 1. Drive left is the reverse sequence. It is also recommended that a programmed power supply be utilized to reduce power consumption during periods of inactivity to lower the operating temperature.
P1-5	Motor Supply Voltage (+VMOT); $+32 \text{ Vdc}$ at 1.50 amps for 300 cps; $+28 \text{ V}$ at 1.35 amps for 200 cps operation. $+10 \text{ Vdc}$ for programmed standby operation. The resistance of each motor winding is 35 ohms/phase.
P1-6	Key Position.
P1-7	0VDC return (signal ground) for +5V lamp supply (P1-8). This signal is isolated from P2-10.
P1-8	Lamp Supply Voltage: $+5 \pm 0.2 \text{ VDC} @ 800 \text{ ma}$ .
P2-1 thru P2-9	Data Track Outputs 1 thru 8 and Sprocket (Pin 9). Each cell output is an analog signal indication of a data hole condition. A negative voltage is generated by a photovoltaic cell when it is activated by a light source. Minimum cell output, hole condition is 70 micro amps into 1K load. Maximum cell output, no hole condition with oil yellow paper tape is 20 micro amps into 1K load.
P2-10	0VDC return (signal ground). This signal is isolated from P1-7.
P2-11	Key Position.
P2-12	Not Used.

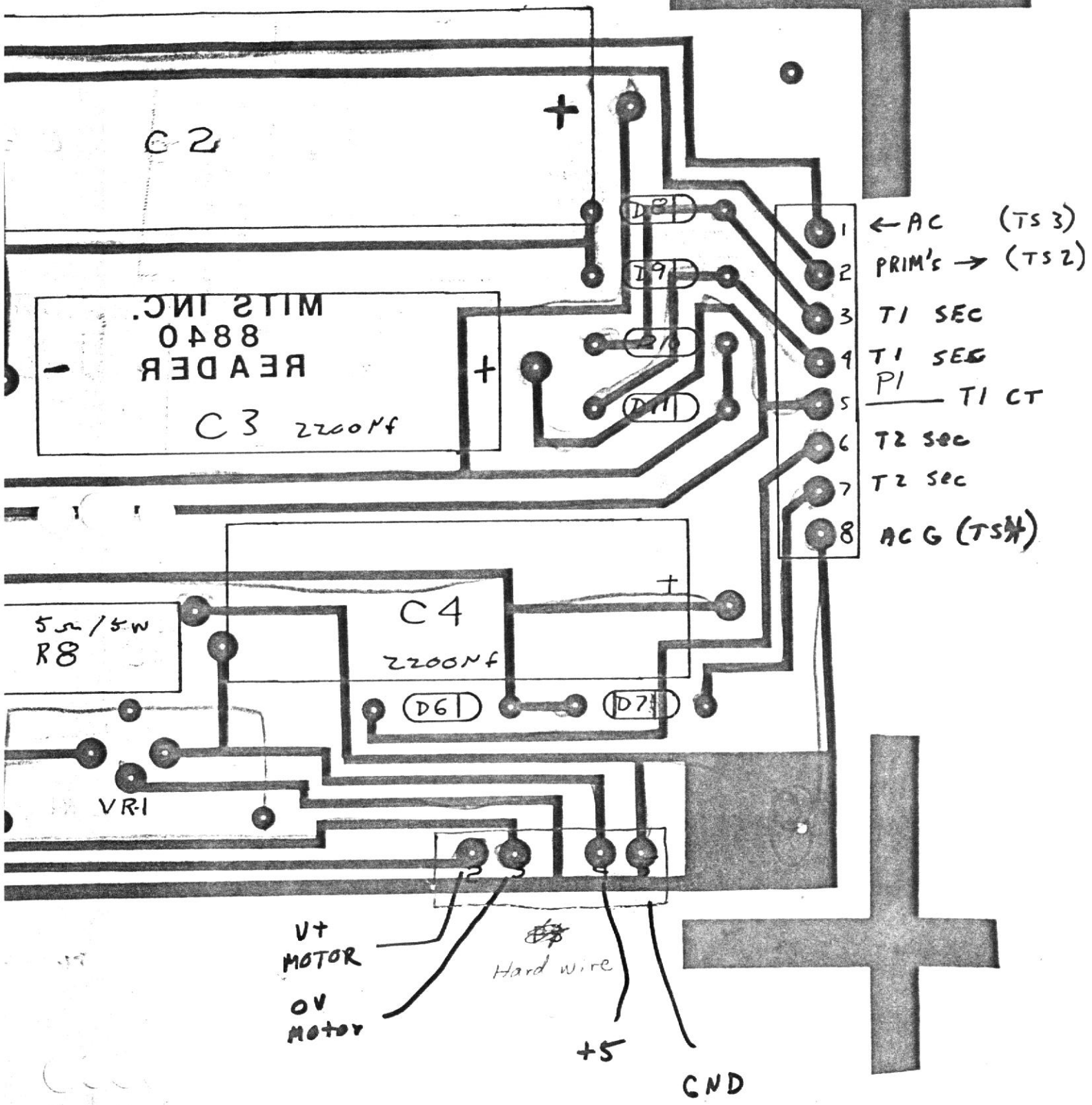
Mating connector for P1 is Molex 09-60-1081 and mating connector for P2 is Molex 09-60-1121. Other 8 and 12 pin connectors are available from Molex depending upon the application.

34  
33



RUN EMULSION U





UP - BOTTOM SIDE