ALTAIR 8800

THEORY of OPERATION

MANUAL & SCHEMATICS

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SCHEMATICS

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INTRODUCTION

The ALTAIR 8800 computer system is designed around Intel's 8080 microprocessor. The Intel 8080 is a complete central processing unit (CPU) on a single LSI chip using n-channel silicon gate MOS technology. This chip uses a separate 16-line address and 8-line bidirectional data bus configuration to greatly simplify design.

The ALTAIR 8800 uses a 100 line bus structure for data transfer between the CPU and memory or I/O devices. This bus structure contains all of the data and address lines, along with the unregulated supply voltages and all control and status signal lines. Cards other than the CPU will have control of the bus only when addressed by the CPU.

The schematic diagrams for the ALTAIR system are located at the end of this section. Specific schematics will be referred to in each particular section of the theory of operation.

On the schematics for each particular board components are identified by letters for the integrated circuits (A, B, C, etc.), and letters and numbers for the resistors and capacitors (R1, R2, C1, C2, etc.). Specific pins on the IC's are identified by numbers external to the symbol for that particular IC. The boxed numbers next to signal lines with arrows that exit or enter a given schematic refer to the bus number for those signals. Other notations on the schematics are self-explanatory.

CPU BOARD OPERATION

The 8800 CPU Board is the "heart" of the ALTAIR system. This board contains the 8080 microprocessor chip, bus drivers, the system clock, miscellaneous gating logic and the system status latch.

Refer to the following schematics for the CPU Board operation: 880-101, 880-102 and 880-103.

BUS DRIVERS

All signals entering or leaving the CPU Board are buffered using 8T97 tri-state drivers. These signals include: 16 address lines through IC's B, C and 4 gates of D; 8 data output lines through IC E and 2 gates of D; 8 data input lines through IC F and 2 gates of H.

The terms "in" and "out" are always defined with respect to the processor. Note that the 8080 bidirectional bus is split at the processor into an input and an output data bus.

The address and data out drivers (IC's B, C, D and E) can be disabled using the $\overline{\text{ADDR DSBL}}$ and $\overline{\text{DO DSBL}}$ bus signals through 2 of the gates of IC M. The data in drivers (IC F and 2 gates of H) are enabled under control of the processor through one gate of IC R, etc. (see schematic).

The 8 status output signals are buffered using 8T97's (4 gates of G and 4 gates of H). These signals are SINTA, SWO, SSTACK, SHLTA, SOUT, SMI, SINP, and SMEMR. The $\overline{\text{STATUS DSBL}}$ signal can be used to disable these outputs.

The 6 command/control output signals are also buffered using an 8T97 (IC J). These signals are SYNC, DBIN, WAIT, WR, HLDA, and INTE. The $\overline{\text{C/C DSBL}}$ signal can be used to disable these outputs.

The 4 command/control input signals (READY, HOLD, INT and RESET) are buffered using 4 gates of the 8T97 IC I. Note that the PRDY and $\overline{\text{PHOLD}}$ signals are synchronized to the leading edge of the Ø2 clock. This is required since the transition of either of these signals during the second half of Ø2 will cause the processor to enter an undefined state.

SYSTEM CLOCK

The ALTAIR 8800 system clock employs a standard TTL oscillator (IC P) with a 2.000 MHz crystal as the feedback element. The correct pulse widths and separations for the two phases are obtained using the dual single-shots (IC Q) and the delay circuit (R43 and C6). The 8080 processor requires a 12 volt swing on the clock. This is accomplished using a 7406 driver (IC N). TTL clock levels are sent to the system bus using 8T97 drivers (2 gates of IC I). The $\overline{\text{CLOC}}$ signal is sent to the system bus through one gate of the 8T97 IC G.

GATING LOGIC

The only external gating logic on the CPU Board consists of IC O (3 gates) and IC R (1 gate). If we define the output on IC O pin 13 to be G1 ENB (Data Input Enable), then:

$$\text{G1 ENB} = (\text{DBIN} + \text{HLDA}) \bullet (\text{RUN} + \text{SS})^*$$

Further, if we define G1 DSB = $\overline{\text{G1 ENB}}$; then the output of IC R pin 8, which is the disable input for the input data drivers, is:

$$\text{DI DSB} = \text{G1 DSB} + \text{SSW DSB}$$

G1 DSB, as can be seen from the schematic, is a processor generated signal. When the 8080 is ready for input data, it will allow G1 DSB to go low thus enabling the input data drivers.

$\overline{\text{SSW DSB}}$ is a signal generated on the Display/Control Board. This signal is used to disable the input data drivers when an input from the sense switches (device address 377_8) takes place.** This is necessary since the sense switch inputs are tied directly to the bidirectional data bus at the processor.

SYSTEM STATUS LATCH

The system status latch consists of IC K (8212). At the start of each machine cycle the processor places the system status on the bidirectional data bus. When SYNC and $\overline{\text{Q1}}$ are coincident, this data is latched by IC K and remains latched for the remainder of the machine cycle.

*In these notations, + means or, and • means and.

**This address is listed in octal format. It is the same as the decimal address "255" listed in the assembly manual.

DISPLAY/CONTROL BOARD OPERATION

The 8800 Display/Control Board provides the operator with RUN/STOP and Single Step control of the processor. It also allows him to examine and modify the contents of any location in memory using the front panel switches.

Refer to the following schematics for the Display/Control Board operation: 880-104, 880-105 and 880-106.

The primary function of the D/C Board is controlling the ready line (PRDY), or a combination of the PRDY and the bidirectional data bus, to allow the above functions to be performed. Control of the PRDY line is exercised at IC O (7430). The output of IC O pin 8 (PRDY) logically appears:

PRDY = RUN + SS + EXM + EXM NXT *

For the ready line to be released one of these inputs to IC O must go high. The circuitry preceding IC O will insure that only one of these signals is high at any given time.

RUN/STOP

The RUN/STOP circuit consists of an R-S flip-flop and gating to establish the stop condition. The RUN/STOP flip-flop exercises control over PRDY as described above through its Q output. The gating insures that a STOP will occur when DO5, Q2 and PSYNC are true and the STOP switch is depressed.

SS

The Single Step circuit consists of a dual single shot (IC M) for debounce and the SGL STP flip-flop (R-S type). When the machine is in a stopped mode, depressing the SS switch will set the SGL STP flip-flop. (The machine must be stopped for any of the front panel switches except RESET to be active.) This allows PRDY to go high. The machine will execute one machine cycle and PSYNC, on the next cycle, will reset the SGL STP flip-flop. This will pull PRDY low, stopping the machine.

EXM

The Examine circuit consists of a dual single shot (IC L) for debounce, a 2-bit counter (IC J), the top 3 sets of 7405's on schematic 880-106 (IC's A, B, C and 2 gates of D), and some gating.

* In this notation, + means or.

When the Examine switch is depressed the counter (IC J) is started. On the first count, a jump instruction (JMP 303) is strobed directly onto the bi-directional data bus at the processor. This is accomplished by enabling 2 gates of IC C and 2 gates of IC D through the output pin 6 of one gate of IC T. These open collecter gates then pull down data lines D2, D3, D4 and D5. This puts a 303 on the data bus, which is the code for a JMP.

On the second count, the settings of switches SA 0 through SA 7 are strobed onto the data bus in a similar manner to the JMP instruction through IC A and 2 gates of B. This provides the first byte of the JMP address.

The third count strobes the settings for switches SA 8 through SA 15 onto the bus. This provides the second byte of the JMP address. The processor will then execute the JMP to the location set on the switches SA 0 through SA 15, allowing the examination of the contents of that particular memory location.

The fourth count resets the counter and pulls the EXM line low, which in turn pulls PRDY low and stops the processor.

EXM NXT

Examine Next operates in the same manner as Examine, except a NOP is strobed onto the data lines through 4 gates of IC D and 4 gates of IC E. This causes the processor to step the program counter.

DEP

The Deposit circuit places a write pulse on the MWRITE line and enables the switches SA 0 through SA 7. This causes the contents of these eight switches to be stored in the memory location currently addressed.

DEP NXT

The Deposit Next circuit simply causes a sequential operation of the EXM NXT and the DEP circuits.

1K STATIC MEMORY BOARD OPERATION

The 8800 1K Static Memory Board is designed around the Intel 8101 256 X 4 bit static RAM. Two of these RAM's provide 256 8-bit bytes of memory. The board may be configured with a minimum of two 8101's (256 bytes) and may be expanded in increments of 256 bytes by adding pairs of 8101's up to 1024 bytes.

In addition to the RAM's, the board includes 4 circuit units: Address Decoding, Processor Slow Down Circuit, Memory Protect Circuit and Buffers and Buffer Disabling Gating.

Refer to the following schematics for the 1K Static Memory Board operation: 880-107 & 880-108.

ADDRESS DECODING

The address decoding circuitry is in the lower left corner of schematic 880-107. Address bits A10 through A15 are used to select a particular 1K of memory, using IC A and IC B. By patching the inputs of IC B to either the "1" or "0" address inputs for A10 through A15 a board can be assigned any address for a 1K block from 0 to 63.

Address bits A9 and A8 are used to select a particular 256 bytes within the 1K on the board. The gating (IC D, IC F, 2 gates of IC C and 4 gates of IC E) forms a standard 2 to 4 line decoder.

PROCESSOR SLOW DOWN CIRCUIT

Since the 8101 RAM's require 850 nanoseconds for stable data on a read output, it is necessary to insert 2 wait cycles (1us) when the processor reads data from memory.

This is accomplished by IC K, 2 gates of IC N and 1 gate of IC C. This circuit causes the output from pin 8 of IC K to go low for approximately 2 clock cycles starting with PSYNC. If the 1K card has been addressed, and the processor is in a memory read cycle, two of the drivers of IC H will be enabled. This will transmit the low from IC K pin 8 to PRDY on the bus; which will in turn cause the processor to wait for 1us for the data from memory to stabilize.

MEMORY PROTECT CIRCUIT

The Memory Protect circuit consists of an R-S flip-flop (IC L) which can be set or reset by the PROT and UNPROT lines from the system bus when the card is addressed (CE is true).

When the flip-flop is set the pin 11 output of IC N is disabled and MWRITE pulses from the bus cannot get to the 8101's. A status signal, $\overline{PS}$, is returned to the front panel display via the system bus to indicate when the protect flip-flop for a particular memory card is set.

BUFFERS

The output drivers on the 1K board are 8T97 tri-state drivers (IC's J & H). Gating for enabling and disabling these drivers is accomplished with IC G and 1 gate of IC C.

The logic for this is as follows: *

$$\overline{G2} = SINP + SOUT + \overline{CE}$$

OR

$$G2 = \overline{\overline{SINP}} \bullet \overline{\overline{SOUT}} \bullet CE$$

AND

$$\overline{G1} = \overline{SMEMR} + \overline{CE}$$

OR

$$G1 = SMEMR \bullet CE$$

* In this notation + means "or" and • means "and".

POWER SUPPLY OPERATION

The 8800 Power Supply provides two +8 and + & − 16 volts to the system bus and the display/control board. These voltages are unregulated until they reach the individual cards. Each separate card has all the necessary regulation for its own operation.

Refer to schematic 880-109 for the Power Supply operation.

Transformer T1 provides +8 volts unregulated to the system bus. This voltage is rated at 8 Amps. All boards except the display/control board use this supply for their regulated +5 volts.

Transformer T2 provides two unregulated voltages; +8 volts rated at 1 Amp for the display/control board, and +16 rated at .8 Amps to the system bus.

Transformer T3 provides the -16 volt supply rated at .3 Amps to the system bus.

All of the AC and DC voltages are wired to a terminal block for distribution to the other boards.

8800 SYSTEM BUS STRUCTURE

The 8800 system bus structure consists of 100 lines. These are arranged 50 on each side of the plug-in boards. Refer to drawing # 880-110 for the following explanation.

The following general rules apply to the 8800 system bus:

SYMBOLS: "P" prefix indicates a processor command/control signal

"S" prefix indicates a processor status signal

LOADING: All inputs to a card will be loaded with a maximum of 1 TTL low power load.

LEVELS: All bus signals except the power supply are TTL

BUS DEFINITION

No.	SYMBOL	NAME	FUNCTION
1	+8V	+8 volts	Unregulated input to 5v regulators
2	+16V	+16 volts	Positive unregulated voltage
3	XRDY	External Ready	For special applications: Pulling this line low will cause the processor to enter a WAIT state and allows the status of the normal Ready line (PRDY) to be examined
4	VI0	Vectored Interrupt Line #0	
5	VI1	Vectored Interrupt Line #1	
6	VI2	Vectored Interrupt Line #2	
7	VI3	Vectored Interrupt Line #3	
8	VI4	Vectored Interrupt Line #4	

BUS DEFINITION

No.	SYMBOL	NAME	FUNCTION
9	VI5	Vectored Interrupt Line #5	
10	VI6	Vectored Interrupt Line #6	
11	VI7	Vectored Interrupt Line #7	
12 to 17	TO BE DIFINED		
18	$\overline{\text{STA DSB}}$	$\overline{\text{STATUS DISABLE}}$	Allows the buffers for the 8 status lines to be tri-stated
19	$\overline{\text{C/C DSB}}$	$\overline{\text{COMMAND/CONTROL DISABLE}}$	Allows the buffers for the 6 output command/control lines to be tri-stated
20	UNPROT	UNPROTECT	Input to the memory protect flip-flop on a given memory board
21	SS	SINGLE STEP	Indicates that the machine is in the process of performing a single step
22	$\overline{\text{ADD DSB}}$	$\overline{\text{ADDRESS DISABLE}}$	Allows the buffers for the 16 address lines to be tri-stated
23	$\overline{\text{DO DSB}}$	$\overline{\text{DATA OUT DISABLE}}$	Allows the buffers for the 8 data output lines to be tri-stated
24	ϕ2	Phase 2 Clock	
25	ϕ1	Phase 1 Clock	
26	PHLDA	Hold Acknowledge	Processor command/control output signal which appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state

BUS DEFINITION

No.	SYMBOL	NAME	FUNCTION
27	PWAIT	WAIT	Processor command/control output signal which acknowledges that the processor is in a WAIT state
28	PINTE	INTERRUPT ENABLE	Processor command/control output signal indicating interrupts are enabled: indicates the content of the CPU internal interrupt flip-flop; F-F may be set or reset by EI and DI instruction and inhibits interrupts from being accepted by the CPU if it is reset
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15	
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DO1	Data Out Line #1	
36	DO0	Data Out Line #0	
37	A10	Address Line #10	
38	DO4	Data Out Line #4	
39	DO5	Data Out Line #5	
40	DO6	Data Out Line #6	
41	DI2	Data In Line #2	
42	DI3	Data In Line #3	
43	DI7	Data In Line #7	

BUS DEFINITION

No.	SYMBOL	NAME	FUNCTION
44	SM1	M1	Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction
45	SOUT	OUT	Status output signal which indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{\text{PWR}}$ is active
46	SINP	INP	Status output signal which indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active
47	SMEMR	MEMR	Status output signal which indicates that the data bus will be used for memory read data
48	SHLTA	HLTA	Status output signal which acknowledges a HALT instruction
49	$\overline{\text{CLOCK}}$	$\overline{\text{CLOCK}}$	Inverted output of the 2MHz oscillator that generates the 2 phase clock
50	GND	GROUND	
51	+8V	+8 volts	Unregulated input to 5v regulators
52	-16V	-16 volts	Negative unregulated voltage
53	$\overline{\text{SSW DSB}}$	$\overline{\text{SENSE SWITCH DISABLE}}$	Disables the data input buffers so the input from the sense switches may be strobed onto the bidirectional data bus right at the processor
54	$\overline{\text{EXT CLR}}$	$\overline{\text{EXTERNAL CLEAR}}$	Clear signal for I/O devices (front panel switch closure to ground)

BUS DEFINITION

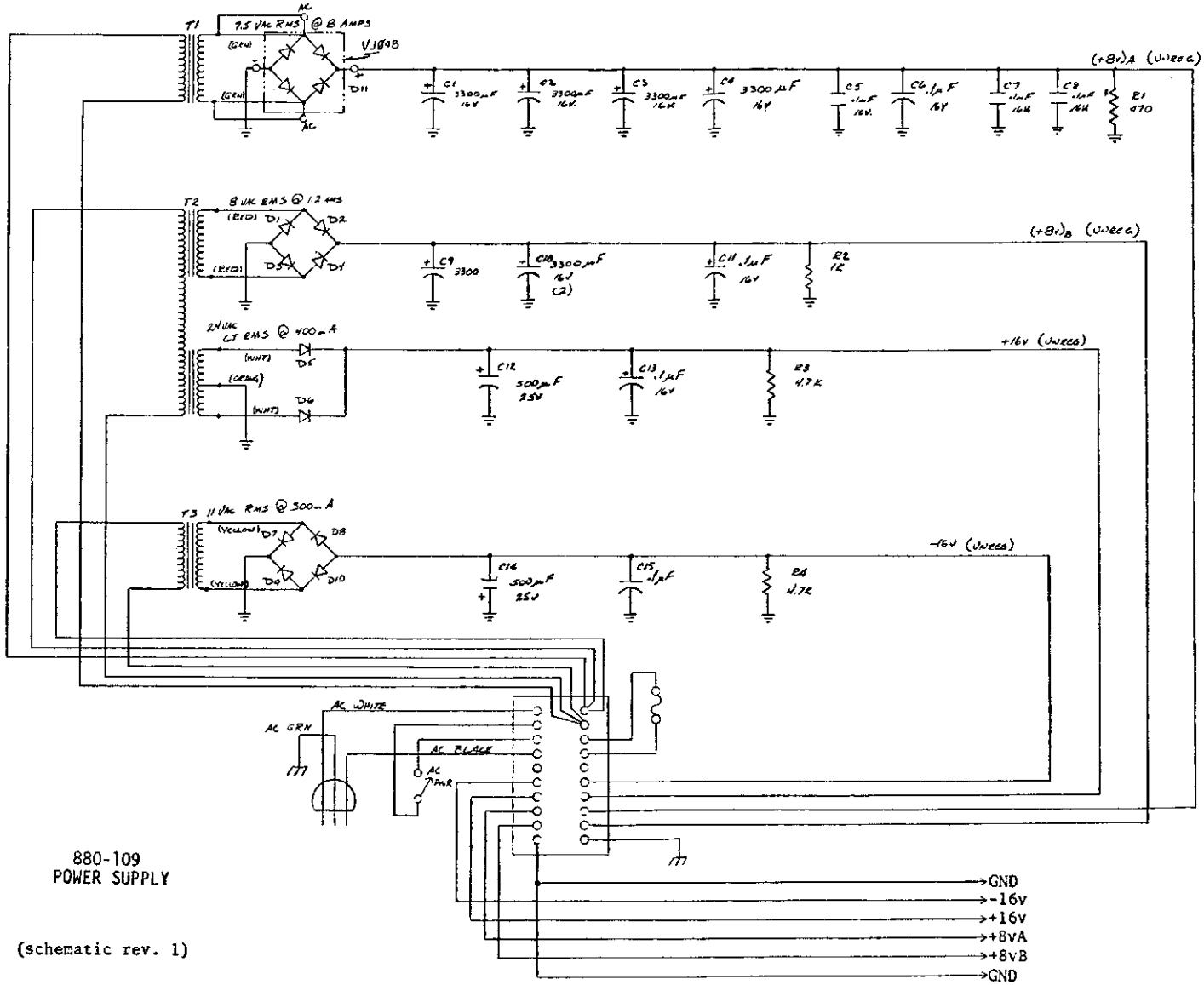
No.	SYMBOL	NAME	FUNCTION
55 to 67	TO BE DEFINED		
68	MWRT	MEMORY WRITE	Indicates that the current data on the Data Out Bus is to be written into the memory location currently on the address bus
69	$\overline{\text{PS}}$	$\overline{\text{PROTECT STATUS}}$	Indicates the status of the memory protect flip-flop on the memory board currently addressed
70	PROT	PROTECT	Input to the memory protect flip-flop on the memory board currently addressed
71	RUN	RUN	Indicates that the RUN/STOP flip-flop is Reset
72	PRDY	READY	Processor command/control input that controls the run state of the processor; if the line is pulled low the processor will enter a wait state until the line is released
73	$\overline{\text{PINT}}$	$\overline{\text{INTERRUPT REQUEST}}$	The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request.
74	$\overline{\text{PHOLD}}$	$\overline{\text{HOLD}}$	Processor command/control input signal which requests the processor to enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle

BUS DEFINITION

No.	SYMBOL	NAME	FUNCTION
75	$\overline{\text{PRESET}}$	$\overline{\text{RESET}}$	Processor command/control input; while activated the content of the program counter is cleared and the instruction register is set to 0
76	PSYNC	SYNC	Processor command/control output provides a signal to indicate the beginning of each machine cycle
77	$\overline{\text{PWR}}$	$\overline{\text{WRITE}}$	Processor command/control output used for memory write or I/O output control: data on the data bus is stable while the $\overline{\text{PWR}}$ is active
78	PDBIN	DATA BUS IN	Processor command/control output signal indicates to external circuits that the data bus is in the input mode
79	A0	Address Line #0	
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DO2	Data Out Line #2	
89	DO3	Data Out Line #3	
90	DO7	Data Out Line #7	
91	DI4	Data In Line #4	

BUS DEFINITION

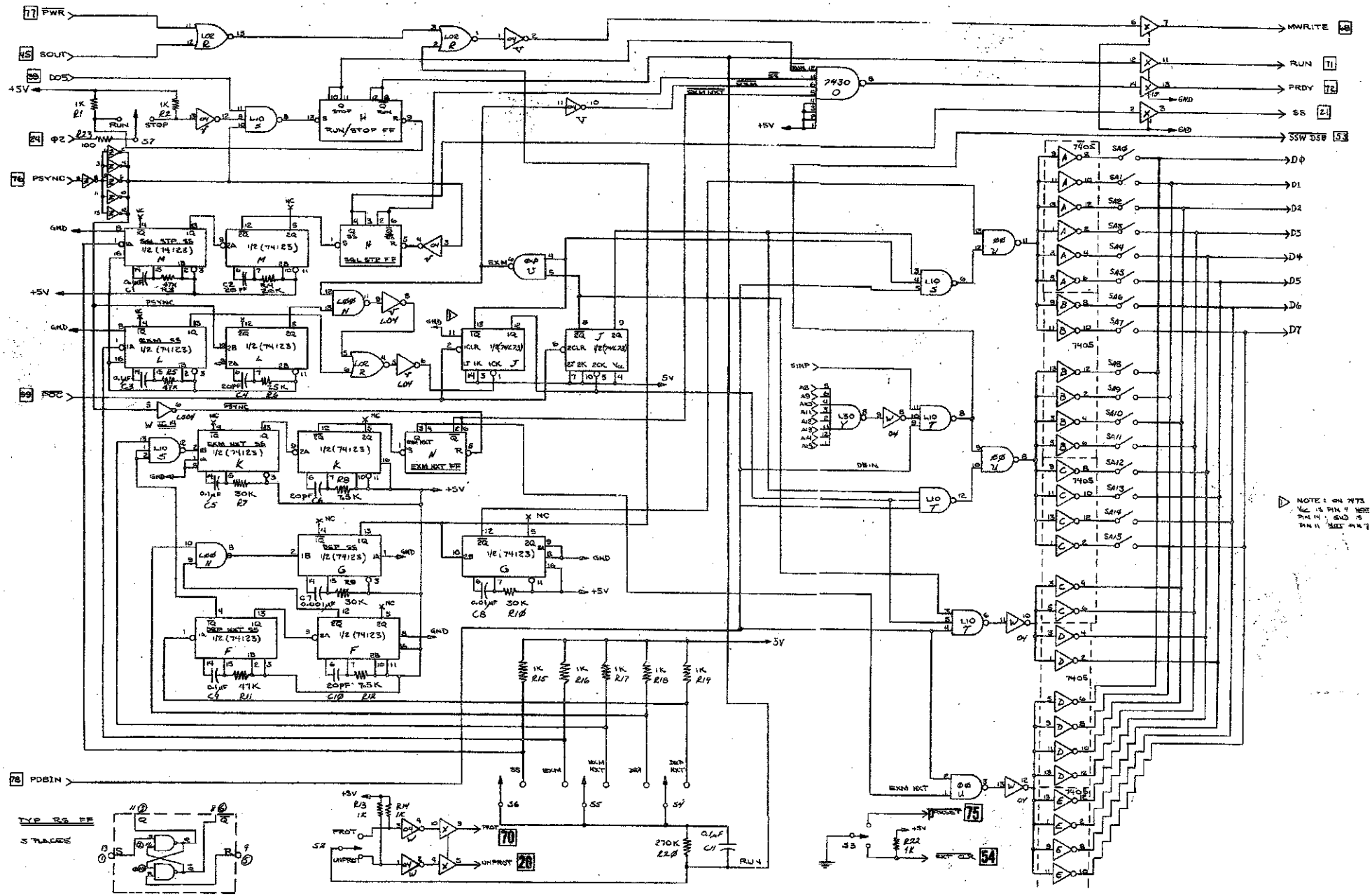
No.	SYMBOL	NAME	FUNCTION
92	DI5	Data In Line #5	
93	DI6	Data In Line #6	
94	DI1	Data In Line #1	
95	DI0	Data In Line #0	
96	SINTA	INTA	Status output signal to acknowledge signal for INTERRUPT request
97	SWO	WO	Status output signal indicates that the operation in the current machine cycle will be a WRITE memory or output function
98	SSTACK	STACK	Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer
99	$\overline{\text{POC}}$	Power-On Clear	
100	GND	GROUND	

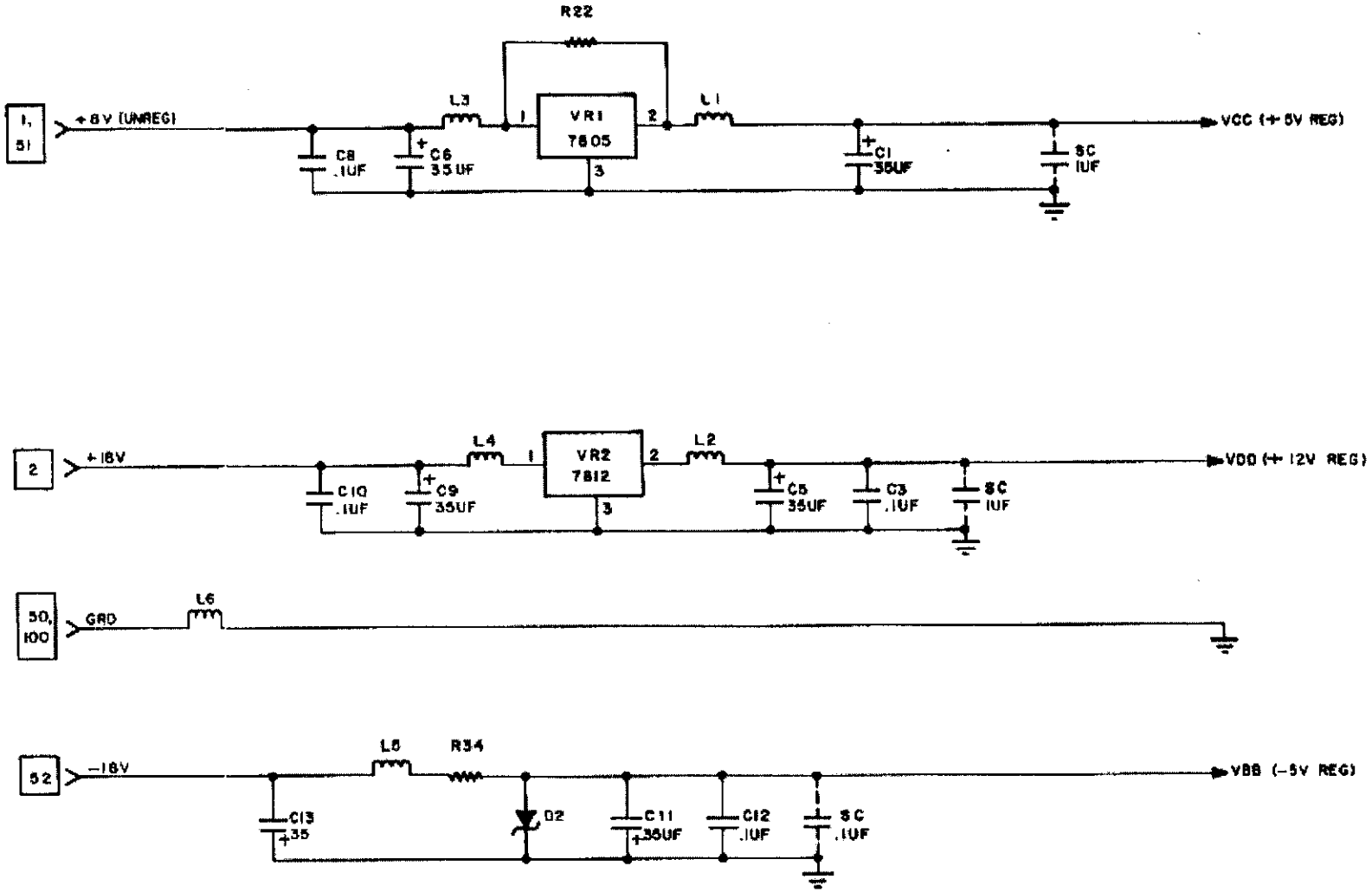


880-109
POWER SUPPLY

(schematic rev. 1)

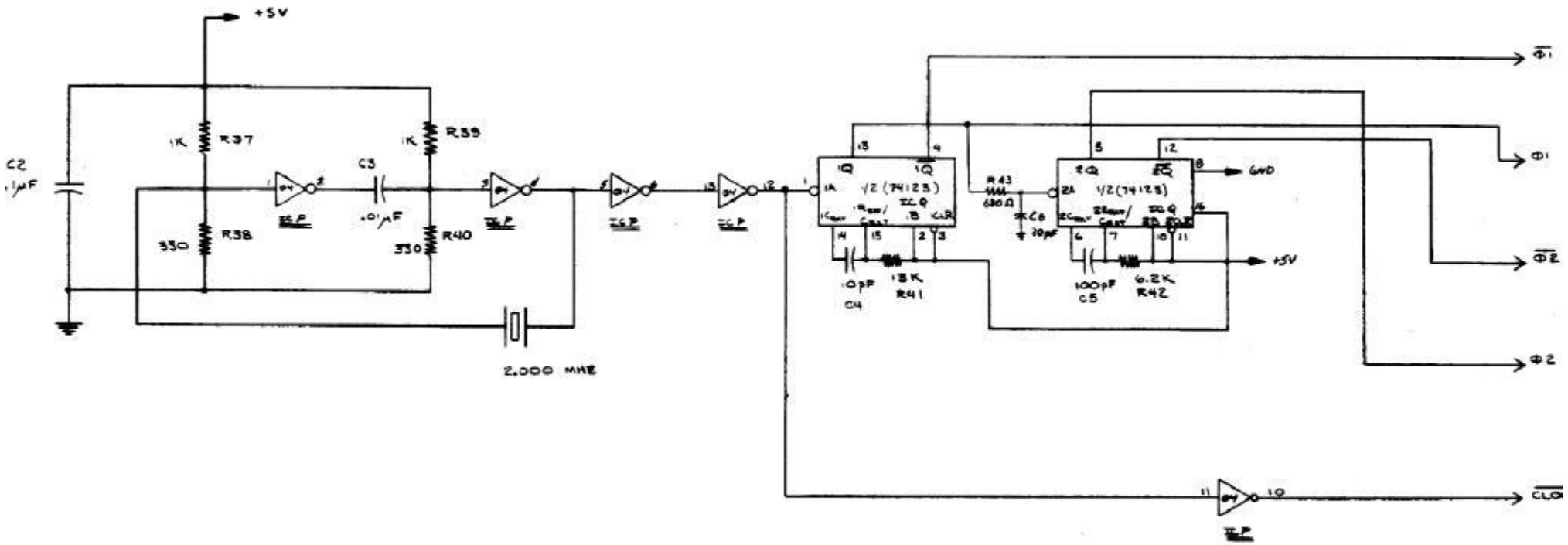
880-106
COMPUTER FRONT PANEL CONTROL





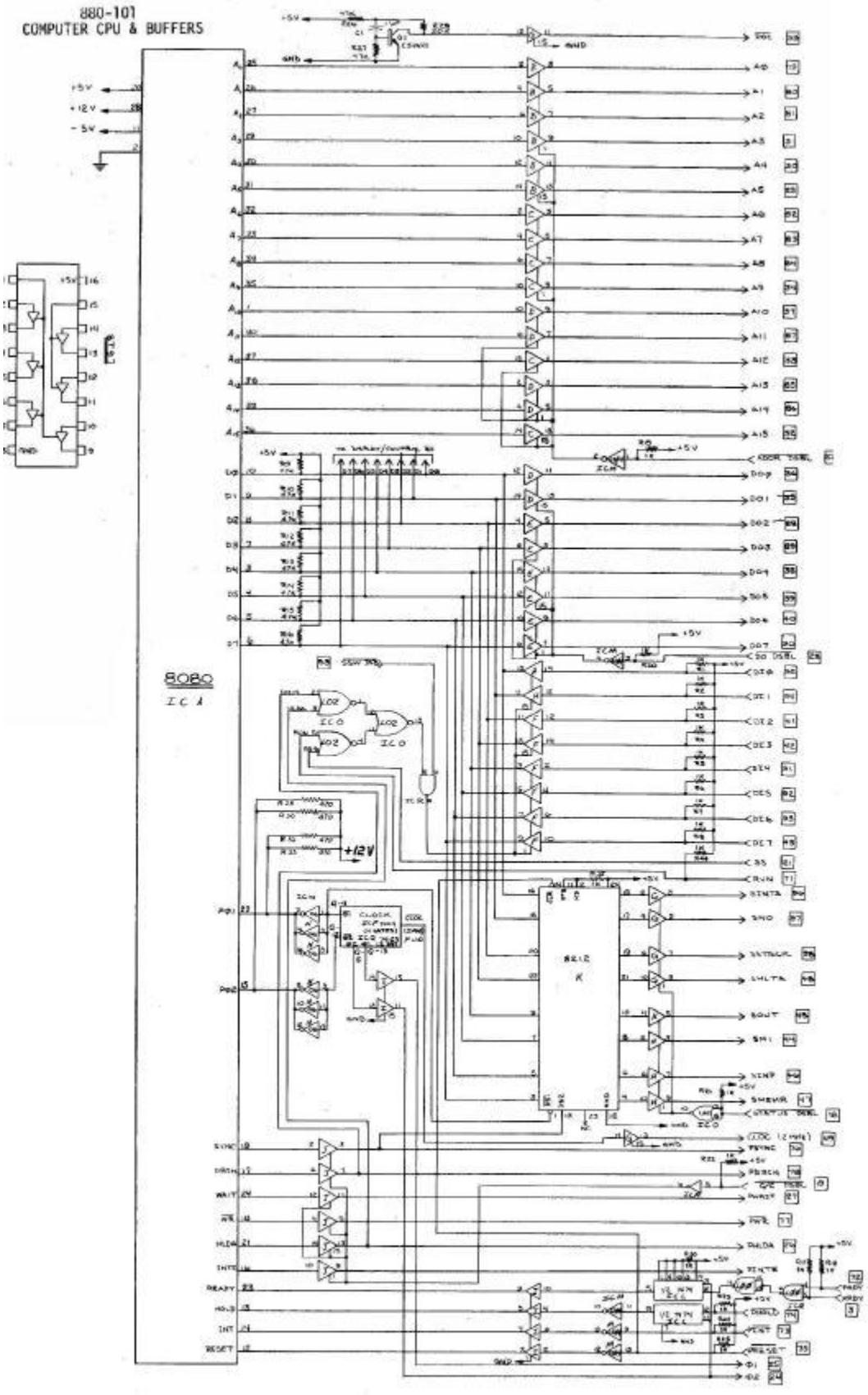
REF DESIG	TYPE	VCC	GRD	OTHER	REF DESIG	TYPE	VCC	GRD	OTHER
					M	8080A	20	2	
G, B	74LS04	14	7		J, X, R, V, N, U, P	74368 OR 8T98	16	8	
C	74LS13 OR 74LS20	14	7		K	8212	24	12	
S, Y	74LS14	14	7		D, E	8216	16	8	
					F	8224	18	8	VDD = 9
P, W	74367	16	8		A	4009	1	8	VDD = 16

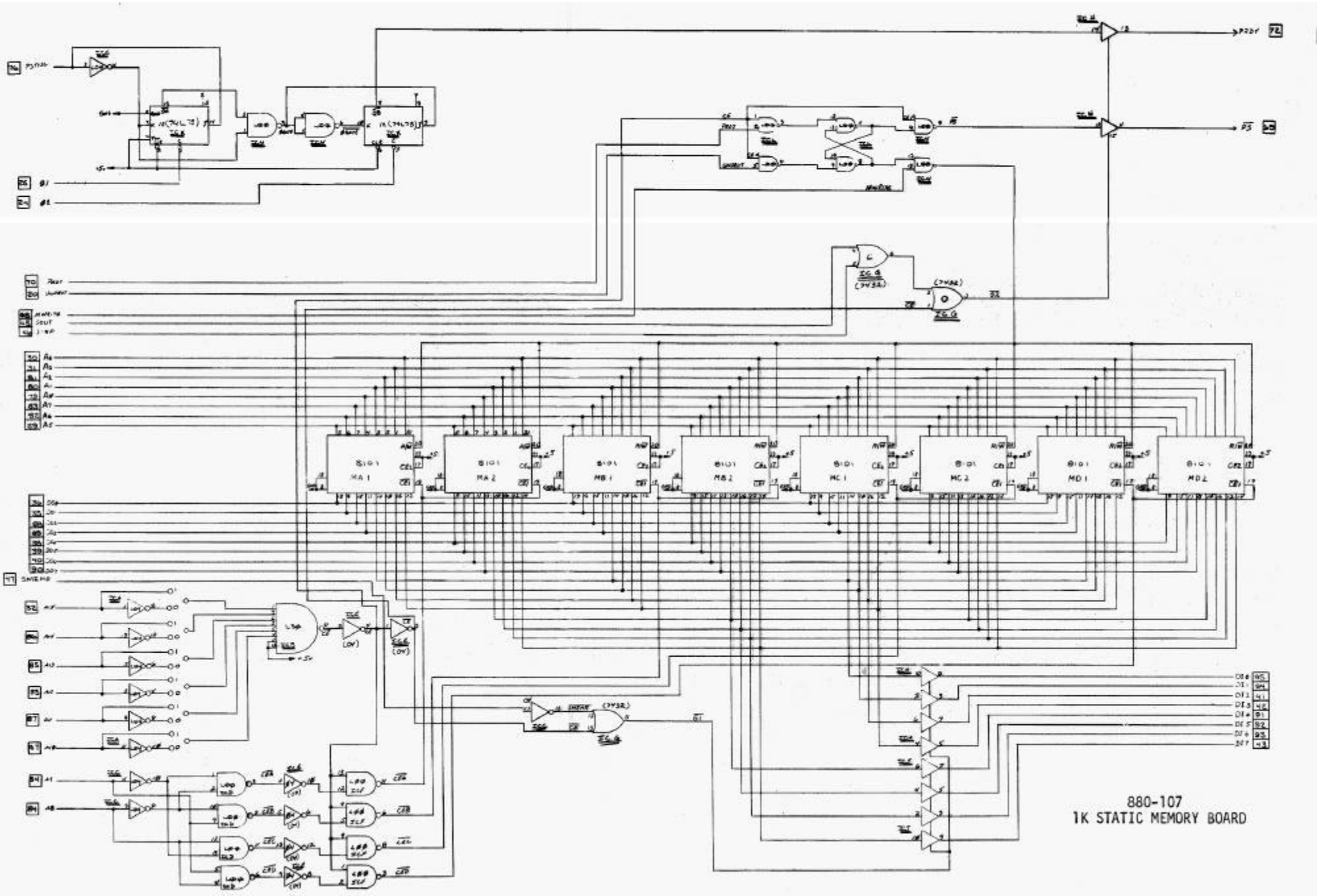
Figure 3-18. CPU Voltage Regulator Schematic

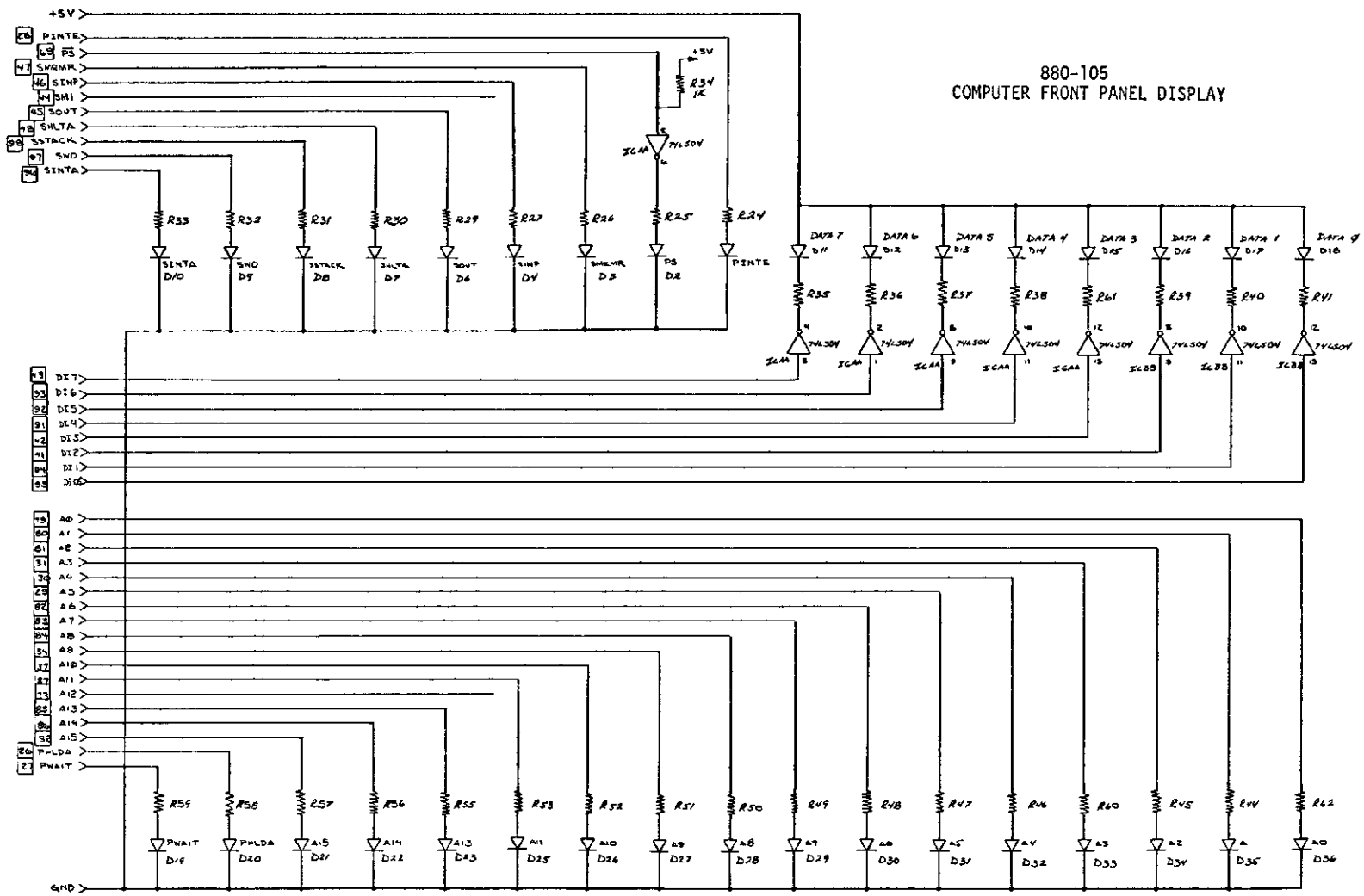


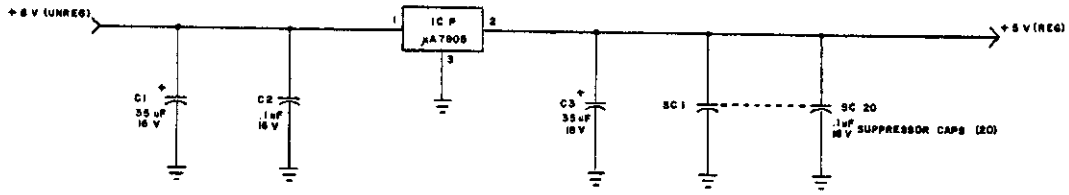
880-102
SYSTEM CLOCK

880-101
COMPUTER CPU & BUFFERS

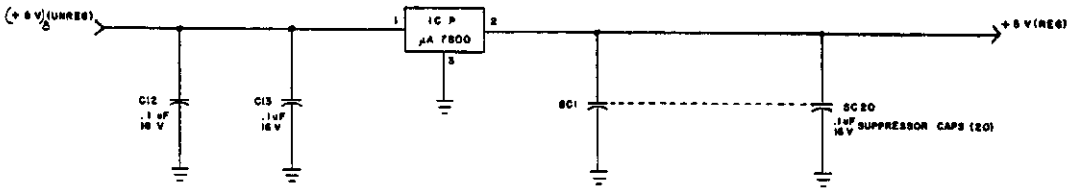



880-107
1K STATIC MEMORY BOARD


880-105
COMPUTER FRONT PANEL DISPLAY
+5V
PINTE
PS
SWRMR
SINP
SMI
SOUT
SHLTA
SSTACK
SWO
SINTA
R33
R32
R31
R30
R29
R27
R26
R25
R24
R34
1K
74LS04
SINTA D10
SWO D9
SSTACK D8
SHLTA D7
SOUT D6
SINP D4
SWRMR D3
PS D2
PINTE
DATA 7 D11
DATA 6 D12
DATA 5 D13
DATA 4 D14
DATA 3 D15
DATA 2 D16
DATA 1 D17
DATA 0 D18
R35
R36
R37
R38
R61
R39
R40
R41
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
PHLDA
PWAIT
R59
R58
R57
R56
R55
R53
R52
R51
R50
R49
R48
R47
R46
R60
R45
R44
R42
PWAIT D19
PHLDA D20
A15 D21
A14 D22
A13 D23
A12 D25
A10 D26
A9 D27
A8 D28
A7 D29
A6 D30
A5 D31
A4 D32
A3 D33
A2 D34
A1 D35
A0 D36
GND

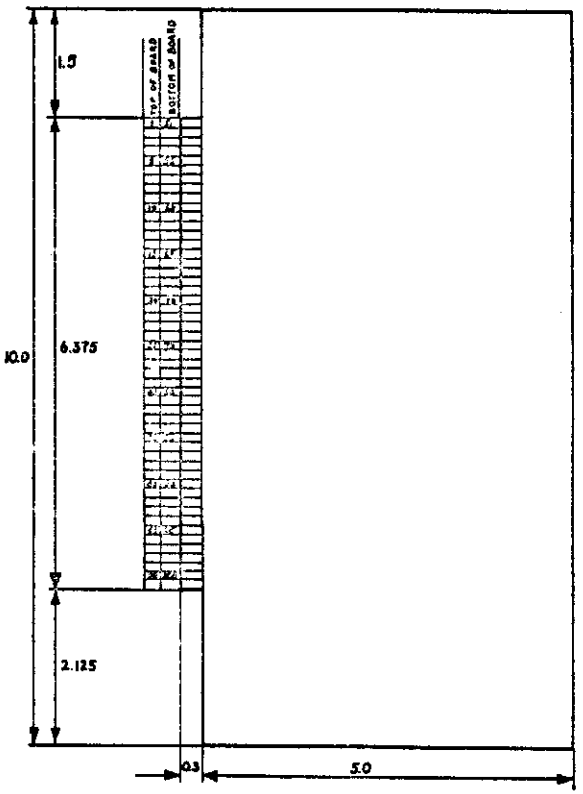


880-108
1K STATIC MEMORY ON-BOARD REGULATOR



880-104
DISPLAY/CONTROL ON-BOARD REGULATOR

TOP OF BOARD		BOTTOM OF BOARD		
1	+ 5 V	51	+ 5 V	A
2	+ 15 V	52	-15 V	B
3	XRDY	53	SSW DSB	C
4	VI 0	54	EXT CLR	D
5	VI 1	55		E
6	VI 2	56		F
7	VI 3	57		H
8	VI 4	58		J
9	VI 5	59		K
10	VI 6	60		L
11	VI 7	61		M
12		62		N
13		63		P
14		64		R
15		65		S
16		66		T
17		67		U
18	STAT DISABLE	68	MWRT	V
19	C/C DISABLE	69	PS	W
20	UNPROTECT	70	PROT	X
21	SS	71	RUN	Y
22	ADD DISABLE	72	PRDY	Z
23	DO DISABLE	73	PINT	a
24	ø2	74	PHOLD	b
25	ø1	75	PRESET	c
26	PHLD	76	PSYNC	d
27	PWAIT	77	PWR	e
28	PINTE	78	PDBIN	f
29	A5	79	A9	h
30	A4	80	A1	j
31	A3	81	A2	k
32	A15	82	A6	l
33	A12	83	A7	m
34	A8	84	A8	n
35	DO1	85	A13	o
36	DO0	86	A14	r
37	A10	87	A11	s
38	DO4	88	DO2	t
39	DO5	89	DO3	u
40	DO6	90	DO7	v
41	DI2	91	DI4	w
42	DI3	92	DI5	x
43	DI7	93	DI6	y
44	SM1	94	DI1	z
45	SOUT	95	DI0	AA
46	SINP	96	SINTA	AB
47	SMEMR	97	SWO	AC
48	SHLTA	98	SSTACK	AD
49	CLOCK (2MHz)	99	POE	AE
50	GND	100	GND	AF



880-110
SYSTEM BUS STRUCTURE