Old Style Altair 8800bt Turnkey Board

Pages from 8800bt Manual

2-3. The Turnkey Module

The Turnkey Module contains 1Ø24 bytes each of RAM and PROM, a serial I/O channel, AUTO-START logic, sense switch, the front panel board and logic and miscellaneous logic. The Turnkey Module schematic is shown in Figures 2-4 a, b and c.

A. RAM and PROM. The RAM and PROM memories and their control logic are shown in the schematic diagrams, Figures 2-4 a and c.

1) The incoming PROM address is compared with the starting PROM address by the NAND gate IC D. If the incoming address is in the 1K block selected for PROM, the output of IC D, active LOW, enables the PROM address decoder, IC Za, which selects one of the PROM ICs. Up to four PROM chips may be installed. The output of IC D is also combined with the output of the I/O address detector in a NOR gate, the output of which causes the CPU to execute a WAIT state and enables the data bus interface, IC's P and R. The selected PROM drives the bidirectional data bus and the interfaces P and R put the selected data on the Data-In system bus.

2) An address of a byte in RAM is detected by IC B. The output of IC B is active if a start sequence is not in progress and the current machine cycle is not an I/O cycle or an interrupt. Therefore, the only time a RAM address is detected is when the machine cycle is a memory cycle or a Halt cycle. The output of IC B enables the RAM ICs and the data bus interfaces P and R. The direction of the data bus is controlled by the MWRT pulse described in paragraph 2-3F. When RAM is selected, data at the address is put on the bidirectional bus. If the cycle is a memory read, the cycle is complete. If it is a write cycle, the direction of the data bus interfaces is momentarily reversed, overdriving the RAM output drivers. Pulsing the RAM write inputs then causes the data on the bus to be written in the addressed location.

B. AUTO-START. The AUTO-START logic causes the computer to jump to the address designated by the AUTO-START switches when the power is turned on or the START switch is actuated. Figure 2-5 shows the arrangement of the AUTO-START logic. The switches represent the variable byte in a JMP instruction. The JMP instruction is generated by a multiplexer, ICs M and N, which is controlled by flip-flops Ta, Sa and Sb. The flip-flops are cleared by PRESET, a bus signal derived from POC or generated by the START switch on the front panel. Subsequent PDBIN pulses cause the flip-flops to change from one state to the next as shown in the sequence diagram, Figure 2-6. The pulses generated by the flip-flops cause the multiplexer to choose one of three possible bytes; 303 octal, 000 octal or byte designated by the AUTO-START switches.

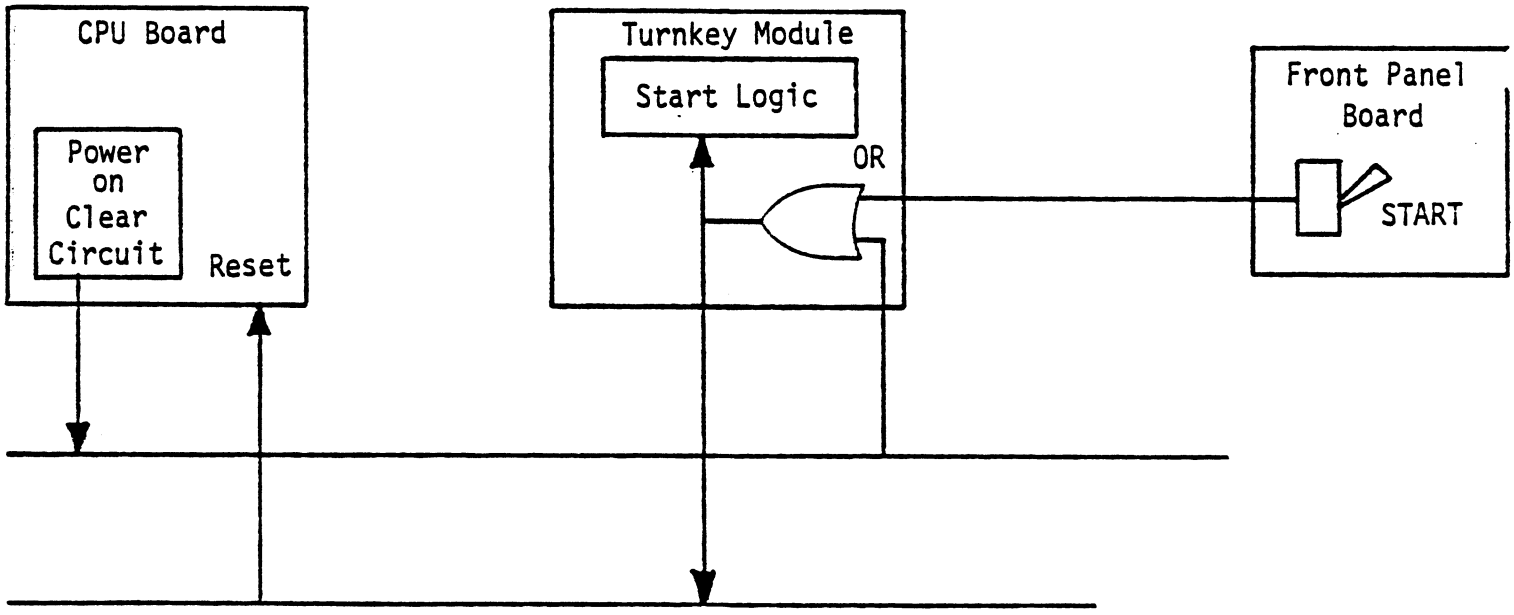

Figure 2-5
AUTO-START Block Diagram

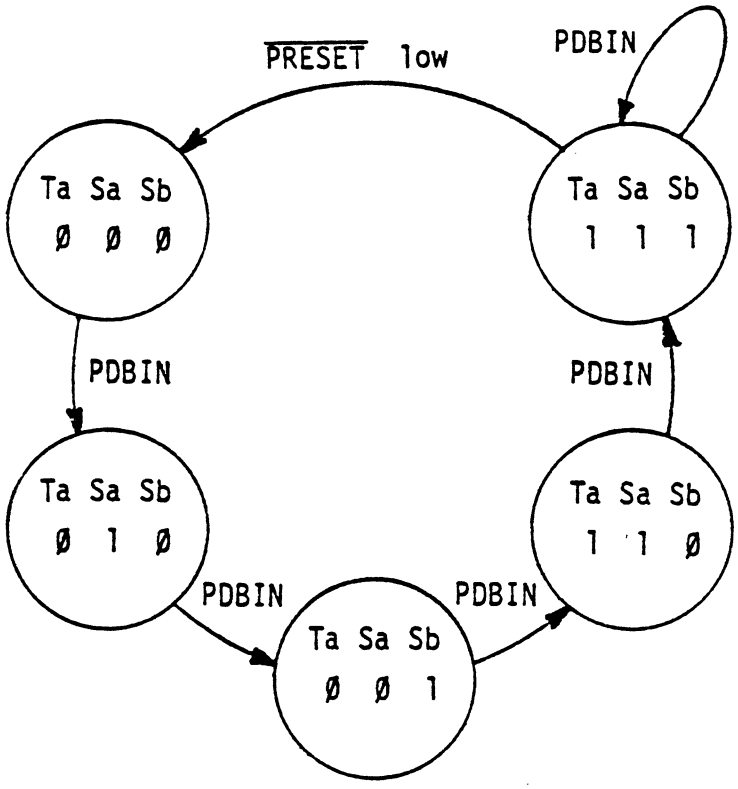

Figure 2-6
AUTO-START Logic
Control State Diagram

These bytes are placed on the bidirectional data bus in sequence and become the AUTO-START JMP instruction. Table 2-A shows the sequence of events in the AUTO-START procedure.

Table 2-A

Signal In	Control State	Function
PRESET	000	Mux. outputs enabled, Bus interface enabled, 303 octal put on bus.
PDBIN	010	000 put on bus.
PDBIN	001	Byte in address switches put on the bus.
PDBIN	110	First byte of PROM program
PDBIN	111	Next byte of PROM program
.	.	.
.	.	.
.	.	.

During the three bytes of the JUMP instruction, the HIGH Q output of flip-flop Ta is used to drive transistor Q2 to hold MEMR low and keep memory data off the bus. Once the JUMP instruction is complete, Q goes LOW and memory instructions can be fetched.

C. Sense Switches. The sense switch circuitry is shown in Figure 2-4 a and b. IC K (Figure 2-4a) detects I/O port address 255 decimal (377 octal), which is reserved for the sense switches. The output, active LOW, enables the tri-state buffers connected to the sense switches (Figure 2-4b) putting the bits represented by the switch positions on the bidirectional bus. IC K also enables the bus interface, so the sense switch bits are placed on the Data-In system bus.

D. Serial I/O Channel (SIO). The SIO schematic is shown in Figure 2-4b. The heart of the SIO is the 6850 Asychronous Communications Interface Adapter. The ACIA contains all the Status and Control registers discussed in section 3-2 and most of the timing and control circuitry. The bit rate is generated by a 34702 integrated circuit whose timing

reference is a 2.4576 MHz crystal. Jumpers are provided to set the output rate of the 34702 at 1, 16 or 64 times the required bit rate.

Input signals are received by RS232 receivers that may be made compatible with TTL or current loop signals by means of jumper-selected pullup resistors. TTL or RS232 outputs may be selected by jumpers or by internal cable wiring.

E. Front Panel. The front panel logic is contained on the Turnkey Module board. The indicators and switches are connected to the Turnkey Module by a cable and Molex connectors. The schematic diagram for the front panel circuitry is in Figure 2-4a.

The bus signals PHLTA, PINTE and $\overline{\text{PINT}}$ are buffered to drive the indicators HALT, INTE and INT, respectively. The I/O indicator is driven by the logical sum (OR) of the INP and OUT signals. The POWER indicator monitors the +5 volt supply on the Turnkey Module.

The bus signal PRDY is grounded when the RUN/STOP switch is in the STOP position. PRESET is grounded momentarily by the START switch which, in turn, initiates the AUTO-START sequence. Contact bounce is filtered out on the CPU board to generate a reset signal suitable for the CPU.

F. Miscellaneous Signals. Several miscellaneous signals are handled by the rest of the circuitry on the Turnkey Module. Some are optional and may be selected by jumpers.

1. MWRT is generated if the jumper from M1 to M2 is installed. In the full front panel version, MWRT is generated by the front panel logic and is used by memory boards of write functions.
2. PROT and UNPROT are used on the standard model of the Altair 8800b for memory protect and unprotect functions. As supplied, the Turnkey Module grounds PROT and pulses UNPROT with phase 2 of the clock to unprotect all memory as it is accessed. This feature may be disabled by removing the jumpers from 2 to UM and from G to PM.

3. AUX CLR is normally pulled HIGH by a resistor on the Turnkey Modlue, but insertion of optional jumpers as described in section 3-4b allows the signal to be used.

G. Power. All power used on the Turnkey Module and Front Panel boards comes from the +18 volt, -18 volt and +8 volt lines on the motherboard. The Turnkey Module's power regulator circuitry is shown in Figure 2-4a. The +5 volt supply is derived from the +8 volt line by an IC regulator. The +9 volt supply comes from the +18 volt line through a zener regulator and the -0 volt supply is derived by a transistor-zener regulator from the -18 volt line.

Figure 2-6 is the schematic for the power circuits in the 88ØØb case. The +18 and -18 volt supplies are pre-regulated. The +8 volt supply is not regulated, but it is adjusted by the taps on the secondary of the power transformer. See Section 3-5.