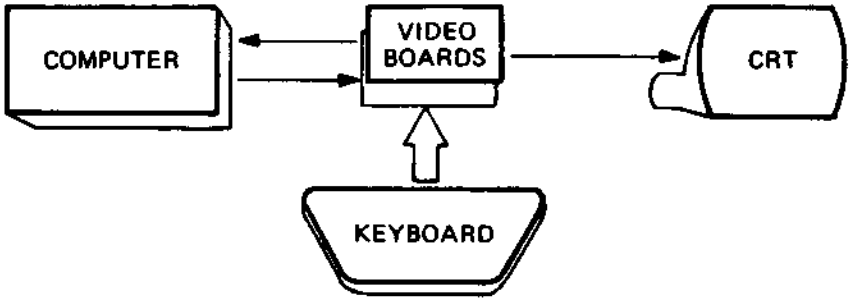
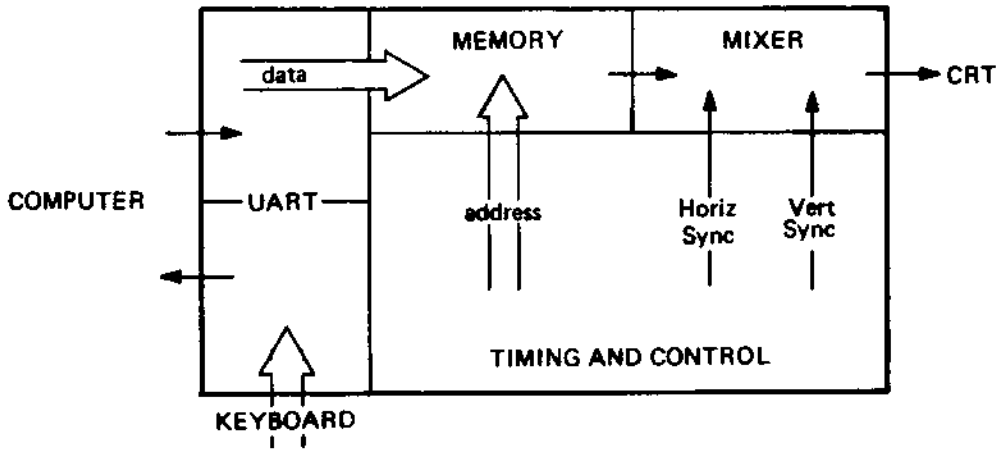
APPENDIX A

VIDEO BOARD THEORY OF OPERATION

The video boards integrate a CRT, keyboard, and computer. Parallel information from the keyboard is serialized and sent to the computer. The boards store and transform serial data from the computer for display on the CRT. Other than characters, the CRT requires synchronization signals for scanning.



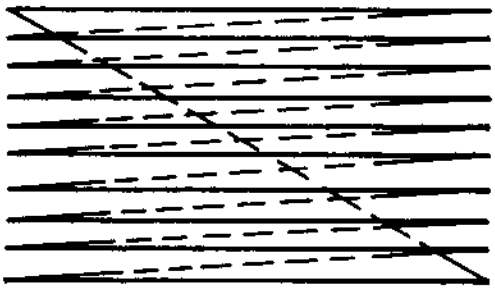
A universal asynchronous receiver transmitter (UART) performs the serial-parallel task between keyboard and computer; and computer and video memory. The video memory refreshes the screen. Timing and control logic addresses the memory and creates synchronization signals (syncs). The characters of the memory are mixed with the sync signals and are made available to the CRT chassis through a coaxial cable.



The Timing and Control Section is composed of a timing chain, character insertion logic, power up clear, character generator, and a cursor comparator. The timing chain creates the sync signals and supplies the cyclic memory addresses. The character insertion logic respondsto the UART, inserting the new character at its cursor address without disturbing the refresh. Power up clear removes all images from the CRT with carriage return characters. The character generator transforms parallel ASCII forms from memory to serial dots and no-dots for the screen. The cursor comparator places a white square on the CRT so the operator may pin-point his location along the bottom row.

Timing and control is a dot refresh cycle, cleared upon power-up, capable of adding new characters, which provides an operator cursor.

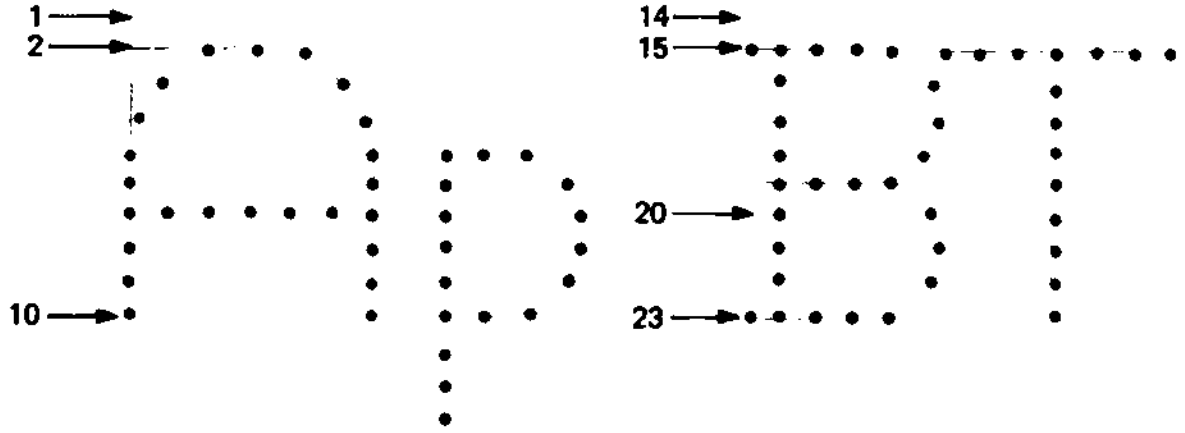
The CRT requires a Composite Video signal. The 13.4784 MHz dot frequency is related to the CRT raster by the 15.75 KHz horizontal sync and the 60 Hz vertical sync. These signals are separated in the CRT chassis by band pass filters. The raster scan traverses the screen in the following manner:



Horizontal: frequency = 15.75 KHz
period = 63.5 μsec

Vertical: frequency = 60 Hz
period = 16.67 msec

The dashed raster retraces are very quick and occupy little of the scan time. The slope of the horizontal trace is about 60 Hz/15.75 KHz or 0.0038. The entire screen is crossed by about 256 very nearly horizontal traces. Each row of characters is composed of 13 traces leaving about 50 unused traces divided above and below the full character screen. The 13 MHz wave turns the beam on and off for dots while the syncs trigger the raster at its endpoints along the margins of the scan. In painting the two rows shown below the beam must make 26 passes. On row 15 below, B's top then T's top is painted before retracing and lower sections are refreshed.



The data frequency is switching the beam on and off. The blank row between the p and t is produced by the generator itself. Vertical blanks between the characters is loading time for the shift register which follows the character generator. Each row is constructed of strata. All of this information in the Composite wave passes through a coaxial cable.

On the board the Composite wave is synthesized. The data wave from B-4, the sync wave from B-6, and the cursor wave from B-12 are added at the node below R9. The relative amplitude of the waves are set through resistors R11, R10, and R12. M-5 is the vertical sync, Y-5 the horizontal sync, Z-6 the data wave, and D4 is the cursor wave. R9 matches the impedance of the coaxial cable.

All the different frequencies needed to generate the data as well as the sync pulses range from 60 Hz to 13 MHz. The 13 MHz wave is available at chip R pin 10. Chip T uses the 13 MHz to convert the parallel dots from the generator C1, to a serial stream for the video. Chip S converts the 13 MHz dot rate to a slower character rate. A rate about one eighth as fast is available at S-11 (MSCLK) and A-12. S-11 is used to load the shift register T with a new dot character from the generator. A-12 synchronizes the timing chain. E1 and F address one line of characters. E-3 forms a sharp negative going pulse rate at the beginning of each line, which is used to clear the RS flop at E-8 and E-6 to unblank for the new line. E-3 resets F at pin 9 as the new row is to begin. We recall that 13 passes are needed to paint a character row. C-6 with the aid of N-10 decodes G and looks for a 13 to increment H via A-10. H is the character row counter. When H counts out (16 rows) it toggles P to the set state, which in turn presets H to 12 and blanks the screen until H counts out again. After 4 counts H toggles P again, ending the vertical blank period which lasted 1/5 of total time (16+4)/4). Once at the top of the screen dots may pass through to Z-6. P also provides a level from its Q side to the pulse shaping circuitry of the vertical sync at M-2. Before leaving the timing chain, G-14 to G-11, are used to inform the generator of the present strata of the character row we are on so that it lays out the proper layer of dots for the character presently being painted.

The majority of the time, the video boards are merely refreshing the CRT with the RAMS. When a key is struck on the keyboard or information is received from the computer, changes occur.

The keyboard pulls pin 23 of the UART low to signal the validity of the data bus over pins 26-33. Over pin 25 the UART transmits the ASCII key at a rate specified by 1/16th of pin 40. If in local a low from the keyboard shall select the K-14 to K-13 path back to the UART at pin 20. A line high from the keyboard enables the K-2 to K-3 path to let the computer send data to pin 20. Pin 20 is set to receive data at 1/16th the rate specified at pin 17. The baud rate figures in the sketch account for this division by 16.

When a signal is received at pin 20, the UART sets DA-H. It will remain high until the interstate machine is done and resets it. DA-H raises pin 7 of W allowing it to count, beginning at zero. At the count of 1, pin 2 falls as pin 1 joins the rest of the outputs at a high level. The high fan-in flip-flop at T brings CA-SEL to a low, which selects the cursor address for RAMS rather than the refresh address of the timing chain. At the count of 2, pin 3 falls pulling RAM R/W low. With the cursor address available to the RAMS, the character present on the RD0 to the RD6 lines from the UART is written into

the memory at the cursor location. After pin 3 rises RAM R/W rises and pin 4 falls.

Pin 4 puts a low at M-3 anticipating a possible carriage return which will be valid until pin 6 time, when the RS flop M is reset. If the key was a carriage return, then the cursor row counter H is to be incremented through N-1, P-11, and H-8. During pin 5 time, the CA-SEL is no longer low and CRDET-L may reset the cursor count through pin 6 of P. At pin 6 time besides disabling CRDET-L's from bumping the cursor row count, chip E is bumped advancing the cursor address. If a control character is detected through CTL-L no advance of the cursor is possible. Notice the chips E and F which hold the cursor address within a line may advance the row count at H through P12. This provides an automatic line advance on the CRT. At pin 9 time, the CA-SEL is brought low again, and the RS flop L output FCR-L is lowered. FCR-L via L-6 tri-states the UART from the RD0-RD6 bus and places a carriage return on the bus with the drivers U and D. At pin 10 time, the CR is written into the RAMS as RAM R/W falls low. The CR is a dummy used to blank the remaining portion of the row as it is placed immediately after the newly inserted character. The DA-H level of the UART is reset as RDA-L falls. The machine will then finish counting to zero when pin 1 will fall breaking the loop through X-5. The interstate machine has written the new key into the RAMS at the old cursor address, updated the address by one, written a dummy blank CR at the new cursor address, and reset the flag in the UART. The refresh cycle may resume.

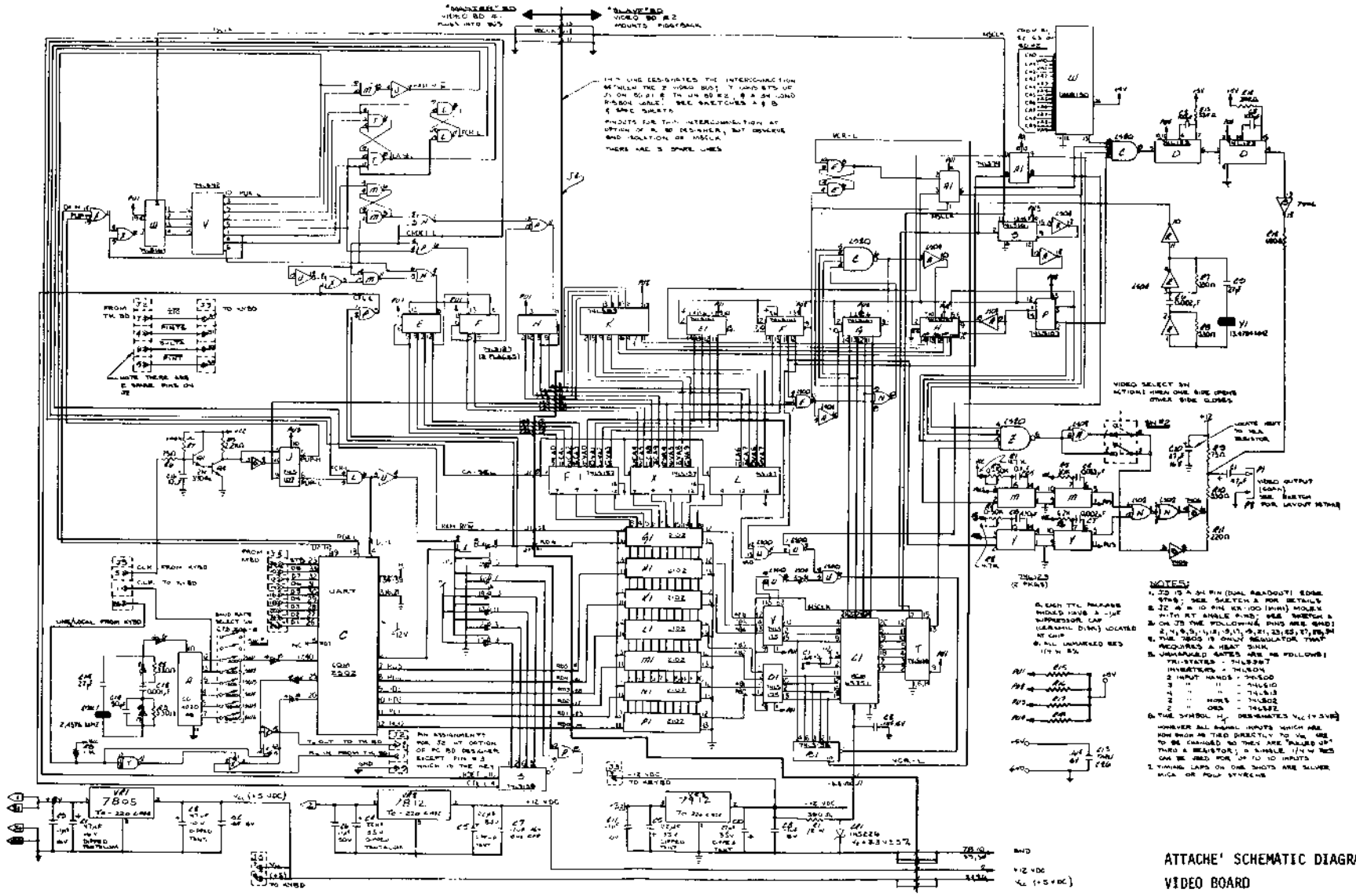
There is another possible interruption to the refresh cycle - a clear. When Vcc comes up on the boards, C16 begins to charge up through R7. Until Q1 is switched on, Q2 is off holding the j side of the flop J high and its k side low. When VA4 clocks the flop is set with PUP-H. PUP-L tri-states the RD0-RD6 pins of the UART and places a CR on the bus through the U and D drivers. PUP-H enables the interstate machine at X-12. The J-K flop J will reset after 16 cycles since the MSCLK at W-2 is 16 times faster than VA-4 at J-9. Each CR will force a CRDET-L to bump the cursor row counter through N-3 at H-8, since it will be valid between W-4 and W-6 time. VCR-L will blank out a memory with all sixteen rows led by a carriage return. A clear button on the keyboard is also provided a line to the base of Q1 to simulate a power on clear.

The cursor row is always presented at the bottom of the CRT due to the activity of chip K. K adds the cursor row address to the timing row address (PVA6-PVA9) making the video row relative to the cursor row in time. The relation between the PVA count and the vertical blank sets the cursor row at the bottom of the screen.

The cursor, unlike the rest of the characters, is placed on the screen by means of a comparator and pulse shapers. W, a comparator, puts out a high at pin 13 when the VA and CA lines are in agreement. The other inputs are related to the blanks that appear at the lower Z nand gate. C8 then represents a cursor sync. Passing through the first single shot the cursor is delayed to appear at the appropriate moment just after the last inserted character. D-1 takes this delay and widens to the appropriate pulse width, so that the cursor may appear at standard character width of 7 dots. After the 7406 open collector inversion the 680Ω resistor holds the intensity of the cursor down as it is

actually drawn with bars as opposed to dots. From here on, the cursor resembles a regular character, except the cursor is taller and dimmer.

The sync pulses are to be shaped also, before they may join the composite video. The rough vertical sync pulse is high going at M-2. This single shot is used to narrow the square wave available at M-4 by means of the 50K pot. A narrow sync pulse is made at M-5 of the square wave at M-10. The pulse width at M-5 is fixed, but may be delayed due to the width of the square wave at M-10. This delay is relative to the timing chain and the dot stream at Z6. As a result the image may be moved vertically on the screen. The horizontal sync is formed in a similar manner and may be used to move the image horizontally as well.



ATTACHE' SCHEMATIC DIAGRAMS
VIDEO BOARD

250272A