from the MITS Repair Dept.

# Altair 8800 Clock Modification

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Have you ever found yourself in this situation? You finally find some time to play with your computer, you turn the power on and only the data and address LEDs light. No amount of fooling with the switches will change the situation. Or perhaps the computer does run for a short time, then the data and address lights all come on while the status lights go out.

If you have experienced any of the above situations, you have been the victim of clock failure. While there are many possible causes and cures, we feel the following modification is the proper cure to use.

Step 1: Remove R37, R38, R39, and R40 from the Altair 8800 CPU Board.

Step 2: On the back of the board cut the land to R39 from pin 3 of IC "P". Make sure the land between R40 and pin 3 of IC "P" remains intact (see figures 1-a and 1-b).

Step 3: Also on the back of the board, remove the land that connects the lower ends of resistors R37 and R38 (figures 1-a and 1-b).

Step 4: Install two 470 ohm resistors vertically in the holes of R37, R38, R39, and R40 closest to IC "P" (see figure 2).

Step 5: Install a 50 picofarad capacitor as shown in figure 3.

Step 6: On the back of the board install a jumper from pins 4 and 5 of IC "P" to the bottom hole for R39 (see figure 1).

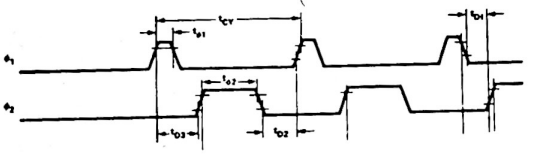
Step 7: Install another jumper from the bottom hole for R38 to the land immediately above it. The land goes to pin 2 of IC "P" (see figure 1).

The above steps will produce a clock circuit that oscillates much more reliably.

One other area of the CPU clock circuit that may give trouble is IC "Q". This chip is a 74123 single shot. It is used to derive Ø1 and Ø2 from the 2MHz clock. We have found that a TI74123 is most reliable with the components supplied on our board.

In any case, the relationship between Ø1 and Ø2 should conform to the diagram below.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{CY}$[3] | Clock Period | 0.48 | 2.0 | μsec |
| $t_r$, $t_f$ | Clock Rise and Fall Time | 5 | 50 | nsec |
| $t_{\phi 1}$ | $\phi_1$ Pulse Width | 60 | | nsec |
| $t_{\phi 2}$ | $\phi_2$ Pulse Width | 220 | | nsec |
| $t_{D1}$ | Delay $\phi_1$ to $\phi_2$ | 0 | | nsec |
| $t_{D2}$ | Delay $\phi_2$ to $\phi_1$ | 70 | | nsec |
| $t_{D3}$ | Delay $\phi_1$ to $\phi_2$ Leading Edges | 130 | | nsec |




Two other changes have been made on the CPU since it first came out. Resistors R9 through R16 have been changed from 4.7K ohm to 4.3K ohm. This gives a faster rise time on the bidirectional data bus. The other change was to use a 74LS74 for IC "L" rather than a 74L74. As the Schottky device is faster, it synchronizes the PRDY pulse to the leading edge of Ø2 more closely.

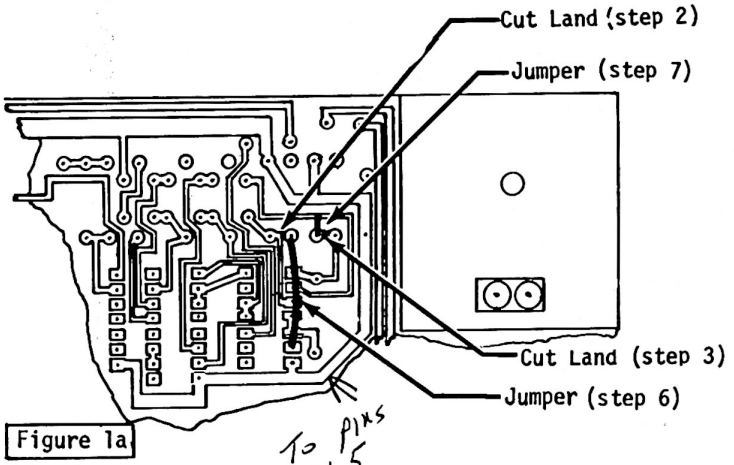



Figure 1a

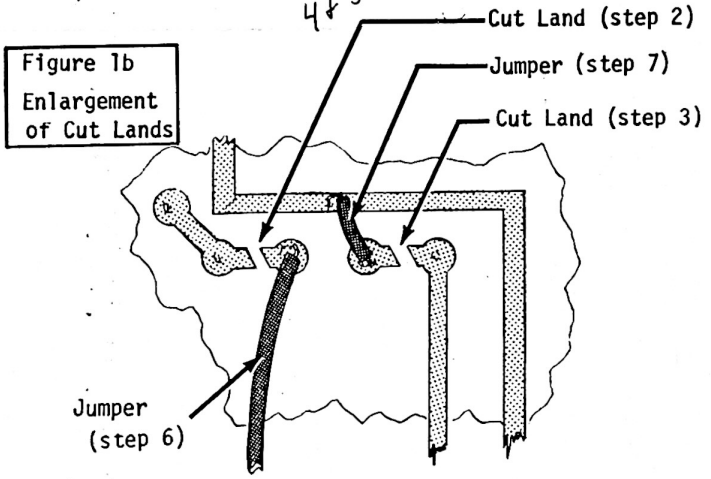



Figure 1b
Enlargement of Cut Lands

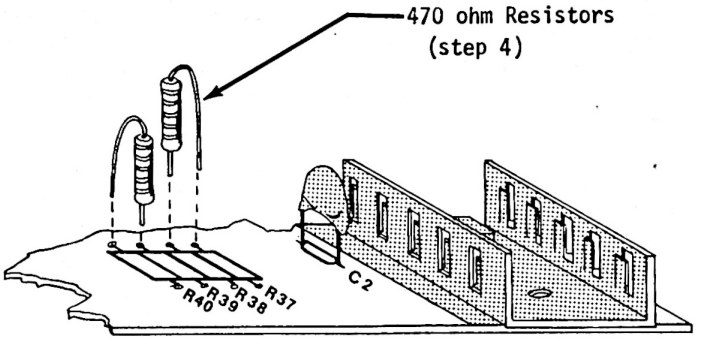



Figure 2

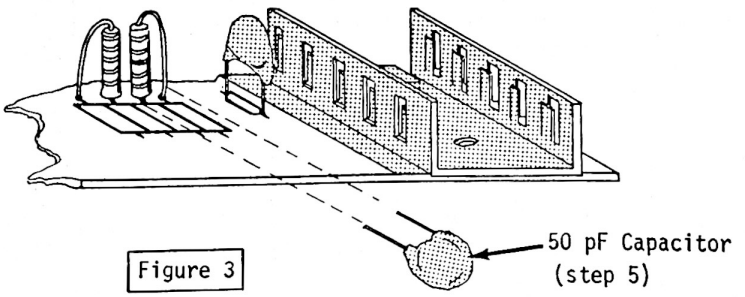



Figure 3