altair™8800

88-PROCESS CONTROL INTERFACE BOARD DOCUMENTATION

Second Printing, March, 1977

mits
2450 Alamo S.E. /Albuquerque, New Mexico 7106

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF PROGRAMS

LIST OF ILLUSTRATIONS

SECTION I
88 PCI
INTRODUCTION

1-1. SCOPE AND ARRANGEMENT

The 88-Process Control Interface documentation is divided into four major sections:

I. Introduction
II. Theory of Operation
III. User Information
IV. Troubleshooting

Section I contains the scope and arrangement of the manual along with a brief description of the board and its capabilities.

Section II contains the information needed to understand the operation of the board at a technical level. It covers the logic circuits; the input and output devices (optical isolators and relays, respectively); and the input, output and interrupt functions of the board.

Section III provides the general information necessary to set up and initialize the board from both hardware and software standpoints. Several detailed applications and software programs are included, along with a list of various uses.

Section IV contains a preliminary board check and several procedures for locating specific problems.

1-2. DESCRIPTION

The 88-Process Control Interface board allows interfacing with the real world of relays, switches, motors, fans, contacters, alarms, solenoids, heaters, etc. The board is compatible with the Altair 8800 series computers--Altair 8800, 8800a and 8800b.

The output section of the board consists of eight relays, each capable of switching 120 volts AC at 1 amp. The input section consists of eight opto-isolators which can be configured by the user to accept a wide range of voltages. The 88-PCI contains four more opto-isolated signal lines which are configured as two pairs of handshake lines; one pair associated with the input section, and one with the output section. Each pair consists of one optically-isolated input line and one optically-isolated output line. All of the lines are completely isolated and balanced for use in environments with high levels of electrical noise.

SECTION II
88 PCI
THEORY OF OPERATION

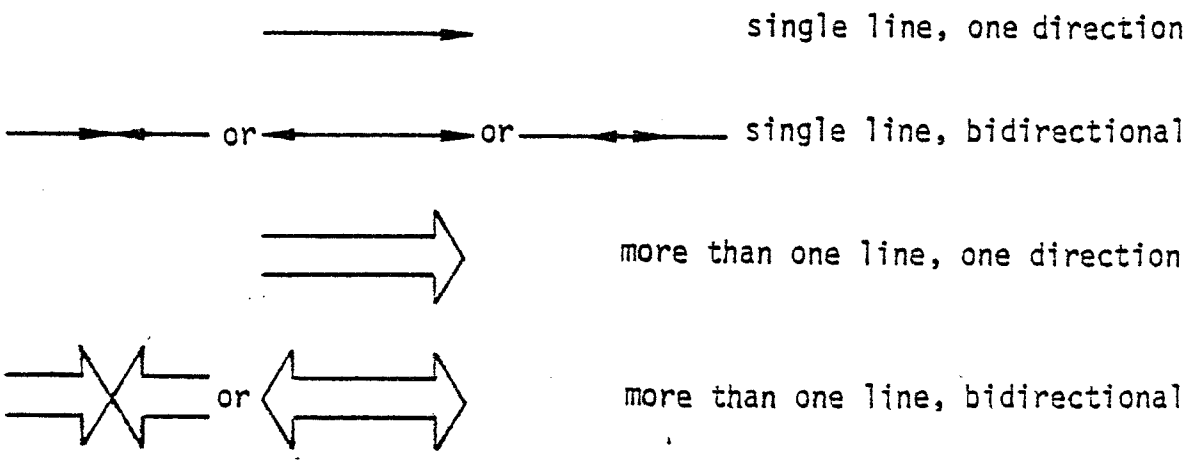
2-1. GENERAL CONTENTS

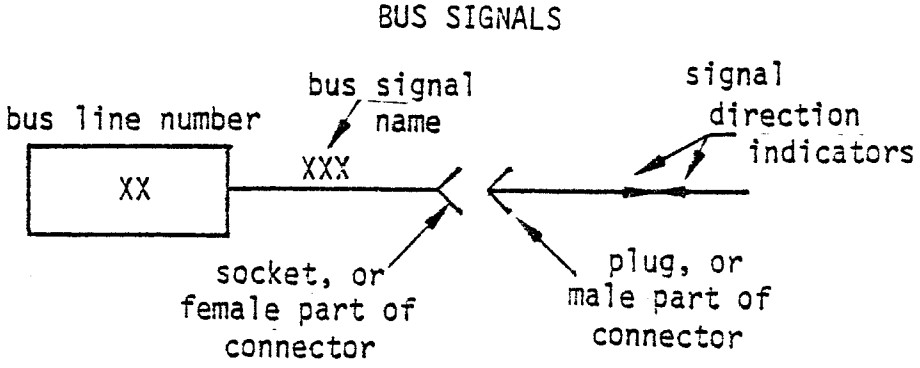
Section II contains technical information to aid in understanding the 88-Process Control Interface board's operation. Provided in this section is information on schematic referencing including a chart showing signal and bus line designations; information on logic circuits containing truth tables and a chart with a description of each circuit and its Boolean Algebra equivalent; a circuit description section explaining the support logic; and a description of the board's input, output and interrupt functions.

2-2. SCHEMATIC REFERENCING

The detailed schematics of the 88-PCI are provided to aid in determining signal direction. Table 2-A shows how signal direction is indicated on signal lines and how to interpret signal bus designations.

Table 2-A. Signal Direction and Bus Signals





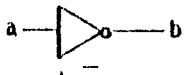
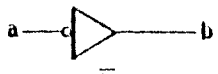
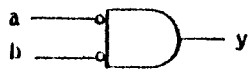
2-3. LOGIC CIRCUITS

The logic circuits shown in the 88-PCI illustrations are presented in Table 2-B. This table presents the functional name, symbolic representation, and brief description of each logic circuit. Also provided are truth tables which show the relation of all output logic levels of a digital circuit to all possible combinations of input logic levels.

The active state of the inputs and outputs of the logic circuit is graphically displayed by the presence or absence of small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

Table 2-B

Logic Circuits

Name	Normal	Equivalent	Description
Inverter or Buffer	 $b=\overline{a}$	 $a=\overline{b}$	An inverter is a gate whose output is the inverse of its input.
NAND gate	 $y=\overline{a \cdot b}$	 $y=\overline{a}+\overline{b}$	The NAND gate gives a LOW output when all of its inputs are HIGH. As the truth table will show, it is the equivalent of an OR gate with all of its inputs inverted.
NOR gate	 $y=\overline{a+b}$	 $y=\overline{a} \cdot \overline{b}$	The NOR gate gives a LOW output when any of its inputs are HIGH. It is equivalent to an AND gate with all of its inputs inverted.

a	b
0	1
1	0

a	b	y
0	0	1
0	1	1
1	0	1
1	1	0

a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

1=HIGH
0=LOW
X=don't care
↓=transition from HIGH to LOW

Table 2-B, continued.

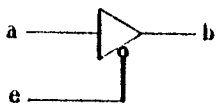
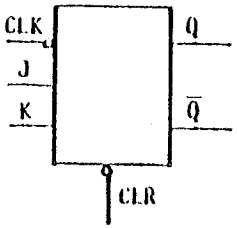
Name	Normal	Equivalent	Description
Bus Driver		for E HIGH, B floats. for E LOW, B=A	The Bus Driver is a tri-state device. It gives an output equal to the input when it is enabled. It is enabled with a logic LOW signal. When it is not enabled (logic HIGH), the output goes to a HIGH impedance state. e a b 0 0 0 0 1 1 1 X F
J-K Flip-Flop			Applying a LOW to the clear input (labelled here CLR) resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. This reset is not dependent on the clock at all. When J and K are both HIGH, Q and $\overline{Q}$ change to their opposite logic states with each negative going edge of the clock pulse. This is called toggling. When J is HIGH and K is LOW, a negative going clock pulse will set Q HIGH and $\overline{Q}$ LOW. When J is LOW and K is HIGH, a negative going clock pulse will set Q LOW and $\overline{Q}$ HIGH. If the clock does not change, Q and $\overline{Q}$ will not change, regardless of any changes in J and K. When both J and K are LOW, the state

Table 2-B, continued.

Name	Normal	Equivalent	Description
			of Q and $\overline{Q}$ do not change with the clock pulse.

CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	+	L	L	Q0	$\overline{Q0}$
H	+	H	L	H	L
H	+	L	H	L	H
H	+	H	H	Toggle	
H	H	X	X	Q0	$\overline{Q0}$

2-4. CIRCUITRY

Paragraphs 2-5 through 2-8 describe the circuitry of the 88-PCI board. Included in this section is an overall block diagram (Figure 2-1) along with smaller diagrams detailing individual circuit areas. Schematic zone references are also provided for use with these diagrams.

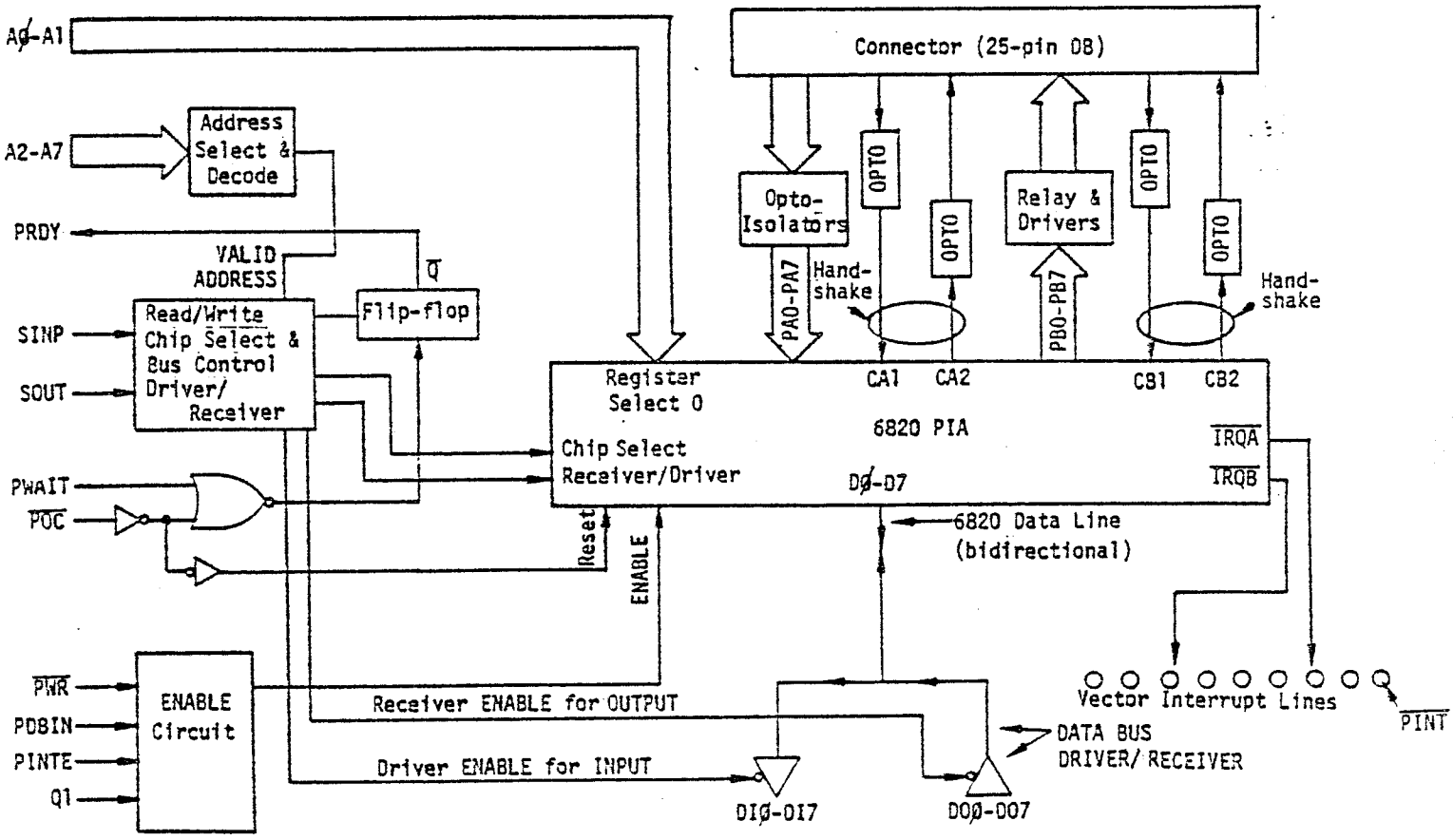


Figure 2-1. Process Control Interface Board Block Diagram

2-5. 6820 Peripheral Interface Adapter (Figure 2-2)

The 6820 Peripheral Interface Adaptor (PIA) contains all the circuitry necessary to implement and control the eight incoming data lines (PAØ-PA7) from the opto-isolators, the eight outgoing data lines (PBØ-PB7) which control the relays, and the two sets of bidirectional handshake (control) lines. Handshake lines CA1 and CA2 are used with Section A, and CB1 and CB2 are used with Section B. The lines that connect the 6820 to the rest of the system consist of eight bidirectional data lines (DØ-D7), two interrupt request lines ($\overline{\text{IRQA}}$ from Section A, and $\overline{\text{IRQB}}$ from Section B), lines to do chip select (CSØ, CS1 and $\overline{\text{CS2}}$) and register select (RSØ and RS1) within the chip to control read and write states (R/W), to enable the chip (E), and to reset the chip (RST).

The 6820 has a large number of software controllable functions. For instance, the PA and PB lines can be enabled as either inputs or outputs by software, and many of the functions of the control lines can be changed or controlled through software. The configuration of the peripheral interface (how the data lines are set up with their inputs or outputs) is under the control of the Data Direction Register. In the initialization process it is necessary to do an output to the Data Direction Register to tell the PIA which lines to set up as inputs and which to set up as outputs. The relationship of control lines CA1 and CA2 to the Interrupt Request line ($\overline{\text{IRQA}}$) is controlled by Control/Status Register A. CB1 and CB2 are related to Interrupt Request line $\overline{\text{IRQB}}$ and are controlled by Control/Status Register B.

The 6820 contains four addresses. (Refer to Table 2-C, Register Selection.) The first address (or base address) selects Control/Status Register A. The second address (base address + 1) selects the Data Direction Register or the Data Channel Registers* themselves. The Control/Status Register determines which of these registers will be used. The next address (base address + 2) selects Control/Status Register B, and the last address (base address + 3) selects Data Direction Register B or Data Channel Register B.

Table 2-C

Register Selection						
RS0	A0	RS1	A1	CRA-2	CRB-2	Register Selected
1	0	0	0	X	X	Control/Status Register (Section A)
1	0	1	1	0	X	Data Direction Register (Section A)
1	0	1	1	1	X	Data Register (Section A)
0	1	0	0	X	X	Control/Status Register (Section B)
0	1	1	1	X	0	Data Direction Register (Section B)
0	1	1	1	X	1	Data Register (Section B)

The ENABLE signal is the only timing signal required by the 6820 PIA. All data is transferred from one register to the other on this signal.

*The Data Channel Register used for inputs is shown on the 6820 PIA Block Diagram as the Peripheral Interface (A or B). The Data Channel Register used for outputs is shown as the Output Data Channel Register. The Peripheral Interface is regarded as a Data Channel Register only during inputs, and the Output Data Channel Register is regarded as a Data Channel Register during outputs.

The RESET signal sets up the peripheral interface lines as inputs by resetting the contents of all registers to Ø. RESET is activated when the system is turned on.

The READ/WRITE line controls the input or output state of the bidirectional data bus (DØ-D7).

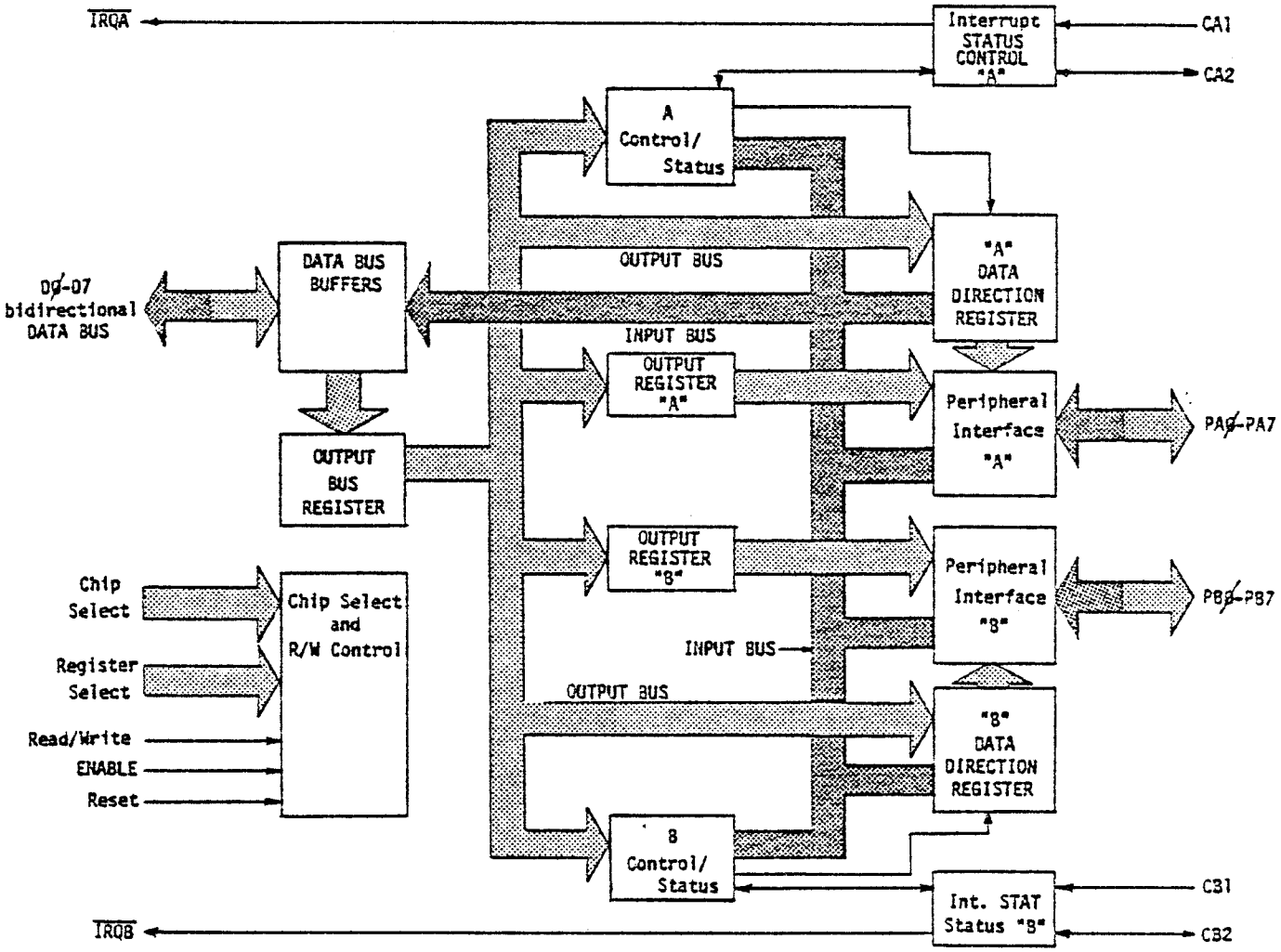


Figure 2-2. 6820 PIA Block Diagram

2-6. SUPPORT LOGIC

A. Addressing

The 88-PCI board may be addressed at 64 possible locations which may be selected in increments of four. Refer to the Addressing Logic Diagram, Figure 2-3. The address line comes onto the board from the bus through an edge connector (shown by two interlocking arrows). The next (solid) arrow on the line indicates the signal direction into inverter J. Inverter J acts as a bus line receiver, and it also inverts the signal. The inverted signal goes to the "$\overline{A}$" pole of Switch 1 and into inverter F. Inverter F brings the signal back to its original polarity. The output of inverter F is brought to the "A" pole of Switch 1. Address selection of the board is done by Switch 1. Only one address line is shown here, but there are actually six address lines that go into the NAND gate labelled "B" in this diagram. Refer to the schematic, Figure 2-10. All six address lines are inverted in this manner and brought to six separate address switches. ADDRESS VALID is indicated by a LOW signal at output pin 8 of IC B (zone C7) which is HIGH at output pin 2 of inverter E (zone B7). ADDRESS VALID occurs only when all of the inputs to IC B are HIGH. This means that if the address lines (A2-A7) themselves have been selected at Switch 1 rather than the inverted address lines ($\overline{A2}$-$\overline{A7}$), all of those address lines must be HIGH at the bus. If any inverted address lines have been selected with Switch 1, those lines must be LOW at the bus, so that after inversion they will appear HIGH at IC B (zone C7). For example, if you wanted the board to be at address Ø, you would select all inverted lines at Switch 1; thus, all the inputs to IC B (zone C7) would be HIGH, and the gate would be enabled.

Refer to Table 2-C and Figure 2-10, pages 2-8 and 2-19, respectively. Address lines AØ and A1 are also brought in from the bus. AØ is inverted at output pin 2 of IC A (zone B8) and brought to Register Select Ø (RSØ) where it selects between the Control/Status Register (when AØ is LOW and RSØ is HIGH) and the Data Channel Registers or the Data Direction Registers (when AØ is HIGH and RSØ is LOW). This is in keeping with the Altair standard of even order addresses for control/status and odd order addresses for data. A1 is inverted by output pin 4 of IC A (zone B8) and again by

output pin 6 of IC A (zone B8) and brought to RS1 where it selects either Section A (when A1 and RS1 are LOW), or Section B (when A1 and RS1 are HIGH). Section A, the input channel, reads from the opto-isolators; and Section B, the output channel, controls the relays.

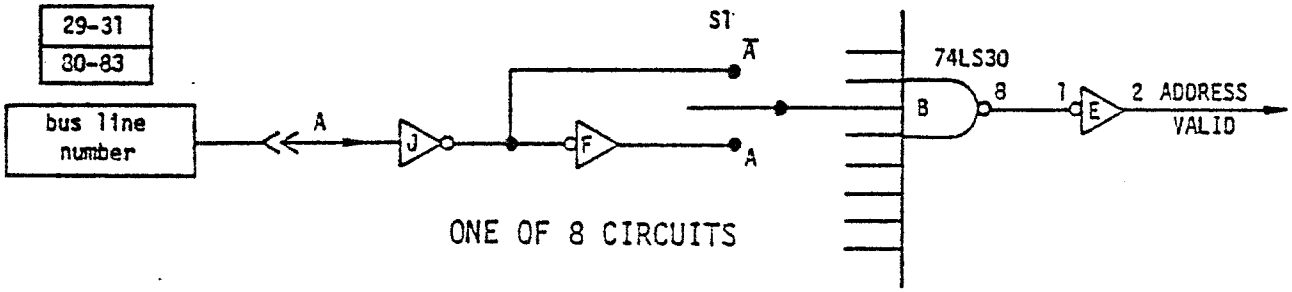


Figure 2-3. Addressing Logic Diagram

B. READ/WRITE, CHIP SELECT and BUS DRIVER/RECEIVER CONTROL Logic

The READ/WRITE, CHIP SELECT and BUS DRIVER/RECEIVER CONTROL Logic selects the 6820 chip, sets up its bidirectional data lines as either inputs or outputs, and enables either the bus drivers or the bus receivers. The inputs to this section are SINP, SOUT and ADDRESS VALID.

The ADDRESS VALID signal comes into the READ/WRITE, CHIP SELECT and BUS DRIVER/RECEIVER CONTROL section from output pin 2 of IC E (zone B7). SINP comes onto the board through IC A (zone B8) and is inverted at output pin 8. From here the inverted SINP signal performs two functions. First, it is inverted again by IC A at output pin 10 (zone B7) and is gated with the ADDRESS VALID signal in IC D (input pins 9 and 10, zone B7). The signal is then output at pin 8 of IC D and goes directly to the WAIT State Generator and RESET circuitry. It also enables the Bus Drivers so that the bidirectional data lines (DØ-D7) from the 6820 drive the DI data bus. Secondly, the SINP signal is gated with SOUT in IC D at pin 6 (zone B7). (SOUT has been inverted by IC A at pin 12, zone B8). The resulting signal is gated with the ADDRESS VALID signal in IC D at output pin 11 (zone B7). This signal goes to $\overline{CS2}$ where it enables the 6820 PIA. SOUT's inversion is also sent to two additional locations. First, it goes directly to the READ/WRITE input of the 6820

where it tells the 6820 whether to use its bidirectional data lines (DØ-D7) as inputs or outputs. When SOUT is HIGH (during output), the inversion at pin 12 of IC A (zone B8) is LOW so that the input to the signal at the 6820's READ/WRITE input is also LOW. When this signal is LOW, it corresponds to a WRITE situation so that the bidirectional data bus is set up as an input. The data bus is enabled as an output at all other times. Secondly, the inverted SOUT signal is inverted again at IC E pin 10 (zone B7) bringing it back to its original polarity. It is gated again with the ADDRESS VALID signal in IC D (zone B7). The output at pin 3 of IC D enables the bus receivers so that the data from the Data Out Bus is transferred onto the bidirectional data lines (DØ-D7) of the 6820.

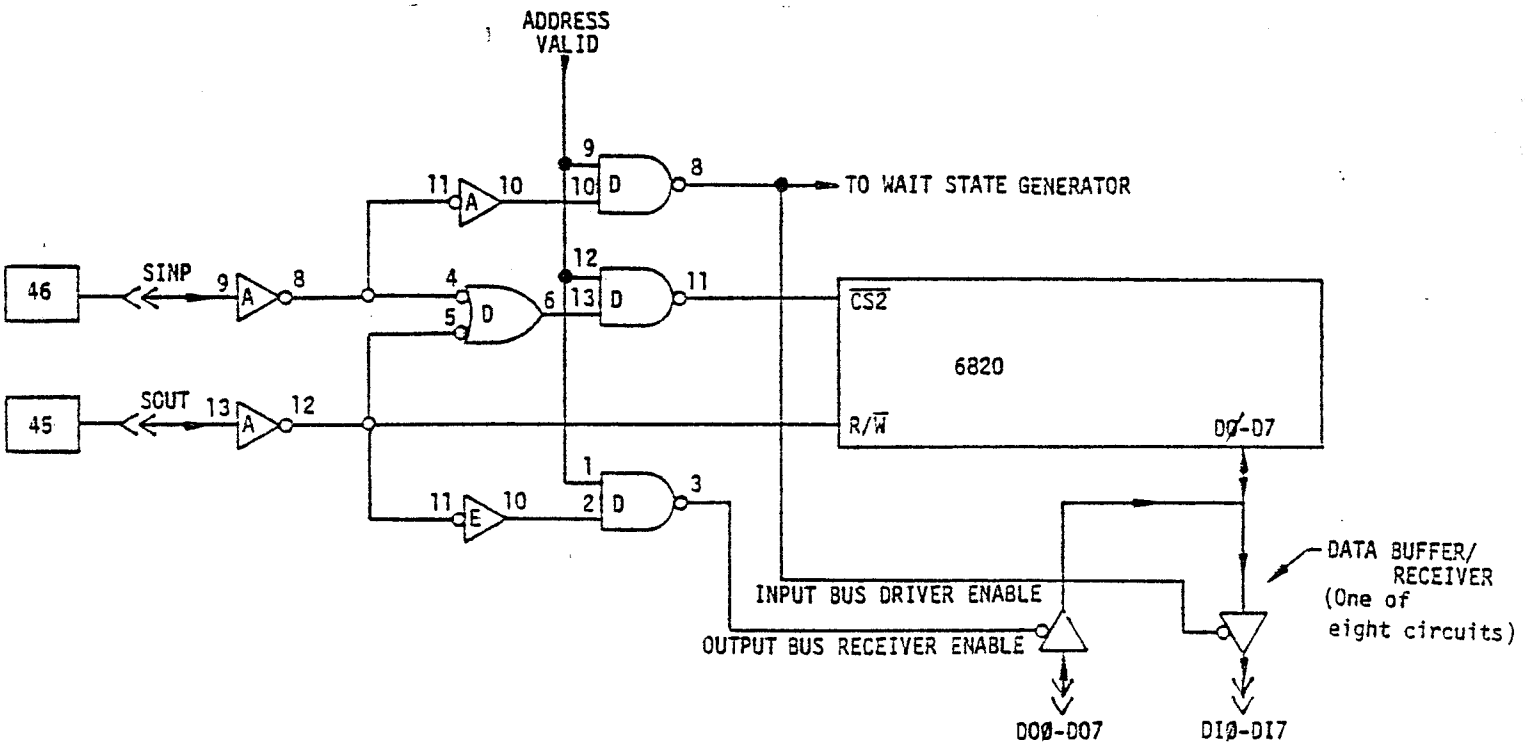


Figure 2-4. READ/WRITE, CHIP SELECT and BUS DRIVER/RECEIVER Control

C. WAIT State Generator and RESET Circuit

When the computer accepts an input from the Process Control Interface, the WAIT State Generator and RESET circuit causes a short processor delay in order to synchronize the processor with the 6820 chip. The operation of the WAIT State Generator and RESET Circuit is as follows.

The J input of IC G (zone B6) is tied HIGH and the K input is tied LOW, causing IC G to clock a LOW to the $\overline{Q}$ output. The $\overline{Q}$ output will enable another bus driver, IC K at pin 15 (zone B6). The output of IC K at pin 12 will pull the ready line (PRDY) LOW, causing the processor to enter a WAIT state. When the WAIT state is acknowledged on the PWAIT bus line, PWAIT will be brought through IC H (zone A7). A HIGH at either input of IC H will cause the pin 10 output to go LOW which will clear flip-flop G (zone B6). This allows the PRDY line to go HIGH, and the processor to continue.

$\overline{POC}$ is inverted by IC E at output pin 8 (zone A8) and is sent to two locations. First, it goes to input pin 9 of IC H (zone A7). When active, this signal will also reset IC G (zone B6). Secondly, the signal is inverted by IC M (zone A7) at output pin 8 which resets the 6820.

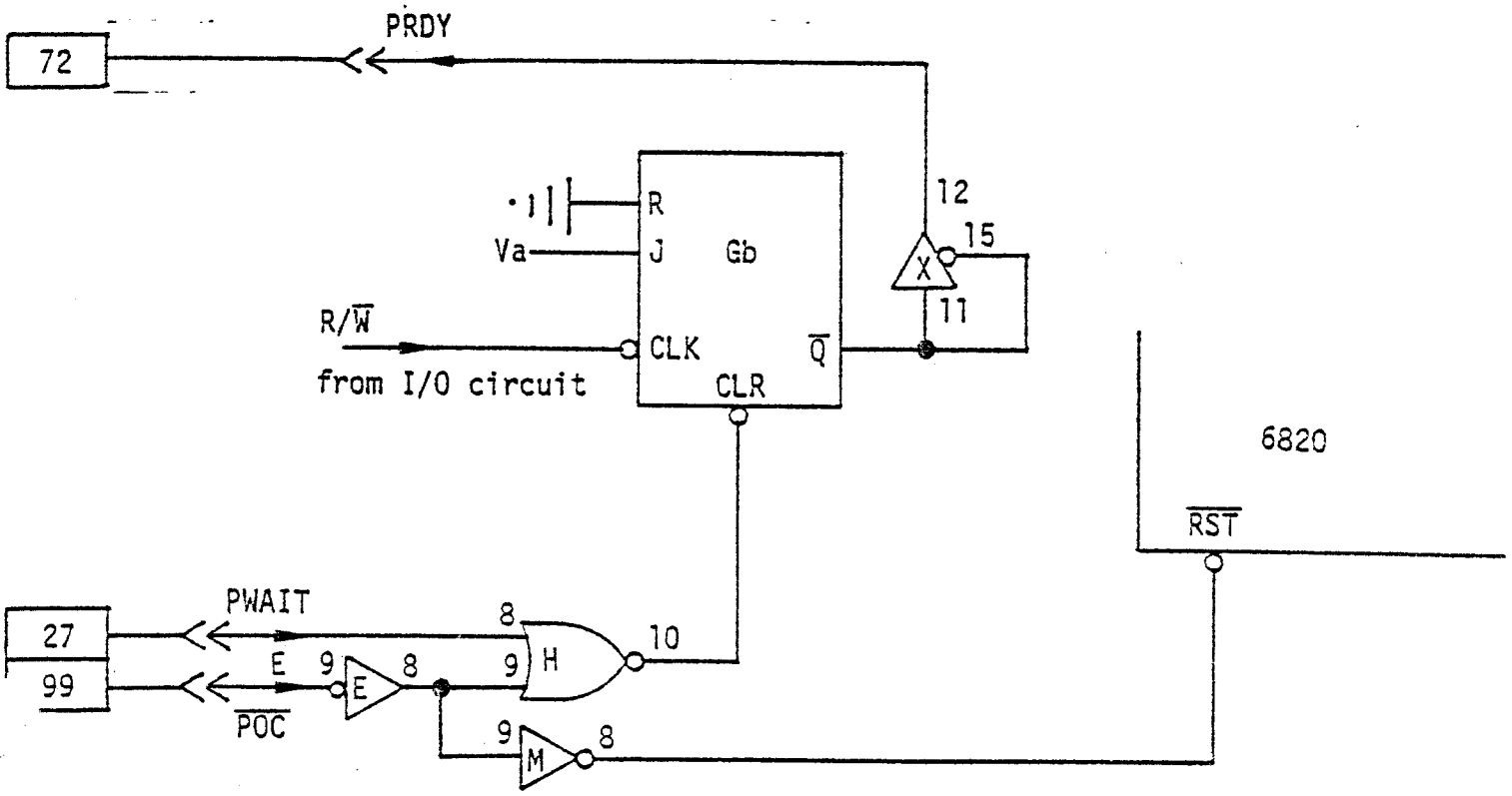


Figure 2-5. Wait State Generator and RESET Circuit

D. ENABLE Circuit Logic

The only timing signal required by the 6820 PIA is the ENABLE signal (or E pulse). This signal is generated by the ENABLE circuit logic. The inputs to the ENABLE circuit logic are the bus signals $\overline{PWR}$, PDBIN, PINTE, and Ø1 clock. For normal read or write operations either $\overline{PWR}$ or PDBIN cause the E pulse. $\overline{PWR}$ is LOW active. It comes onto the board through IC E, input pin 13 (zone A8). It is then inverted at pin 12 of IC E. PDBIN comes directly onto the board and is HIGH active. Both of these signals are brought to input pins 11 and 12 of IC H (zone A7). If either $\overline{PWR}$ or PDBIN is active, the output at pin 13 of IC H will be LOW. This output goes to input pin 2 of IC H (zone A7). A signal (normally LOW) from the flip-flop is sent to input pin 3 of IC H. When both input pins 2 and 3 of IC H go LOW, a positive going E pulse from output pin 1 of IC H is produced. This pulse is directly connected to the ENABLE input of the 6820.

The rest of the ENABLE circuit logic is designed to ENABLE the 6820 to generate an interrupt while the processor is halted. When PINTE is active, the Ø1 clock, which is inverted at pin 4 of IC E (zone A8), clocks LOWs to IC H (zone A7), producing a HIGH at output pin 1.

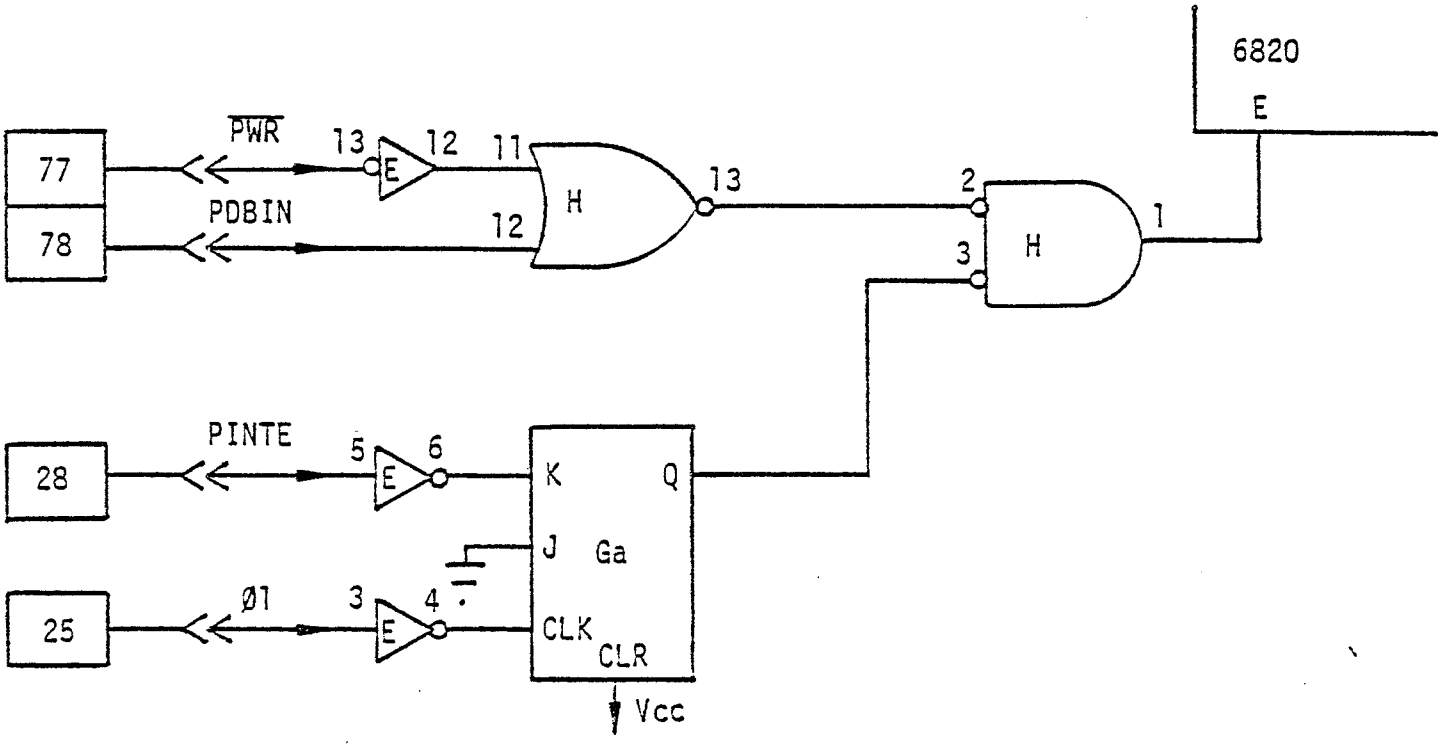


Figure 2-6. ENABLE Circuit

2-7. RELAY OUTPUTS

Refer to Figure 2-7. The line labelled "FROM 6820" is an output line (PBØ-PB7) which drives the base of the switching (or driving) transistor through a limiting resistor. When this transistor conducts, the unregulated supply is dropped across the relay coil, thereby energizing the relay. The diode and resistor (in series across the coil) act as a suppression circuit for the inductive transient that is generated when the transistor is turned off and the coil is deenergized.

Increased contact life and lower electrical noise are two of the benefits of protection and suppression for the relay contacts. Because the protection scheme is different for each type of load and power supply, this should be supplied by the user when his particular needs have been determined. The various methods of protection and suppression are covered in detail in Section III, Paragraph 3-4.

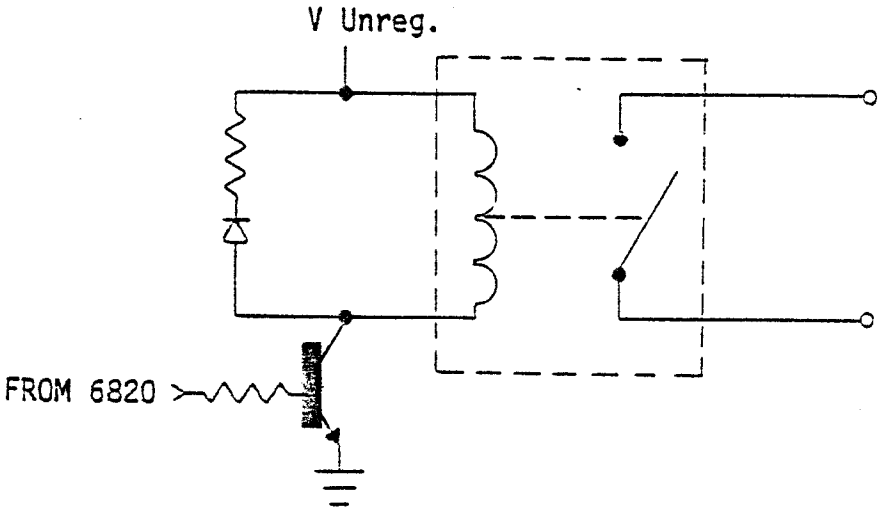


Figure 2-7. Relay Outputs

2-8. OPTO-ISOLATORS

An opto-isolator consists of an LED (or other light source), optically coupled to a photo transistor (or other detecting device). The purpose of the opto-isolator is to maintain a high degree of electrical isolation between input and output, while transmitting data. While this function can be carried out with other devices (such as relays, isolation transmformers, or blocking capacitors), the opto-isolator can be used with higher switching speed, lower cost, and easier interfacing with other semiconductor circuitry. The opto-isolators used on the 88-PCI board are the LED/photo-transistor type. The operation of these circuits is shown in Figure 2-8.

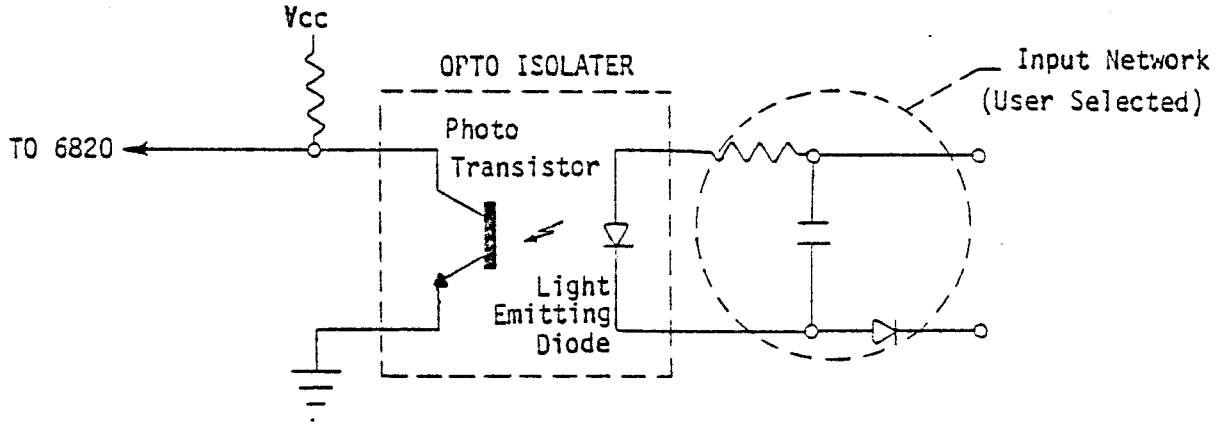


Figure 2-8. Opto-Isolator Inputs

A. Inputs

The input to the LED is a network consisting of a diode, a resistor, and a capacitor. LEDs are very sensitive to damage by reverse biasing. The diode provides protection against this type of damage. The resistor is used to limit current through the LED, and the capacitor (in conjunction with the diode) acts as a debouncing circuit. When current flows through the LED, the photo-transistor conducts. When the photo-transistor is conducting, the junction of the collector of the transistor, the pullup resistor, and the line labelled "TO 6820" is essentially grounded, producing a logic LOW. When the transistor is not conducting, the pullup resistor pulls the junction HIGH, producing a logic HIGH. (Further details on input network selection will be given in Section III of this manual.) Optically isolated inputs, CA1 and CB1 (which are handshake lines), are identical in operation to the other opto-isolated inputs.

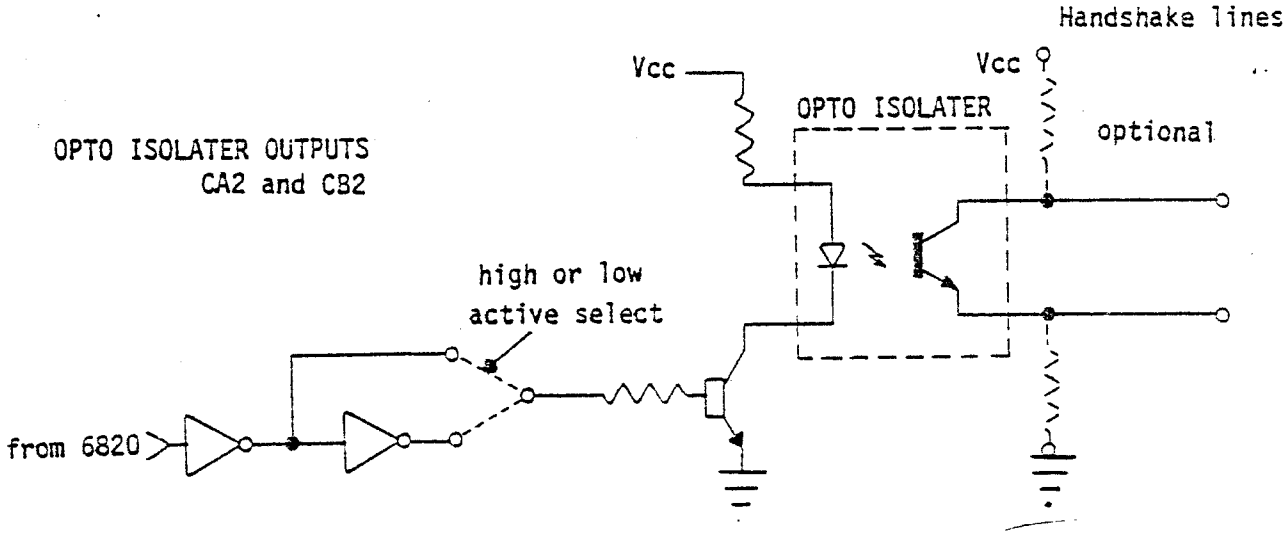
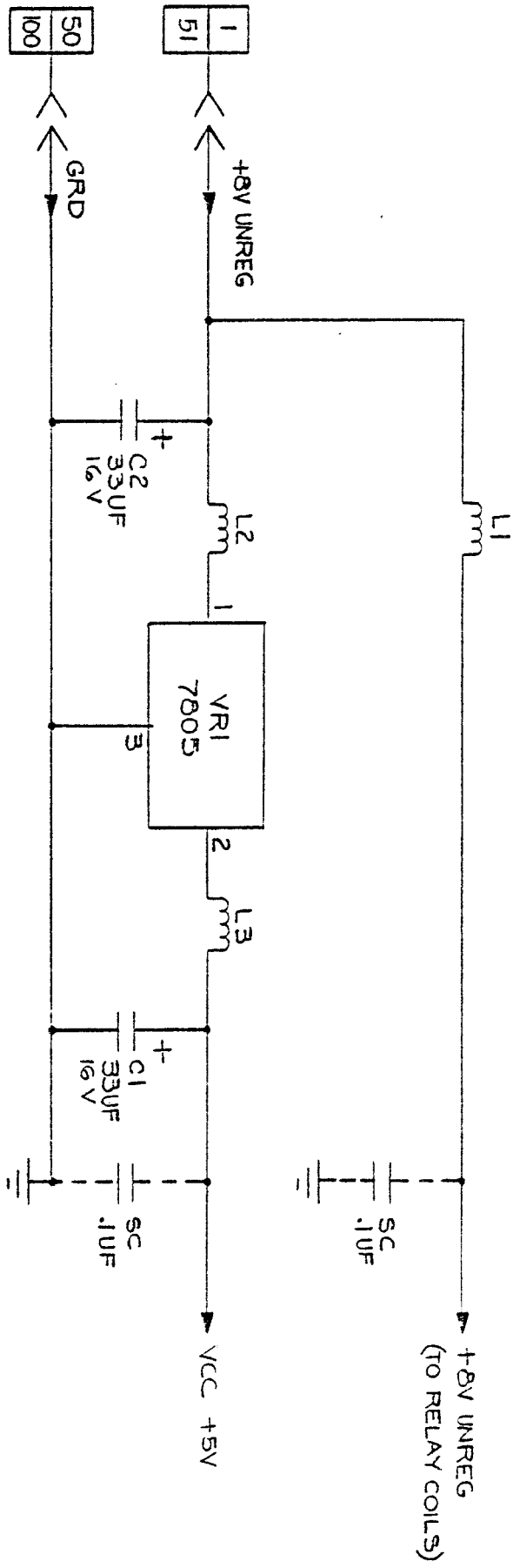


Figure 2-9. Opto-Isolator Outputs



REF DESIG	TYPE	VCC	GRD
R,P,Z,Y,W,X,V,U,S,T,AA,BB	IL74		
C	6820	1	20
M	7404	14	7
A,E,J,F	74L04	14	7
D	74L500	14	7
H	74L02	14	7
B	74L530	14	7
G	74LS73	4	11
K,L,N	74367	16	8

Figure 2-11. 88-PCI Power Supply Schematic

B. Outputs

Handshake lines CA2 and CB2 are the opto-isolated outputs. Refer to Figure 2-9. The line labelled "FROM 6820" is an output line which goes through two inverters so that both the inverted and non-inverted signals are available at the jumper, thus allowing selection of either HIGH or LOW active signals. These signals are applied to the base of the transistor through a current-limiting resistor. When the transistor is conducting, it carries current through the LED in series with the current-limiting resistor. When the LED conducts, it emits light which falls on the photo-transistor. This produces a conducting output to the two handshake lines going out to the connector, CA2 and CB2.

These lines can be configured in two ways. If a resistor is connected from the collector line to a positive voltage and the emitter line is grounded, the collector line then becomes a signal line. Thus, when the LED and the photo-transistor are conducting, a logic LOW is produced.

When neither the LED nor the photo-transistor is conducting, a logic HIGH is produced. If the collector is connected to a positive voltage and a resistor is connected between the emitter and ground, the emitter lead then becomes an output that produces a HIGH logic signal when the transistor is conducting and a LOW logic signal when it is not conducting.

NOTE
Pads are provided on the board for the kind of implementation described in the two preceeding paragraphs. However, it is advisable to do the implementation externally, since use of the internal pads reduces the isolation of the board and the balancing of the lines.

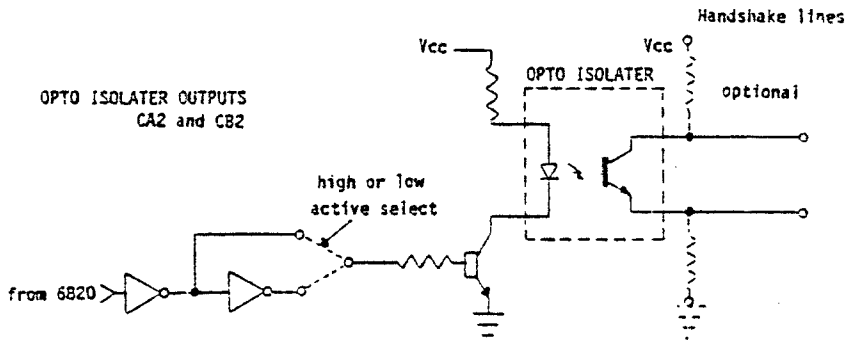


Figure 2-9. Opto-Isolator Outputs

2-9. OPERATIONS

The 88-Process Control Interface performs three basic operations--the input, output and interrupt operations. The following paragraphs describe each operation in detail.

2-10. INPUT OPERATION

Refer to the schematic, page 2-19. To begin an input operation the address lines should correspond to the preselected addresses so that the inputs to IC B (zone C7) are HIGH, thus producing an ADDRESS VALID signal at IC E pin 2 (zone B7). The SINP bus line is also HIGH. When SINP is gated with the ADDRESS VALID signal, a LOW at IC D pin 11 (zone B7) is produced. This LOW signal is connected to $\overline{CS2}$ which selects the 6820. ADDRESS VALID at IC D pin 9 (zone B7) and NAND SINP at IC D pin 10 (zone B7) will give a LOW enabling signal at IC D pin 8 to the bus drivers, thus giving control of the DATA INPUT bus to the Process Control Interface. It will also clock flip-flop G (zone B6), which will start a WAIT state. As soon as the WAIT state is finished, the PDBIN signal will cause an ENABLE. This ENABLE signal will clock the data at the PA lines through the 6820 to the D lines which are directly connected to the bus drivers.

2-11. OUTPUT OPERATION

The output operation is quite similar to the input operation. To begin the output operation, the address lines should be valid. The SOUT bus line going HIGH will cause a LOW at IC A pin 12 (zone B8) which is connected to the READ/WRITE INPUT line. The READ/WRITE INPUT line tells the 6820 to receive data. When gated with the DATA VALID signal at IC D pin 1 (zone B7), SOUT at IC D pin 2 (zone B7) also produces a LOW signal at IC D pin 3, which enables the bus receivers to receive data from the DATA OUT bus. The receivers drive data lines DØ-D7 on the 6820. The WAIT state is not needed for this output signal. $\overline{PWR}$ will send an ENABLE signal through the inverter and the H gates (zone A7). The data present on bidirectional data lines DØ-D7 will then be clocked through the 6820 and will appear on outgoing data lines PBØ-PB7. The HIGH signals will turn on the relays and the LOW signals will leave them turned off.

2-12. INTERRUPT OPERATION

An interrupt can be brought about by a signal change in the opto-isolated inputs related to CA1 or CB1. During the board initialization, the Control/Status Registers determine whether this change will be from HIGH to LOW or from LOW to HIGH. Assuming the interrupts are enabled, either $\overline{\text{IRQA}}$ (for Section A) or $\overline{\text{IRQB}}$ (for Section B) will be LOW on the ENABLE pulse when this transition takes place. In other words, the Interrupt Request is clocked out of the 6820 by the ENABLE pulse. The type of interrupt that is requested depends upon whether the Interrupt Request lines are tied to the PINTE bus line (which is normal) or to one of the vector interrupt lines (if a vector interrupt card is used).

SECTION III
88 PCI
USER INFORMATION

3-1. INTRODUCTION

Section III is designed to help the user set up and initialize the 88-Process Control Interface board for his own individual needs. Contained in this section are information and charts on hardware set-up procedures, Relay Contact life, opto-isolator inputs and outputs, software initialization, applications software including sample programs, and several suggested applications.

3-2. HARDWARE SET-UP

The first step in the hardware set-up procedure is to determine the number of relays that will be needed, the amount of current and voltage each relay must carry, and the manner in which the relays on the board will connect to the external circuit.

When an amount of current and voltage has been determined, check the Relay Life Chart (Figure 3-3) to make sure that combination will yield an acceptable relay life. For example, 120 VAC at 1 amp resistive (power factor = 1) yields a life of approximately 500,000 operations. If the resulting life of the chosen combination is unacceptable, the relay on the board may be used to drive a contacter or a larger relay.

3-3. CABLE CONNECTIONS

When connecting the voltage and current to the board to be switched, the connections should be made (25-pin DB to P1) according to Table 3-A.

Table 3-A. Cable Connections

P2 to 25-pin DB			P1 to 25-pin DB	
PA0	22 21 —	16+ 17-	PB0	20 21	20 Gray 21 Black
PA1	20 19	18+ 19-	PB1	18 19	18 Violet 19 Black
PA2	4 3	5+ 4-	PB2	16 17	16 Blue 17 Black
PA3	6 5	7+ 6-	PB3	14 15	14 Green 15 Black
PA4	10 9	11+ 10-	PB4	7 8	7 Yellow 8 Black
PA5	8 7	9+ 8-	PB5	3 4	3 Red 4 Black
PA6	1 2	2+ 3-	PB6	1 2	1 Brown 2 Black
PA7	12 11	13+ 12-	PB7	5 6	5 Orange 6 Black
CA1	18 17	20+ 21-	CB1	+23 -22	23 White (Anode) 22 Black (Cathode)
CA2	24 (Coll.) 23 (Emit.)	14 (Coll.) 15 (Emit.)	CB2	25 (Coll.) 24 (Emit.)	25 Brown (Coll.) 24 Black (Emit.)
			Note: Pin 11 should be keyed.		

Use #24 (or larger) wire with insulation sufficient to withstand the anticipated maximum voltage that will be encountered. The wire must also be able to withstand any abrasion, oil, or weather exposure that may be expected during normal use.

CAUTION

When hazardous voltages and currents are to be used, be sure to check the local electrical codes for your area. All lines having such voltages should be fused.

Figure 3-1 illustrates the general connection for the relay section of the board.

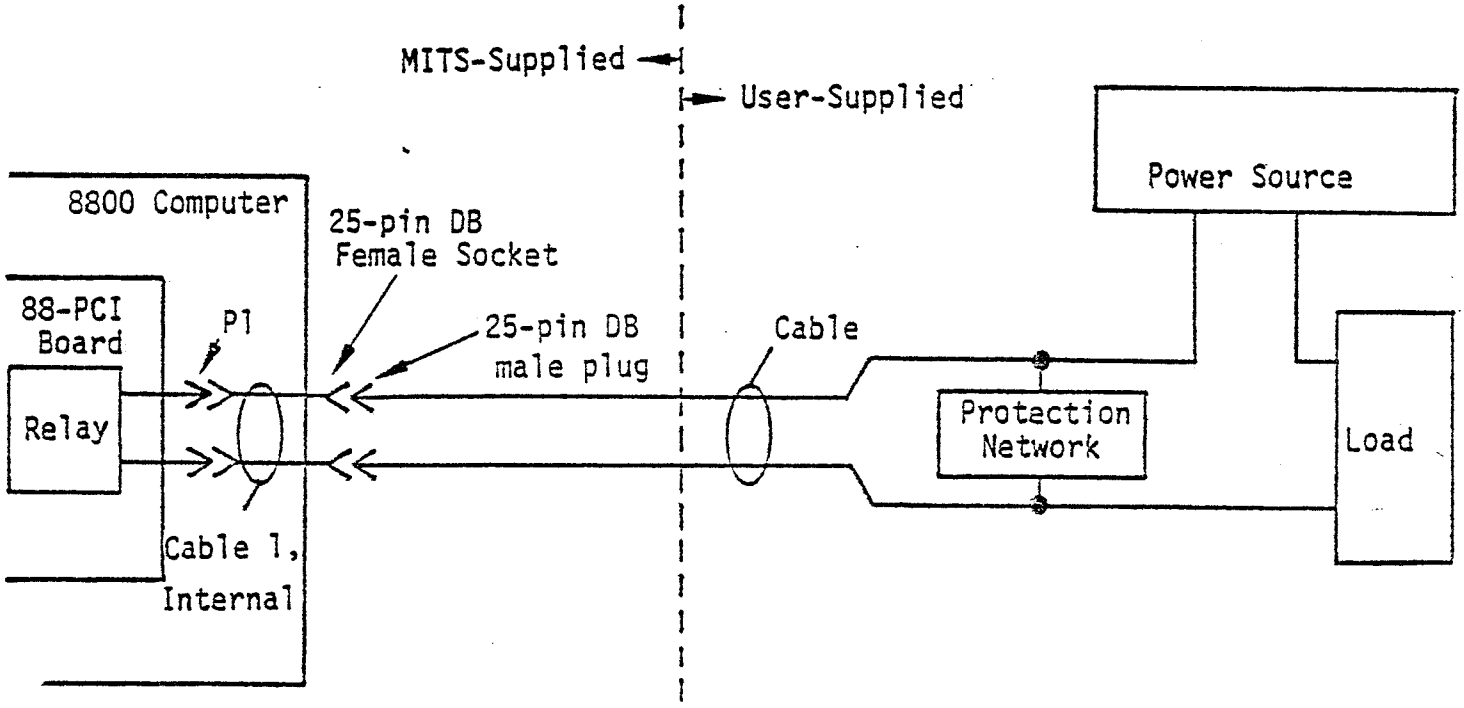


Figure 3-1. General Relay Connections

3-4. RELAY CONTACT PROTECTION AND SUPPRESSION

There are two important advantages to relay protection. First, relay life can be doubled, or tripled in some cases, by protecting the relays from arcing when the contacts open and close. During normal use, unprotected relays may become pitted because of this arcing. Second, electromagnetic and radio frequency interference that can cause erratic circuit performance can be reduced through arc suppression.

Protection networks and their interconnections should be assembled in a suitable chassis. (Note: They can be assembled within the chassis of an existing piece of equipment.) The protection networks should be located as close to the relays as possible in order to minimize the induction effects of long lines.

A resistor and a capacitor used in series across the contacts is one means of protection for the contacts used in DC circuits. Refer to Figure 3-2a. Component values should be selected to suppress arcing, but they should not affect load performance. The best way to select these values is through empirical testing. The capacitance should be large enough for worst-case conditions, and the resistance large enough to limit capacitor charge/discharge. If the resistance is too small, the contacts will weld shut; but if the resistance is too large, the purpose of the capacitor may be defeated. The formula shown below is a good estimated starting value.

$C=I^2/10$, where:

C=Capacitance in microfarads

I=Current in amps

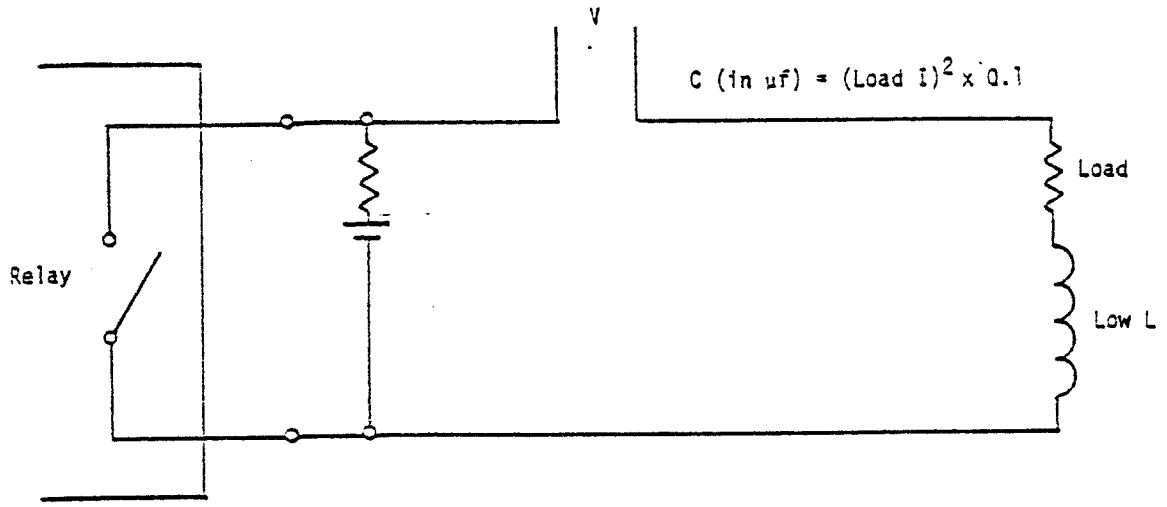


Figure 3-2a. Relay Contact Protection for DC Loads (Resistor and Capacitor Circuit)

The protection circuit shown in Figure 3-2b is another method used with DC loads. When separation occurs, it gives a near-zero voltage drop across the contacts (even on highly inductive loads). The values of the capacitor and the diode are selected so that at the instant of separation, the peak voltage to which the capacitor charges will not cause breakdown of the diode, the contact gap, or the capacitor itself.

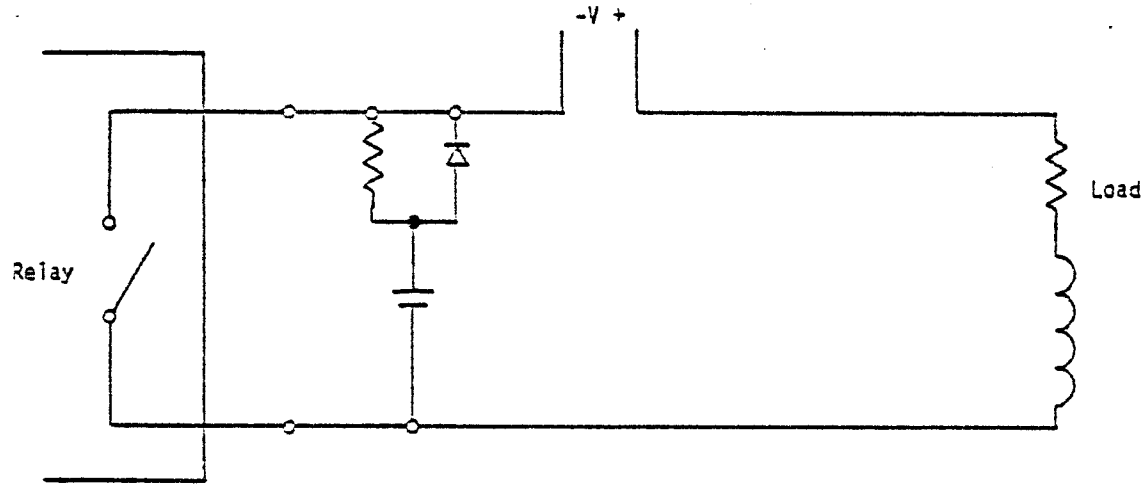


Figure 3-2b. Relay Contact Protection for DC Loads (Capacitor and Diode Circuit)

In AC loads, after contact separation, an alternating current arc is extinguished when current passes through zero. Therefore, contact protection for AC loads (particularly resistive loads) is not as critical as for DC loads. An arc can last no longer than 8.3 milliseconds on a 60 Hz line since current reversal occurs 120 times per second. Thus, the higher the frequency, the shorter the duration of the arc.

Figure 3-2c illustrates a contact protection circuit for an AC inductive load. This network allows the arc to extinguish naturally by making an inductive load appear resistive to the contacts.

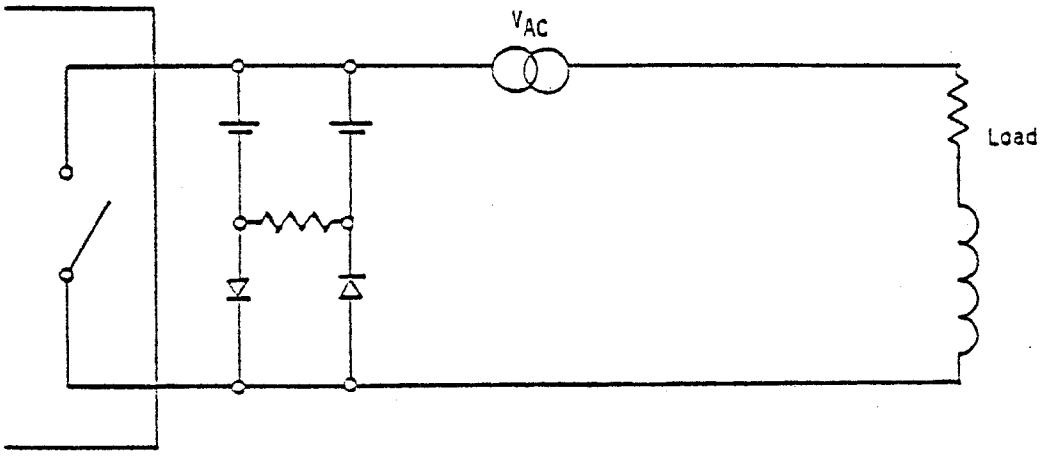


Figure 3-2c. Relay Contact Protection for AC Inductive Loads

Figure 3-3 shows the expected life of relay contacts vs. load current for various voltages and power factors.

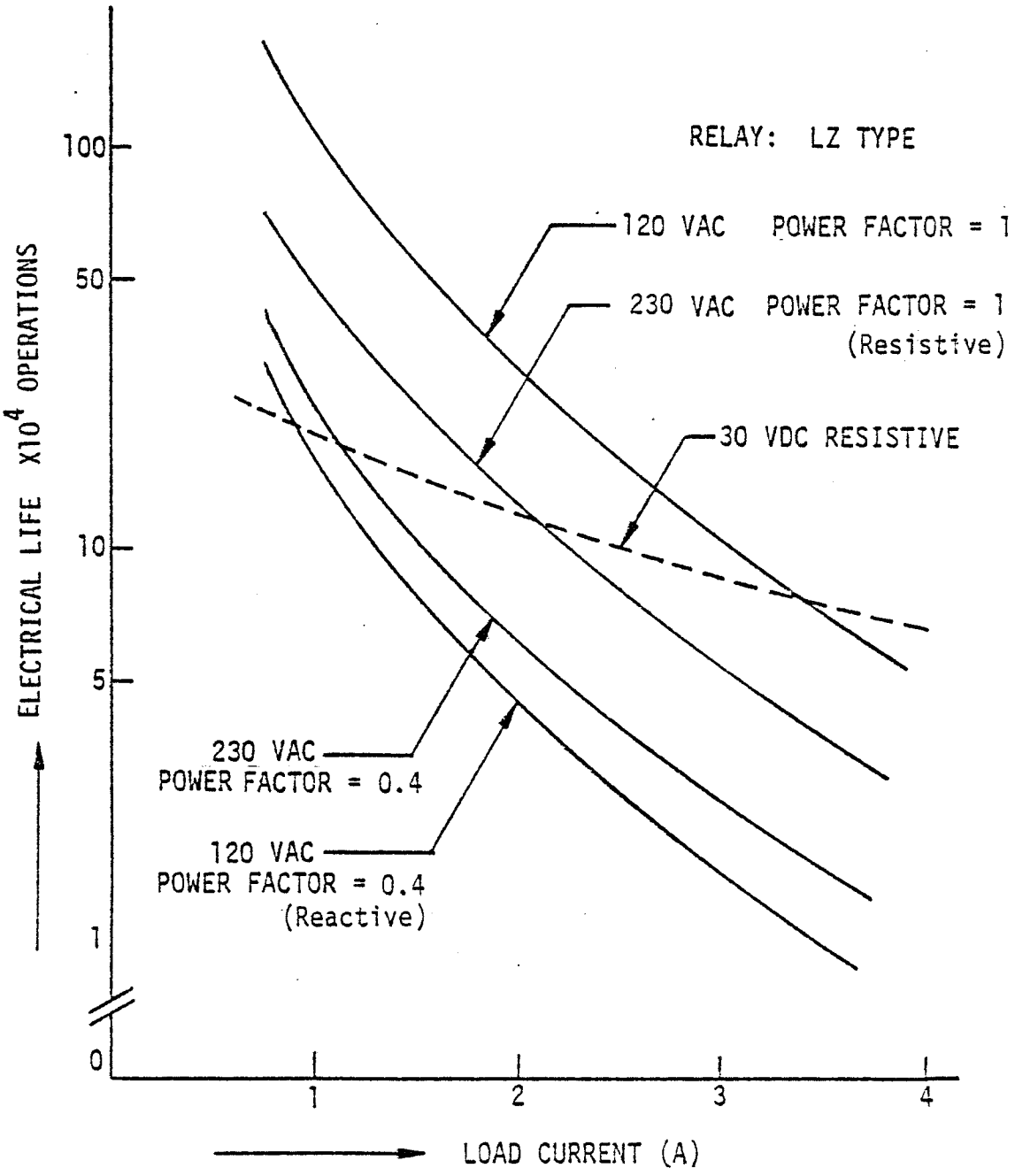


Figure 3-3. Relay Contact Life

3-5. OPTO-ISOLATOR INPUT CONNECTIONS

Connecting the opto-isolator inputs is fairly simple. The main concerns are:

a) the amount of voltage applied to the inputs

b) the length of switching time and propagation delays of the opto-isolators

c) how to transmit the signals to the board

A simplified general connection scheme is shown below in Figure 3-4.

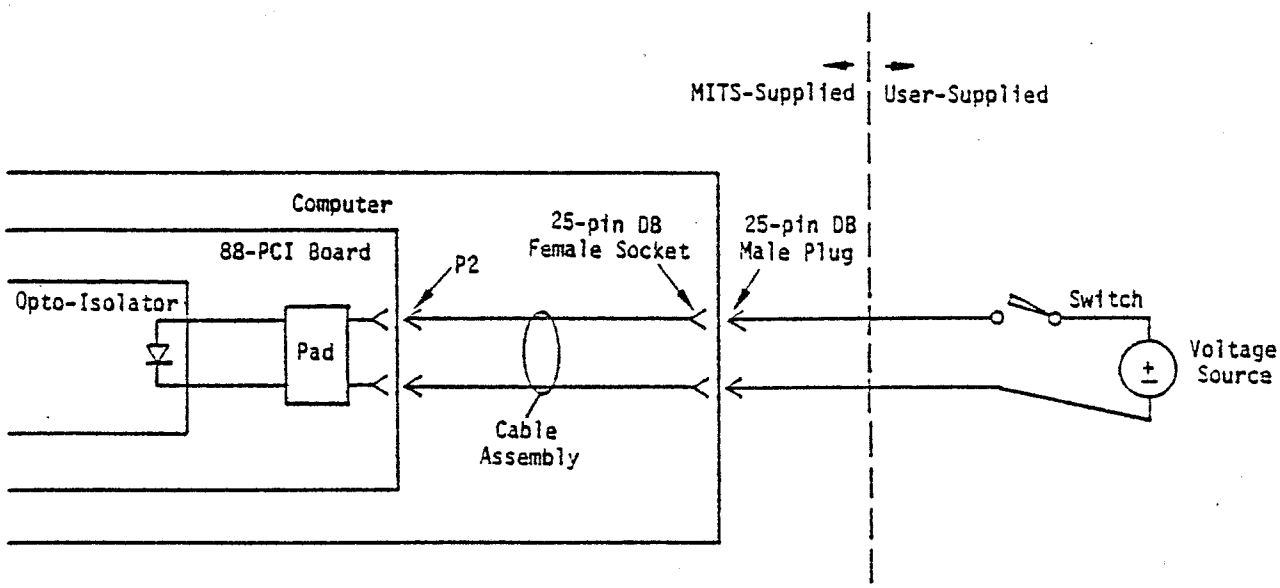


Figure 3-4. Opto-Isolator General Connections

The Process Control Interface board contains pads to provide a circuit which adapts the inputs to a wide range of voltage and pulse widths. A diagram of this circuit is shown in Figure 3-5. A description of the MITS-supplied circuit configuration is given on page 3-13.

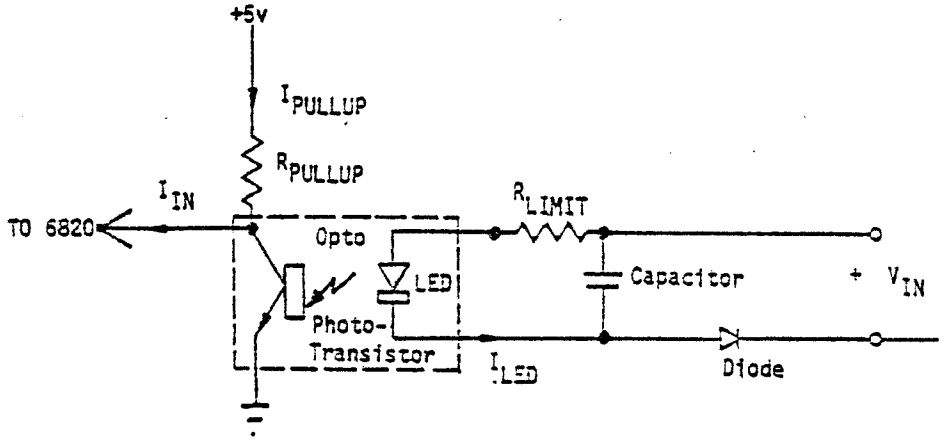


Figure 3-5. Input Voltage Adaptor Circuit

Use the following calculations to determine the active and non-active ranges of the forward current in the LED (I_{LED}).

For CA1 and CB1:

Input leakage is 2.5 microamps (max). Since this amount is negligible, the input current to the 6820 (I_{IN}) is virtually 0. Therefore, the current through the pullup resistor (I_{PULLUP}) is equal to I_C, where I_C is the collector current in the photo transistor of the opto-isolator. Input high voltage (V_{IH}) is 2.0 volts (min) which makes the voltage across the R_{PULLUP} equal to Vcc (+5v) - V_{IH} (+2.0) = 3 volts.

$$I_{PULLUP}\ (max) = I_C\ (max) = \frac{3\ volts}{2.2K\ ohms\ (R_{PULLUP})} = 1.36\ milliamps\ (max)$$

With current transfer ratio (CTR) = 35%, I_{LED} = 3.90 milliamps (max)

Therefore, the maximum input current through the LED (I_{LED}) allowable for a logic HIGH at the CA1 or CB1 input to the 6820 is 3.9 milliamps.

Input low voltage (V_{IL}) is 0.8v (max). Therefore, the minimum voltage across the R_{PULLUP} = Vcc - V_{IL} = 5.0 - 0.8 = 4.2v.

$$I_{PULLUP}\ (min) = I_C\ (min) = \frac{4.2v}{2.2K\ ohm} = 1.91\ milliamps\ (min).$$

With CTR = 35%, I_{LED} = 5.45 milliamps (min)

Thus, the minimum input current through the LED (I_{LED}) for a logic LOW at the CA1 or CB1 input to the 6820 is 5.45 milliamps.

For inputs PA0-PA7:

Input high current (I_{IH}) = -100 microamps (min)
Input low current (I_{IL}) = -1.6 milliamps (max)
Input high voltage (V_{IH}) = 2.0 (min)
Input low voltage (V_{IL}) = 0.8 (max)

For a logic HIGH at the 6820:

$$I_{PULLUP}\ (max) = \frac{Vcc - V_{IH}}{R_{PULLUP}} = \frac{5.0 - 2.0}{2.2K} = 1.36\ milliamps\ (max)$$

$$I_C = I_{PULLUP} - I_{IH} = 1.36 - (-.1) = 1.46\ milliamps\ (max)$$

$$I_{LED}\ (max) = I_C/CTR = \frac{1.46}{35} = 4.17\ milliamps\ (max)$$

For a logic LOW at the 6820:

$$I_{PULLUP}\ (min) = \frac{Vcc - V_{IL}}{R_{PULLUP}} = \frac{5.0 - 0.8}{2.2K\ ohms} = 1.91\ milliamps\ (min)$$

$$I_C = I_{PULLUP} - I_{IL} = 1.91 - (-1.6) = 3.51\ milliamps\ (min)$$

$$I_{LED}\ (min) = I_C/CTR = \frac{3.51}{.35} = 10.03\ milliamps\ (min)$$

The active and inactive LED currents are shown in Table 3-B.

Table 3-B

Active and Inactive LED Currents

	For CA1, CB1			For PA0-PA7		
All in mA	Min.	Nominal	Max.	Min.	Nominal	Max.
I_{LED} for input LOW	5.45	10	100	10.03	15	10
I_{LED} for input HIGH	-0.1μA	0	3.90	-0.1μA	0	4.1

When the input voltage to the network (V_{IN}) is a pulse less than 20 microseconds in duration, the switching time of the opto-isolator may be too slow to react to it. To add flexibility to the inputs so that short pulses can be detected, pads are provided to form a pulse stretching capacitor (C) as shown in Figure 3-6.

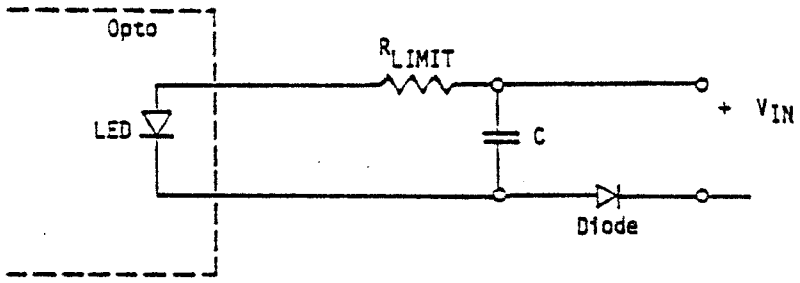


Figure 3-6. Pulse Stretching Capacitor

With a short pulse condition, the values of R_{LIMIT} and C for the user's own pulse height, width and shape can best be determined by empirical testing and by the capacitive drive capability of the input signal. The following paragraph and Figure 3-7 contain starting information that is helpful for this purpose.

The capacitor will be charged to the maximum input voltage (V_{IN}) less the forward voltage of the diode (V_D = approximately 0.7v). When the input voltage returns LOW, use the following formula to find the LED current.

$$I_{LED} = \frac{Vc - 1.3}{R} \; e^{(-t/RC)}$$

t=time in seconds
Vc=Initial Cap. Voltage
R=R limit
C=Capacitor Size
e=2.71828

Figure 3-7. LED Current Formula

Because the LED in the opto-isolator has a maximum reverse current of 0.1 microamps or 100 nanoamps, the diode should be chosen for low reverse current leakage (I_R).

The opto-isolator inputs supplied by MITS are arranged in an STD TTL interface as shown in Figure 3-8.

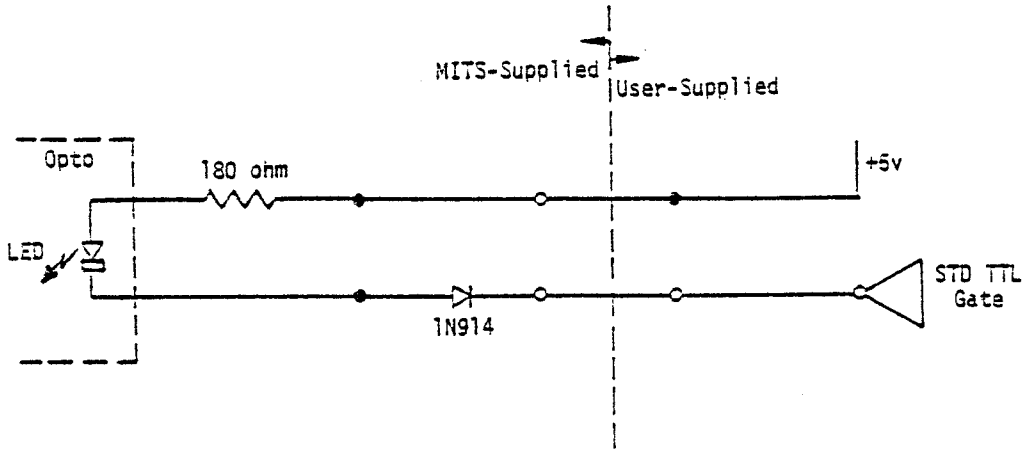


Figure 3-8. STD TTL Interface

In this form the output of the TTL gates will sink approximately 15 milliamps in the LOW state and 5-10 microamps in the HIGH state. Each of these currents is well within the limits shown in Table 3-B, page 3-11.

Table 3-C identifies the names of the individual components in each circuit shown as the general case in Figure 3-9. The two optically isolated outputs (ICAA and ICR) coupled to CA2 and CB2, respectively, are configured as follows:

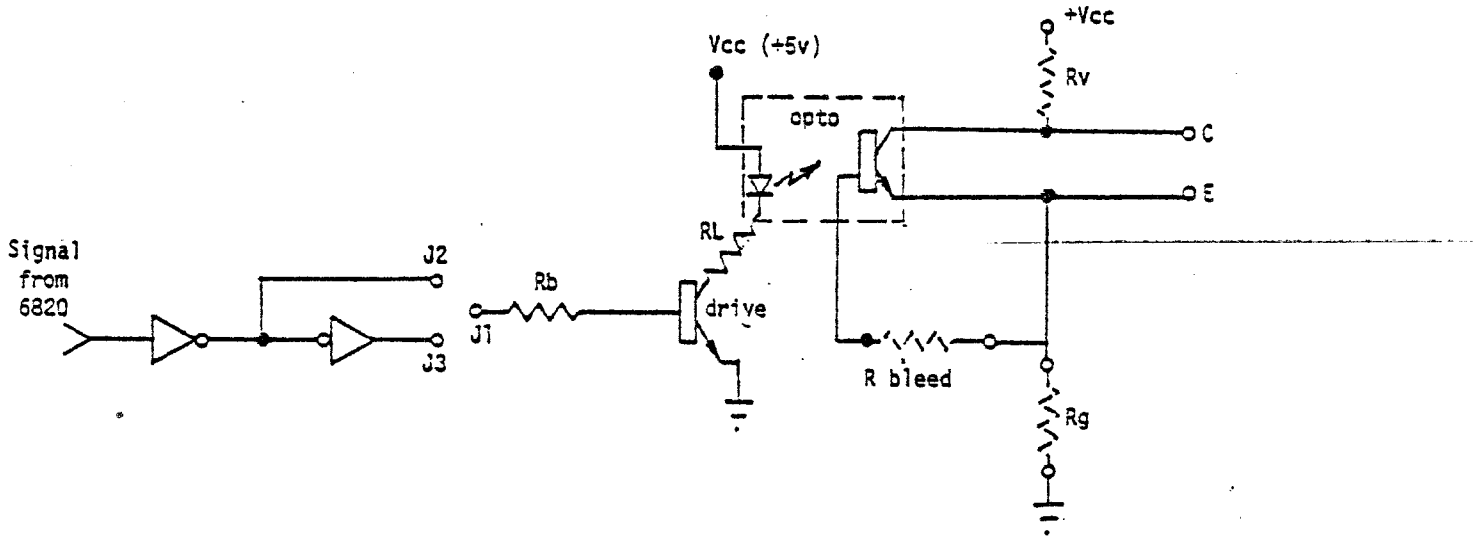


Figure 3-9. R bleed Circuit

Table 3-C

Opto-Isolator Output Configurations								
Signal				Component				
	J1	J2	J3	R_B	R_L	R_V	R_{BLEED}	R_G
CA2	JD	JE	JF	R43	R42	R44	R46	R45
CB2	JA	JC	JB	R18	R17	R20	R47	R19

By connecting a jumper from J1 to J2 or J3, the user can select an operation that will determine whether or not the photo-transistor in the opto-isolator will conduct when CA2 or CB2 is active (HIGH).

When a logic HIGH appears at the base of the drive transistor through R_B, approximately 36 milliamps flow through the LED. Thus, with a CTR of 35%, the photo-transistor can conduct approximately 12.6 milliamps in this HIGH state. The maximum voltage which should be applied to the photo transistor (BV_{CEO}) is 20v, collector to emitter.

The user should be sure not to exceed the maximum dissipation limits of the opto-isolator, which is a total of 200 milliwatts (LED + photo-transistor). When the LED is conducting 36 milliamps, it is dissipating approximately 47 milliwatts. Dissipation in the transistor should therefore be limited to about 150 milliwatts (max).

3-6. OPTO-ISOLATOR OUTPUTS

The speed with which an opto-isolator responds to a signal (bandwidth) depends almost entirely upon the sensor. For example, switching time is a function of the transistor base storage time and the output-circuit time constant. For better sensitivity, these parameters are traded off. The larger the collector base junction, the more sensitive the photo-transistor. This results in longer storage time and slower switching time.

One problem often encountered when applying opto-isolators is minimizing switching time while using practical values of load resistance. (Time is directly proportional to R_L and C_{ob}, where R_L = Load Resistance and C_{ob} = Open Circuit Base Capacitance.) In most photo transistors, relatively long time constants occur in the output circuit because the typical value of C_{ob} is approximately 25 picofarads. This time will be proportional to β where β is the photo transistor's current gain. For example, for a 500 ohm load, a photo-transistor with a typical minimum β value of 100 and a C_{ob} of 25 picofarads yields a time constant of 1.25 microseconds--(500) (25 x 10 - 12) (100) = 1.25 msec. Switching time is 5 time constants of 6.25 microseconds. This corresponds to a bandwidth of only 130 KHz. When using load resistance values greater than 1K ohm, signals of no more than 500 KHz are executable with conventional opto-isolators.

The solution to the problem of long time constants is to provide an external path for removal of the stored charge. This can be accomplished by adding a base-to-emitter bleed resistor (R bleed in Figure 3-9, page 3-13) which will reduce sensitivity and Current Transfer Ratio (CTR), and which will decrease the photo-transistor's switching time. The limiting condition is zero ohms of bleed resistance which shorts the base to emitter of the photo transistor, thus converting the device to a photo diode. It is at this point that the highest possible speed and the lowest sensitivity occur.

A resistor is not supplied for R bleed because current switching ability associated with infinite resistance is desirable, and switching speed is adequate for most applications. If a higher speed is needed, it can be achieved by experimenting with various values for R bleed. However, this will reduce the CTR considerably, and provisions in the external circuitry may have to be made to compensate for the lower switched current in the photo transistor.

Pads are provided for Rv and Rg (see Figure 3-9, page 3-13) which may be used to implement signals referenced to the computer's Vcc and GND. It is advisable to use these pads only where short cable runs are used and where isolation is unimportant. Generally, the supply and ground for the signals should be implemented in an external isolated chassis. Some examples of external output connections are shown below in Figures 3-10a through 3-10d.

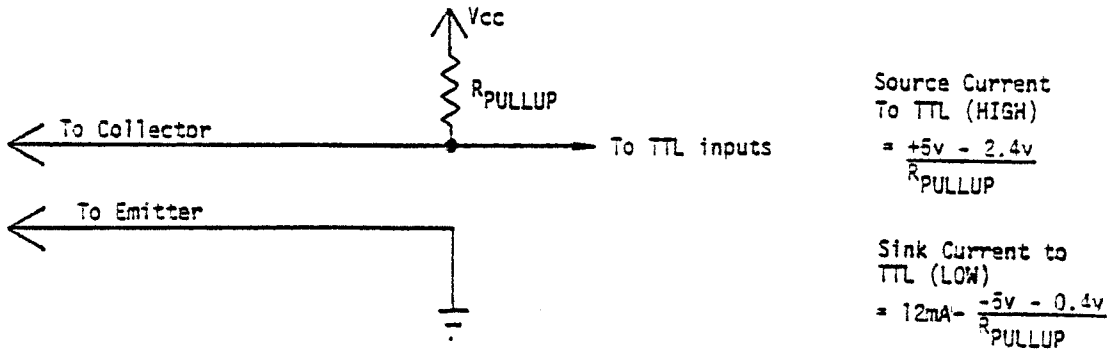


Figure 3-10a. External Output Connections

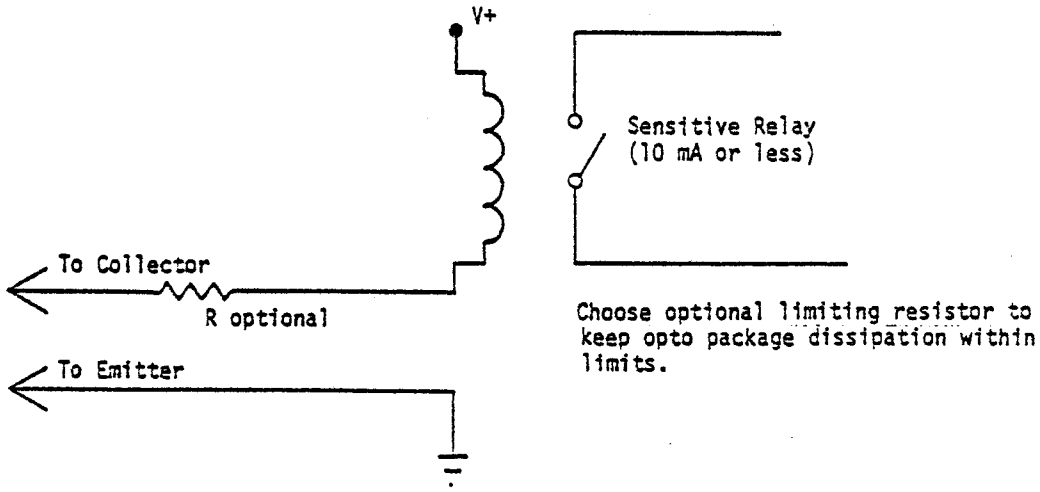


Figure 3-10b. External Output Connections.

For more source current:

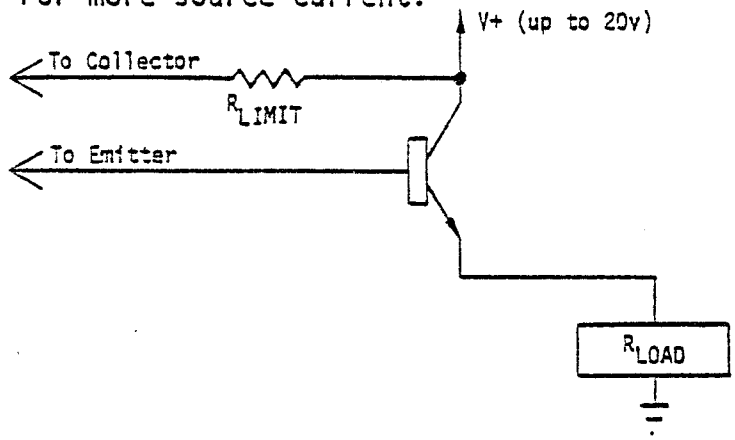


Figure 3-10c.
External Output Connectio..

For more sink current:

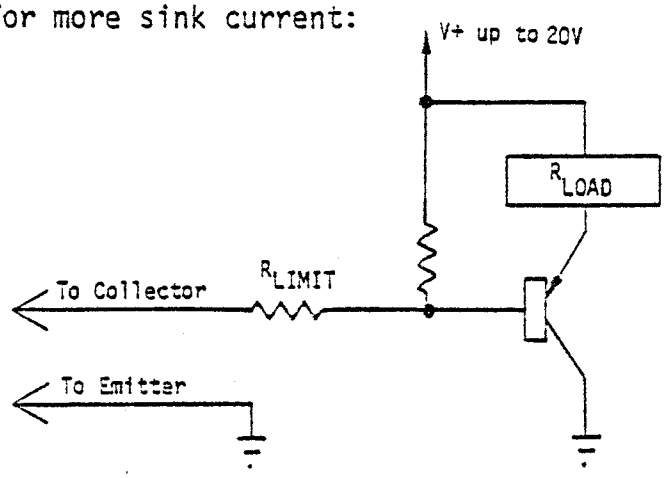


Figure 3-10d.
External Output Connections

3-7. SOFTWARE INITIALIZATION

Before the Process Control Interface board can be used, the 6820 PIA's Data Direction Registers and Control/Status Registers must be initialized. Refer to the Internal Register Addressing Diagram, Table 3-D. The two Data Direction Registers tell the peripheral interface whether to set up its lines as inputs or outputs. The two Control/ Status Registers control the functions of the CA1, CB1, CA2 and CB2 signals.

Table 3-D

Register Selection						
RS0	A0	RS1	A1	CRA-2	CRB-2	Register Selected
1	0	0	0	X	X	Control/Status Register (Section A)
1	0	1	1	0	X	Data Direction Register (Section A)
1	0	1	1	1	X	Data Register (Section A)
0	1	0	0	X	X	Control/Status Register (Section B)
0	1	1	1	X	0	Data Direction Register (Section B)
0	1	1	1	X	1	Data Register (Section B)

The Control/Status Registers also determine whether to write to the Data Register or the Data Direction Register. When writing to the Data Direction Register, it is necessary to set bit 2 of the Control/Status Register to Ø. This is accomplished by writing a Ø to the Control/Status Register of the section you are working with (A or B). The A Section Data Direction Register is enabled by writing Ø's to the base address ("A" Control/Status Register); and the B Section Data Direction Register is enabled by writing Ø's to the base address + 2 ("B" Control/Status Register).

Refer to Table 3-D, page 3-17. With Bit 2 of the Control/Status Registers set at Ø, the next time the user writes to the Data Channels (base address + 1 and base address + 3), he would be writing to the Data Direction Registers. Section A is connected to the opto-isolator inputs, and Section B is connected to the relays (outputs). Therefore, to initialize Section A (at base address + 1) as an input section, Ø's should be written to the Data Direction Register. To initialize Section B (at base address + 3) as an output section, 1's should be written to the Data Direction Register. (See example initializations in the Applications Software Section, page 3-21).

When the Data Direction Registers of Sections A and B have been initialized, the Control/Status Registers may be set up for their final operating form. Bit 2 of the Control/Status Register must be set to 1. This will move the addressing from the Data Direction Registers to the Data Registers.

Refer to Tables 3-E.1 through 3-E.4 for information on the various options of the control lines and their interaction with the interrupt request lines and status bit in the Control/Status Register.

Table 3-E.1. Control Line Options

Bit #	7	6	5 4 3	2	1 0
C/S Section A	IRQA 1 flag	IRQA 2 flag	CA2 Control	DDR-A Access	CA1 Control
C/S Section B	IRQB 1 flag	IRQB 1 flag	CB2 Control	DDR-B Access	CB1 Control

Table 3-E.2. Control Line Options

C/S bit 1	C/S bit 2	CA1 or CB1	Intr. flag C/S bit 7	MPU $\overline{IRQ}$
0	0	↓ active	Set HIGH	disabled
0	1	↓ active	Set HIGH	Goes LOW when C/S bit 7 goes HIGH
1	0	↑ active	Set HIGH	Disabled
1	1	↑ active	Set HIGH	Goes LOW when C/S bit 2 goes HIGH
↓ = from HIGH to LOW signal transition				1=Logic HIGH
↑ = from LOW to HIGH signal transition				0=Logic LOW
Section A: C/S bit 7 (Int. flag) is Reset (LOW) by a read of A Section Data Channel Register.				
Section B: C/S bit 7 (Int. flag) is Reset (LOW) by a read of B Section Data Channel Register.				

Table 3-E.3. Control Line Options

CB2:				
C/S Bit 5	C/S Bit 4	C/S Bit 3	Cleared	Set
1	0	0	Low on ↑ of first E pulse after write of B Data Channel Register after C/S bit 7 is reset by a read of B Data Channel Register.	HIGH when Int. flag (C/S bit 7) is SET.
1	0	1	LOW on ↑ of first E pulse after a write of B Section Data Channel Register	HIGH on ↑ of next E pulse.
1	1	0	Always LOW when bit 3 LOW	
1	1	1		Always HIGH when bit 3 is HIGH.
CA2 and CB2 differ slightly in function.				

Table 3-E.4. Control Line Options

For CA2:				
C/S Bit 5	C/S Bit 4	C/S Bit 3		
1	0	0	LOW on ↓ of E pulse after read of "A" Data Channel Register	HIGH when Int. flag (C/S bit 7) is set.
1	0	1	LOW on ↓ of E pulse after read of "A" Data Channel Register	HIGH on ↓ of first E pulse which occurs while device is deselected.
1	1	0	Same as CB2	
1	1	1		Same as CB2.

3-8. APPLICATIONS SOFTWARE

Note: Throughout the Applications Software section the 88-PCI board is assumed to be addressed at location 100 (octal):

base address = 100 (octal) 64_{10} - opto-isolator input Control/Status

base address + 1 = 101 (octal) 65_{10} - opto-isolator input data + Data Direction Register

base address + 2 = 102 (octal) 66_{10} - Relay Control Control/Status

base address + 3 = 103 (octal) 67_{10} - Relay Control Data + Data Direction Register

The following programs are sample initialization programs for the 88-PCI in Machine Language and in BASIC.

Program I. Machine Language Initialization

Address	Contents	Mnemonic	Description
000	076	MVI→A	Load all Ø's to Accumulator A
1	000	data	
2	323	OUT	Zero Control/Status Register (making bit 2 = 0, giving access to DDR)
3	100	address	
4	323	OUT	Write zeros to DDR of Section A, making PA lines inputs
5	101	address	
6	323	OUT	Zero "B" Control/Status Register (make Bit 2 = 0, giving access to "B" DDR)
7	102	address	
010	076	MVI→A	Load all 1's to Accumulator
1	377	data	
2	323	OUT	Write 1's to DDR of Section B. Make PB lines outputs.
3	103	address	
4	076	MVI→A	Load Accumulator with 00100100 bit pattern
5	044	data	
6	323	OUT	Write 044 (octal) to "A" C/S set function as in Table 3-E.
7	100	address	
020	323	OUT	Write 044 (octal) to "B" C/S set functions as in Table 3-E.
1	102	address	

Program II. BASIC Language Initialization

```
Out 64, 0
Out 65, 0
Out 66, 0
Out 67, 255 (377 octal = 255 decimal)
Out 64, 36 (044 octal = 36 decimal)
Out 66, 36
```

Some examples of input and output software are shown below.

Program III. INPUT

Address	Contents	Mnemonic	Description
n	333	IN	—input from A data (opto inputs)
n+1	101	address	
n+2	346	ANI	—logical AND with immediate data (mask for bits of interest)
n+3	XXX	data	
n+4	302 or 312	JNZ or JZ	—conditional jump or subroutine call
n+5	XXX	low address	
n+6	XXX	high address	

Program IV. OUTPUT

(to turn on a specific bit without affecting others)

Address	Contents	Mnemonic	Description
n	333	IN	—read output register for existing condition
n+1	103	address	
n+2	366	ORI	—OR with data of bits to turn on (to turn on bit 0, data would be 001 octal)
n+3	XXX	data	
n+4	323	OUT	—output new control word
n+5	103	address	

Program V. OUTPUT

(to turn off a specific relay without affecting others)

Address	Contents	Mnemonic	Description
n	333	IN	—read existing output register
n+1	103	address	
n+2	346	ANI	—AND with complement of bits to be turned off (to turn off bit 0, data would be 376 octal)
n+3	XXX	data	
n+4	323	OUT	—output new control word
n+5	103	address	

Program VI. OUTPUT

(when you know what state you want the relays in, the output is simple):

Address	Contents	Mnemonic	Description
n	076	MVI→A	load on and off bit pattern
n+1	XXX	data	to accumulator
n+2	323	OUT	output to relay control
n+3	103	address	channel

3-9. HARDWARE APPLICATIONS

The 88-PCI board can be used in almost any instance in which the computer must control large amounts of power. The relays can directly control up to 120 watts, and with external contacters and solenoids added, the amount of power that can be controlled is essentially unlimited. Paragraph 3-10 contains a list of possible applications, and paragraph 3-11 gives detailed descriptions of two specific applications.

NOTE

Before actually beginning a project, it may be necessary to review the Hardware Set-Up procedure, paragraphs 3-2 through 3-6.

3-10. APPLICATIONS IDEAS

The applications listed below are just a few of the many areas in which the 88-PCI may be utilized. Hopefully, these applications will stimulate new ideas; and any interesting concepts developed by users will be welcomed in the MITS Technical Publications Department. Original and imaginative applications ideas will be published in Computer Notes or as an "Application Note".

1. Household:

Input	Output
a. thermostats	e. heater/cooler
b. alarm sensors	f. alarms
c. clock	g. coffee
d. manual switches, remote control transducers	h. stereo

2. Ham Radio:

Input	Output
a. signal strength comparator	c. antenna rotater
b. end of tape sensor	d. recording equipment
	e. power switch for transmitters

3. Test Control:

Input	Output
a. thermostats	d. heaters/coolers
b. remote logic input	e. power supplies
c. comparators	f. load switching

4. Agriculture:

Input	Output
a. flow meters	f. pumps
b. pressure sensors	g. solenoid valves
c. automatic material weighing	h. conveyor motors
d. position switches	i. hopper control
e. thermostats	j. distribution control

5. Chemical Process Control:

Input	Output
a. ph meters	e. agitator motors
b. thermostats	f. pumps
c. viscosity testers	g. valves (solenoid)
d. flow meters	h. hopper control
	i. heaters

6. Industrial Process Control:

Input	Output
a. strain gauges	g. tool motor power
b. limit switches	h. tool position motors
c. pressure transducer	i. valves (solenoid)
d. thermostats	j. heaters
e. position sensor	k. rejector solenoid
f. miscellaneous tester outputs	l. solenoid operated stampers

3-11. SPECIFIC APPLICATION DESCRIPTIONS

The following paragraphs describe two specific applications (lawn sprinkler control and solar tracking) in detail.

A. Lawn Sprinkler Control

There are several factors to be considered with this application. Naturally, the most important factor is the amount of moisture in the ground. Moisture can be measured by installing a humidistat in the lawn. Another consideration is the amount of water absorption compared to the level of evaporation. This data will help determine the most effective time to do the watering. A measurement of wind speed may be used as a simple parameter for this purpose. An elementary "go/no-go" device can be set up which will inhibit watering if wind speed exceeds a set limit.

Temperature and relative humidity also have an effect on evaporation. These two parameters may be sensed directly. However, in any given 24-hour period, optimum temperature and humidity usually occur at night. With this in mind, a photo cell may be implemented to tell the computer whether it is day or night.

When the lawn is too dry to wait for optimum watering conditions, a more complex humidistat or a second humidistat with a different setting may be installed to signal this condition.

If it is necessary to water different areas of the lawn separately, additional humidistats and solenoid valves may be installed in each area.

If your city charges premium water prices during heavy usage hours, an input from a clock can tell the computer when the lower rates are in effect.

If there is an irrigation system as well as a normal water system in your area, a float switch may be installed in the irrigation ditch. This will enable the computer to sense the presence of water. The irrigation water can then be pumped from the ditch to water the lawn.

B. Solar Tracking

In recent years the use of solar tracking mechanisms has become well-recognized for such uses as solar boilers for heating, solar boilers (fed to small turbines) for electrical generation, solar cooking ovens, and many scientific uses.

Several questions to consider when designing a solar tracker control system are:

1. How will the tracker know if it is on target?
2. If it is not on target, how will it know which way to go?
3. How will it know how far to go?
4. Will it search endlessly at night, or will it track the moon?

One means of resolving these problems is to construct a solar collector and solar sensor in a common chassis with parallel center focal axes, as shown in Figure 3-11.

Refer to Figure 3-12. The sensor is aligned so that it can detect an offset in rotation. Thus, when the sun is not on the sensor's focal axis, light will fall on one of the photo-transistors. The geometry of the sensor can be adjusted for the degree of tracking accuracy desired.

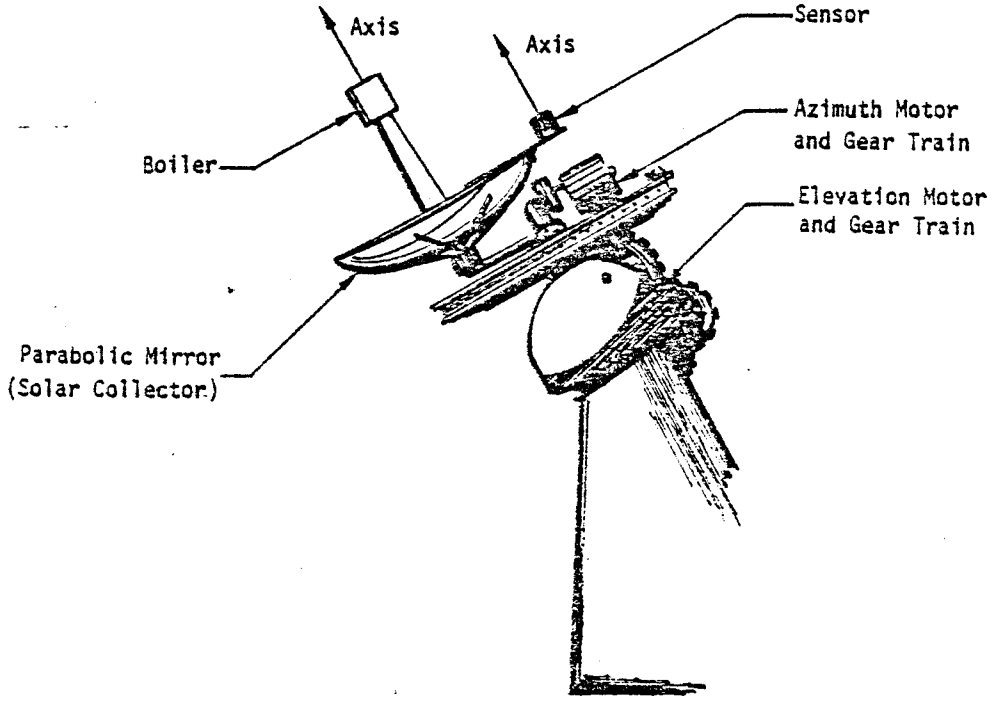


Figure 3-11. Solar Collector and Sensor

Two sensors are required; one for the elevation axis, and one for the azimuth. Infrared type photo-transistors should be used as they are the most discriminating, i.e., they will not track the moon, clouds, etc.

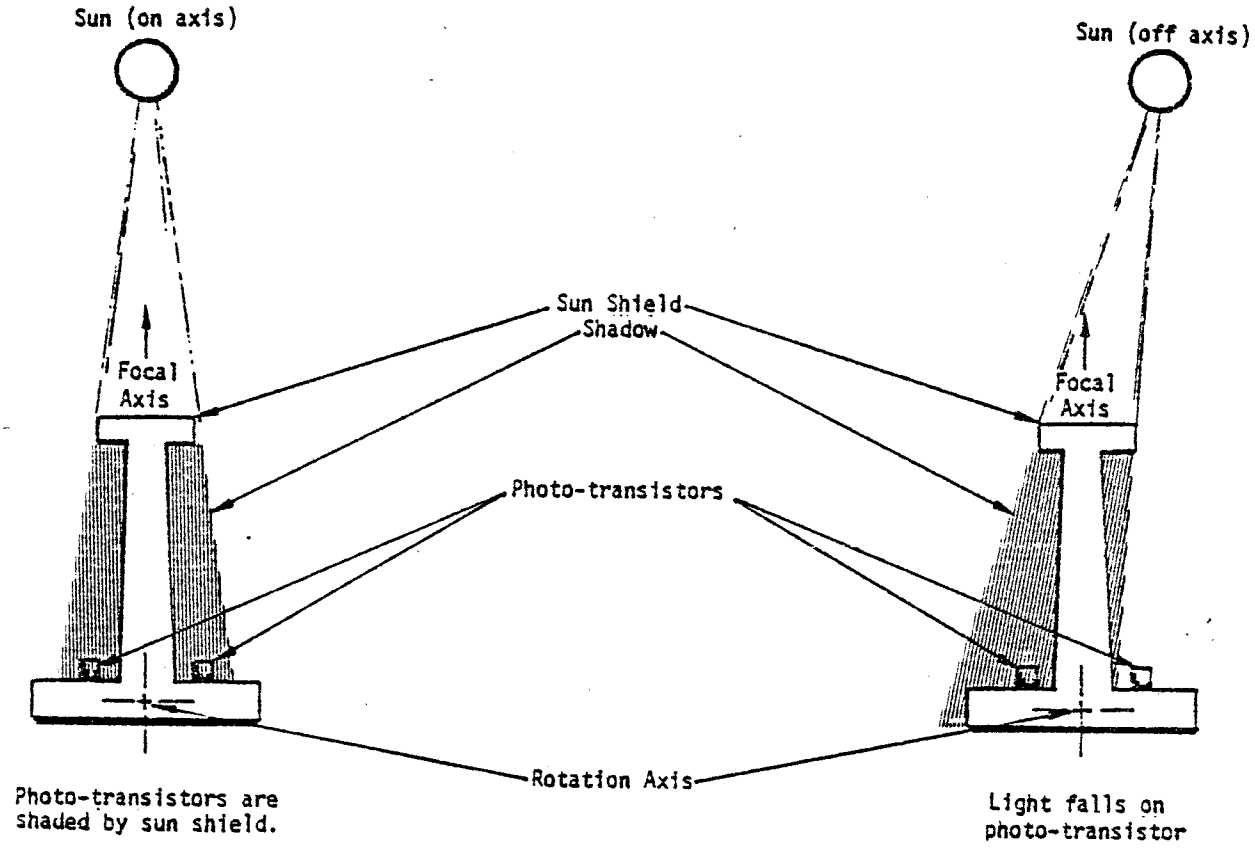


Figure 3-12. Solar Sensor Diagram

The circuit shown in Figure 3-13 can be used to connect the sensors to the 88-PCI. Four such circuits should be used to provide the four inputs to the board (above, below, right and left). All are low active at the PIA. The software should scan the inputs periodically and adjust the position until all the signals are extinguished. The adjustment may use four relay outputs; two for the elevation motor (up, down) and two for the azimuth motor (right, left).

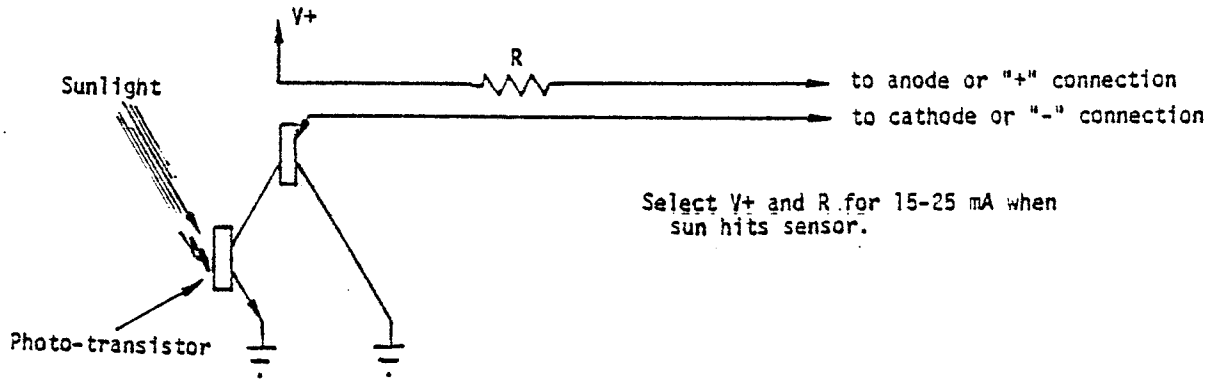


Figure 3-13. Sensor Connections

A general sun sensor which measures the amount of sunlight is another possible input. Refer to Figure 3-14. This sensor enables the computer to sense whether or not there is sufficient light to track. The sensor can also be used to signal the computer during damaging weather conditions (wind, hail, etc., since the sky is usually dark). In this case, the computer will cause the elevation motor to turn the collector face down. The sensor should be placed where it can sense the sun at any time of day.

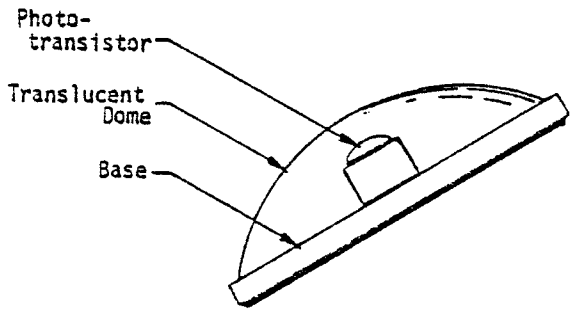


Figure 3-14. General Sun Sensor

SECTION IV
88 PCI
TROUBLESHOOTING

4-1. INTRODUCTION

Section IV is designed to aid the user in pinpointing trouble areas and correcting problems that may be encountered with the 88-Process Control Interface board. Contained in this section are: a preliminary check to make sure the board has no obvious mechanical problems (such as loose or missing parts, foreign articles, etc.), a power supply check (Table 4-A), an Address Decoding Circuit and RESET check (Table 4-B), a Relay Output check (Table 4-C) along with a test program, an Opto-Isolator check (Table 4-D) and a Control Line check (Table 4-E).

These troubleshooting procedures are intended only as a guide. They contain basic instructions that should help in locating and correcting most malfunctions. However, if the problem(s) encountered cannot be rectified with the help of this section, send the board to the MITS Repair Department or your local Altair dealer.

Before beginning the troubleshooting procedures, it is helpful to have a clear understanding of the board's operation. Refer to the Theory of Operation portion of this manual (Section II) whenever necessary.

4-2. PRELIMINARY CHECK

The first step in troubleshooting is to carefully examine the board for solder bridges, open lands or misplaced components. Each 88-PCI board is carefully assembled and tested at the MITS factory, and problems of this kind should not occur. However, to avoid long hours of troubleshooting, a preliminary check should always be made, as improper handling could cause broken leads, lost parts or foreign articles to be lodged on the board.

4-3. POWER SUPPLY VOLTAGE CHECK

The next step in troubleshooting is the power supply voltage check. A defective power supply can cause problems on every part of the board. Refer to Table 4-A, page 4-2, for proper voltages. If the voltages check out, but the board is still inoperative, double check your program. If the program is correct, proceed to Table 4-B, page 4-4. If only one or two inputs or outputs appear to be defective, refer to the Relay Test Program, Page 4-7, and Table 4-C, page 4-6, for outputs and to Table 4-D, page 4-9, for inputs.

Table 4-A

Step	Instructions	Power Supply Voltage Check If Correct	If Incorrect
1	Check the output pin (far right pin) of the Voltage Regulator.	It should read approximately +5v. If so, proceed to Step 3.	If +5v is not read, proceed to Step 2.
2	Check the input pin (far left pin) of the Voltage Regulator.	It should read +5v to +9v unreg. If so, proceed to Step 4.	Possible problem with the 8800 system. Refer to the 8800 manual.
3	Check the Vcc pins on each of the ICs (pin 14 of the 14-pin ICs) for proper voltage.	Proceed to Table 4-B.	Check the Vcc lines for opens. Correct as necessary.
4	Check for shorts in the +5v line to GND.	If no shorts are found, the Voltage Regulator is probably defective and should be replaced.	Repair shorts, if found.

4-4. ADDRESS DECODING AND RESET CHECK

The 88-Process Control Interface board must have a unique address. When this address is on the bus, the board must be able to distinguish it from any other. If this distinction is not made, problems will occur. Table 4-B, page 4-4, will aid in locating and correcting these problems.

Table 4-B

Address Decoding Circuit and RESET Check

*Note: This check should be made while the computer is in the Halt mode. The board is assumed to be addressed at location 100 (octal).

Step	Instructions	If Correct	If Incorrect
1	Check pin 34 of IC C for a HIGH.	If HIGH, proceed to Step 2.	If LOW, check ICs E and M.
2	Examine Address 00100 (octal). Check pin 8 of IC B for a LOW.	If LOW, Address and Decode are OK.	If HIGH, Address or Decode problem. Proceed to Step 3.
3	Check the position of the address dip switches (SW1 and SW2) on the board. $\overline{A2}$, $\overline{A3}$, $\overline{A4}$, $\overline{A5}$, $\overline{A7}$ and A6 should be selected.	Proceed to Step 4.	Make correct address selection.
4	Check pins 1, 2, 3, 5, 6 and 12 of IC B for HIGHs.	If all pins are HIGH, IC B is defective and should be replaced.	If all pins are not HIGH, proceed to Step 5.
5	Referring to the schematic, trace the signals from the edge connector through ICs J and F and Switch SW1 or SW2.	Proceed to Step 6.	Replace defective components.
6	Deposit the following program. If you have an oscilloscope to check the signals, actuate RUN. If you are using an ohmmeter, single step the program while watching the meter.		

Table 4-8, continued.

Step	Instructions	If Correct	If Incorrect
	Location Contents 040 333 041 101 042 323 043 102 044 303 045 040 046 000 Check IC D, pins 8, 11 and 3. Pin 8 should go LOW on the input cycle. Pin 3 should go LOW on the output cycle. Pin 11 should go LOW on both cycles.	If correct, proceed to Step 7.	If incorrect, use the schematic to trace the signals back through ICs A, E and D to the connector. Replace defective chips and repair any opens or shorts.
7	Check IC C, pin 25, for LOW going "E" pulses.	If pulses are present, proceed to Paragraph 4-5, Relay Output Check.	If pulses are not present, use the schematic to trace the signals back through ICs E, G and H. Replace defective parts.

Table 4-C

Relay Output Check

*Note: If the contacts did not cause the ohmmeter to deflect, proceed with the following table while continuing to run the program.

Step	Instructions	If Correct	If Incorrect
1	Connect an ohmmeter across the contacts of each relay. As the program runs, the contacts should open and close.	If correct, the Relay Output Section is working properly. Proceed to Paragraph 4-6.	If incorrect, proceed to Step 2.
2	Check the collector of the transistor associated with the inoperative relay.	The collector of the transistor should change from approximately +9v when the transistor is off to approximately -.5v when the transistor is on. If correct, the relay may be defective or a bad connection may exist.	If incorrect, proceed to Step 3.
3	Check the base of the transistor.	The signal should alternate from approximately 0v to approximately +2v. If the reading is correct, the transistor is probably defective and should be replaced.	If a 0v to +2v signal is not read, the problem may lie within the PIA itself. Replace the PIA or send the board to the MITS Repair Department.

4-5. RELAY OUTPUT CHECKS

Refer to the Machine Language Initialization program in Paragraph 3-8, page 3-22. Enter that program and the following program to check the relay outputs. The program below causes the relays to open and close with a 50% duty cycle at approximately 1Hz (one cycle per second). A click should be heard each time the relays open followed by another click when the relays close.

Connect an ohmmeter across each relay contact on the P2 connector. The meter will deflect as the contacts open and close. If the meter fails to deflect, proceed to Table 4-C.

Program VII. Relay Output Check

Address	Contents	Mnemonic	Comments
040	001	LXI B←C	
1	000	data	Load starting Count to B←C Registers
2	202	data	
3	013	DCX B←C	Decrement
4	170	MOV A←B	Move B Register to Accumulator
5	346	ANI	Set status flags
6	377	data	
7	302	JNZ	
050	043	address low order	Jump if not zero
1	000	address high order	
2	171	MOV A←C	Move C Register to Accumulator
3	346	ANI	Set status flags
4	377	data	
5	302	JNZ	
6	043	address low order	Jump if not zero
7	000	address high order	
060	172	MOV A←D	Move D Register to Accumulator
1	057	CMA	Complement Accumulator
2	127	MOV D←A	Move Accumulator to D Register
3	323	OUT	OUTPUT to Relays
4	103	address	
5	303	JMP	
6	040	address low order	Jump back to Start
7	000	address high order	

4-6. 6820 INPUT CHECK

To test the 6820's input lines and control lines, refer to Table 4-D.

Table 4-D

Input Check

*Note: This troubleshooting procedure is written assuming that R33-R41 and R21 are 180 ohm resistors, and D9-D18 are 1N914's as supplied by MITS.

Step	Instructions	If Correct	If Incorrect
1	Leave the input connections to the opto-isolators open. Measure pin 5 of the opto-isolators; it should be approximately 5v.	Proceed to Step 3.	Proceed to Step 2.
2	Check the Vcc connections to pullup resistors R23-R32 and R21. Check the GND connection to pin 4 of the opto-isolators.	If correct, an opto-isolator is probably defective and should be replaced.	If incorrect, make connections.
3	Connect the "+" (anode) input line (pins 1, 4, 6, 8, 10, 12, 18, 20 and 22 of P2 and pin 23 of P1) to Vcc (+5v). Connect the "-" (cathode) input line (pins 2, 3, 5, 7, 9, 11, 17, 19 and 21 of P2 and pin 22 of P1) to GND. Check the voltage on pin 5 of the opto-isolators. It should be less than 0.8v.	If correct, the opto-isolator inputs and associated circuitry are OK. If problems still exist, the PIA may be defective.	Proceed to Step 4.
4	Measure the voltage from pin 1 to pin 2 of the opto-isolator. It should be approximately 1.3v.	Proceed to Step 5.	If the voltage is 5v, the opto-isolator is defective. If the voltage is 0, check connections.
5	Check the voltage from pin 4 to pin 5 of the opto-isolators. It should be less than 0.8v.	If correct, check connections.	If incorrect, the opto-isolator is defective and should be replaced.

4-7. CA2 and CB2 CONTROL LINE CHECK

Table 4-E is provided to aid in troubleshooting the CA2 and CB2 control lines. This table is written assuming the 88-PCI is addressed at location 100 (octal). Place 1K ohm (or higher) resistors at R44 and R20. Jumper R45 and R19, and enter the following program.

Program VIII. Control Line Check

Location	Contents	Mnemonics
040	076	MVI, A
1	064	data
2	323	OUT
3	100	address
4	323	OUT
5	102	address
6	076	MVI, A
7	074	data
050	323	OUT
1	100	address
2	323	OUT
3	102	data
4	303	JMP
5	040	low order address
6	000	high order address

As you make each check, single step completely through the program at least once.

Table 4-E

Control Line Check			
Step	Instructions	If Correct	If Incorrect
1	Check the voltage at the collectors of the opto-isolators (pin 24 of P2 for CA2, and pin 25 of P1 for CB2). These points should alternate between HIGH and LOW as you single step the program.	If correct, the CA2 and CB2 outputs are OK.	Verify that the active state jumpers (at JA and JD) are in place. Proceed to Step 2.
2	Measure Pin 1 of opto-isolator AA or R. It should be approximately 5v.	If correct, proceed to Step 3.	If incorrect, a bad Vcc connection exists somewhere on the board.
3	Measure the voltage across limit resistors R42 and R17. It should alternate from near 0v to approximately 3v.	If correct, the opto-isolator may be defective.	If incorrect, proceed to Step 4.
4	Check the voltage at the base of driver transistors Q10 and Q9. It should alternate from approximately 0v to approximately 0.7v.	If correct, the driver transistor may be defective.	If incorrect, proceed to Step 5.
5	Check pins 13 and 5 of IC M. They should alternate from approximately 0v to approximately 3-4v.	If correct, IC M may be defective.	If incorrect, the PIA may be defective

SECTION V
88 PCI ASSEMBLY

5-1. INTRODUCTION (Figure 5-1)

Section V contains complete step-by-step instructions for component installation and mounting of the 88-PCI board. Two organizational aids are provided throughout the instructions: 1) parts identification lists with spaces provided to check off each component as it is installed and 2) reproductions of the board's silkscreen showing previously installed components, components being installed and components yet to be installed (see Figure 5-1).

Before beginning the assembly procedure, carefully read the enclosed "MITS Kits Assembly Hints" booklet. It contains helpful suggestions and several important warnings. Failure to heed these warnings could cause you to void the warranty.

Check the contents of the kit using the parts list (Appendix A) to make sure all of the required components are enclosed. As you assemble the board, read each step carefully and follow the instructions in the order in which they are presented. Always complete each step before going on to the next. Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

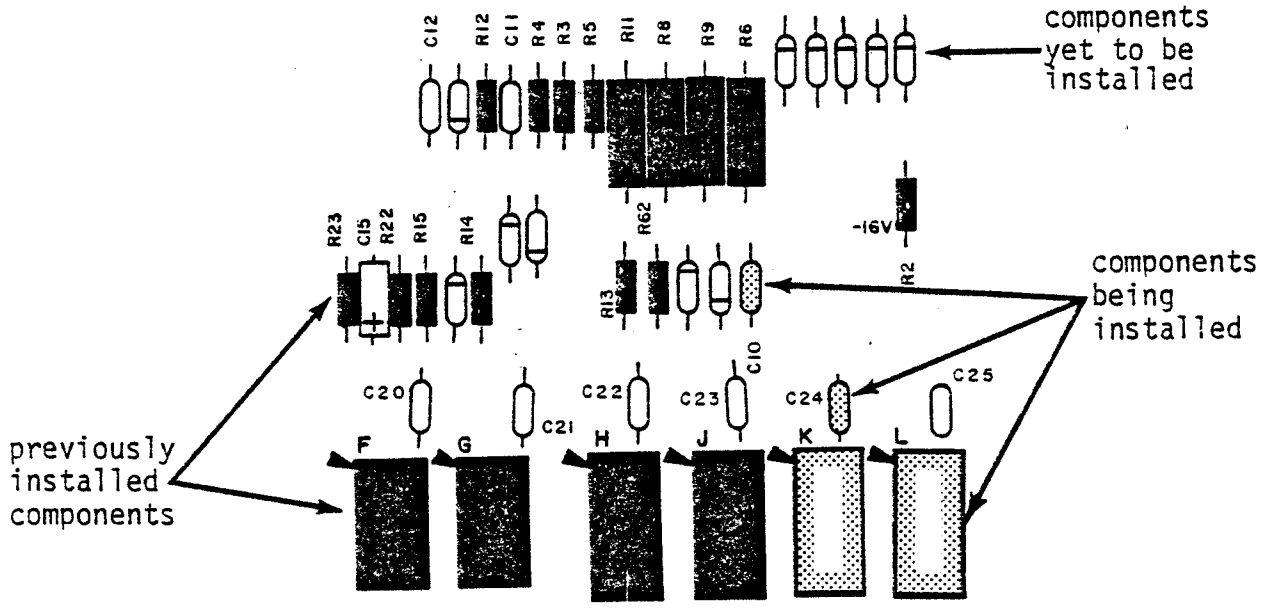


Figure 5-1. Typical Silkscreen

5-2. VISUAL INSPECTION (Figure 5-2)

It is recommended that a visual inspection of the board be made before beginning the assembly procedures. A thorough inspection of this kind will eliminate one possibility for errors should the board fail to operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

Look for etching "bridges" or "opens" in the printed circuit lands, as shown in Figure 5-2 below.

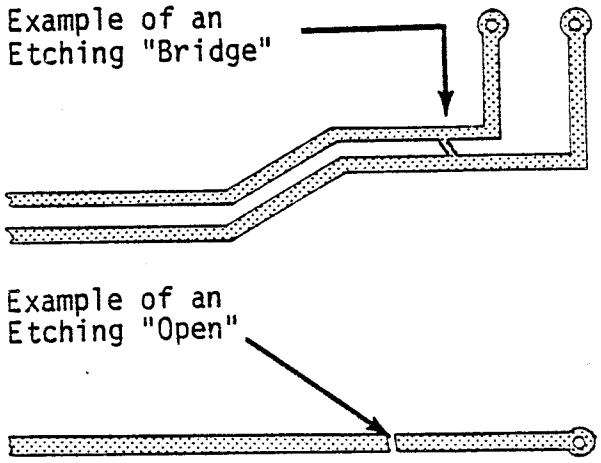


Figure 5-2. Visual Inspection

5-3. COMPONENT INSTALLATION INSTRUCTIONS

Paragraphs 5-4 through 5-11 describe the proper procedures for installing various types of components on the board. Read these instructions carefully, and refer to them when necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void the warranty. Procedures of a less general nature are included in the remainder of the text.

5-4. Resistor Installation Instructions (Figure 5-3)

Resistors have four, or possibly five, color-coded bands as represented in Table 5-A. The fourth band is gold or silver in color and indicates the tolerance. When assembling MITS kits, you need only be concerned with the three bands of color to one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value and the third band represents a multiplier.

For example, a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. Refer to Table 5-A. Red denotes a value of 2 and violet, a value of 7. Multiply 27 by the yellow multiplier band (10,000) to arrive at a total value of 270,000 ohms (270K). The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the specific instructions.

Make sure the colored bands on each resistor match the colors called for in the list of resistor values and color codes given in the specific assembly instructions. When the correct value resistor has been selected, install the resistor according to the following instructions.

1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the board.
2. Install the resistor into its holes on the silkscreened side of the board, and secure by bending the leads slightly outward.
3. Solder the leads to the foil pattern on the back of the board. Clip off any excess lead lengths.

Table 5-A. Resistor Color Codes

Color	Bands 1 & 2	3rd Band (Multiplier)
Black	0	1
Brown	1	10
Red	2	10^2
Orange	3	10^3
Yellow	4	10^4
Green	5	10^5
Blue	6	10^6
Violet	7	10^7
Gray	8	10^8
White	9	10^9

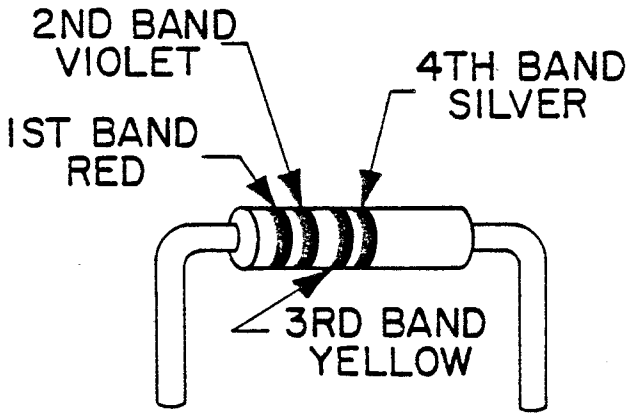


Figure 5-3. Resistor Color Codes

5-5. Capacitor Installation Instructions (Figures 5-4a, 5-4b and 5-4c)

A. Electrolytic and Tantalum Capacitors

Polarity must be noted on electrolytic and tantalum capacitors before they are installed.

Electrolytic capacitors may have one or possibly two of three types of polarity markings as shown in Figure 5-4a.

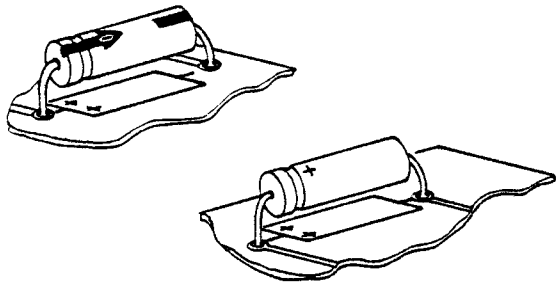


Figure 5-4a. Electrolytic Capacitors

One type has a plus (+) sign on the positive end; another has a band or a groove around the positive side in addition to the plus signs. The third type has an arrow with a negative (-) sign in the tip of the arrow. The capacitor must be oriented so that the arrow points to the negative side.

Tantalum capacitors are marked with "+" signs on the positive side as shown in Figure 5-4b.

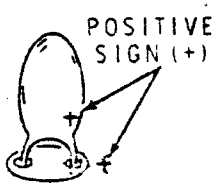


Figure 5-4b. Epoxy Dipped Tantalum Capacitors

Consult the capacitor value chart included with the specific instructions, and install electrolytic and tantalum capacitors according to the following instructions.

1. Bend the two leads of the capacitor at right angles to conform to their respective holes on the board.
2. Insert the capacitor into the holes on the silkscreened side of the board, aligning the positive side with the "+" signs printed on the board. Secure the capacitor in place by bending the leads slightly outward.
3. Solder the leads to the foil pattern on the back of the board. Clip off any excess lead lengths.

B. Epoxy Dipped Ceramic and Ceramic Disk Capacitors

Epoxy dipped ceramic capacitors and ceramic disk capacitors are non-polarized. Both types are shown in Figure 5-4c.

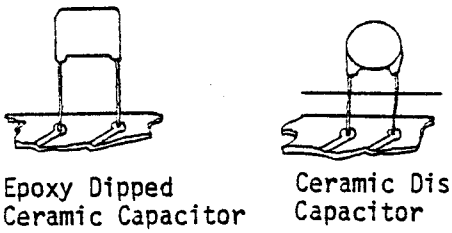


Figure 5-4c. Epoxy Dipped Ceramic and Ceramic Disk Capacitors

Consult the capacitor value chart included with the specific instructions, and install epoxy dipped ceramic and ceramic disk capacitors according to the following procedure.

1. Insert the capacitor into the correct holes from the silkscreened side of the board, and secure in place by bending the leads slightly outward.
2. Solder the leads to the foil (bottom) side of the board. Clip off any excess lead lengths.

5-6. Diode Installation Instructions (Figure 5-5)

Diodes are marked with a band on the cathode end. Each diode must be installed so that the cathode end is oriented towards the band printed on the PC board. Failure to correctly orient the diodes may result in permanent damage to the unit.

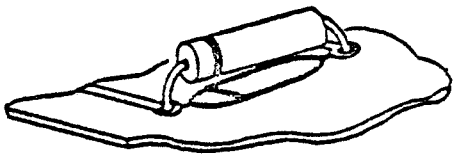


Figure 5-5. Diode Orientation

Use the following procedure to install diodes onto the board. Refer to the list of diode part numbers included in the specific assembly instructions to make sure the correct diode is installed each time.

1. Carefully bend the leads of the diode at right angles to match their respective holes on the board.
2. Make sure the cathode end is properly oriented, and insert the diode into the correct holes on the silkscreen. Secure the diode in place by bending the two leads slightly outward.
3. Solder the two leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

5-7. Transistor Installation Instructions

Use the following instructions to install transistors. Before installation, use the list of transistors included in the specific assembly instructions to check the part number of each transistor. Some transistors may look identical, but differ in electrical characteristics. For this reason, all transistors should be sorted according to part number. If substitute part numbers are given for the transistors, check the transistor identification chart in Paragraph 5-8 to be sure the correct substitutions are made.

Make sure the transistor is oriented so that the emitter lead is installed in the hole on the board labelled with an "E." To determine which lead is the emitter, refer to Figure 5-6.

1. After the correct transistor has been selected and the leads have been properly oriented, insert the transistor into its holes on the silkscreened side of the board, and secure by bending the leads slightly outward.
2. Solder the leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

5-8. Transistor Identification (Figure 5-6)

The outline of each type of transistor and the correct designation for each of the three leads are shown in Figure 5-6. Use this information to determine the correct orientation for transistors.

A list of possible substitutions is given below. If transistors other than the ones shown below are used, damage may occur. When making substitutions, refer to Figure 5-6 to determine the correct orientation for the leads.

2N4410 = EN4410 = CS4410 = CS4437, CS4438, TIS98, ST98, S38473 (NPN)

EN2907 = 2N2907 = PN2907 = ST2907, CS4439 (PNP)

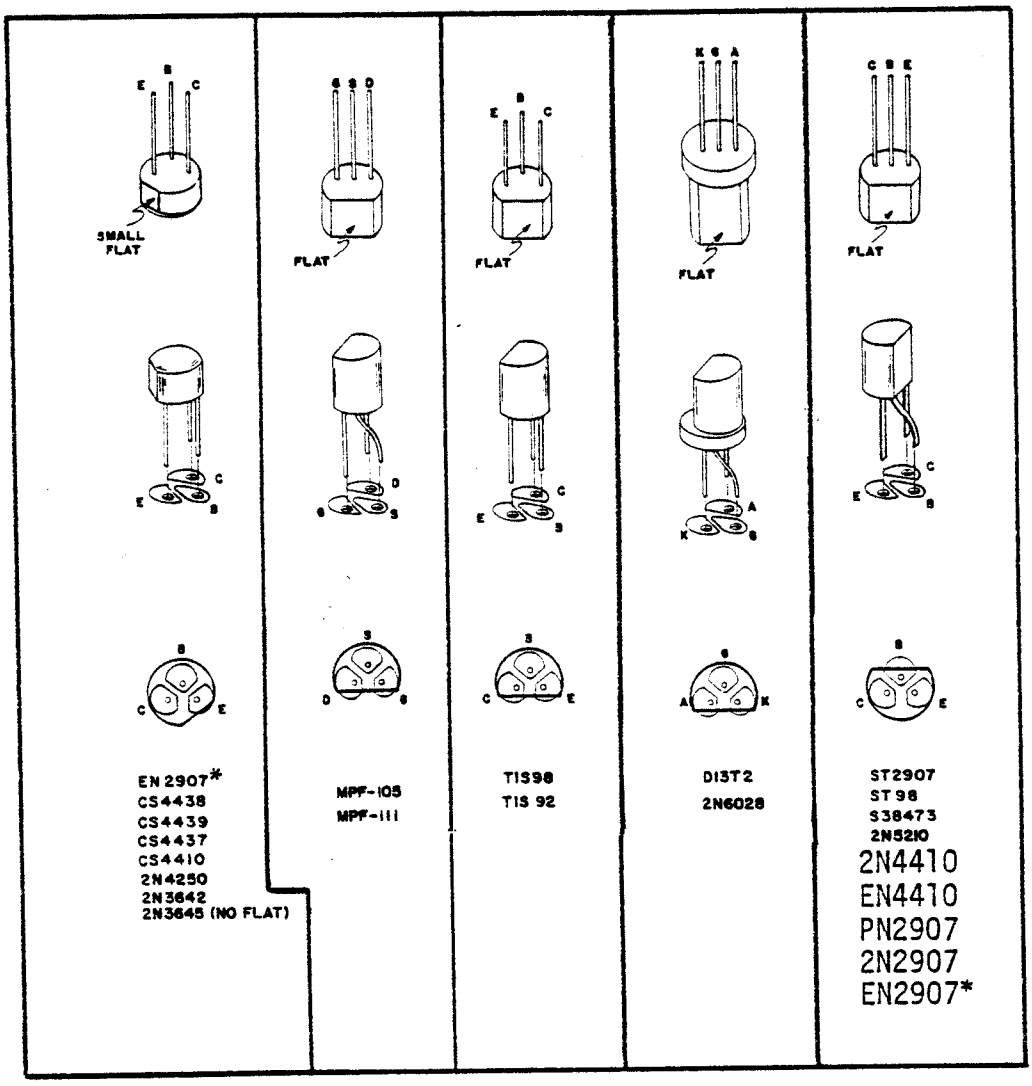


Figure 5-6. Transistor Identification

5-9. IC Installation Instructions (Figure 5-7)

All ICs must be oriented so that pin 1 corresponds with the pad marked with an arrowhead. Refer to Figure 5-8 to identify pin 1. All ICs are easily damaged and should be handled carefully. Always try to hold the IC by the ends and avoid touching the pins as often as possible. When removing the IC from its holder, carefully straighten any bent pins with needle-nose pliers. All pins should be evenly spaced and should be aligned perpendicular to the body of the IC itself.

A. Installing ICs without sockets

1. Orient the IC so that pin 1 coincides with the arrowhead on the PC board.
2. Align the pins on one side of the IC so that just the tips are inserted into their holes on the board.
3. Lower the other side of the IC into place. If the pins do not go into their holes right away, rock the IC back, exert a little inward pressure, and try again. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all of the pins have been started into their holes, push the IC into the board the rest of the way. Secure the IC to the board with masking tape.
4. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges.
5. Clip off any excess lead lengths, and remove the masking tape.

B. Installing ICs with sockets

1. Referring to Figure 5-7, orient the socket so that pin 1 coincides with the arrowhead on the board. Set the socket into its holes, and secure with masking tape.

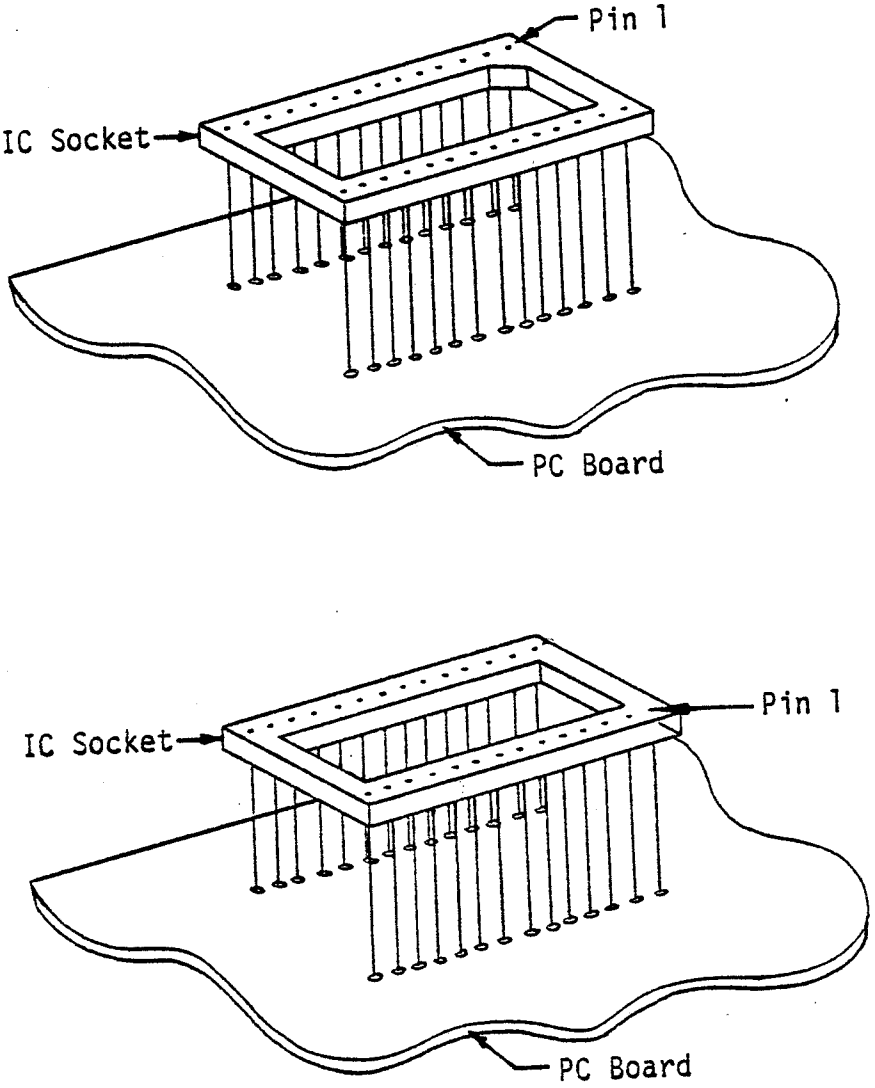


Figure 5-7. IC Socket Installation

2. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges.
3. Clip off any excess lead lengths, and remove the masking tape.
4. Orient the IC over the socket so that pin 1 coincides with pin 1 of the socket.
5. Align the pins on one side of the socket so that just the tips are inserted into the holes.
6. Lower the other side of the IC into place. If the pins do not go into their holes right away, rock the IC back, exert a little inward pressure, and try again. When the tips of all of the pins have been started into their holes, push the IC into the socket the rest of the way.

5-10. IC Identification (Figures 5-8 and 5-8a)

Integrated circuits may have any one, or a combination of, several different markings which are used to determine correct orientation when the ICs are placed on the printed circuit board. Refer to Figure 5-8 to locate pin 1 of the ICs.

Figure 5-8a indicates the various methods used to show the position of ICs on the printed circuit board. These outlines are silkscreened directly on the board. The arrowhead indicates the pin 1 position.

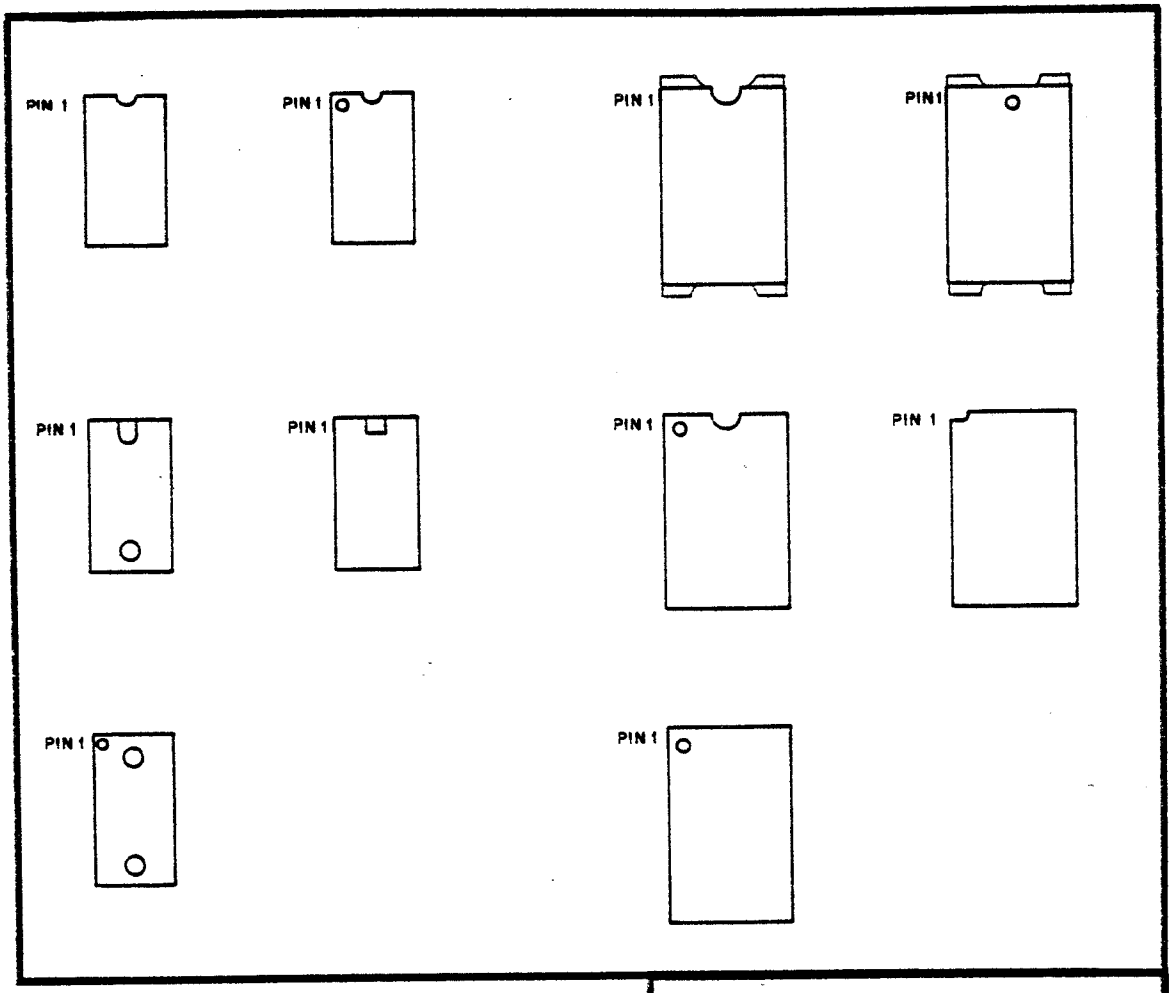


Figure 5-8. IC Identification

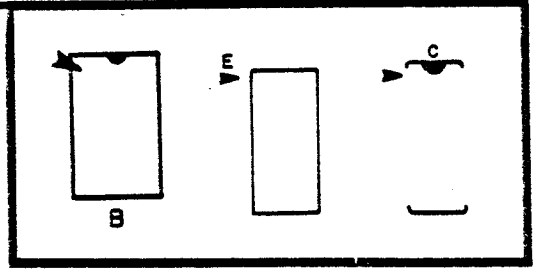


Figure 5-8a. IC Silkscreen Designations

5-11. MOS IC Special Handling Precautions

MOS ICs are extremely sensitive to static electricity and transient voltages. In order to prevent damaging these components, read the following precautions and adhere to them as closely as possible. Failure to do so may result in permanent damage to the IC.

1. All equipment (soldering iron, tools, solder, etc.) should be at the same potential as the PC board, the assembler, the work surface, the IC itself and its container. This can be accomplished by continuous physical contact with the work surface, the components and everything else involved in the operation.
2. When handling the IC, develop the habit of first touching the conductive container in which it is stored before touching the IC itself. If the IC has to be moved from one container to another, touch both containers before doing so.
3. Do not wear clothing that will build up static charges. Cotton is preferable to wool or synthetic fibers.
4. Always touch the PC board before touching the IC to it. Try to maintain this contact as often as possible when installing the IC.
5. Handle the IC by the edges. Avoid touching the pins themselves.
6. Dry air moving over plastic can build up considerable static charges. Avoid placing the IC near any such area or object.

5-12. Diode Installation (Figure 5-9)

Install diodes D1 through D18 (Bag 4) according to the instructions in Paragraph 5-6.

Diode	Part Number
( ) D1 through D8	IN4004
( ) D9 through D18	IN914

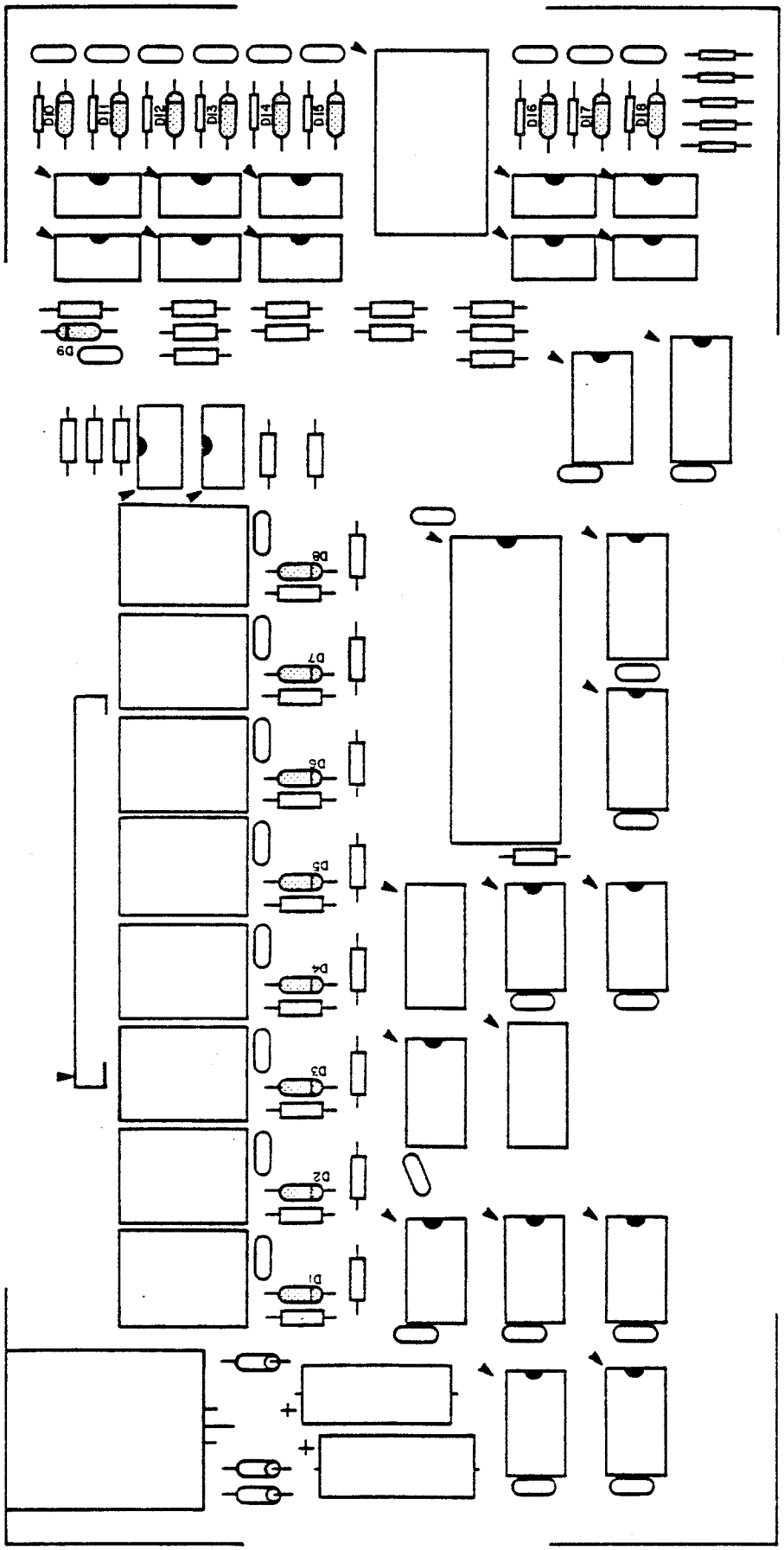


Figure 5-9. Diode Installation

5-13. Resistor Installation (Figure 5-10)

Install the following 41 resistors (Bag 4) according to the instructions in Paragraph 5-4. Save excess resistor leads for later use in ferrite bead and jumper installation.

> NOTE
>
> Although the board has provisions for 47 resistors, only 41 are supplied by MITS. Optional resistors may be installed in the 6 additional spaces provided according to the desired application. Refer to the User Information section for more information.

Resistor	Value
( ) R1, R3, R5, R7, R9, R11, R13, R15	33 ohm, 1/2W (orange, orange, black)
( ) R2, R4, R6, R8, R10, R12, R14, R16	220 ohm, 1/2W (red, red, brown)
( ) R17, R42	100 ohm, 1/2W (brown, black, brown)
( ) R18, R43	470 ohm, 1/2W (yellow, violet, brown)
( ) R21, R23, R24, R25, R26, R27, R28, R30, R31, R32	2.2K ohm, 1/2W (red, red, red)
( ) R22, R33, R34, R35, R36, R37, R38, R39, R40, R41	180 ohm, 1/2W (brown, gray, brown)
( ) R29	1K ohm, 1/2W (brown, black, red)

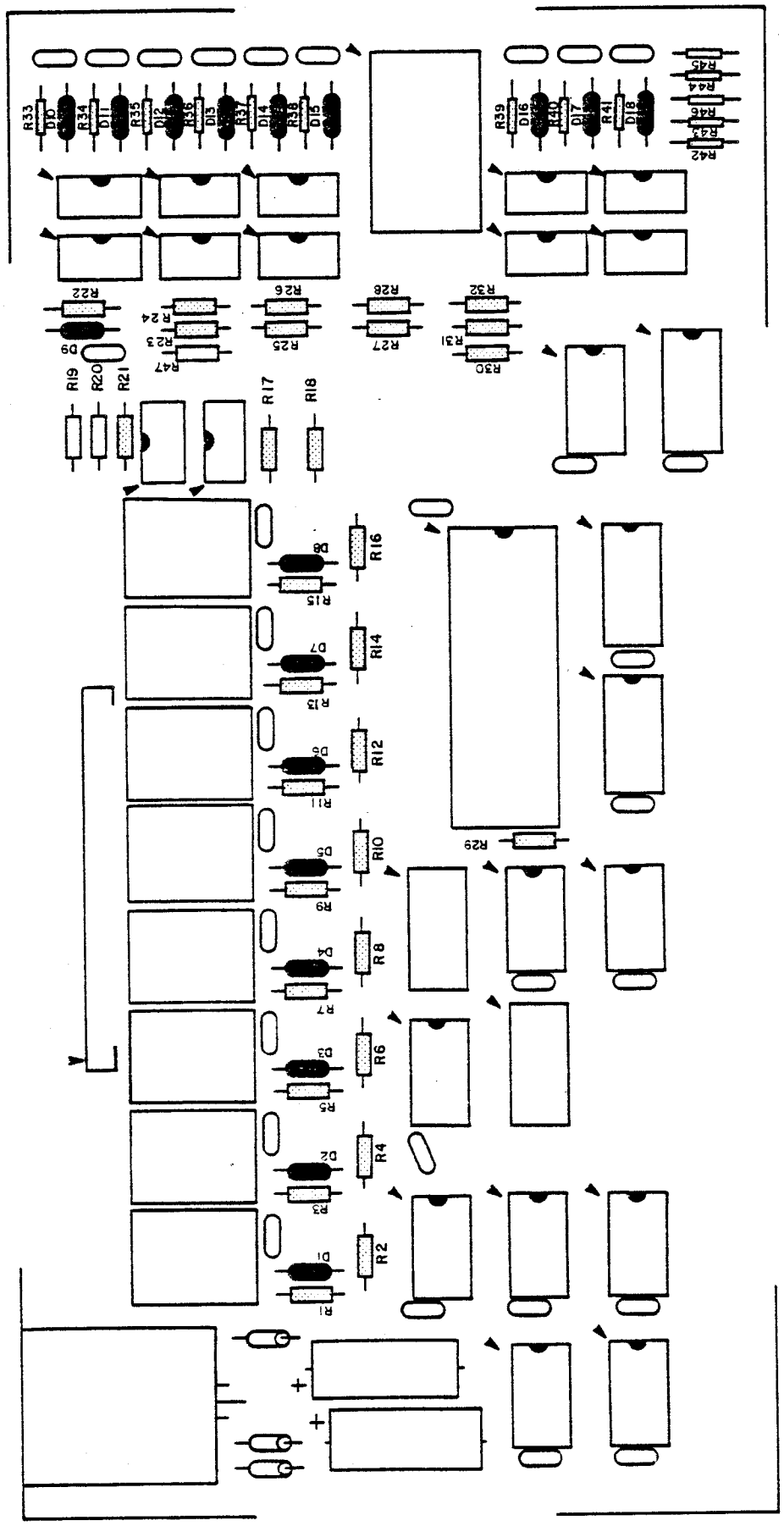


Figure 5-10. Resistor Installation

5-14. Transistor Installation (Figure 5-11)

Install ten transistors (Q1 through Q10, Bag 4) according to the instructions in Paragraph 5-7. Also refer to the transistor identification chart in Paragraph 5-8.

Transistor	Part Number
( ) Q1 through Q10	CS4410

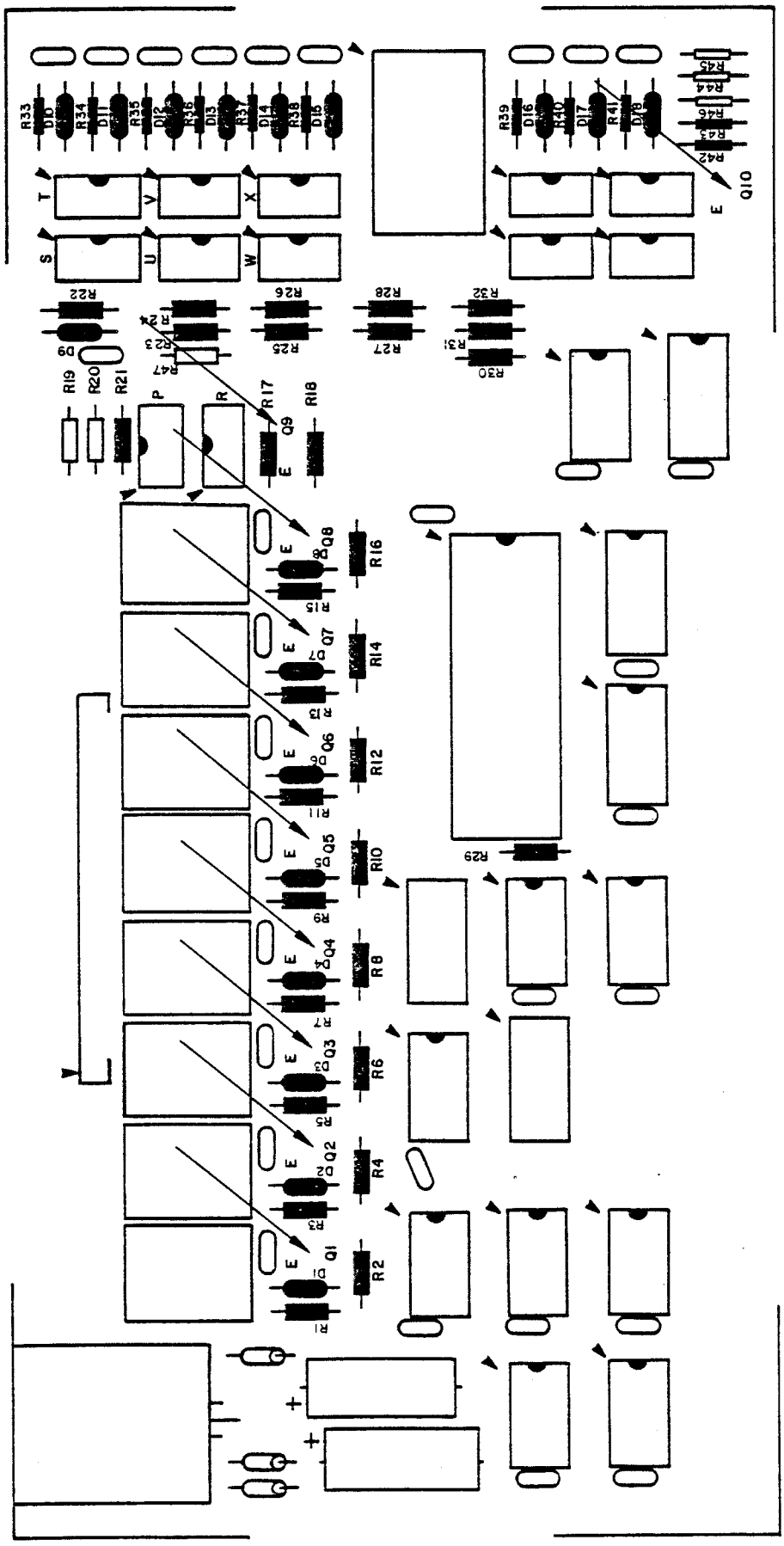


Figure 5-11. Transistor Installation

5-15. Capacitor Installation (Figure 5-12)

There are 23 capacitors (Bag 4) to be installed on the 88-PCI board. C1 and C2 are electrolytic capacitors and should be installed according to the instructions in Paragraph 5-5, Section A. Polarity orientation is very important for electrolytic capacitors; make sure C1 and C2 are correctly oriented before installation. The remaining 21 capacitors, used for noise suppression, are ceramic disk capacitors. They have no silkscreen designations, and are shown only as small oval shapes. Install these capacitors according to the instructions in Paragraph 5-5, Section B. Suppressor capacitors are non-polarized.

NOTE

Although the board has provisions for 31 suppressor capacitors, only 21 are supplied by MITS. Optional capacitors may be installed in the 10 additional spaces provided according to the desired application. Refer to the User Information section for more information.

Capacitor	Value
( ) C1, C2	33mf, 50v, electrolytic
( ) 21 suppressor capacitors	.1mf, 12v, ceramic disk

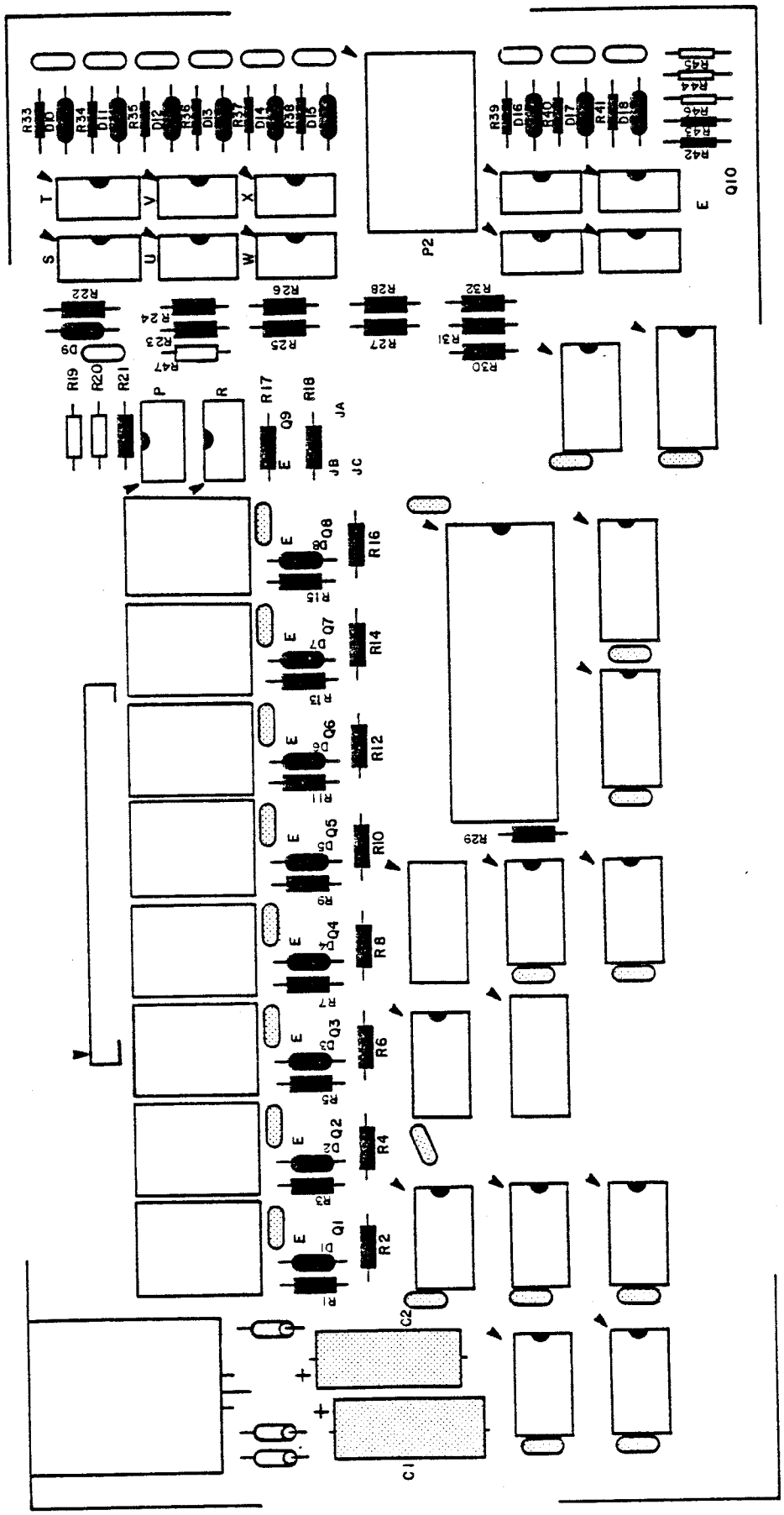


Figure 5-12. Capacitor Installation

5-16. Ferrite Bead Installation (Figure 5-13)

Install three ferrite beads (L1, L2 and L3, Bag 1) according to the following instructions.

1. Using resistor leads saved from Paragraph 5-13, cut three 1 inch lengths.
2. Insert the lead through the bead, and bend the lead ends to conform to their designated holes on the board.
3. Insert the lead into the silkscreened side of the board, and secure in place by bending the leads slightly outward.
4. Solder the leads to the foil pattern on the back of the board. Be sure not to leave any solder bridges.
5. Clip off any excess lead lengths.

( ) L1, L2, L3

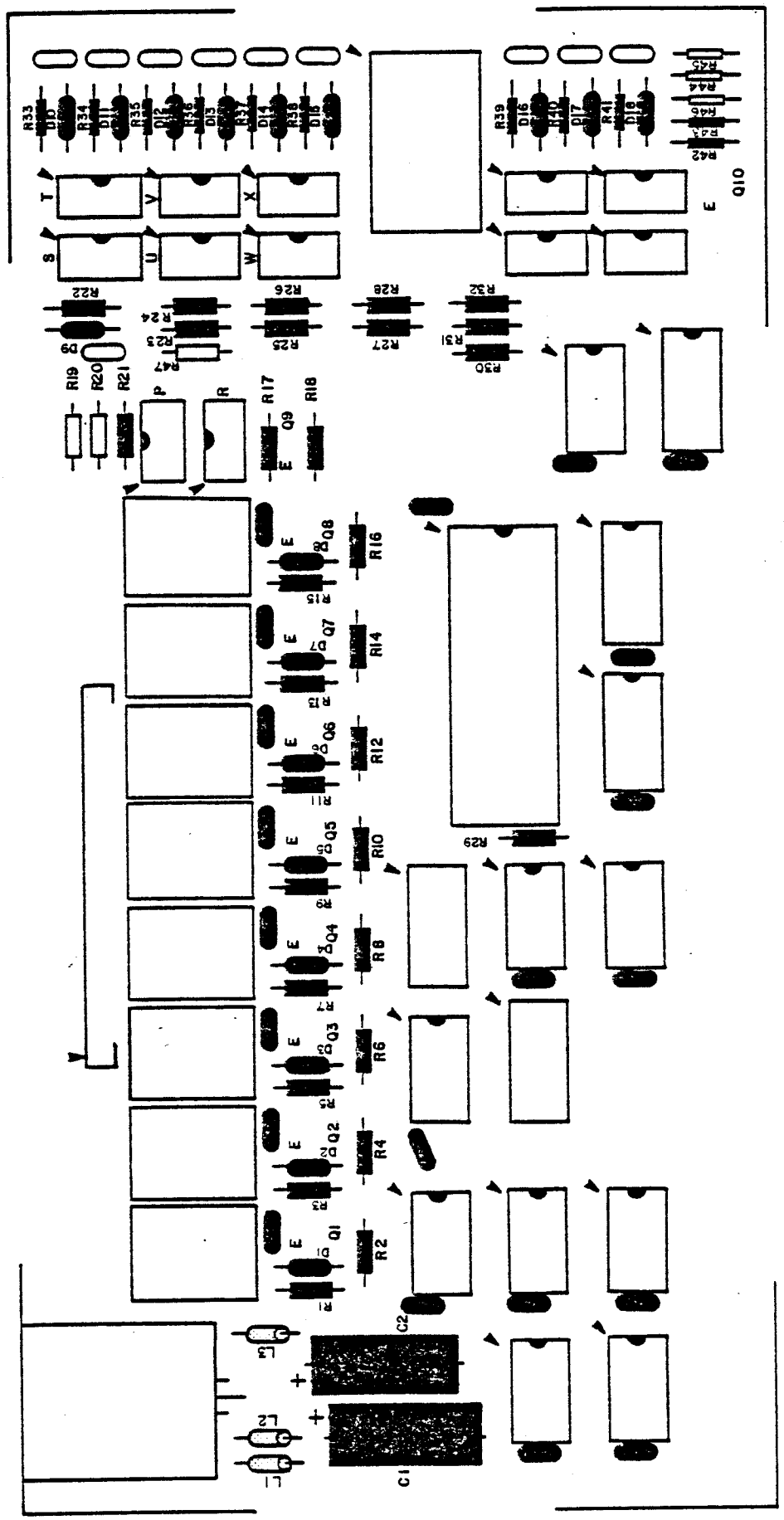


Figure 5-13. Ferrite Bead Installation

5-17. IC and IC Socket Installation (Figure 5-14)

There are 13 ICs (Bag 2) to be installed on the board. IC C is a static-sensitive MOS IC. Refer to the handling precautions in Paragraph 5-11, then install IC C (with the 40-pin socket) according to the instructions in Paragraph 5-9, Section B. Install the remaining ICs according to the instructions in Paragraph 5-9, Section A.

> NOTE
> Although sockets are not supplied for the 12 ICs listed below, the user may wish to purchase and install them with these ICs. Sockets help protect the ICs and will aid in troubleshooting.

Silkscreen Designation	Part Number	Socket Size
( ) C (with 40-pin socket)	6820	40-pin
( ) A, E, F, J, M	74L04	14-pin*
( ) B	74L30	14-pin*
( ) D	74LS00	14-pin*
( ) G	74LS73	14-pin*
( ) H	74L02	14-pin*
( ) K, L, N	74367	16-pin*
*Optional		

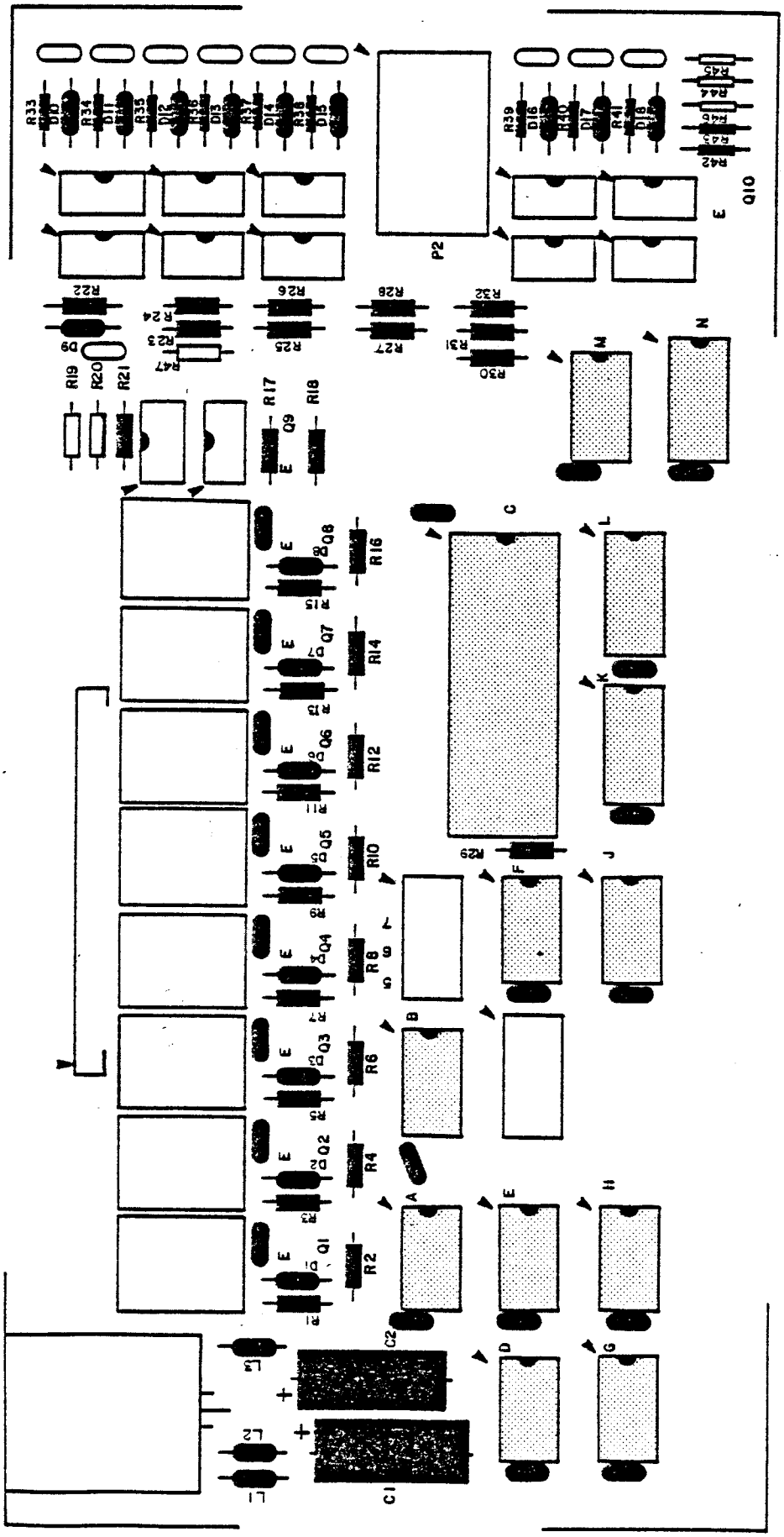


Figure 5-14. IC and IC Socket Installation

5-18. Switch Installation (Figures 5-15a and 5-15)

Install two 16-pin dip switches (S1 and S2, Bag 3) according to the following instructions.

1. Remove the switch from its holder, and straighten any bent pins with needle nose pliers.
2. Orient the switch so that the numbers "1,2,3,4" are towards the top of the board, as shown in Figure 5-15a.
3. Start the pins on one side of the switch into their respective holes on the silkscreened side of the board. Do not push the pins in all the way. If it is difficult to insert the pins into their holes, guide them with the tip of a small screwdriver.
4. Start the pins on the other side of the switch into their holes in the same manner. When all 16 pins have been started, push the switch into place by gently rocking it back and forth until it rests as close as possible to the board. Secure the switch in place with masking tape.
5. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges.
6. Clip off any excess lead lengths, and remove the masking tape.

Switch	Part Number
( ) S1, S2	CTS 206-124

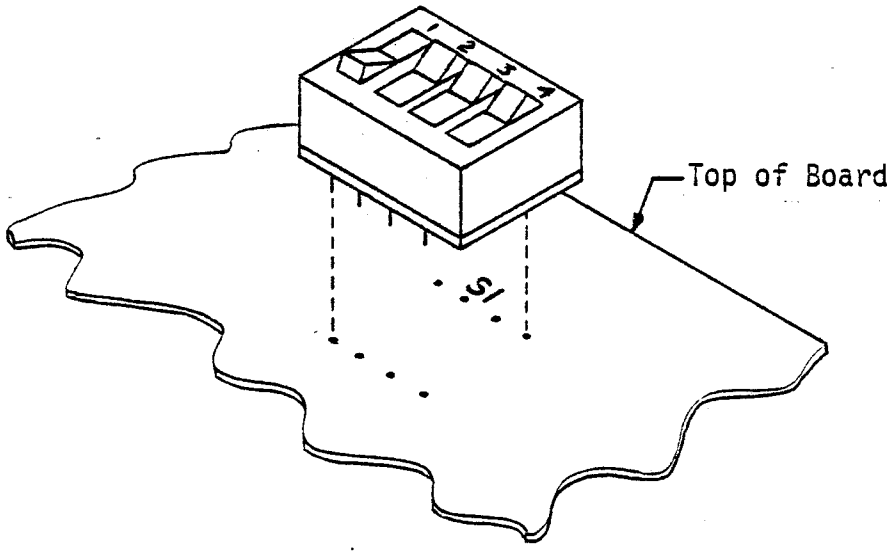


Figure 5-15a. Switch Orientation

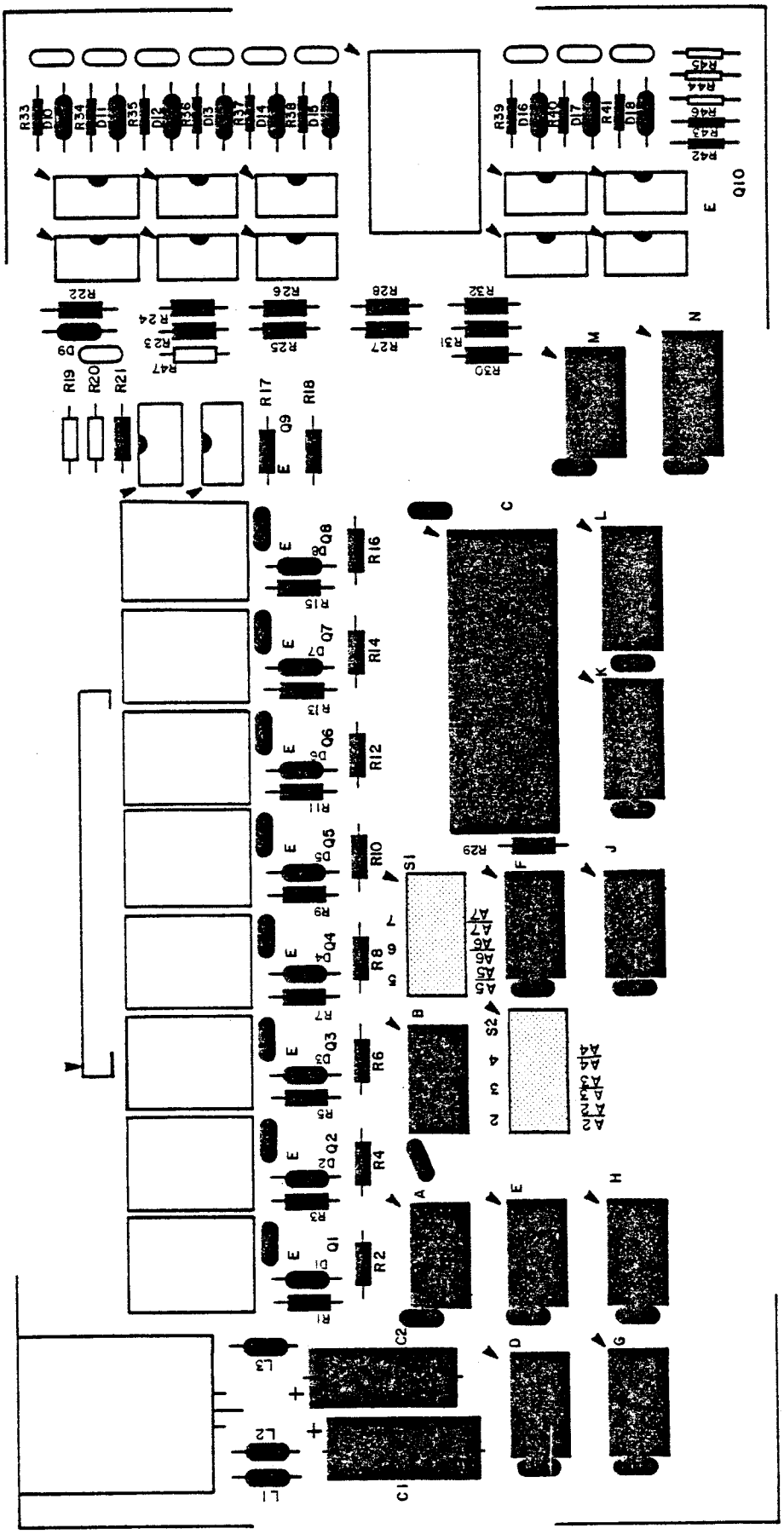


Figure 5-15. Switch Installation

5-19. Opto-Isolator Installation (Figure 5-16)

Install the following 12 opto-isolators with sockets (Bag 4) according to the instructions in Paragraph 5-9, Section B.

Opto-Isolator	Part Number	Socket Size
( ) P, R, S, T, U, V, W, X, Y, Z, AA, BB	1L74	14-pin

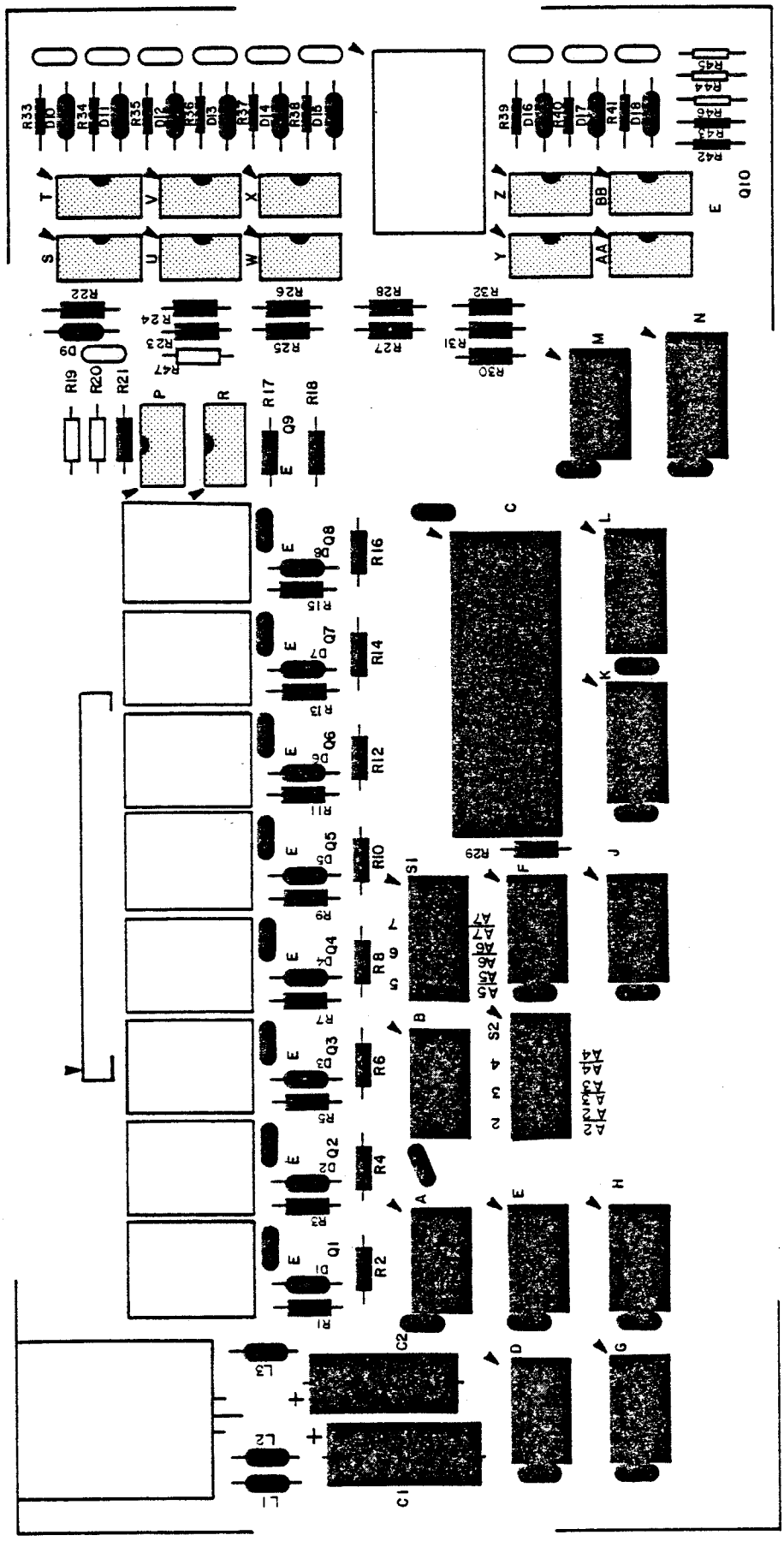


Figure 5-16. Opto-Isolator Installation

5-20. Relay Installation (Figure 5-17)

Install eight relays (K1 through K8, Bag 3) according to the following instructions.

1. Orient the relay over its designated holes on the board.
2. Insert the pins into their holes, and secure the relay in place with masking tape.
3. Solder each of the five pins to the foil pattern on the back of the board. Be careful not to leave any solder bridges.
4. Clip off any excess lead lengths.

Relay	Part Number
( ) K1 through K8	LZ9

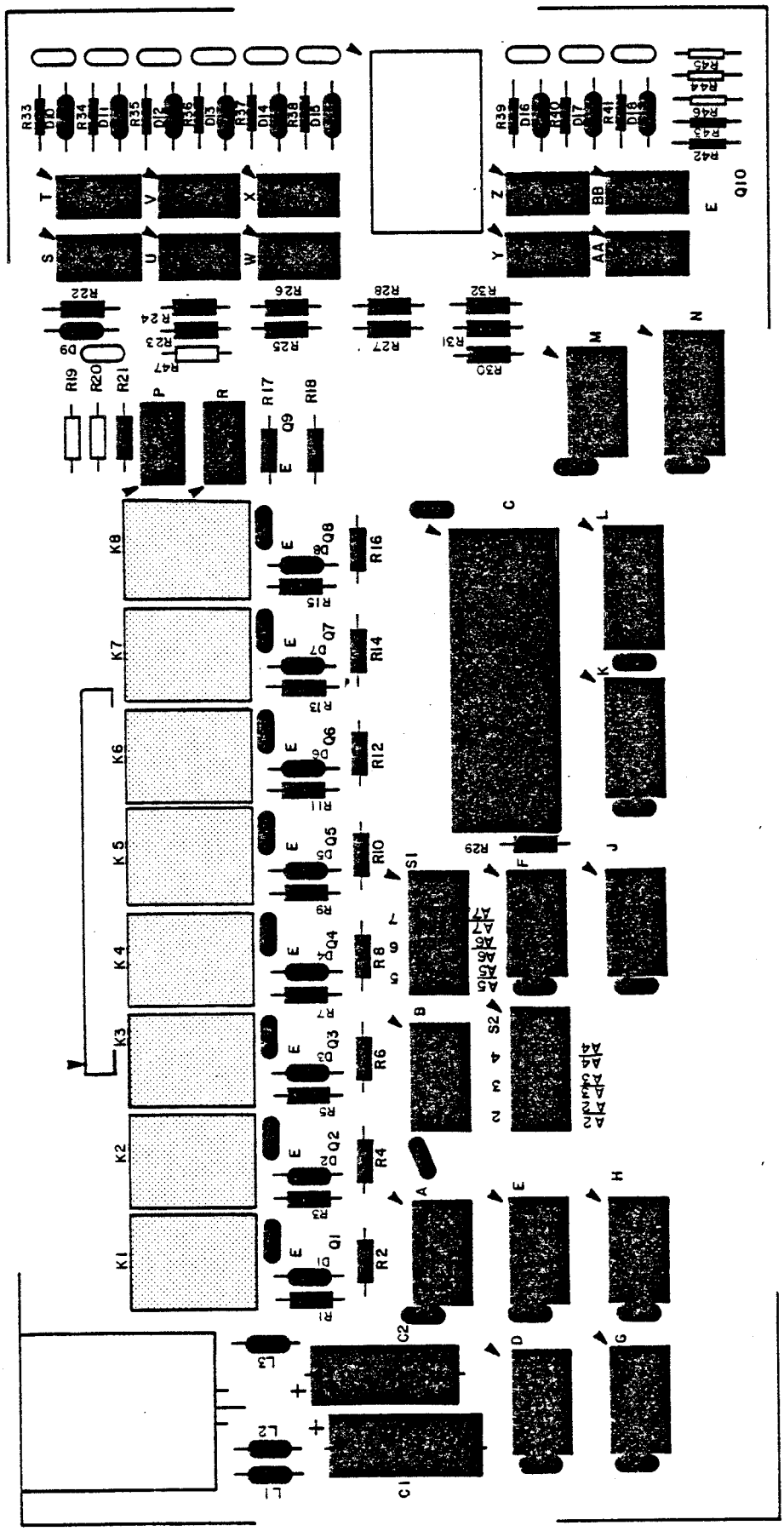


Figure 5-17. Relay Installation

5-21. Voltage Regulator Installation (Figures 5-18a and 5-18)

Install one voltage regulator, VR1, with heat sink (Bag 1) according to the following instructions.

1. Set the regulator in place on the silkscreened side of the board, aligning the leads with their designated holes.
2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

NOTE
Use heat sink grease when installing this component. Apply the grease to all metal surfaces that come into contact with each other.

3. Referring to Figures 5-18a and 5-18, set the regulator and heat sink in place on the silkscreened side of the board. Secure them in place with a #6-32 x 3/8 inch screw, a #6-32 nut and a #6 lockwasher.
4. Solder the leads to the foil pattern on the back of the board. Be sure not to leave any solder bridges.
5. Clip off any excess lead lengths.

Voltage Regulator	Part Number
( ) VR1	7805

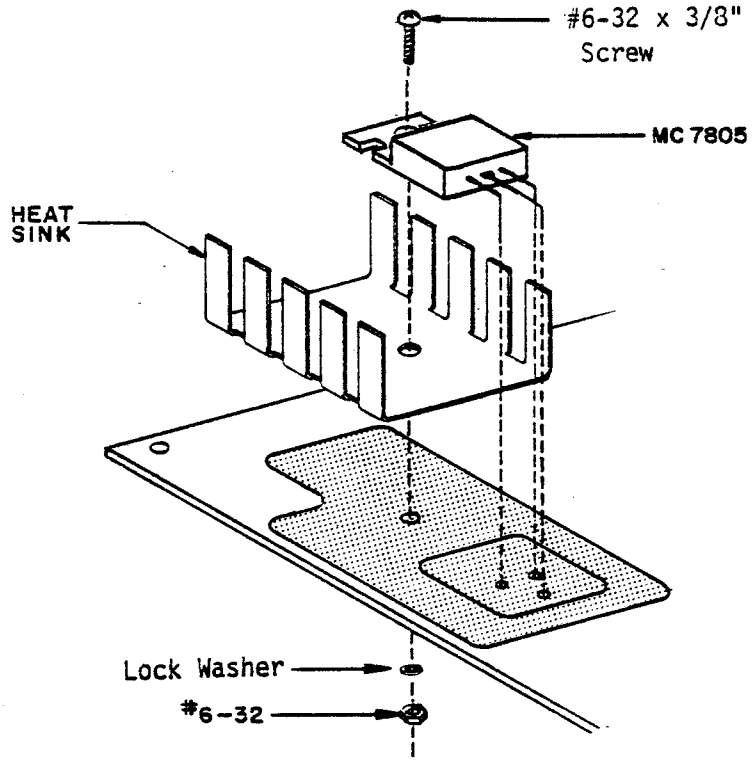


Figure 5-18a. Voltage Regulator Orientation

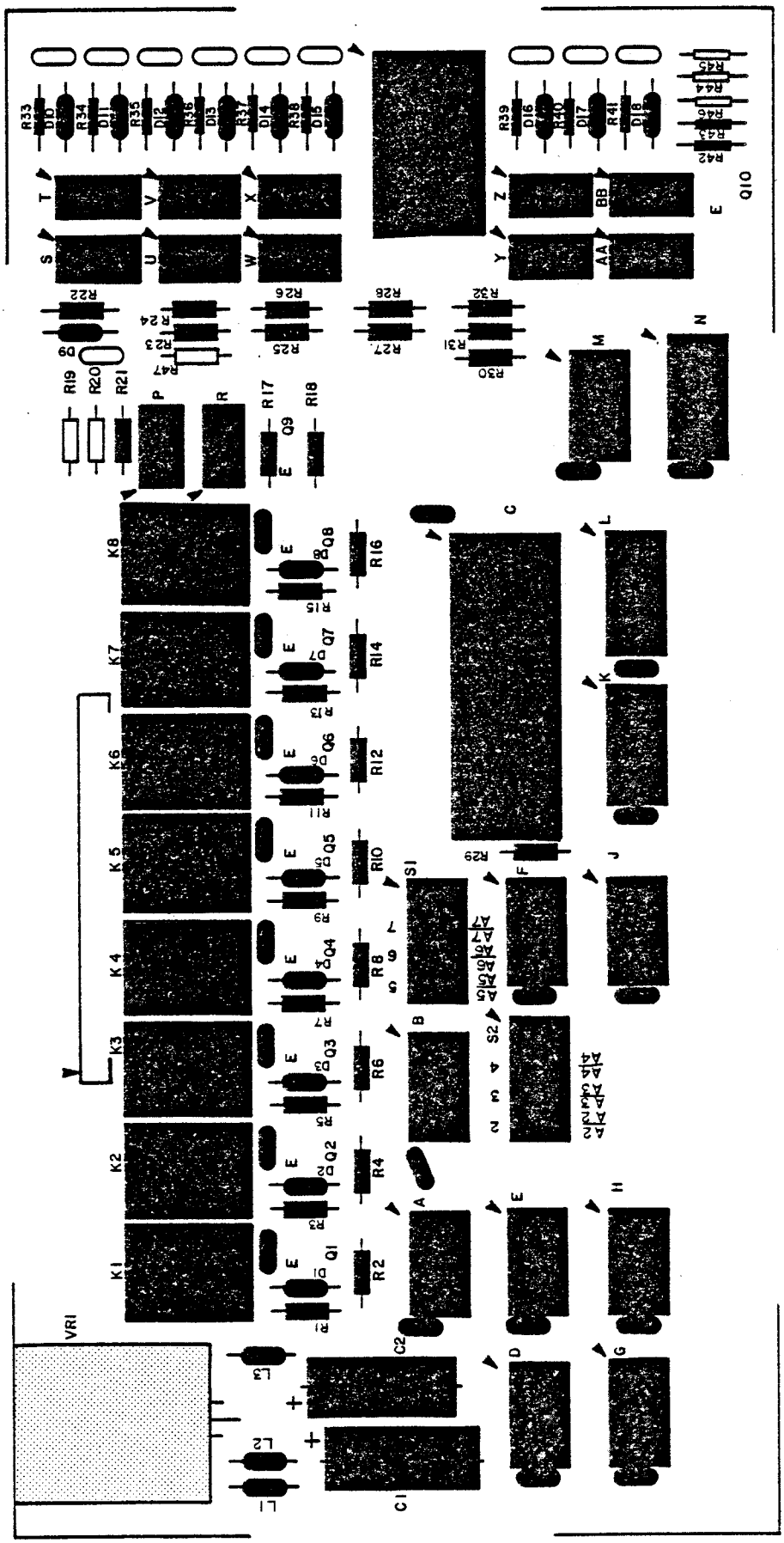


Figure 5-18. Voltage Regulator Installation

5-22. Male Connector Installation (Figures 5-19a and 5-19)

Install one 25-pin male connector (P1, Bag 3) according to the following instructions.

1. Orient the connector so that the bent pins are pointing towards the top of the board.
2. Insert the short pins into their designated holes on the silkscreened side of the board, and secure with masking tape.
3. Solder each pin to the foil pattern on the back of the board. Be sure not to leave any solder bridges. Clip off any excess lead lengths, and remove the masking tape.
4. Starting at the arrowhead on the board, count to pin 11. Pin 11 is not needed, and should be clipped off as close as possible to the body of the connector.

( ) P1

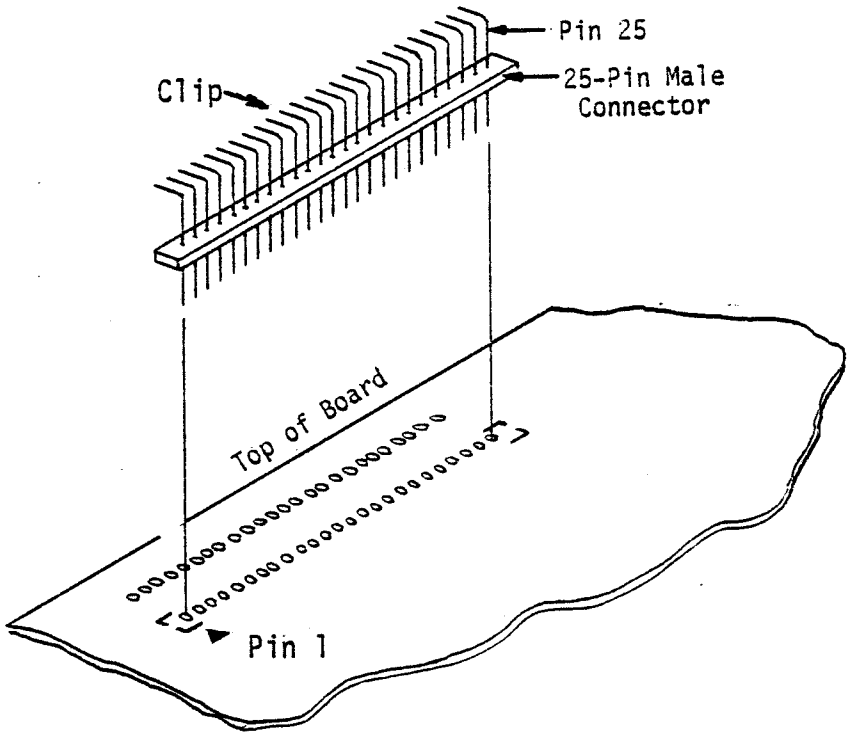
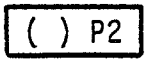


Figure 5-19a. Male Connector Orientation

5-23. 24-Pin Socket Installation (Figure 5-19)

Install one 24-pin socket (P2, Bag 3) according to the following instructions.

1. Orient the connector so that pin 1 is aligned with the arrowhead on the board, and insert the connector into its designated holes on the silkscreened side of the board. Secure in place with masking tape.
2. Solder each pin to the foil pattern on the back of the board. Be sure not to leave any solder bridges. Clip off any excess lead lengths, and remove the masking tape.



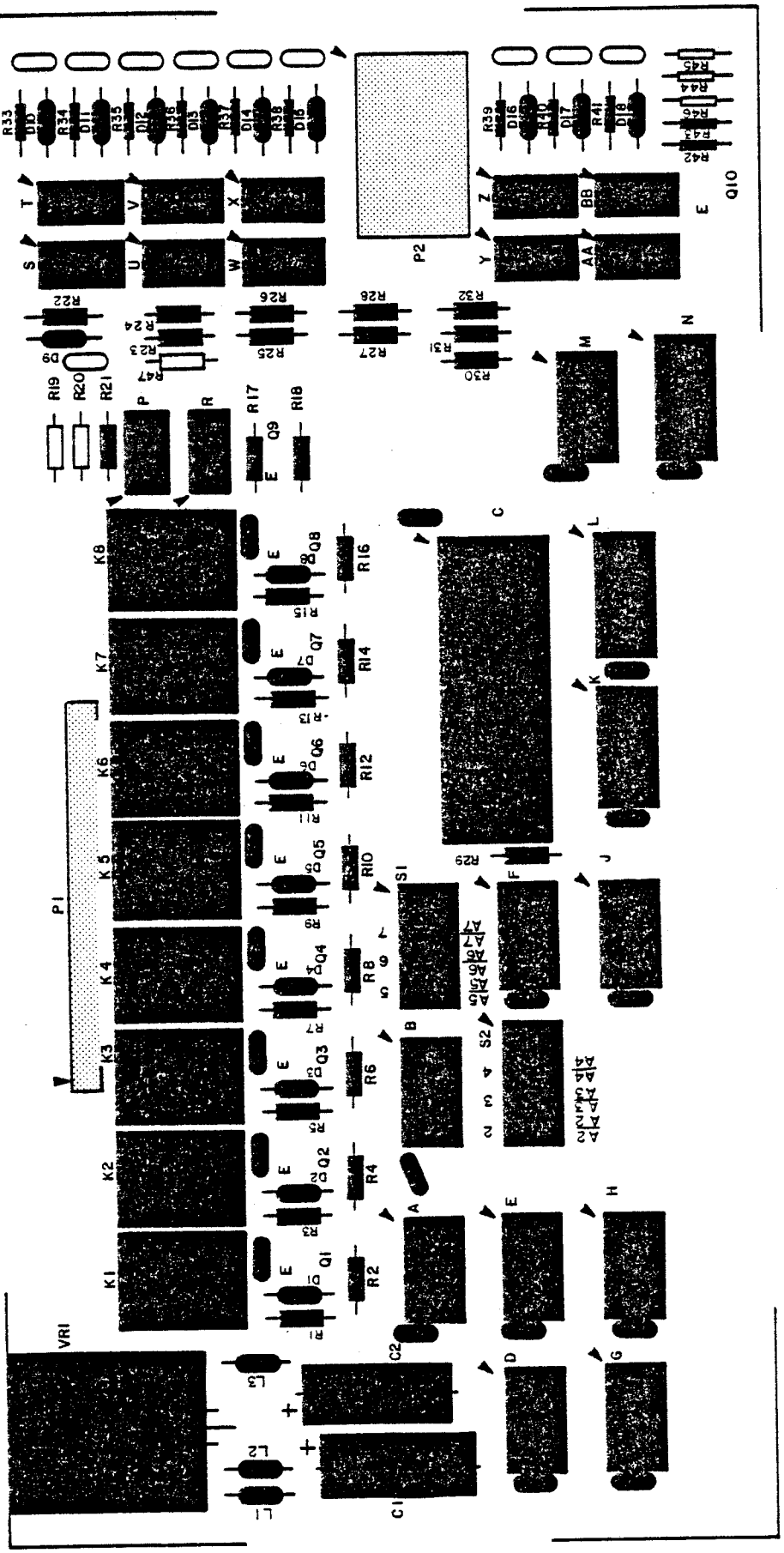


Figure 5-19. Male and Female Connector Installation

5-24. 18-Twisted Pair Cable Assembly

A. Cable Preparation (Figure 5-20)

1. Cut 1 1/2 inches of cable sheath from both ends of the cable. Do not cut into the insulation of the wires inside.
2. Cut 3 inches of cable sheath and inside wire from both ends of the following wires:

   white/black
   gray/black
   purple/black
   blue/black
   green/black
   yellow/black
   orange/black
   pink/black

   These wires will not be used.
3. Strip 1/4 inch of insulation from one end of each of the remaining 20 wires, and tin the exposed portion by applying a thin coat of solder.
4. Referring to Figure 5-20, crimp a terminal pin (Bag 3) onto the tinned ends of the 20 wires. Solder along the crimped edges, if necessary, to insure a good connection.

B. Installation of Cable Assembly Into 25-Pin Female Molex Connector (Figures 5-21 and 5-22)

1. Insert the plastic key (Bag 3) into socket #15 of the 25-pin female connector. (Pin 1 is marked with a large number "1.")
2. Referring to Table 5-B, insert each of the 20 wires into its designated socket. Make sure the terminal pin lock-tabs are facing up as shown in Figure 5-22, and push the wires in as far as possible (needle-nose pliers may be used).
3. Plug the 25-pin connector into P1, aligning the plastic key and the clipped off pin (#11).

C. Installation of Cable Assembly Into 25-DB Female Connector (Figure 5-23)

1. Strip 1/4 inch of insulation off the free ends of the 20 wires. (Terminal pins are not needed.)
2. Referring to Table 5-C, carefully solder each wire into its designated socket.

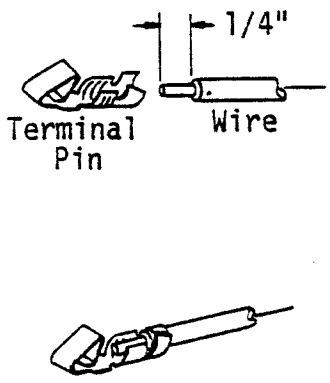


Figure 5-20. Terminal Pin Installation

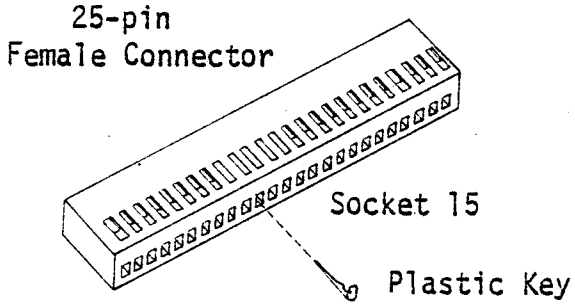


Figure 5-21. Insert Plastic Key Into Socket

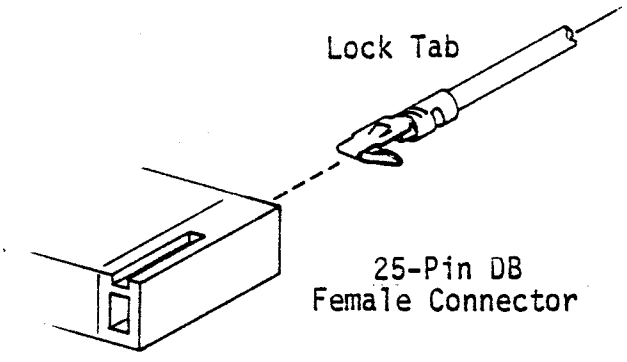


Figure 5-22. Insert Wires Into Socket

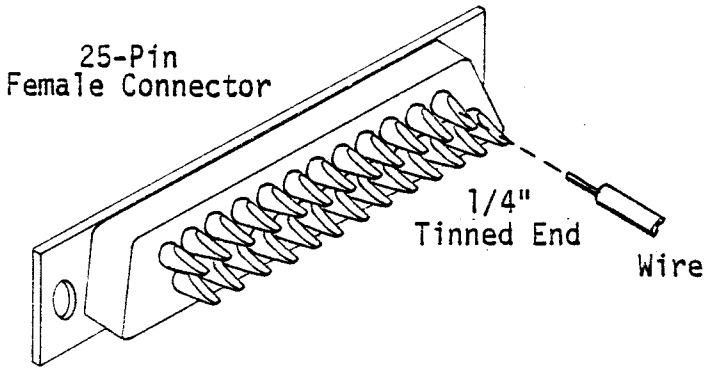


Figure 5-23. Solder Wires to 25-DB Female Connector

Table 5-B. Color Chart for Installation of 18-Twisted Pair Cable Into 25-Pin Female Connector (MOLEX)

Socket Number	Wire Color
1	Brown
2	Black
3	White
4	Black
5	Black
6	Gray
7	Black
8	Purple
9	Black
10	Blue
11	Black
12	Green
18	Black
19	Yellow
20	Black
21	Orange
22	Black
23	Pink
24	Black
25	Brown

Table 5-C. Color Chart for Installation of 18-Twisted Pair Cable Into 25-DB Female Connector (DB-25)

Socket Number	Wire Color
1	Brown
2	Black
3	Pink
4	Black
5	Orange
6	Black
7	Yellow
8	Black
14	Green
15	Black
16	Blue
17	Black
18	Purple
19	Black
20	Gray
21	Black
22	Black
23	White
24	Black
25	Brown

5-25. 24-Pin Flat Cable Assembly

Plug the male end of the cable assembly into P2 so that pin 1 of the cable assembly and pin 1 of connector P2 are aligned.

5-26. Optional Jumper Installation

Refer to Section III for information on jumper options. Use excess resistor leads saved from Paragraph 5-13 to make the jumper connections.

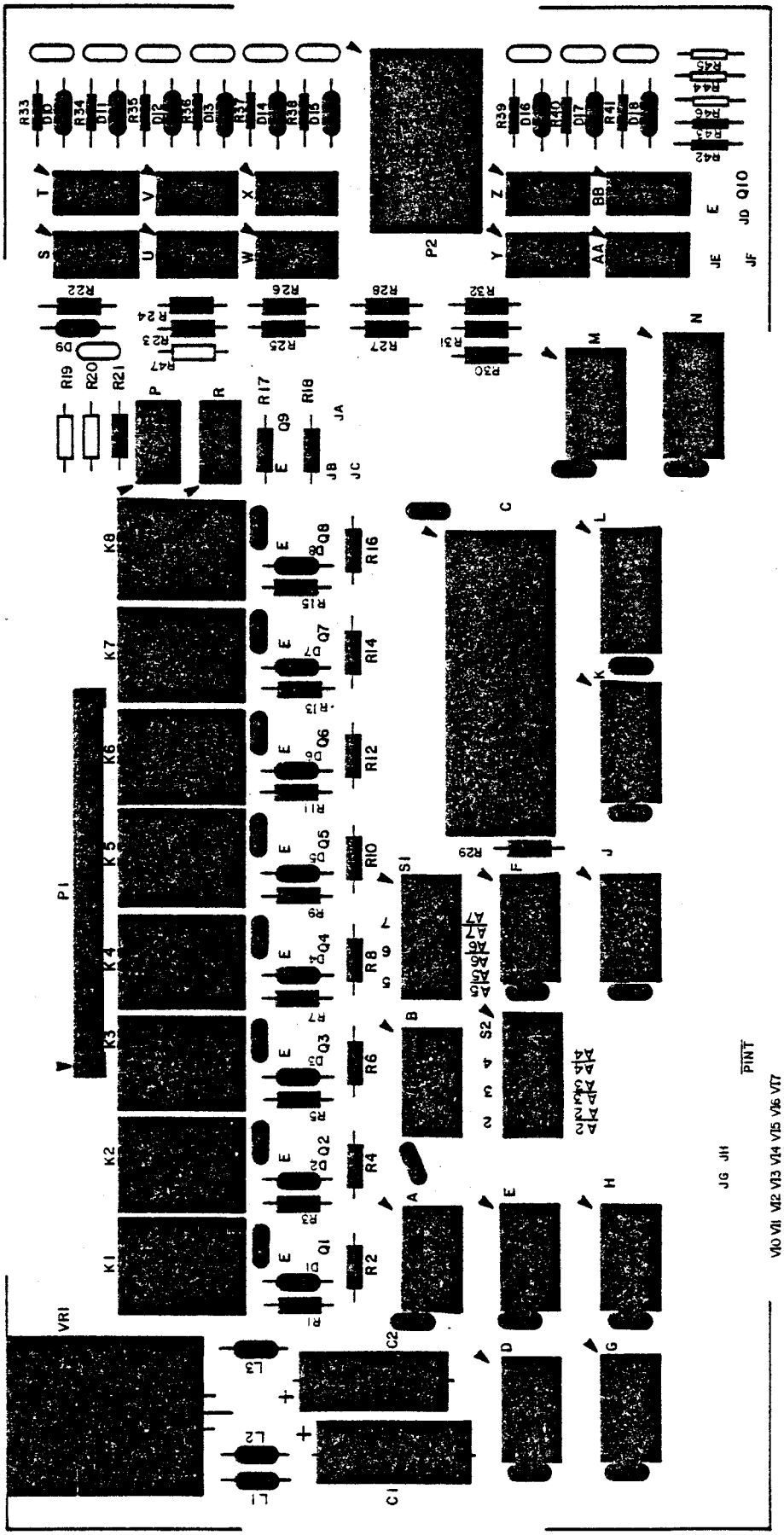


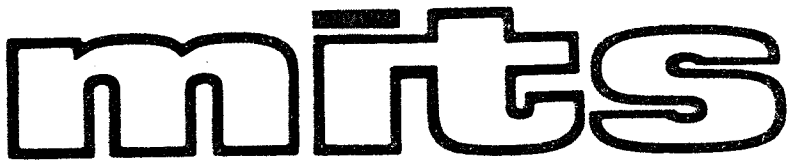
Figure 5-24. Completed Board Assembly

5-27. Installation of Board Into Mainframe

1. Before installing the 88-PCI board, check the board for solder shorts, open lands and missing components.
2. Remove the four #6-32 x 3/8 inch screws (two on each side) from the computer case, and slide the case bottom forward so that the bottom of the motherboard is exposed.
3. Insert the 100-pin edge connector into the motherboard so that pin 1 is in the lower right position (looking at the front of the computer).
4. Solder each pin to the bottom of the motherboard. Be careful not to leave any solder bridges. Clip off any excess lead lengths.
5. Slide the board down through the card guides, and insert the card stab connector into the edge connector so that the silk-screened side is towards the right side of the computer.
6. Slide the case bottom back into place and replace the four #6-32 x 3/8 inch screws.
7. Attach the 18-twisted pair 25-DB connector and the ribbon cable 25-DB connector onto the inside of the back panel by inserting #4-40 x 3/8 inch screws from the outside of the panel.

5-28. Burn-In Procedure

When assembly of the 88-PCI board has been completed, we recommend that a "burn-in" procedure be performed to uncover possible malfunctions that may occur at this time. After the board has been installed, turn the unit on, and set the cover in place. Leave the computer on for a period of 48 to 100 hours. If problems are encountered, refer to the Troubleshooting section of the 88-PCI manual.



2450 Alamo SE
Albuquerque, NM 87106

PCI CABLE P1

P1 = RELAY "OUTPUTS" AND 2 OPTO HANDSHAKES

P1	COLOR	DB-25	FUNCTION
NO 1	ORG	12	K2 / PB6
COMM 2		25	
NO 3	RED	11	K3 / PB5
C 4		24	
5	BRN	10	K1 / PB7
C 6		23	
7	WH	9	K4 / PB4
C 8		22	
9	GRAY	8	N/C OR SPARE
10		21	
11 KEY	KEY		
12		20	N/C OR SPARE
13	VIO	7	
14		19	K5 / PB3
C 15	BLU	6	
16		18	K6 / PB2
C 17	GRN	5	
18		17	K7 / PB1
C 19	YEL	4	
20		16	K8 / PBØ
C 21	ORG	3	
22		15	-5
23	RED	2+	INPUT +5 TO OPTO — CB1 / 1C P
24		14	EMITTER
25	BRN	1	OPTO OUTPUT — CB2 / 1C R
			COLLECTOR

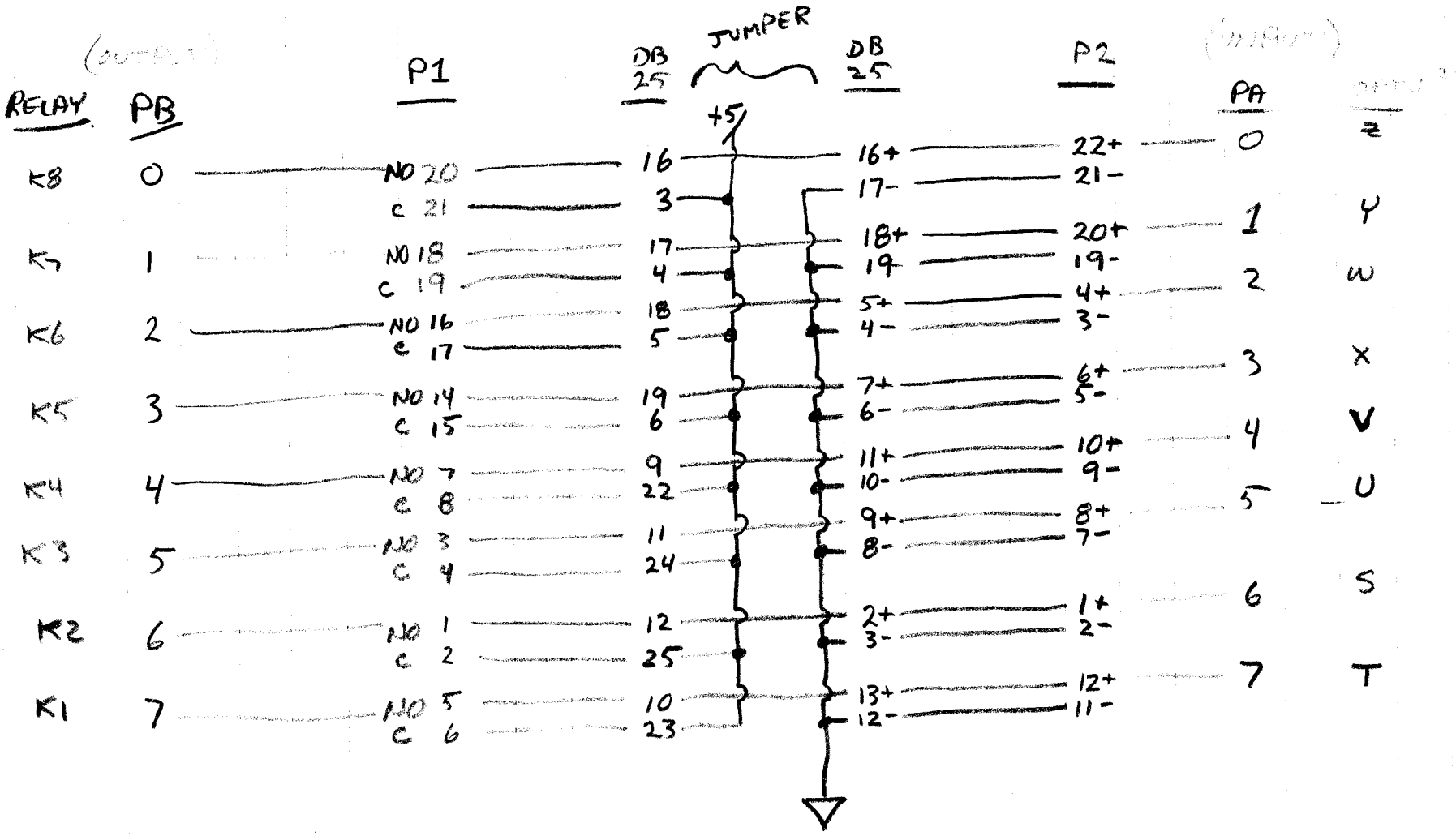
(NO COLOR = BLACK)

DB 25 PIN 13 NOT USED

PCI CABLE P2

(OPTO INPUTS)

P2		DB-25	FUNCTION
1	+	2 +	PA6 / IC S
2	-	3 -	
3	-	4 -	PA2 / IC W
4	+	5 +	
5	-	6 -	PA3 / IC X
6	+	7 +	
7	-	8 -	PA5 / IC U
8	+	9 +	
9	-	10 -	PA4 / IC V
10	+	11 +	
11	-	12 -	PA7 / IC T
12	+	13 +	
13	NC	25	SPARE LINES
14	NC	24	
15	NC	23	
16	NC	22	
17	-	21 -	CA1 / IC BB
18	+	20 +	
19	-	19 -	PA1 / IC Y
20	+	18 +	
21	-	~~17~~ -	PAØ / IC Z
22	+	~~16~~ +	
23	EMIT.	15	CA2 / IC AA
24	COLL.	14	



TEST JUMPER SETUP FOR PCI

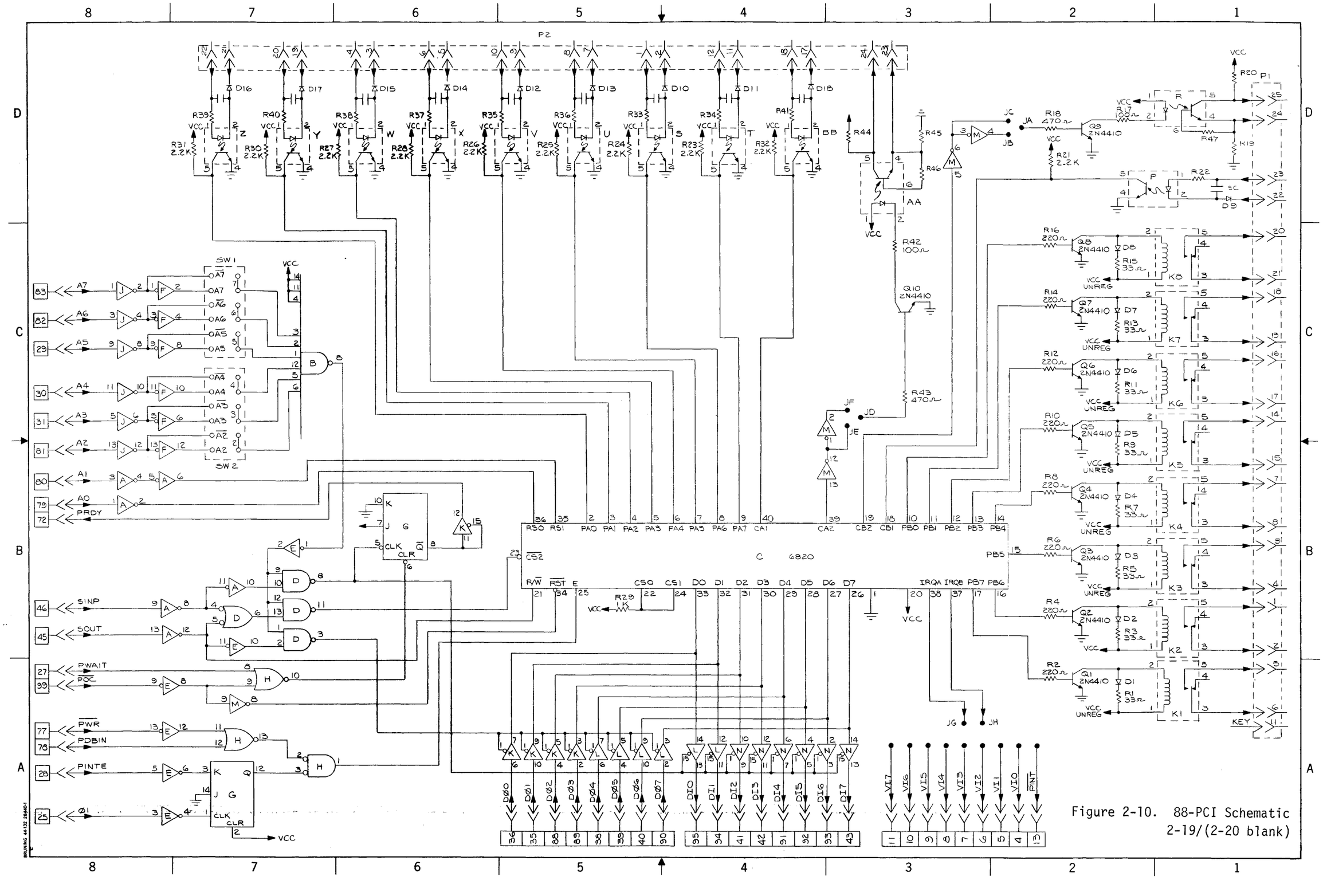


Figure 2-10. 88-PCI Schematic