

The Ithaca InterSystems  
EPROM EMULATOR

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Edition 1.0

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## 1.0 INTRODUCTION

Non-volatile, programmable memory is an important component of many microcomputer systems. The Ithaca InterSystems EPROM Emulator provides a way to develop and test programs to be burnt into EPROMs without requiring the time, cost, and effort of reburning each iteration of the program. The Emulator supports this facility conveniently and at reasonable cost.

Without an EPROM Emulator, proposed EPROM software must be burned into an appropriate EPROM, the EPROM inserted in a system board, and the EPROM software tested. If there is an error in the software, the EPROM must be erased, reburned, and retested.

Using the EPROM Emulator, software is written into the Emulator RAM, then routed to the EPROM location (via one or two connector cables) for testing. Any software errors can be easily corrected. When the software is completely debugged, it can be burned into ROM.

Like all Ithaca InterSystems products, the EPROM Emulator board is completely tested before shipment, and should provide years of trouble-free service. It is important, however, that the board be inspected upon receipt; and in any event, service may some day be required. The InterSystems Policies manual contains information about these subjects.

This manual provides the information required to install and use the InterSystems EPROM Emulator. A description of the board, setup instructions for the board, a description of typical operating procedures, and the board parts list are included.

### 1.1 PHYSICAL DESCRIPTION

The InterSystems EPROM Emulator board is a standard 5 by 10 inch (12.7 by 25.4 cm), S-100 bus, plug-in circuit board. The Emulator board contains two banks of RAMs. Each bank emulates one EPROM. The card provides two headers and two 18-inch, 24-conductor ribbon cables for interconnecting the board to the target EPROM sockets.

## 1.2 FEATURES

Features of the EPROM Emulator board include:

- \* The following EPROM types can be emulated:  
2508, 2708, 2516, 2716, TI2716, 2532, 2732, 2758,  
and 4716.
- \* Either one or two EPROMs can be emulated at a time.
- \* Two different type EPROMs can be emulated at the same time.
- \* Operation at up to 6 MHz is possible.
- \* Emulator reads assert PHANTOM\* allowing the board to overlap system memory.
- \* Write and read operations can be controlled either by software or at the front panel.
- \* The Board Enable/Disable switch can disable board functions on the S-100 bus.
- \* 24-bit extended addressing is jumper selectable.
- \* Two EPROM 16-bit emulation is possible under software control.
- \* Optional wait state generation may be selected.

## 1.3 BANK ORGANIZATION

The Emulator board has two banks of RAMs, each of which can emulate one EPROM. Each bank consists of eight 4Kx1 static RAMs. Bank 1 occupies the lower 4 kbyte space of the Emulator's 8 kbyte address space. Bank 2 occupies the upper 4 kbyte space. Each bank can be independently configured to emulate one of a variety of EPROM types as described in section 2.0 of this manual. The two-bank organization of the board allows the board to be used to emulate an EPROM pair in a 16-bit system.

## 1.4 OPTIONS

### 6-Foot Cables

To allow the board to emulate EPROMs located on equipment that is external to the system in which the EPROM Emulator board is mounted, special 6 foot cables are available. The cables feature a buffer board that reduces noise interference. The buffer board contains two jumpers that are configured to adapt the cable for various EPROMs.

### 1.5 PHANTOM\*

The EPROM Emulator is configured to assert the PHANTOM\* signal (S-100, 67) during a memory read if the board is addressed and enabled by SW1. When PHANTOM\* is asserted and the Emulator board overlaps the memory space of a memory board that can decode PHANTOM, only the Emulator board is read.

PHANTOM\* is not asserted by the Emulator board during a memory write sequence. If the Emulator overlaps the memory space of a system memory board, both the Emulator memory and system memory are written to.

If the Emulator board is to be used in a system in which the memory boards do not decode the Phantom line, it may not be desirable to have the Emulator address space overlap system memory.

## 2.0 BOARD SETUP

This section of the manual provides the information required to prepare the EPROM Emulator board for operation in an S-100 bus system. Descriptions of memory addressing selection, jumper options, and switch settings are provided. Refer to Figure 1 for the location of all components set during board setup.

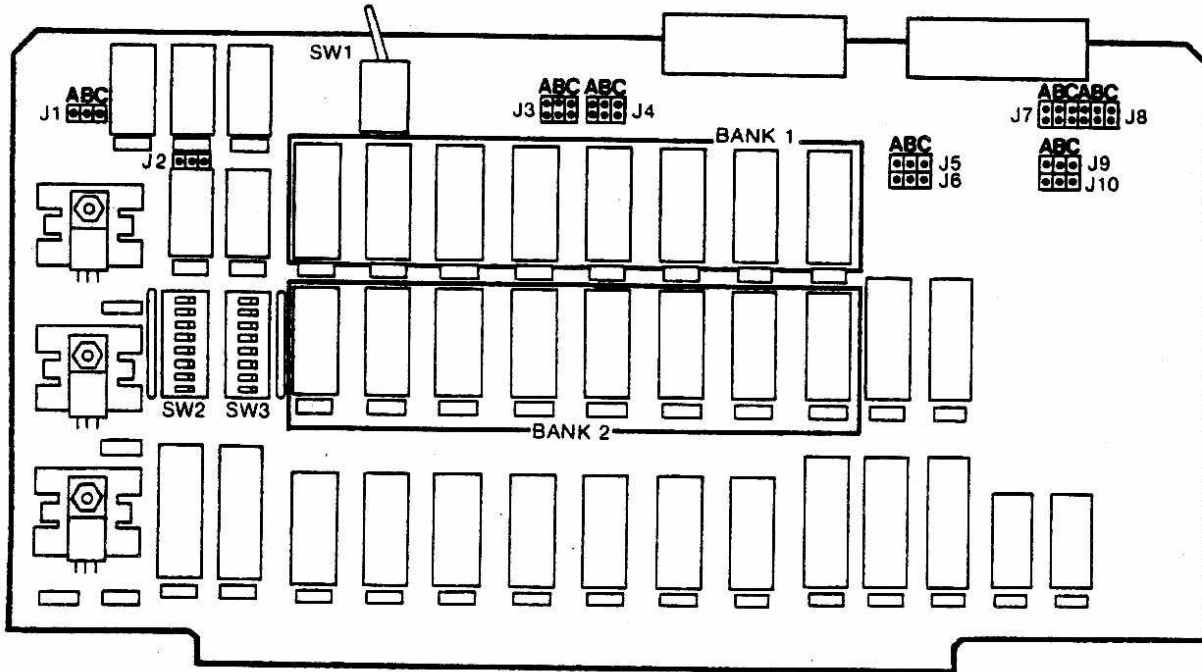


Figure 1 EPROM Emulator board

## 2.1 JUMPER SUMMARY

Jumpers are used to configure the board to function in different S-100 bus systems, and to emulate various EPROM types. There are ten jumper areas on the EPROM Emulator board. Figure 1 shows the location of the jumpers. Each jumper area box contains a group of plated-through holes spaced 0.1" apart. To configure a jumper area, one connection per box is made between adjacent plated-through holes by a shunt that slides onto square posts that are soldered in the holes. Possible connections within jumper areas are designated by letter names. The letters run A, B, C, ... from left to right, or from top to bottom.

Two type of jumper connections are used on the Emulator board. Jumpers J1, J2, J5, J6, J9 and J10 have three adjacent posts labeled A, B, and C. A shunt is used to connect either posts A and B, or B and C. Jumpers J3, J4, J7 and J8 have three adjacent pairs of posts, labeled A, B, and C. These jumpers are configured by installing a shunt (vertically) across the appropriate pair of posts.

J1 J1 is used to configure the board for 16-bit or 24-bit addressing.

A-B 16-bit addressing is enabled.

B-C 24-bit Extended addressing is enabled.

J2 J2 is set to select whether a wait state is generated. Generation of a wait state is required in 6 MHz systems.

A-B One wait state is generated.

B-C No wait state is generated.

J3- Jumpers J3 through J10 configure the board to  
J10 emulate specific EPROMs. Refer to section 2.5. The board can emulate two different EPROM types simultaneously. J3 through J6 are set to configure the board to emulate EPROM 1, and jumpers J7 through J10 are set to configure the board to emulate EPROM 2.



## 2.5 BANK CONFIGURATION, EPROM TYPE: J3-J10

Bank 1 and Bank 2 are independently configured to emulate specific EPROM-types. Jumpers J3 through J6 are set for Bank 1. Jumpers J7 through J10 are set for Bank 2. See Figure 4.

EPROM TYPE	J3(7)	J4(8)	J5(9)	J6(10)
2508	C	A	BC	AB
2708	C	A	BC	AB
2516	A	A	BC	AB
2716	A	A	AB	AB
T.1.2716	B	A	AB	BC
2532	A	C	BC	BC
2732	A	B	AB	AB
2758	C	A	BC	AB
4716	A	A	AB	AB

**Notes:**  
 J3-6 configure EPROM 1 (CONNECTOR 1, BANK 1).  
 J7-10 configure EPROM 2 (CONNECTOR 2, BANK 2).

Figure 4 Bank configuration for EPROM type

## 2.6 CABLE INSTALLATION

Figure 5 illustrates the correct method for installing cables between Emulator board connectors Conn 1 and Conn 2 and target EPROM sockets. Note that the target connector must be installed with Pin 1 correctly oriented. Refer to the documentation for the hardware on which the target EPROM is located to determine the location of pin 1 of the target EPROM socket.

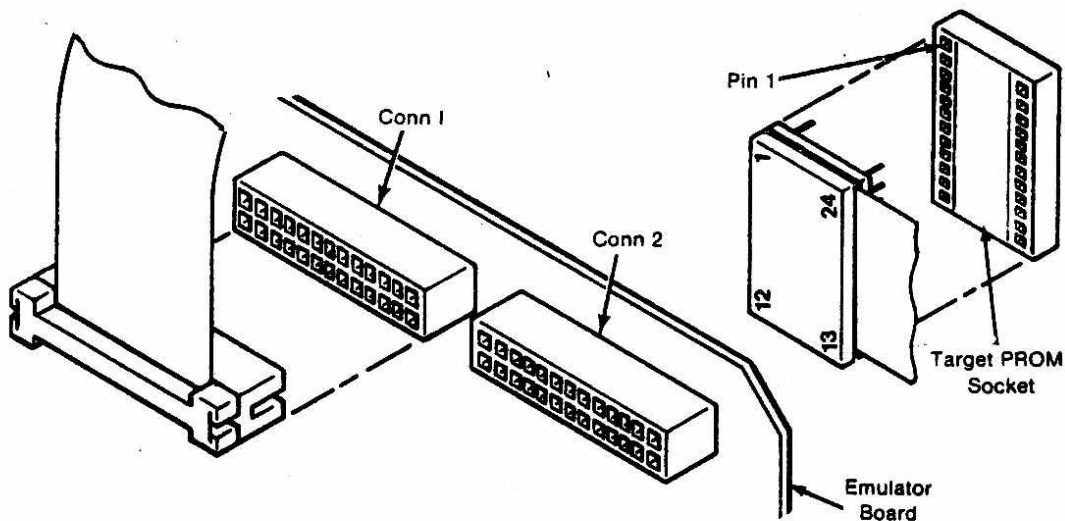


Figure 5 Cable installation

### 2.3 BOARD ADDRESSING: SW2 and SW3, J1

DIP switches SW2 and SW3 are set to select the board address space starting address. See Figure 3. The Emulator board is set to occupy any 8 kbyte memory space on any 8 kbyte boundary within the S-100 bus 16 Mbyte address range; i.e., starting boundaries 0000H to E000H for 16-bit addressing or 00 0000H to FF E000H for 24-bit addressing systems.

Switches SW3-3 through SW3-1 represent address bits A13 through A15 respectively, for both 16-bit and 24-bit addressing schemes. Switches SW2-8 through SW2-1 represent address bits A16 through A23 respectively, when the board is configured for 24-bit addressing. A switch set to OPEN corresponds to a logic ONE; a switch set to CLOSED corresponds to a logic ZERO.

J1 is configured A-B for 16-bit addressing; J1 is configured B-C for 24-bit addressing.

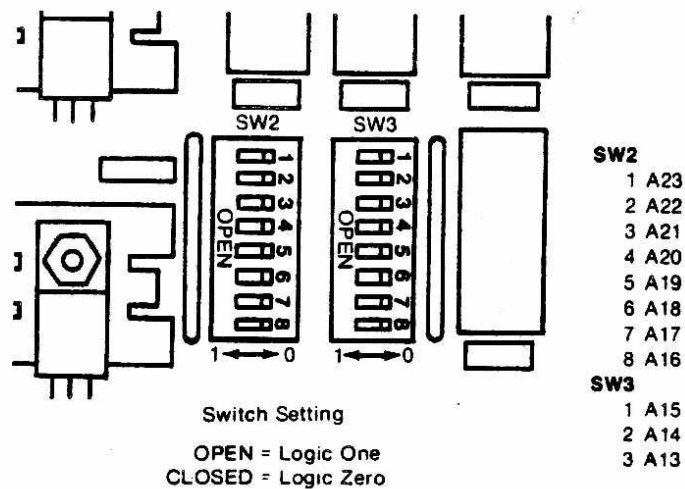


Figure 3 SW2 and SW3

### 2.4 WAIT STATE: J2

When used in 6 MHz systems, the Emulator board should be configured to generate one wait state when accessed. Set jumper J2 to A-B if one wait state is required. Set J2 to B-C if no wait states are required.

## 2.7 OPTIONAL 6-FOOT CABLE

The optionally available 6-foot cables must be configured for the desired EPROM type prior to installation. Figure 6 illustrates the disassembly of the cable buffer board and location of jumpers. Figure 7 details the correct jumper configuration for each EPROM type.

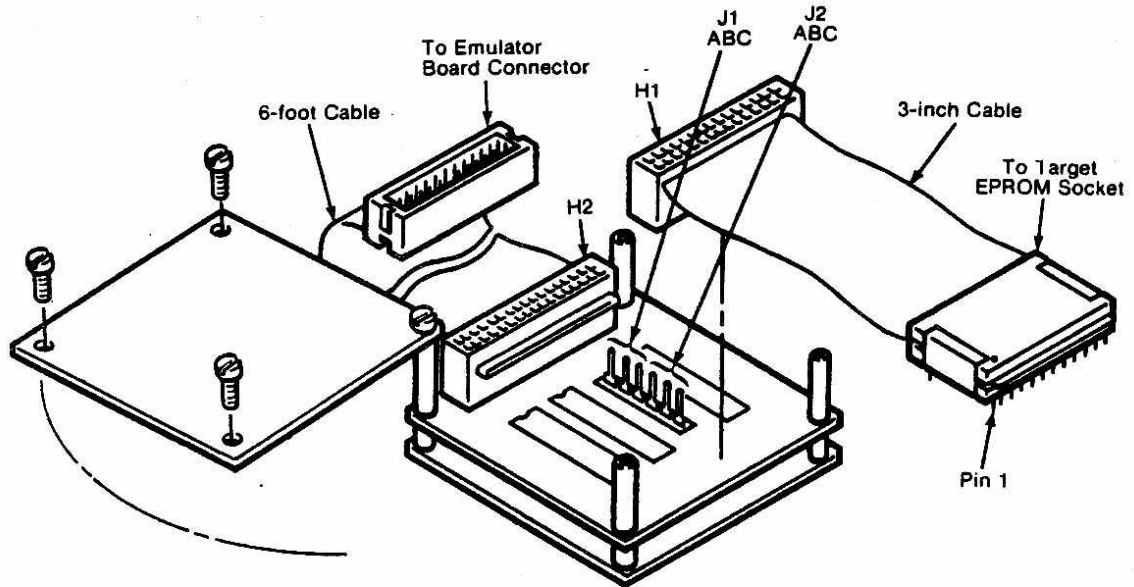


Figure 6 6-foot cable buffer board

EPROM Type	Jumper	
	J1	J2
2508	BC	AB
2708	BC	AB
2516	BC	AB
2716	AB	AB
T.I.2716	AB	BC
2532	BC	BC
2732	AB	AB
2758	BC	AB
4716	AB	AB

Figure 7 Buffer board jumpers

### 3.0 BOARD OPERATION

This section of the manual provides guidelines for the use of the EPROM Emulator board. The instructions are provided as an example of how the board can be used.

#### 3.1 WRITING TO THE EMULATOR

The Emulator board contains two banks of eight 4Kx1 static RAMs. (Each bank emulates one EPROM.) Each bank is organized as 4 kbytes. Bank 1 occupies the lower 4 kbyte space of the Emulator's 8 kbyte address space. Bank 2 occupies the upper 4 kbyte space.

S-100 address line A12 selects which bank is enable for system reads or writes. When A12 is a logic ZERO, Bank 1 is enabled. When A12 is a logic ONE, Bank 2 is enabled.

If the Emulator board overlaps a system memory board both the Emulator memory, and system memory are written to during a memory write sequence.

#### Front Panel Write to Emulator

Refer to the front panel manual for the system. When using the InterSystems Front Panel the procedure will be similar to that which follows.

- 1) Configure the Emulator board as required. See Section 2.0.
- 2) Set Front Panel switches S15 through S0 to the desired starting address for the Emulator bank.
- 3) Momentarily set Front Panel S16 to the EXAMINE position.
- 4) Enter the first byte of code on Front Panel switches S7 through S0.
- 5) Momentarily lift Front Panel S17 to the DEPOSIT position.
- 6) Enter the next byte of code on switches S7 through S0.
- 7) Momentarily lower S17 to the DEPOSIT NEXT position.
- 8) Repeat steps 6 and 7 until all code is entered into the Emulator board RAM.

## Software Write to Emulator

Code to be written into the Emulator can be located anywhere in system memory. The software for transferring code into the EPROM can be elaborate or simple but it should at least accomplish the following.

- \* Read the original data from its location in system memory and write it to the Emulator RAM, byte by byte. This function can be performed by simple monitors that include a block move instruction.
- \* After the transfer of code from memory to the Emulator board, check the Emulator against the source data and verify that there is a match.

## 3.2 READING THE EMULATOR RAM

Contents of the Emulator RAM can be read in two ways. First, the contents of Emulator RAM can be addressed and read enabled across the S-100 bus. Examples of this include CPU reads and Front Panel reads of the addressed data. Second, the Emulator EPROM data buffers can be enabled by the target PROM chip enable signal that is carried by the cable assembly.

The Emulator board asserts PHANTOM\* during a memory read cycle when addressed and SW1 is set to the BOARD ENABLE position. If the Emulator board overlaps a system memory board that can decode the PHANTOM\* line, only the Emulator memory is read.

### CPU Read of Emulator

The CPU Read of Emulator Ram is similar to CPU Read of system RAM.

### Emulator Write to Target EPROM

If the Emulator board jumpers J3 through J10 are correctly configured and a cable (or cables) is correctly installed between the Emulator board connector and the target PROM socket, the byte selected by the target PROM address lines (routed to the Emulator via the cable or cables) is output on the cable data lines.

### 3.3 16-BIT EMULATION

16-bit emulation is possible with the EPROM Emulator board. In a 16-bit system, EPROMs are installed in pairs, due to the 16-bit parallel nature of the processors. One EPROM contains the Odd bytes of code; the second EPROM contains the Even bytes of code.

Therefore, when writing to Emulator RAM, it is important to write sequential Even bytes in one bank, and sequential Odd bytes in the second bank.

NOTE that InterSystems 16-bit systems follow the convention whereby A0 low (logical ZERO) selects the Even byte of the 16 bit word, and A0 high (logical ONE) selects the Odd byte of the 16-bit word.

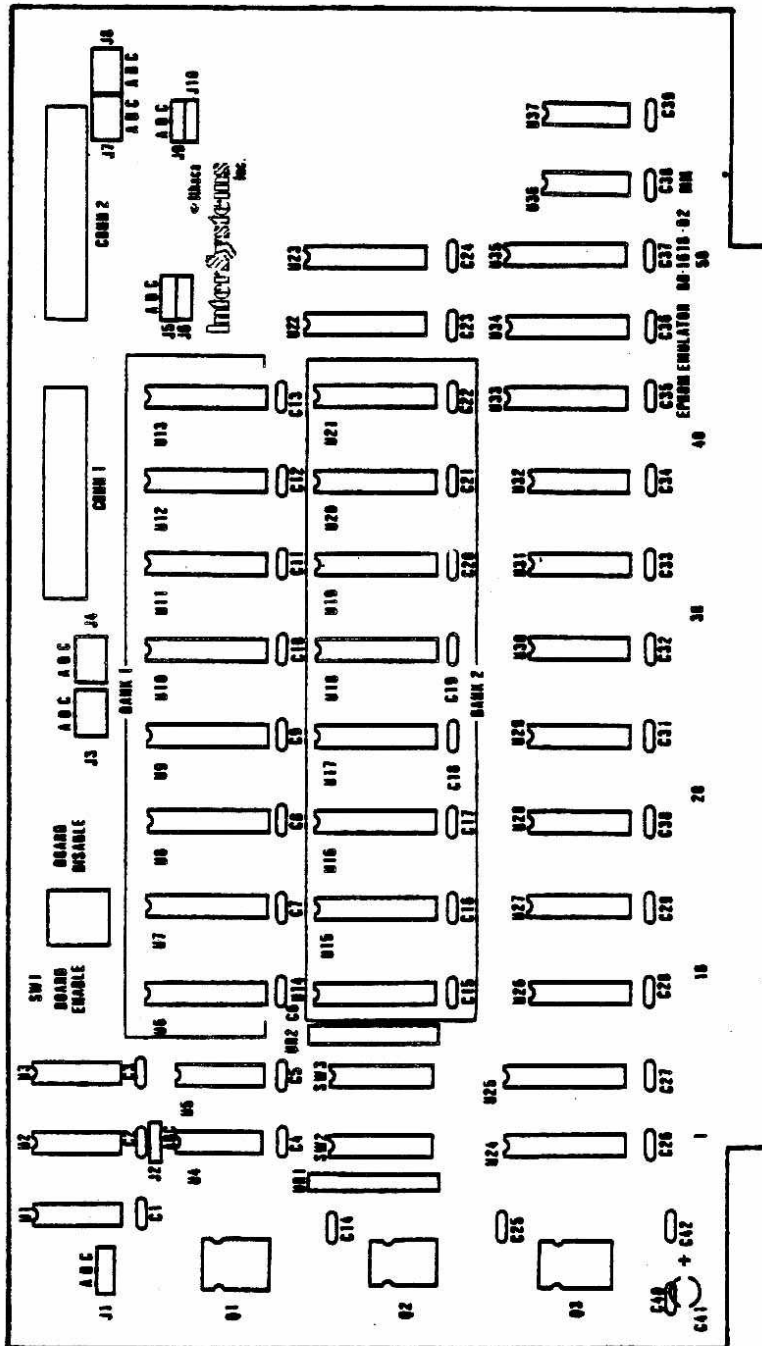


Figure 8 EPROM Emulator board

## 4.0 MANUAL REVISION AND BOARD APPLICABILITY

This manual applies to boards identified as EPROM EMULATOR BD1618-01. Board identification is located on the lower right side of the board.

## 5.0 PARTS LIST

### INTEGRATED CIRCUITS

Location	Part
U1	74LS02
U2	74ALS74
U3	74LS04
U4	74LS38
U5	74LS04
U6-U21	AM9244D
U22, U23	74LS244
U24, U25	25LS2521
U26-U31	74LS158
U32	74LS157
U33-U35	74LS244
U36	74LS10

### CAPACITORS

Location	Part
C1-C40	0.1 uf, AVX MD015E104Z
C41	10 uf, 25 V.

### RESISTOR NETWORKS

UR1, UR2	4.7k, 9 (or 10) pin SIP
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### REGULATORS

Q1-Q3	7805
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CHANGE FORM

Date: 11 JUNE 82

Board Name: EPROM EMULATOR

Board Number: 1618

Problem Occurs in Revision: 01

Requested by: M WILLIAMS

Change #: 1644-01-01 Page 1 of 2

APPROVAL

Approved: \_\_\_\_\_

To be included in PC @ Revision: \_\_\_\_\_

Date: \_\_\_\_\_

What is Change? (Please give brief summary)

TO MAKE BOARD ENABLE  
MEET IEEE S100 SPEC

Priority -- check one or more; each item must be individually approved. APR '82

- Update next PC. \_\_\_\_\_
- Include in new production. \_\_\_\_\_
- Include in all inventory (rework). \_\_\_\_\_
- Issue field update to customers. \_\_\_\_\_

Other: \_\_\_\_\_

(PLEASE use additional pages if required--it is not necessary to use this form for additional pages)

PROBLEM (describe clearly and legibly):

A FALSE BOARD ENABLE IS POSSIBLE UNDER IEEE S100 STANDARDS.

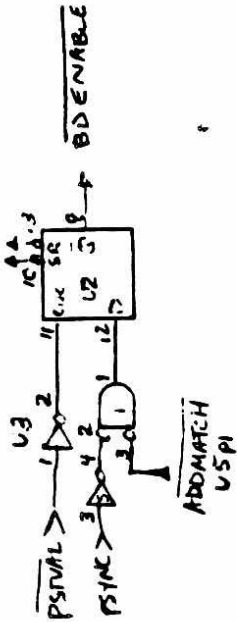
PROPOSED SOLUTION (describe clearly and legibly):

ENABLE BOARD ONLY ON NEGATIVE GOING EDGE OF P<sub>STUAL</sub> DURING P<sub>SYNC</sub> HIGH

PROCEDURE (be specific, detailed, and legible; cuts and jumpers must include exact locations on PC board; future PC changes should be described separately from modifications of current product; parts changes should specify position, old part, and new part):

PLEASE SEE NEXT PAGE.

NEW CIRCUIT:



PROCEDURE:

- 1 CUT U2P11 FROM U1P1
- 2 CUT U2P12 FROM USP2 AND U4P1
- 3 CUT U3P1 FROM TSV (U3P1,2 IS AN UNUSED GATE)
- 4 CUT PSTAT FROM U1P3
- 5 JUMPER PSTAT TO U3P1
- 6 JUMPER USP2 TO U2P11
- 7 JUMPER U3P1 TO U1P3
- 8 JUMPER U1P1 TO U2P12

SOLDER SIDE

