The Ithaca InterSystems 6SIO

Serial Input/Output Interface for the S-1ØØ Bus

Edition 3.Ø

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1.Ø INTRODUCTION

In early systems, a single serial communications link was all that most microcomputers required. This is no longer the case. A new generation of multi-tasking, multi-user operating systems and hardware require I/O in depth, and the InterSystems 6SIO can provide this facility elegantly, reliably, and economically.

Six channels of programmable-baud-rate RS-232 interface are provided; two of the channels may alternately provide current loop capability, and two other channels include the necessary clock connections for synchronous data communication.

In addition, the 6SIO is available in two versions, with or without interrupt controllers. For systems that need the response time and throughput advantages of interrupt-driven I/O, the 6SIO-1 has two 9519 interrupt controllers to provide 16 levels of interrupt response. The interrupts may be individually disabled, masked, and adjusted to a variety of operational modes by a powerful selection of software commands. In many applications, the 6SIO-Ø board, with no interrupt controller, can provide a less expensive means of serial I/O interface. Each of the boards may be operated as the single source of interrupts in the system, or, if vectored interrupt handling is available, as one of eight sources of interrupts.

This manual contains an introduction to the board, a functional overview of the board's operation, and setup instructions.

1.1 PHYSICAL DESCRIPTION

The 6SIO is a standard 5 by 1Ø inch (12.7 by 25.4 cm), S-1ØØ bus, plug-in circuit card that allows terminals and other equipment using serial signals to be connected to an S-1ØØ microcomputer. The board has three top edge connectors.

2.Ø FUNCTIONAL DESCRIPTION

This section of the 6SIO manual provides an introduction to the operation of the 6SIO board. The term "optional" below refers, unless specified otherwise, to board functions that are affected by user-alterable jumpers or other means.

2.1 COMPUTER INTERFACE

The 6SIO is an S-1ØØ card; it is compatible with all Ithaca InterSystems equipment.

Addressing

8-bit or (optional) 16-bit I/O addressing is provided.

Wait States

Ø, 1, 2, or 3 wait states may be generated, as set by the user. With 3 wait states, the card can operate in 6 MHz Z8Ø systems.

Interrupt Requests

The card is available in two versions, with or without interrupt controller. The 6SIO-Ø version has no interrupt controller. The 6SIO-1 version has an interrupt controller.

The interrupt request can optionally be connected to the S-1ØØ pINT* signal line, or to one of the eight S-1ØØ vectored interrupt lines. In the latter case, the system must have an interrupt controller to respond to the vectored interrupt.

6SIO-Ø

The 6SIO supports 18 sources for interrupts; that is, the card may be configured with jumpers and a header, so that 18 different electrical events on the card generate an interrupt.

Associated with each serial channel on the card are three signals which can optionally generate interrupts: Transmitter Ready, Receiver Ready, and Transmitter Empty/Data Set Change. Note that Break Detect can not be used as an interrupt-generating event.

A header area is provided to select which events produce interrupts. Open-drain interrupt sources are are wire ORed' together with the Common Interrupt Output line.

6SIO-1

The 6SIO-1 interrupt controller provides 16 levels of interrupts; that is, the card may be configured with jumpers, and the interrupt controller programmed, so that 16 different electrical events on the card generate an interrupt and, when queried by the system CPU, provide a specific (8-bit) byte depending on which of the 16 events generates the interrupt. The CPU gets the byte during an interrupt acknowledge bus cycle, or, optionally, by reading a port provided on the 6SIO card.

The output of the interrupt controller can optionally be connected to the S-1ØØ pINT* signal line, or to one of the eight S-1ØØ vectored interrupt lines. In the latter case, the system must have an additional interrupt controller to respond to the vectored interrupt.

Associated with each serial channel on the card are four signals which can optionally generate interrupts: Transmitter Ready, Receiver Ready, Transmitter Empty/Data Set Change, and Break Detect. Note that there are restrictions on the use of Break Detect as an interrupt-generating event in combination with the other three signals: briefly, each half of the interrupt system (i.e., eight interrupt levels) must be devoted to either Break Detect interrupts, or interrupts generated by the other three signals.

A header area is provided to select which events produce interrupts. The interrupt controller must also be programmed with a moderately complex set of command codes.

2.2 SERIAL INTERFACE

The 6SIO card provides for RS-232 and current loop serial communication. Each channel has simultaneous input and output (full duplex) capability.

Channels and Options

Each of the six serial channels on the 6SIO has a USART. Each channel provides simultaneous input and output serial communication (full duplex). The USART's have programmable internal baud rate generators. Other functions that may be set by software include data size, stop bit, and general purpose control signals. Each USART is provided with RS-232 drivers for the transmit data (TXD), ready to send (RTS), and data terminal ready (DTR) output lines and RS-232 receivers for the receive data (RXD) and clear to send (CTS) input lines.

Two USART's, (channels A and B) are provided with 20 ma current loop circuits for TXD and RXD. Two USART's (channels E an F) are provided with RS-232 drivers and receivers for external clock signals for synchronous communication. Each channel is provided with half of a mass termination top connector.

RS-232

All six channels of the 6SIO card provide serial communication that adheres to the RS-232 standard. Each RS-232 channel may be operated at one of the following baud rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, 4800, 9600, and 19,200 baud. Baud rates are set by software.

Current Loop

As described above, two channels of the 6SIO card can optionally be set for current loop operation. Current loops may be operated at the following baud rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, and 4800. There exists no standard for current loop operation; the user must determine that equipment to be used with the 6SIO card in current loop mode does not produce voltages or currents that result either in unreliable operation or damage to the card; similarly, the user must determine that the 6SIO current loop circuit provides appropriate currents and voltages for any intended application.

Request-to-Send Malfunction

Note that the USART's used on the 6SIO have a defect which may cause problems when used with some printers. Printers which might be affected are those that use the standard RS-232 signal Request-to-Send; whether the USART malfunctions or not depends

on the timing of the Request-to-Send signal produced by the printer.

Request-to-Send, when active, indicates that the printer is ready to receive data. The signal is inverted and applied to the (6SIO USART) CTS* input. Normally, when the CTS* input goes inactive, the USART does the following. First, if a character is currently being transmitted, transmission continues until the character is finished. Then, the USART stops transmitting. The USART output TxD goes high. TxD remains high as long as the CTS* input is inactive. However, if the CTS* input goes inactive at a vulnerable point in the USART timing scheme, the USART may drive TxD low (when it should drive TxD high).

This low signal appears as a high on the RS-232 signal line Receive Data (a repeated "space" or a "break"). Printer activity can be disrupted by this condition.

If this problem arises in a particular application contact the Ithaca InterSystems Customer Service department.

Top Connector
Pin Assignments

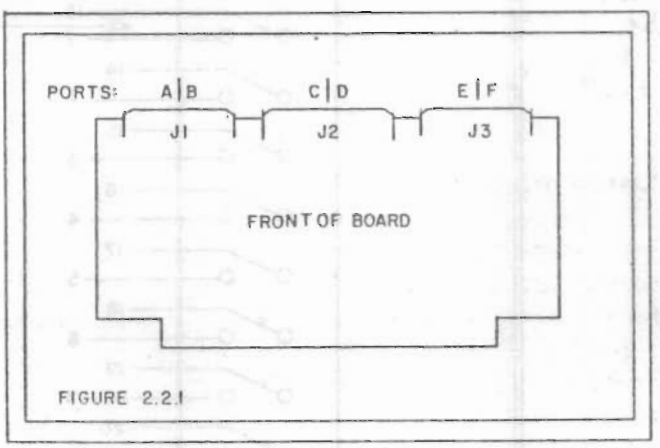

FIGURE 2.2.1

There are three mass termination receptacles on the top edge of the 6SIO card: one 50-pin receptacle (J1), and two 34-pin receptacles (J2 and J3). Each receptacle contains two RS-232 channels; in some cases, extra pins are assigned to special signals, such as current loop, or synchronous clocks. (Cables to connect these mass termination receptacles to two standard RS-232 connectors are available from Ithaca InterSystems.)

The arrangement of the serial channels and the connectors is shown in Figure 2.2.1. Serial channels A and B are located in J1; Figure 2.2.2 depicts the signal pin assignments. Channels C and D are located at J2. Channels E and F are located at J3. J2 and J3 pin assignments are listed in Figure 2.2.3.

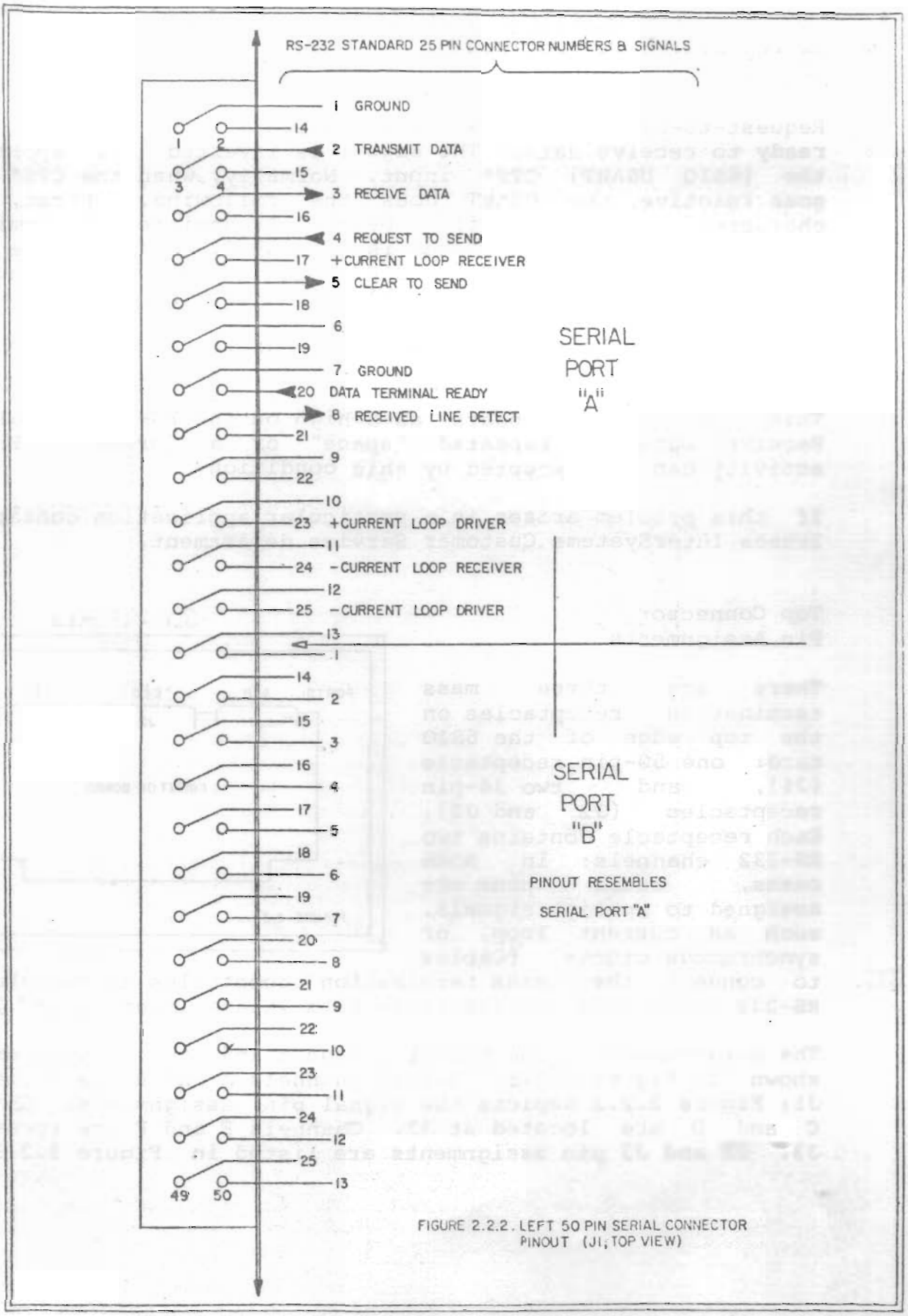

FIGURE 2.2.2. LEFT 50 PIN SERIAL CONNECTOR PINOUT (J1, TOP VIEW)

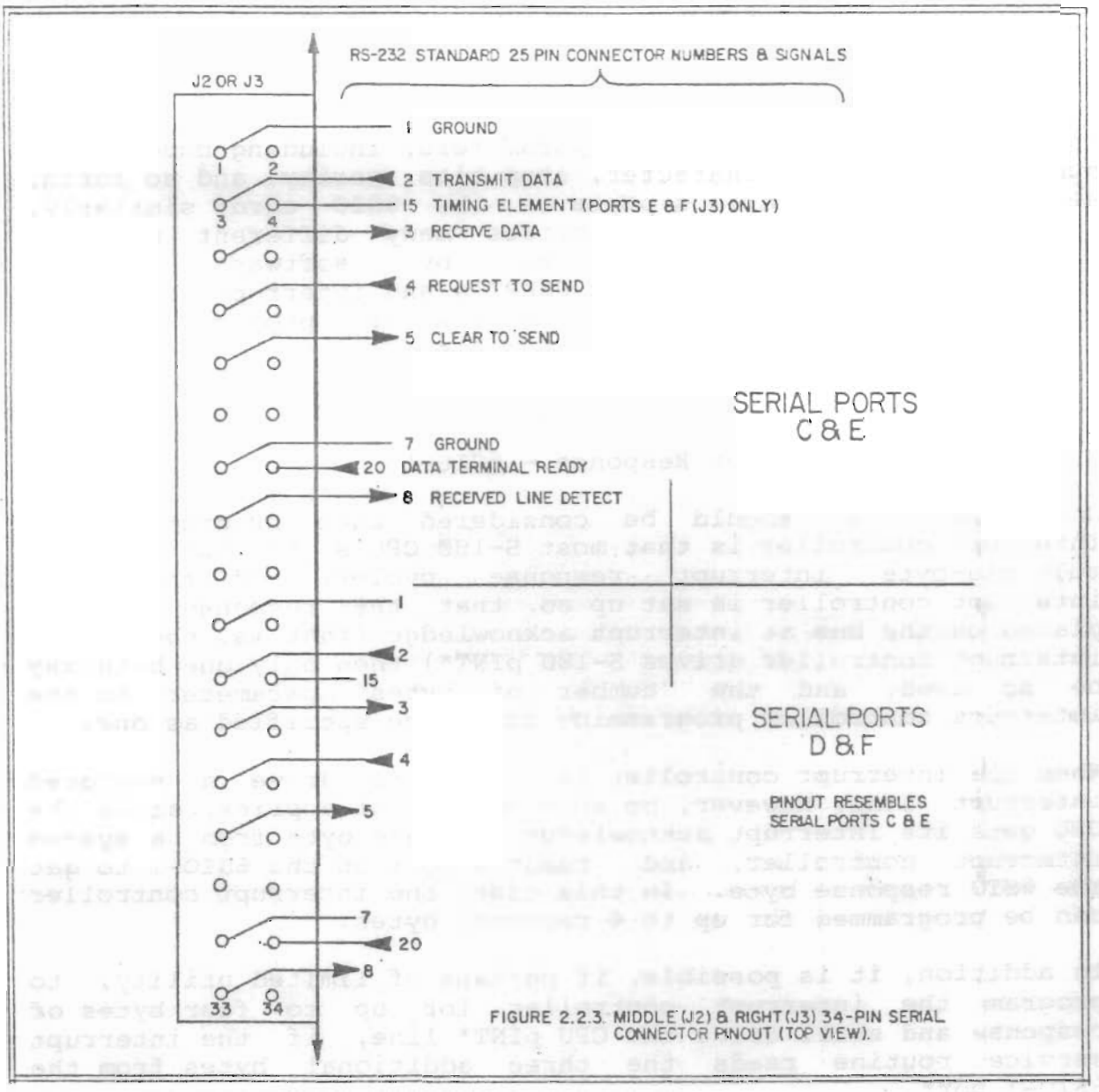

FIGURE 2.2.3. MIDDLE (J2) & RIGHT (J3) 34-PIN SERIAL CONNECTOR PINOUT (TOP VIEW).

2.3 USART AND INTERRUPT CONTROLLER PROGRAMMING

The USART's must have various parameters, including baud rate, number of bits per character, stop bits, parity, and so forth, set by writing to various ports on the 6SIO card; similarly, the interrupt controller provides many different modes of operation which must be set by software. Separate documentation for the 6SIO USART's and interrupt controller must be consulted regarding details of programming these devices. USART and interrupt controller register locations may be found on the Address Map below.

Multiple-Byte Interrupt Response - 6SIO-1

One point that should be considered when programming the interrupt controller is that most S-100 CPU's do not generate multiple-byte interrupt response cycles. If the 6SIO-1 interrupt controller is set up so that the response byte is placed on the bus at interrupt acknowledge (that is, the 6SIO-1 interrupt controller drives S-100 pINT*) then only one byte may be so used, and the "number of bytes" parameter in the interrupt controller programming should be specified as one.

When the interrupt controller is set up to drive a vectored interrupt line, however, no such constraint applies, since the CPU gets its interrupt acknowledge response byte from a system interrupt controller, and reads a port on the 6SIO-1 to get the 6SIO response byte. In this case, the interrupt controller can be programmed for up to 4 response bytes.

In addition, it is possible, if perhaps of limited utility, to program the interrupt controller for up to four bytes of response and still drive the CPU pINT* line, if the interrupt service routine reads the three additional bytes from the 6SIO-1 port.

2.4 ADDRESS MAP

The 6SIO I/O ports are arranged as shown. This map shows the port locations as they are when the board's base I/O address is set to ØØH. The board's base address can be shunt jumper selected by the user to any 2ØH boundary in the S-1ØØ system (2ØH, 4ØH, 6ØH, and so forth). Note that the 6SIO occupies 2ØH I/O locations even though some locations are not used.

I/O address (base address = Ø)	Register	Function
ØØ	Serial channel A	data
Ø1		status
Ø2		mode
Ø3		command
Ø4-Ø7	Serial channel B	same
Ø8-ØB	Serial channel C	same
ØC-ØF	Serial channel D	same
1Ø-13	Serial channel E	same
14-17	Serial channel F	same
18	Interrupt controller A	data
19		command
1A	Interrupt controller B	data
1B		command
1C	Software readable interrupt response byte	
1D-1F	not used	

3.Ø BOARD SETUP

Various user options should be determined before installing the 6SIO card in an S-1ØØ system. This section describes the options in detail; at the end of the section, a typical setup for the 6SIO card is listed. See the typical setup for a quick overview of the available options.

3.1 BOARD BASE ADDRESS

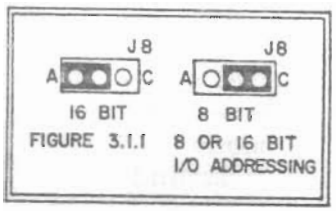

FIGURE 3.1.1

The 6SIO is configured to occupy any 2ØH I/O port space with a 2ØH boundary base address; i.e., ØØH, 2ØH, 4ØH, up to EØH for 8-bit I/O addressing, or ØØØØH, ØØ2ØH, ØØ4ØH, up to FFEØH for 16-bit I/O addressing.

The first decision for the user is whether to use 8 or 16 bit I/O addressing. This decision depends on the user's system. If the system is Z-8Ø/8Ø8Ø based, the I/O addressing is 8 bit. If the system CPU is a Z-8ØØØ or other processor with 16-bit I/O address capability, then 16 bit I/O addressing is possible. The option is set at jumper area J8 (Figure 3.1.1).

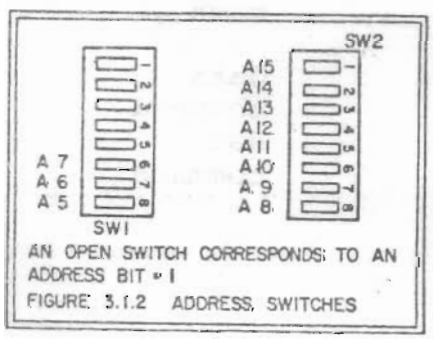

FIGURE 3.1.2 ADDRESS SWITCHES

Next, the board address is selected. The lower address bits, A7-A5, are set with DIP switch SW1 (for both 8-bit and 16-bit addressing) The upper address bits, A15-A8, (set only for 16 bit I/O addressing) are set with DIP switch SW2. See Figure 3.1.2.

3.2 WAIT STATE GENERATION

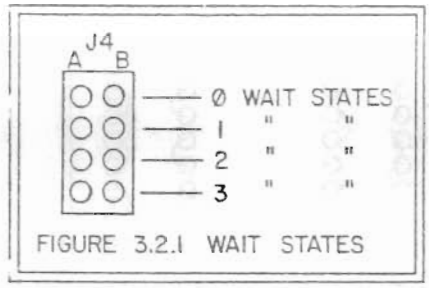

FIGURE 3.2.1 WAIT STATES

The 6SIO can be configured to request Ø, 1, 2, or 3 wait states when accessed by the system master. This allows for the access times of slow LSI parts (3ØØns for 2 MHz 9519, up to 25Ø for the USART). No wait states should be necessary for 2 MHz systems; 1 or 2 may be required for 4 MHz systems, and 2 or 3 wait states for 6 MHz. Actual requirements depend on many variables, including system access times.

To select the desired number of wait states, position the shunt on jumper J2 as shown in Figure 3.2.1.

3.3 STATUS STROBE SIGNAL

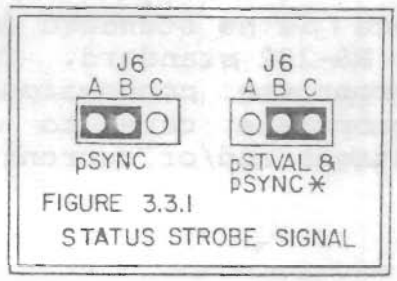

FIGURE 3.3.1
STATUS STROBE SIGNAL

Normally the 6SIO gates certain status signals from the bus when the S-1ØØ signals pSTVAL* and pSYNC are simultaneously active. The card can be configured to gate on the pSYNC signal alone. Some older CPU cards may operate more reliably with the 6SIO set this way. The option is set at jumper J6, depicted in Figure 3.3.1.

3.4 CURRENT LOOP CHANNELS A AND B

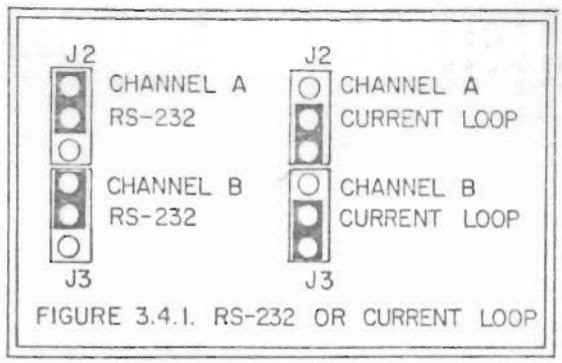

FIGURE 3.4.1. RS-232 OR CURRENT LOOP

Serial channels A and B have (in addition to a set of RS-232 drivers and receivers,) a 2Ø ma current loop data transmitter/receiver pair. The current loop transmitter uses RS-232 lines 23 and 25. The current loop receiver uses RS-232 lines 17 and 24. Current loop data transmission is used when electrical isolation is desired between interfacing devices. The current loop option is selected with jumpers J2 and J3 (Figure 3.4.1).

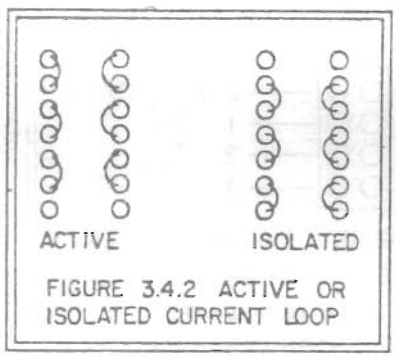

FIGURE 3.4.2 ACTIVE OR ISOLATED CURRENT LOOP

When a current loop circuit is being used, the activity of the current loop must be determined and set. The activity of the current loop circuit refers to whether the 6SIO provides the supply voltage and ground to the current loop (active loop), or the peripheral supplies the voltage and ground, and the current loop is opto-isolated from the rest of the 6SIO (isolated loop). Note that an active current loop pair must be connected to an isolated current loop pair and vice versa.

The current loop activity for channels A and B are determined by the orientation of 14 pin DIP headers H1 and H2 respectively. See Figure 3.4.2.

WARNING:

There is no standard for current loop connections analogous to the RS-232 standard. Consequently, the user must determine the appropriate connections for the application, and take appropriate care to avoid accidentally applying destructive voltages and/or currents to the 6SIO.

3.5 CLOCK SIGNALS, CHANNELS E AND F

Spare RS-232 drivers and receivers on the 6SIO are connected to line 15 on channels E and F to provide clock signal input to those channels for synchronous data communication. These receivers and drivers can be connected to the clock pins on USART's 4 and 5 by shunting at jumper J1 (shown in Figure 3.5.1) as outlined in the following chart.

	J1 Settings	
Function	Channel E	Channel F
Disconnect all clock signals	All J1: A-B	All J1: A-B
TXC drives RS-232 pl5	J1: 6, B-C	J1: 1, B-C
TXC, RXC receives RS-232 pl5	J1: 3,4, B-C	J1: 2,5, B-C
RXC receives TXC	J1: 3, B-C	J1: 2, B-C

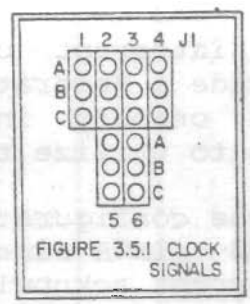

FIGURE 3.5.1 CLOCK SIGNALS

Shunts not specified should be set A-B.

3.6 SYSTEM INTERRUPT LINE SELECTION

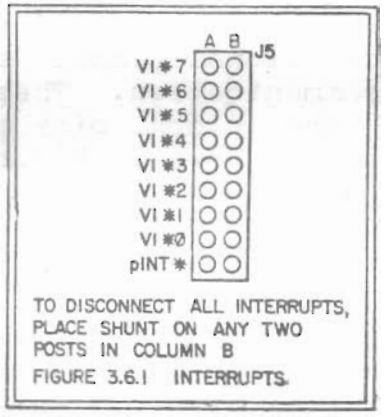

FIGURE 3.6.1 INTERRUPTS

The interrupt controller on the 6SIO-1 generates an interrupt signal when programmed to do so. The 6SIO-Ø generates an interrupt signal in accordance to the configuration of header H3. This signal may be connected to the S-1ØØ pINT* line or to any of the S-1ØØ VI* lines Ø through 7 by positioning the shunt on jumper J5. The option should be set according to the system configuration. See Figure 3.6.1.

The interrupt controller on the 6SIO-1 can be programmed to provide a separate user-defined interrupt response byte for each onboard interrupt source. The 6SIO-1 provides for two ways to utilize this response byte.

In one configuration, the 6SIO-1 is jumpered to respond to the S-1ØØ sINTA signal, and generate the byte in response to a CPU interrupt acknowledge cycle, as a single byte call or a routine pointer, depending upon the CPU and software. This mode usually requires that the 6SIO drive the pINT* line. The 6SIO only responds in this mode if it has an active interrupt request. This does not prevent conflicts between the 6SIO and another board in the same system which drives pINT* and responds to sINTA simultaneously. Therefore, only one board in a system should drive pINT and respond to sINTA.

FIGURE 3.6.2 sINTA RESPONSE

Alternately, the interrupt response byte can be read by the system at a port (see the address map in Section 2), allowing the user to create a customized interrupt status register to facilitate interrupt servicing. The 6SIO drives one of the VI* lines, which then is processed by a system interrupt controller.

The second arrangement of the interrupt response is permanently enabled on the 6SIO. sINTA response may be enabled at jumper J7 as shown in Figure 3.6.2.

The 6SIO-Ø (no interrupt controllers) is shipped with J7 set A-B.

3.7 ON-BOARD INTERRUPT ORGANIZATION

6SIO-Ø

There are three signals generated by each USART available on the 6SIO-Ø for use as interrupt sources: Transmitter Ready (TXR), Receiver Ready (RXR), and Transmitter Empty or Data Set Change (TXEMT/DSCHG). The six USART's generate a total of 18 onboard interrupt sources. The Break Detect (BKDET) signals can not be used as interrupt sources.

The 18 interrupt sources and a single interrupt request output are brought together at a single 40-pin DIP header, where the user connects the selected sources to pin 12 of the header. Note that TXR, RXR, and TXEMT/DSCHG are active-low open-drain signals and therefore may be "wire ORed" together in groups and connected to pin 12.

The pinout of the 40-pin DIP header where these signals are available (header H3) is shown below. The user may wire any combination desired; system software, of course, must support the arrangement.

6SIO-Ø Layout of Header H3

	1-Pins-40	
	1 40	Chan. B TXR*
Chan. A DS/TE*	2 39	Chan. B RXR*
Chan. A RXR*	3 38	Chan. B DS/TE*
Chan. A TXR*	4 37	
	5 36	Chan. C TXR*
	6 35	Chan. C RXR*
	7 34	Chan. C DS/TE*
	8 33	
	9 32	Chan. D TXR*
	10 31	Chan. D RXR*
	11 30	Chan. D DS/TE*
Common Interrupt Output	12 29	
	13 28	Chan. E TXR*
	14 27	Chan. E RXR*
	15 26	Chan. E DS/TE*
	16 25	
	17 24	Chan. F TXR*
	18 23	Chan. F RXR*
	19 22	Chan. F DS/TE*
	20 21	

The 6SIO interrupt controller has 16 interrupt request inputs (IREQs) to which the user may attach onboard interrupt sources. There are four signals generated by each USART available on the 6SIO for use as interrupt sources: Transmitter Ready (TXR), Receiver Ready (RXR), Transmitter Empty or Data Set Change (TXEMT/DSCHG), and Break Detect (BKDET). Six USART's generate a total of 24 onboard interrupt sources.

The 16-input interrupt controller consists of two 8-input 9519 interrupt controllers cascaded together. Controller A (U24) has higher priority than controller B (U23); at each interrupt controller, IREQØ has the highest priority and IREQ7 the lowest. Thus IREQ7 of interrupt controller A has higher priority than IREQØ of interrupt controller B. The two controllers have independent data and control ports and are therefore programmed separately.

The 24 interrupt sources and 16 interrupt request inputs are brought together at a single 4Ø pin DIP header, where the user connects sources to desired IREQ inputs. Note that TXR, RXR, and TXEMT/DSCHG are active-low open-drain signals and therefore may be "wire ORed" together in groups and connected to the same IREQ. Note also that the active polarity of the IREQs of a 9519 controller may be set by software, but they must be set together; i.e., on one controller they may either be all active low or all active high but not mixed. Therefore, if the BKDET interrupts are to be used, they must all be connected to IREQs of the same 9519 controller, since BKDET is active high and that controller is to be programmed for active high IREQs.

The pinout of the 4Ø pin DIP header where these signals are available (header H3) is shown below. The user may wire any combination desired; system software, of course, must support the arrangement.

6SIO-1 Layout of Header H3

Chan. A BKDET	1-Pins-40	Chan. B TXR*
Chan. A DS/TE*	2 39	Chan. B RXR*
Chan. A RXR*	3 38	Chan. B DS/TE*
Chan. A TXR*	4 37	Chan. B BKDET
Int. Cont. B IREQ 7	5 36	Chan. C TXR*
Int. Cont. B IREQ 6	6 35	Chan. C RXR*
Int. Cont. B IREQ 5	7 34	Chan. C DS/TE*
Int. Cont. B IREQ 4	8 33	Chan. C BKDET
Int. Cont. B IREQ 3	9 32	Chan. D TXR*
Int. Cont. B IREQ 2	10 31	Chan. D RXR*
Int. Cont. B IREQ 1	11 30	Chan. D DS/TE*
Int. Cont. B IREQ 0	12 29	Chan. D BKDET
Int. Cont. A IREQ 7	13 28	Chan. E TXR*
Int. Cont. A IREQ 6	14 27	Chan. E RXR*
Int. Cont. A IREQ 5	15 26	Chan. E DS/TE*
Int. Cont. A IREQ 4	16 25	Chan. E BKDET
Int. Cont. A IREQ 3	17 24	Chan. F TXR*
Int. Cont. A IREQ 2	18 23	Chan. F RXR*
Int. Cont. A IREQ 1	19 22	Chan. F DS/TE*
Int. Cont. A IREQ 0	20 21	Chan. F BKDET

3.8 TYPICAL SETUP

The chart below describes a typical 6SIO setup which is depicted in Figure 3.8.1. It should be emphasized that there is no "standard" setup for the 6SIO. The user must determine the appropriateness of any set of options.

Implemented Option	Jumpers, Switches
Clock signals at channels E and F disconnected (no synchronous operation)	J1: 1-6, AB
RS-232 operation for channel A	J2: AB
RS-232 operation for channel B (no current loops)	J3: AB
2 wait states	J4: shunt 3rd pair down
Interrupt controller drives S-100 VI2*	*J5: shunt 6th pair down
Certain signals on the board are gated at pSYNC AND pSTVAL* (standard) not pSYNC (non-standard)	J6: BC
Board does not respond to sINTA (external interrupt controller is used)	J7: AB
8-bit addressing	J8: BC
Base address = 00H	SW1: 5, 6, 7, Closed SW1: Others, not used SW2: Not used
Active current loop, channel A (if channel A current loop used)	Header H1: Shunt pins 1-2, 3-4, 5-6, 9-10, 11-12, 13-14
Active current loop, channel B (if channel B current loop used)	Header H2: Shunt pins 1-2, 3-4, 5-6, 9-10, 11-12, 13-14
	*Header H3: Shunt pins
Channel A RXR* drives Interrupt Controller A, IREQ 5	3-15,
Channel B DS/TE* drives Interrupt Controller A, IREQ 6	14-38,
Channel B RXR* drives Interrupt Controller A, IREQ 7	13-39

* Not applicable to 6SIO without interrupt controller

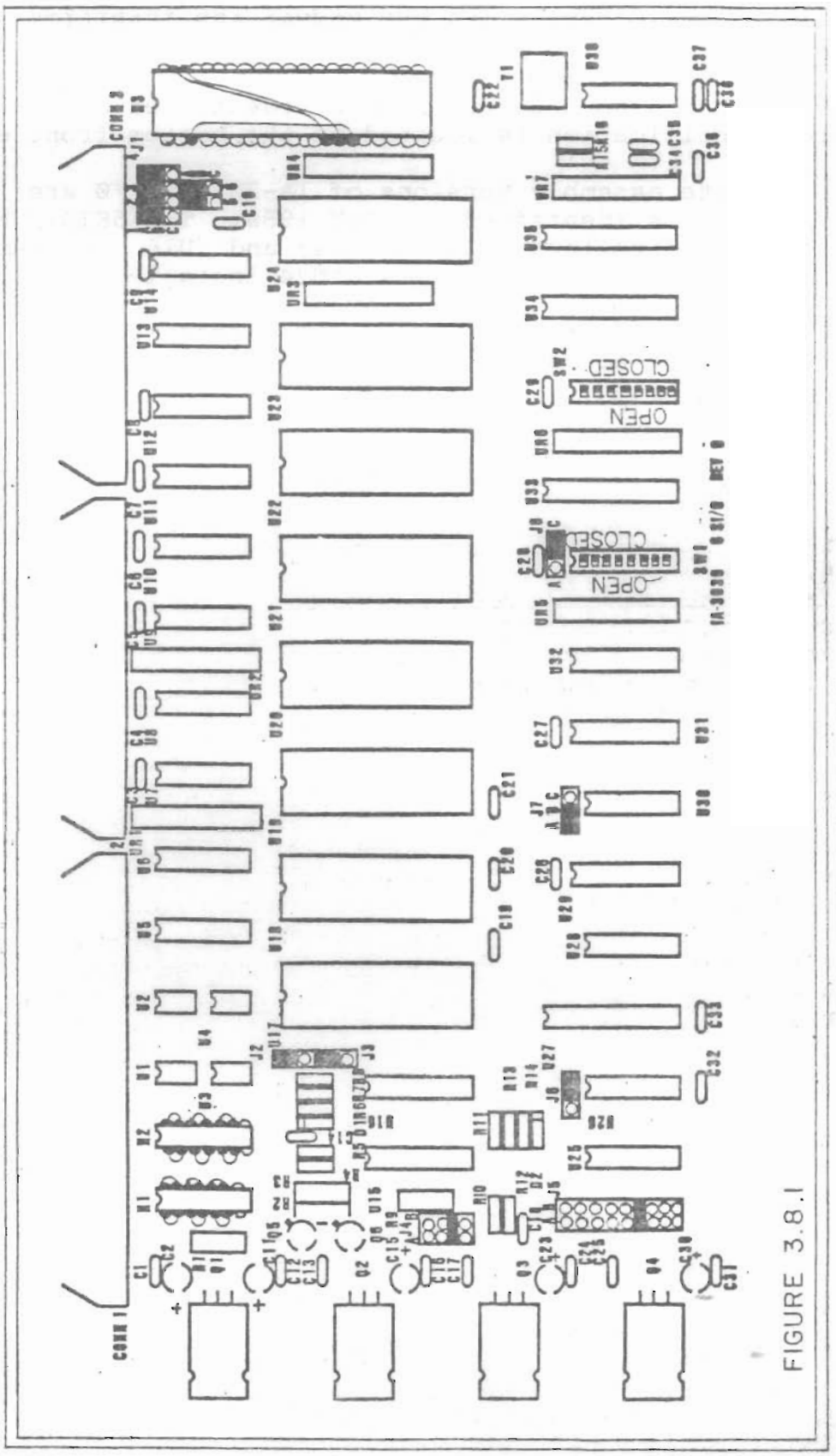

FIGURE 3.8.1

6SIO

4.Ø REVISIONS AND MANUAL APPLICABILITY

6SIO Serial Input/Output cards identified as 1A-3Ø3Ø REV Ø. Board identification is located on the bottom front edge.

Two separate assembly versions of 1A-3Ø3Ø Rev Ø are supported. The 6SIO-Ø is identified as ASSY 198Ø. The 6SIO-Ø has no 9519 interrupt controllers (U23 and U24) and U16 is removed. The 6SIO-1 version has U16, U23, and U24 installed.

Edition 2.Ø of the 6SIO manual described only the 6SIO-1 version of the board.