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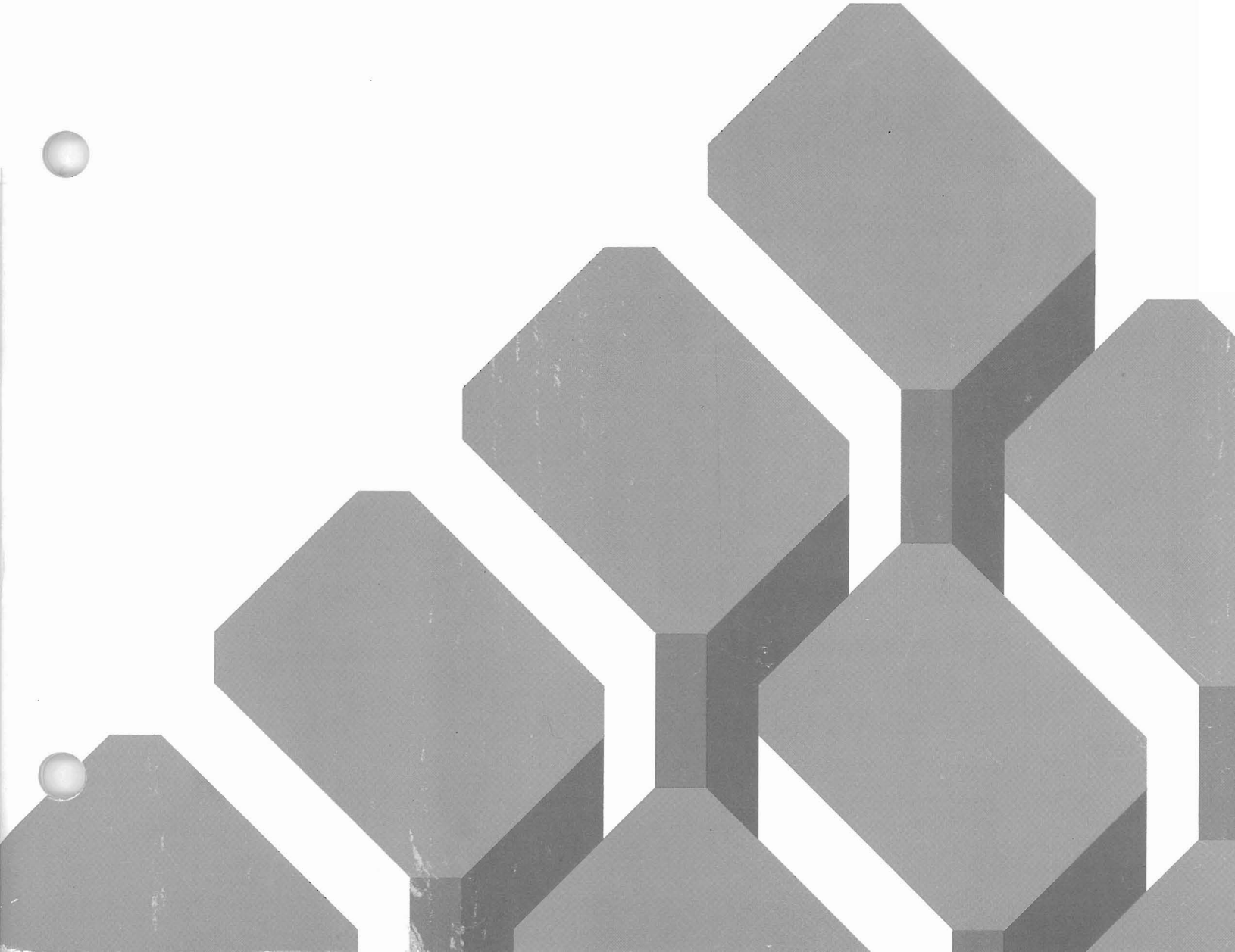
PERSONAL COMPUTER SYSTEMS

Z-329 MONOCHROME VIDEO CARD

INSTALLATION MANUAL



Monochrome Video Card

Z-100 PC Series Computers and IBM PC Computers

Installation Manual

595-3354

Z-329

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Zenith Data Systems Corporation
St. Joseph, Michigan 49085

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Introduction and Specifications

Introduction

The Z-329 Monochrome Video Card interfaces between the computer system and the video monitor. The Z-329 Card provides a video output compatible with the output from an IBM monochrome video card.

The Z-329 Card provides one page of memory stored in static RAM. Two pages (interlaced) or four pages (non-interlaced) of data can be stored if the optional 8K $\times$ 8 RAMs are installed. The characters are stored in ASCII code. An 8-bit attribute byte, also stored in RAM, is associated with each ASCII character. The characters are converted into pixel drive data by a character ROM located on the card. The ROM converts the ASCII code into the correct pixel drive data to create the characters on the monitor.

Up to 80 characters can be displayed in each of the 25 lines of the display. The attributes allow any character to be blanked (not displayed), blink, underlined, intensified, or displayed in reverse video (black on white).

The addresses of the control registers and of the memory on this card are different than those of the other video cards available with the Z-100™PC. This means that the standard video card (red-green-blue display, low/high-resolution graphics) and the Z-319 Bit-Mapped Video Graphics Card (Z-100 compatible, high-resolution graphics) can be left in the computer.

Specifications

Display Format: 25 rows of 80 characters (50 rows of 80 characters can be displayed when the optional 8K × 8 RAMs are installed and the interlace mode is used)

Character Type: 9 × 14 dot matrix

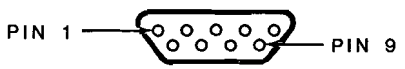
Character Set: "Hard", redefinable by ROM (1 character font is supported, a second font may be present on the standard ROM, and up to 4 fonts may be custom programmed into the optional 128K ROM)

Attributes: Non-display, blink, underline, intensify, and reverse video

Pages: 1 (up to 4 pages non-interlaced or 2 pages interlaced are available with optional RAM chips)

Outputs: Video, intensity, horizontal sync, and vertical sync

Z-329 Output Connector



(REAR VIEW)

PIN #	DESCRIPTION
1	CHASSIS GROUND
2	SIGNAL GROUND
3-5	NO CONNECTION
6	INTENSITY
7	VIDEO
8	HORIZONTAL SYNC
9	VERTICAL SYNC

Chapter 2

Installation, Configuration, and Initial Tests

Z-100 PC Series Computers

Z-150 Disassembly

If your computer is a Z-150 Desktop Computer, use this disassembly procedure.

WARNING: When the line cord is connected to an AC outlet, hazardous voltages can be present inside your computer.

- Switch off the computer and unplug the line cord from the AC outlet.
- Refer to Figure 2.1. Remove and save the seven screws (labeled 6-32 × 3/8) that secure the top cover to the computer.
- Carefully lift the top cover slightly to the rear and then lift it straight up and set it aside.

Disassembly is now complete. Proceed to Configuration.

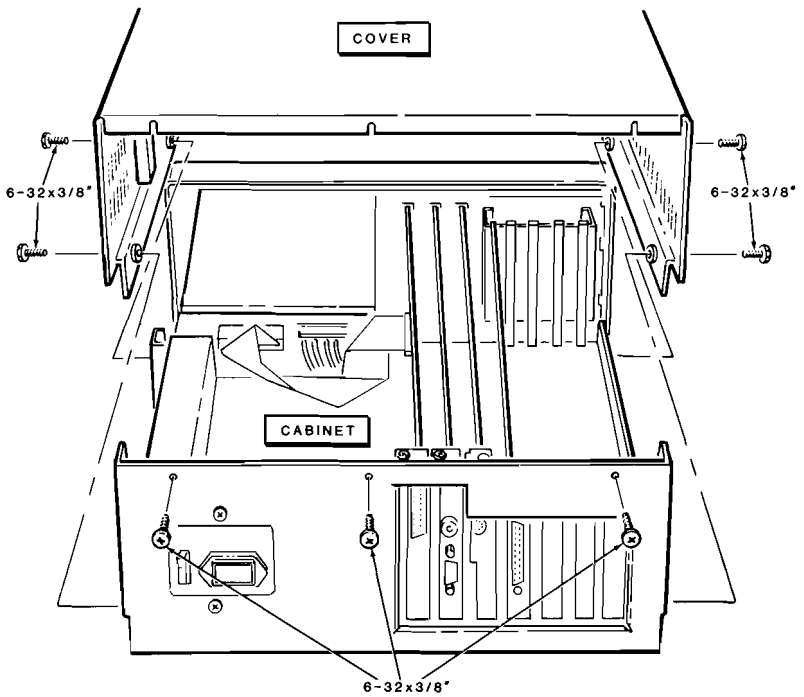


Figure 2.1. Z-150 Disassembly

Z-160 Disassembly

If your computer is a Z-160 Portable Computer, use the following disassembly procedure.

WARNING: When the line cord is connected to an AC outlet, hazardous voltages can be present inside your computer. Be especially cautious of the area marked HAZARDOUS VOLTAGE in Figure 2.2.

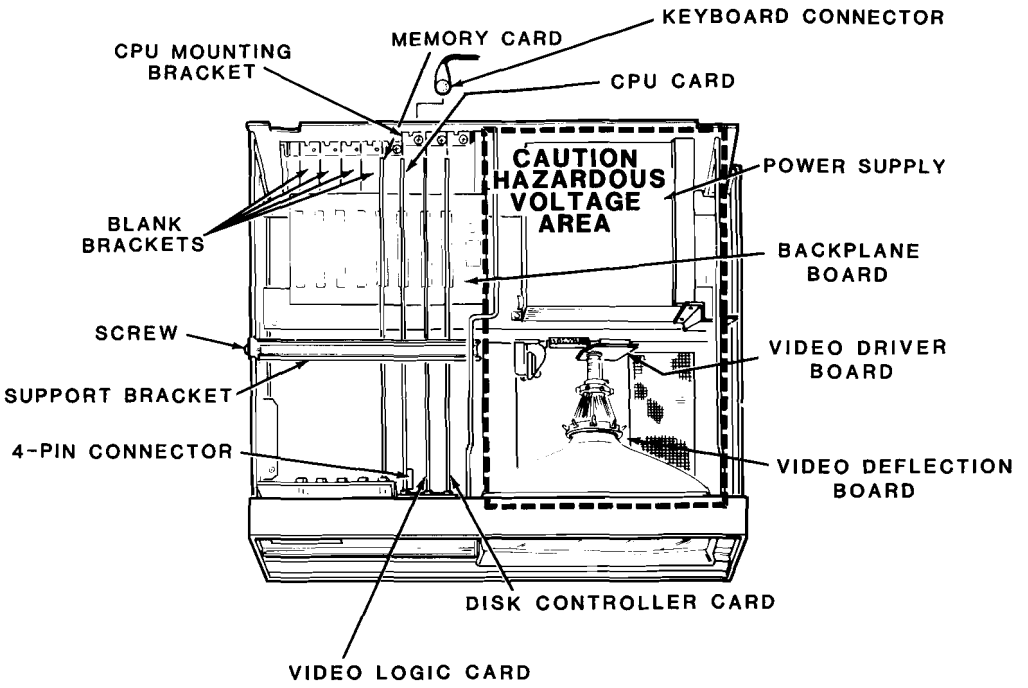


Figure 2.2. Z-160 Chassis

- Unplug the line cord from the AC outlet.
- Refer to Figure 2.3. Slide the drive assembly latches (shown in inset) toward the front of the computer and hold them in that position while lifting the disk drive assembly. Lift the drive assembly until the latch arms are free of the slot in the cabinet top.
- Lift the disk drive assembly until it is nearly vertical and hold it or prop it in this position.
- Disconnect the ground strap (shown in inset) from the computer chassis and disconnect the drive ribbon cable and the power supply cable(s).
- Push the connectors, which were disconnected in the previous step, through the opening in the cabinet top.
- Lift the disk drive assembly until it is vertical and then lift it off the computer. Carefully place the disk drive assembly aside.
- Remove and save the four screws (labeled 6-32 × 3/8) which secure the cabinet top to the computer.
- Slightly lift the rear of the cabinet top. Move the cabinet top rearward until the front lip of the cabinet top is no longer under the computer front panel.
- Lift the cabinet top straight off the computer and set it aside.
- Locate the card support bracket (Figure 2.2) which secures the printed circuit cards. Remove the card support bracket screw and the bracket and set them both aside.

Disassembly of the Z-160 is now complete. Proceed to the Installation of Video Card section.

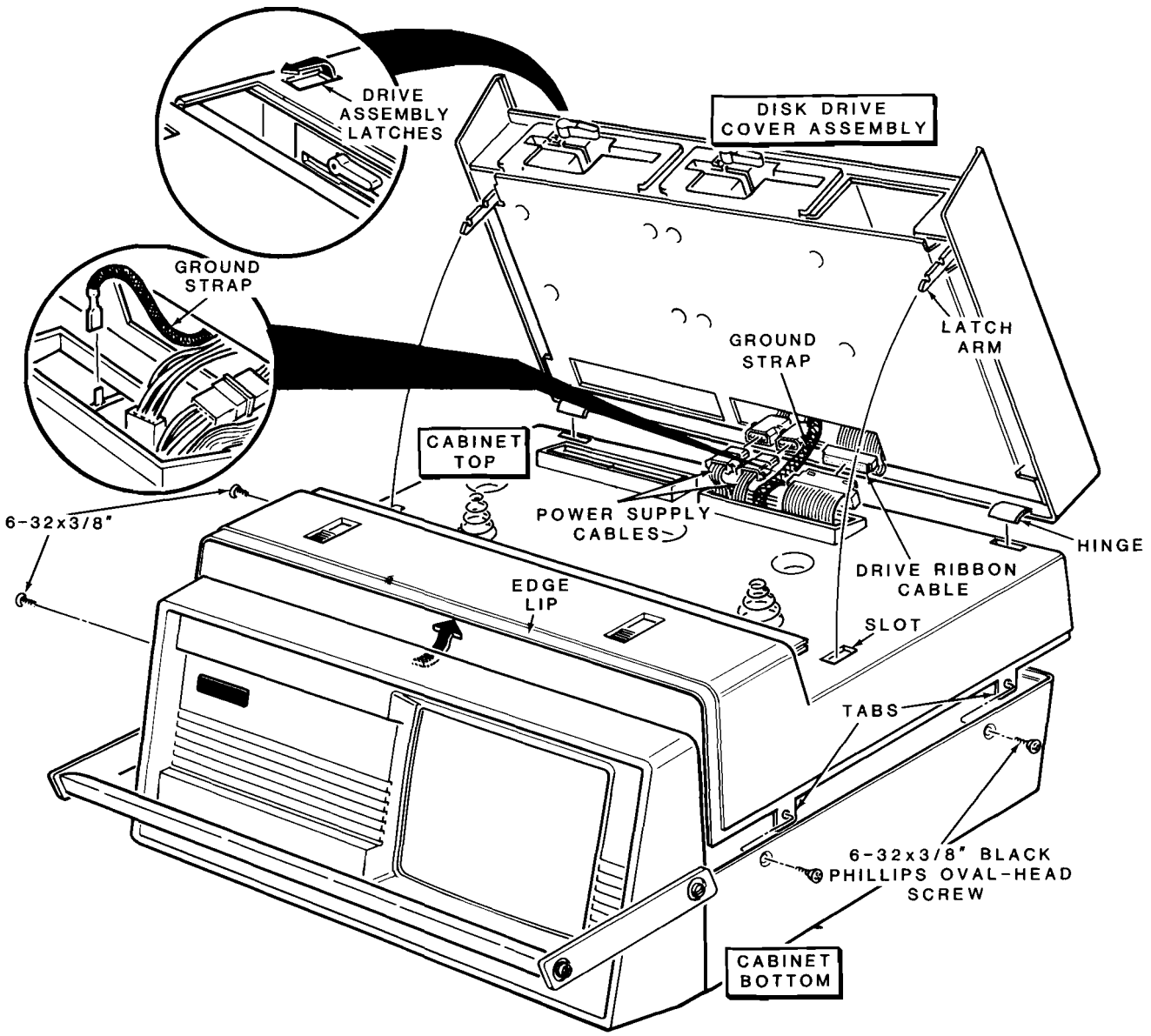


Figure 2.3. Z-160 Disassembly

Configuration

Simplified Configuration (Default)

NOTE: The card should come from the factory in this configuration.

Position the Z-329 Card as shown in Figure 2.4. All jumpers should be installed as shown in the figure. These jumper positions are detailed below:

- ☐ The two RAM size jumpers (J6 and J7) should be in the 2K position.
- ☐ The video control jumpers (J2, J3, and J4) all should be in the positive (POS) position.
- ☐ Vertical sync jumper J1 should be in the negative (NEG) position.
- ☐ ROM size jumper J5 should be in the 64K, 128K position.

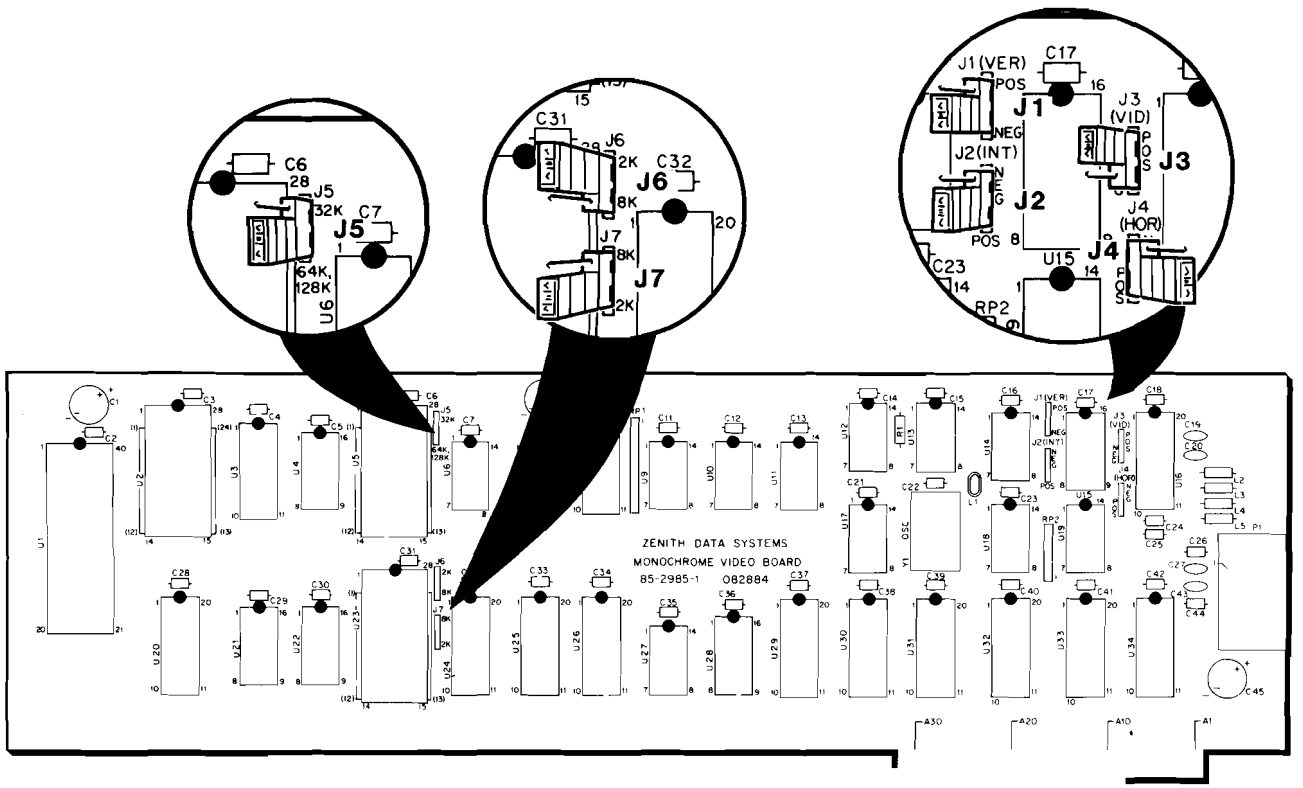


Figure 2.4. Z-329 Card Component Layout

Detailed Configuration

- Jumpers J6 and J7 are used to "size" the RAM chips on the Z-329 Card. The card is shipped with 2K × 8 static RAM ICs installed. It is possible to install 8K × 8 static RAM ICs. When this is done, these jumpers must be moved to the 8K position.

- Jumper J5 is used to "size" the ROM chips on the Z-329 Card. The card is shipped with a 8K × 8 ROM IC installed. It is possible to install 4K × 8 or 16K × 8 ROM ICs. When this is done, J5 must be moved to the position corresponding to the size of the ROM installed.

- Jumper J3 controls the polarity of the video data. When this jumper is in the POS position, +5 VDC is used to light a pixel and ground drives dark pixels. When this jumper is in the NEG position, ground is supplied to the monitor for all lighted pixels and +5 VDC is used for dark pixels.

- Jumper J2 controls the polarity of the intensity signal. In the POS position, an intensified character is signified by a logic high and a standard display by a ground. In the NEG position, logic high is used for the standard display and intensified characters are created by a ground.

- Jumper J4 controls the polarity of the horizontal sync. In the POS position the sync pulses are positive-going. In the NEG position the pulses are negative-going.

- Jumper J1 controls the polarity of the vertical sync. In the POS position the sync pulses are positive-going. In the NEG position the pulses are negative-going.

CPU Card Configuration

The configuration switches on the CPU card must be properly set for the computer to automatically select video from the Z-329 Card when it is switched on. The Z-329 Card can be selected from the monitor mode or by software regardless of the switch setting. The following instructions describe resetting these switches.

- Locate the CPU card (Figure 2.2 or Figure 2.5).
- Unplug the keyboard from the back of the computer.
- Unplug the 4-pin connector from the front of the CPU card (Figure 2.2 or Figure 2.5).
- Remove and save the screw from the CPU mounting bracket (Figure 2.2 or Figure 2.5).
- Gently pull upward on the CPU card to remove it from the computer.

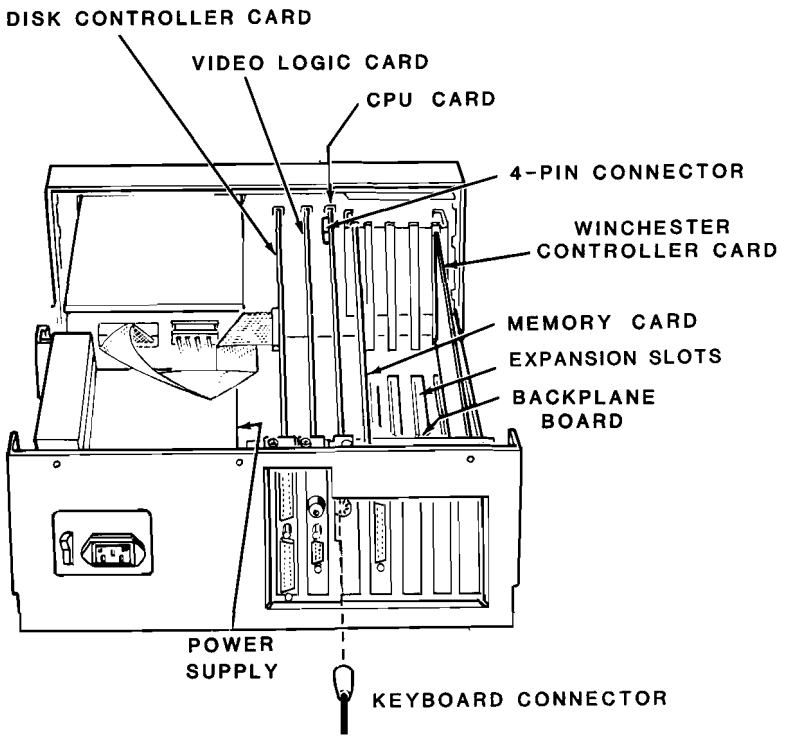


Figure 2.5. Z-150 Chassis

- Locate SW1 (Figure 2.6) and set switch sections 4 and 5 to the OFF (left) position.

Reinstall the card as follows:

- Align the front edge of the card in the card guide.
- Insert the card into the card guide.
- Line up the card edge-connector with the backplane connector.
- Gently, but firmly push the card into the backplane connector until the card is fully inserted.
- Secure the card to the back of the computer with the screw removed from the blank bracket.

CAUTION: The computer can be damaged if a metal object is dropped into the computer and not removed before power is switched on. Recover all objects before applying power.

- Connect the 4-pin connector to the front of the CPU card.
- Connect the keyboard to the CPU card through the back of the computer.

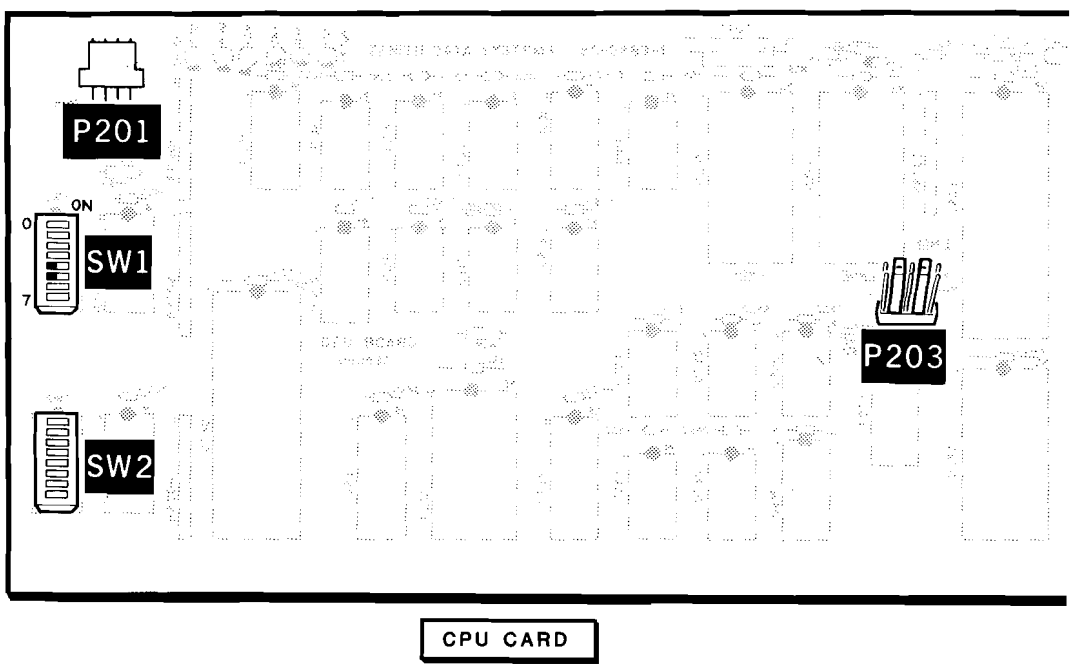


Figure 2.6. CPU Card Switch Setting

Installation of Video Card

- The new Z-329 Video Card may be installed in any empty backplane expansion slot. Select any available slot (Figure 2.2 or 2.5).
- Remove and save the blank bracket screw (Figure 2.7) from the blank bracket and then remove and discard the blank bracket.

Install the card as follows:

- Align the front edge of the card in the card guide.
- Insert the card into the card guide.
- Line up the card edge-connector with the backplane connector.
- Gently, but firmly push the card into the backplane connector until the card is fully inserted.
- Secure the card to the back of the computer with the screw removed from the blank bracket.

You are now ready to reassemble your computer. Proceed to the reassembly instructions.

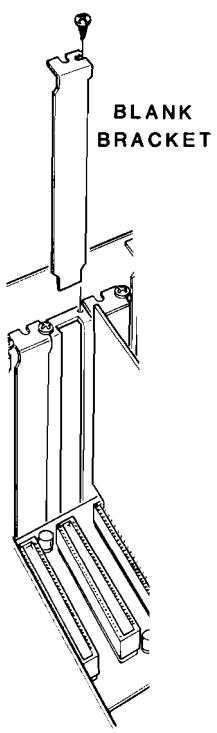


Figure 2.7. Blank Bracket

Z-160 Reassembly

Use the following procedure to reassemble your Z-160 Portable Computer.

- Place the card support bracket (Figure 2.8) in position along the top of the cards. Secure the card support bracket to the computer frame with the card support bracket screw which was removed earlier.
- Refer to Figure 2.9. Push the drive ribbon cable and the power supply cable(s) through the cutout in the cabinet top.
- Slide the front of the cabinet top under the lip in the front panel and then lower the top cover onto the computer.
- Reinstall the four screws (labeled 6-32 × 3/8) which secure the cabinet top to the computer.
- Lift the disk drive assembly into position and engage the hinge pieces into the slots in the top cover.

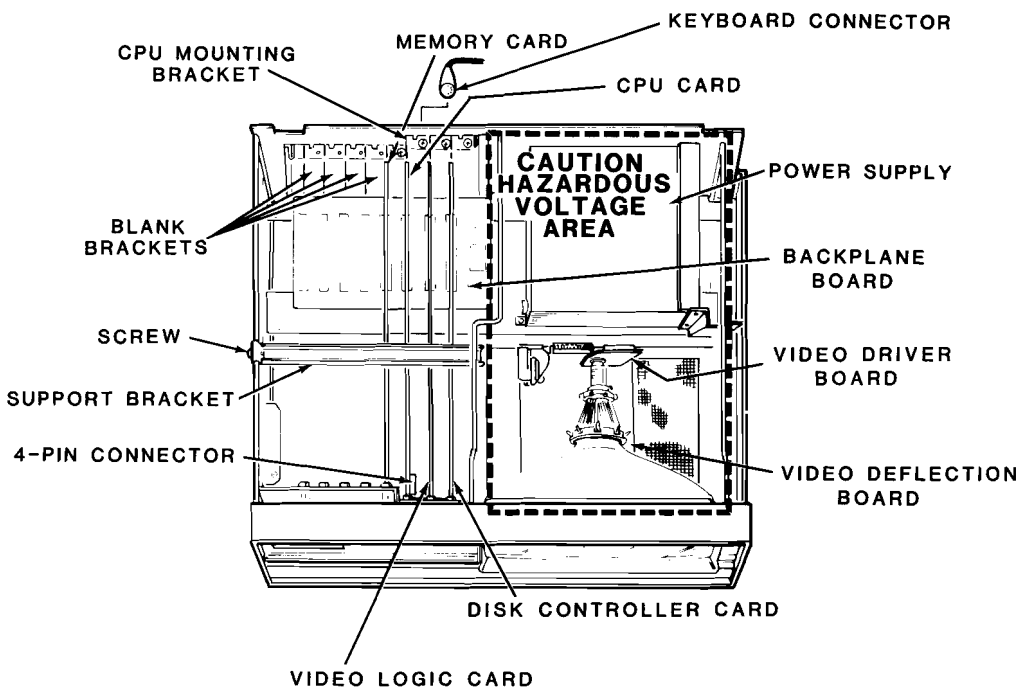


Figure 2.8. Z-160 Chassis

- Hold or prop up the disk drive assembly and connect the drive ribbon cable so that the striped sides of both cables are on the same side when connected. Connect the power supply cable(s). Connect the ground strap to the computer frame as shown in the inset.
- Gently lower the disk drive assembly onto the cabinet top. Pull the latch arms back slightly so that they enter the slot in the cabinet top.
- Proceed to the checkout procedure.

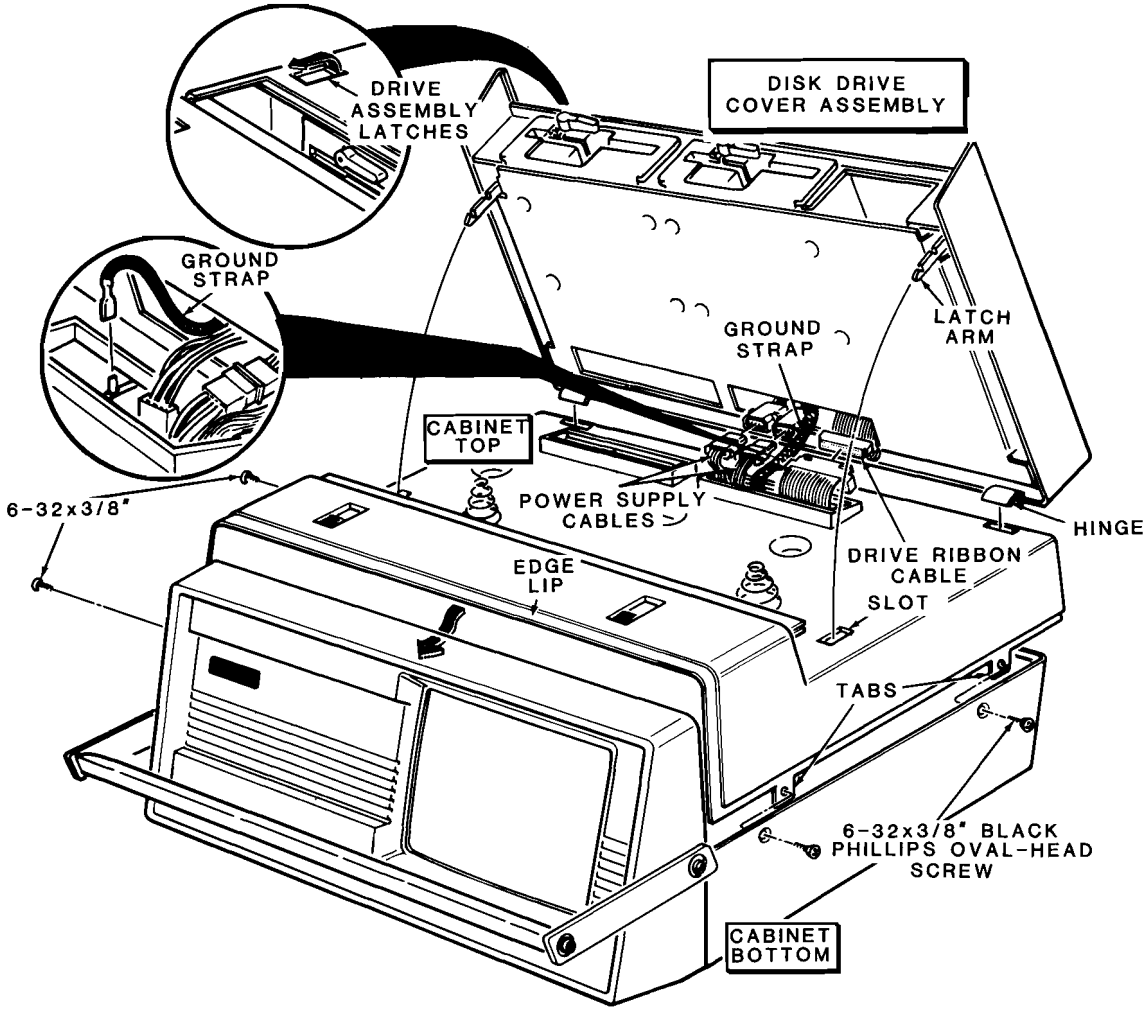


Figure 2.9. Z-160 Reassembly

Z-150 Reassembly

Use the following procedure to reassemble the Z-150 Desktop Computer as shown in Figure 2.10.

- Switch off the computer power switch.
- Remove the computer line cord from the AC outlet.
- Carefully place the top cover on the computer.
- Secure the cover to the computer with the seven screws labeled 6-32 × 3/8 which were removed during disassembly.
- Reconnect the computer line cord to an AC outlet.
- Proceed to the checkout procedure.

Checkout for Z-100 PC Series Computers

☐ Connect a monitor to the output from the Z-329 Card.

☐ Connect the computer and monitor to electrical power, and switch both units on.

Video can be selected from the Z-329 Card in one of three ways. If the CPU is configured for the monochrome display (see Configuration), the Z-329 Card is automatically selected. The monitor mode can be entered (hold down the **Esc** key during powerup or hold down the **Ctrl, Alt,** and **Ins** keys) and then enter **VM 7** and press the **Return** key. Software also can select the monochrome card.

☐ Select video from the Z-329 Card.

☐ A blinking cursor should be displayed on the monitor. This signifies that the CRTC and most of the circuitry is operating correctly. If further problems are suspected, a more complete test of the memory is contained in the disk-based diagnostics (CB-5063-13).

This completes the installation.

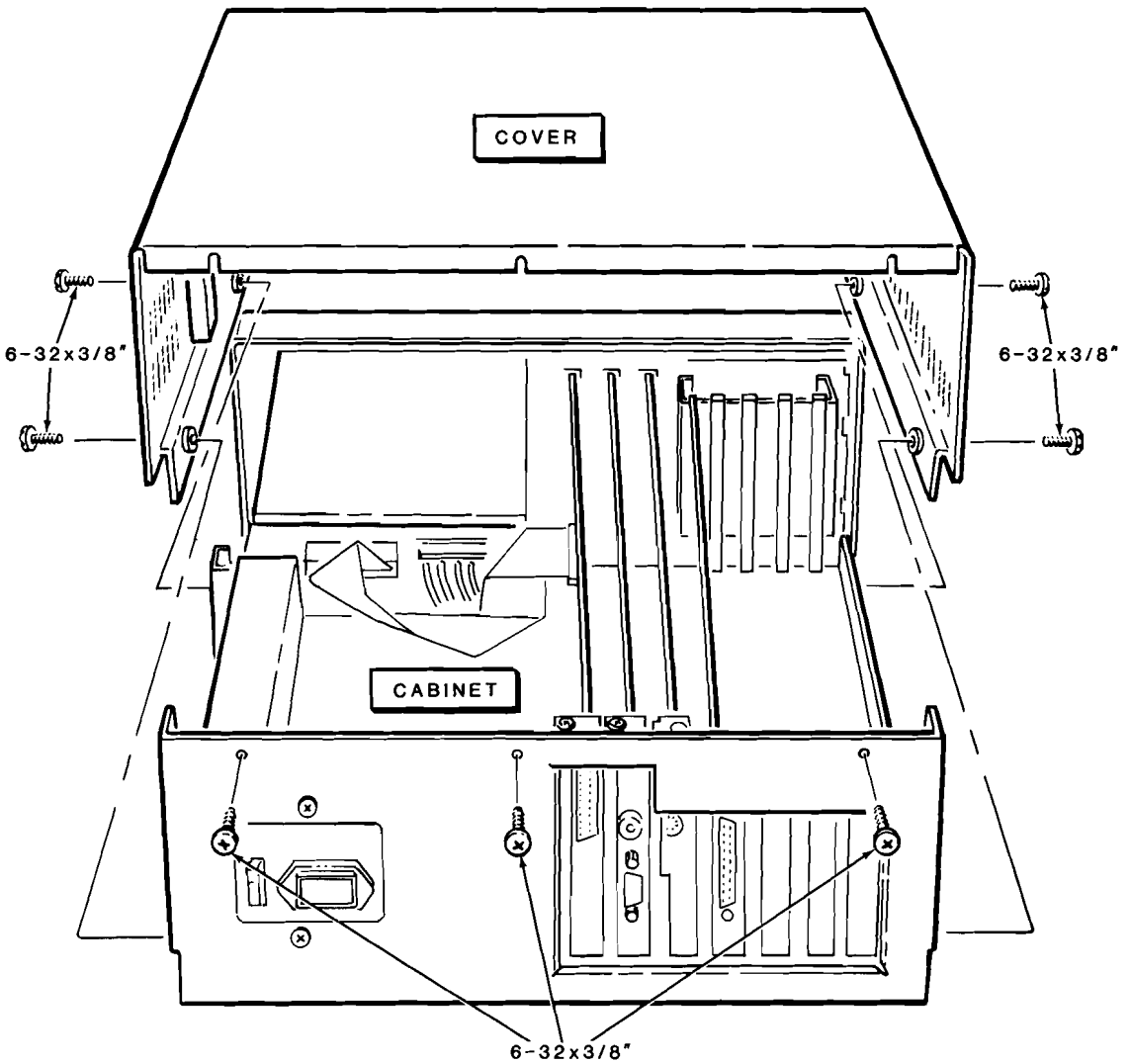


Figure 2.10. Z-150 Reassembly

IBM PC Computer

Disassembly

CAUTION: Check to make sure the power is off before proceeding. Installing components into the computer with the power on can damage the system.

- Switch off the unit, and disconnect the power cord and all peripherals from electrical power.
- Remove the screws from the back panel of the computer (there are four screws on the PC-2 and PC-XT models, one in each back corner, and two screws in the PC-1, located in the lower-back corners).
- Slide the cover toward the front until it will go no further (Figure 2.11).
- Carefully lift the cover off the computer.

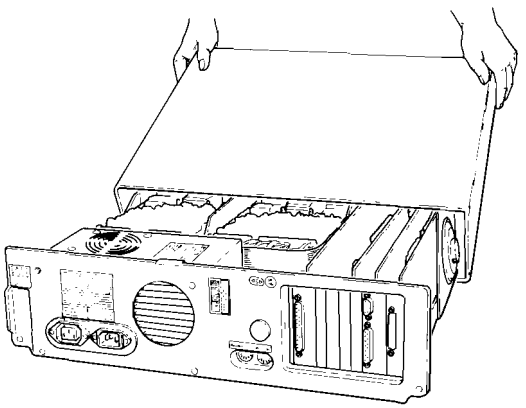


Figure 2.11. IBM PC Cover Removal

Configuration

Simplified Configuration

Position the Z-329 Card as shown in Figure 2.12. All jumpers should be installed as shown in the figure. These jumper positions are detailed below:

- ☐ The two RAM size jumpers (J6 and J7) should be in the 2K position.
- ☐ The video control jumpers (J2, J3, and J4) all should be in the positive (POS) position.
- ☐ Vertical sync jumper J1 should be in the negative (NEG) position.
- ☐ ROM size jumper J5 should be in the 64K position.

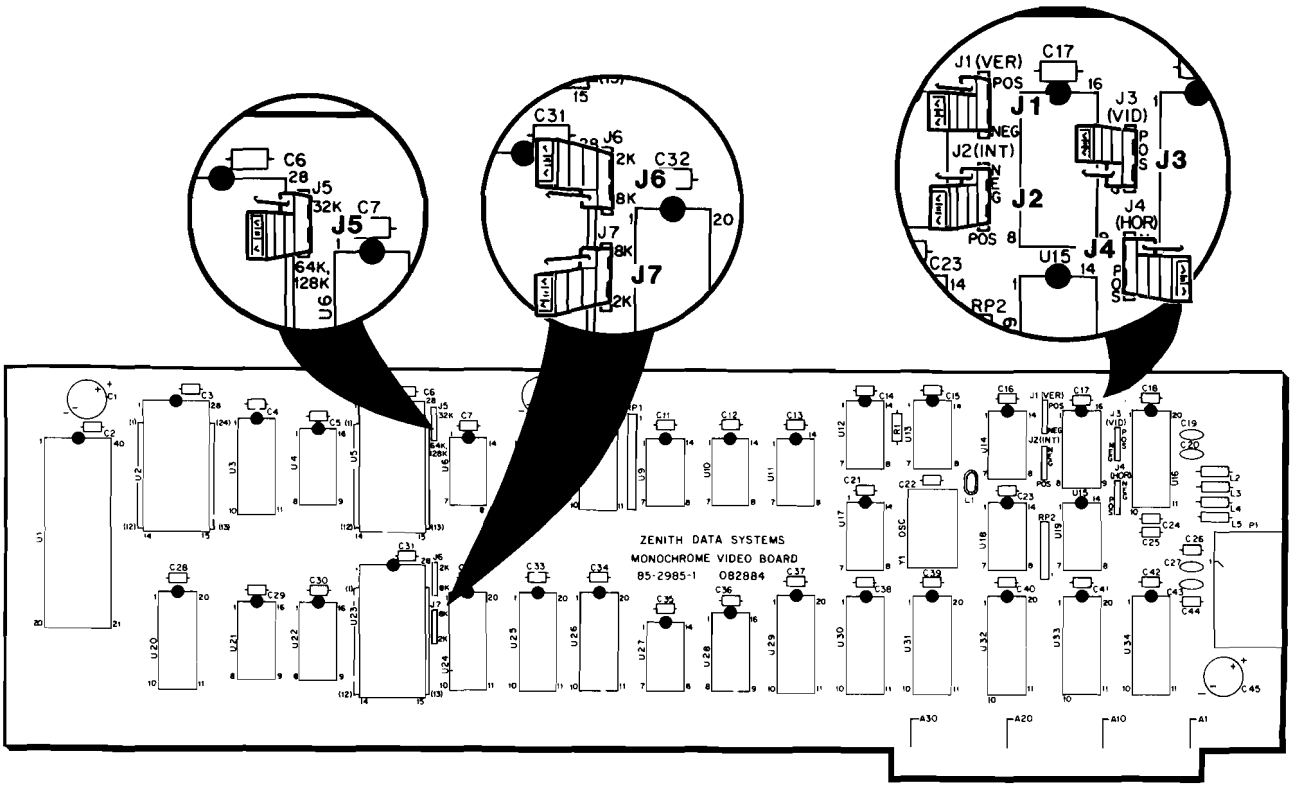


Figure 2.12. Z-329 Component Layout

Detailed Configuration

- Jumpers J6 and J7 are used to "size" the RAM chips on the Z-329 Card. The card is shipped with 2K × 8 static RAM ICs installed. It is possible to install 8K × 8 static RAM ICs. When this is done, these jumpers must be moved to the 8K position.

- Jumper J5 is used to "size" the ROM chips on the Z-329 Card. The card is shipped with a 4K × 8 ROM IC installed. It is possible to install 8K × 8 or 16K × 8 ROM ICs. When this is done, J5 must be moved to the position corresponding to the size of the ROM installed.

- Jumper J3 controls the polarity of the video data. When this jumper is in the POS position, +5 VDC is used to light a pixel and ground drives dark pixels. When this jumper is in the NEG position, ground is supplied to the monitor for all lighted pixels and +5 VDC is used for dark pixels.

- Jumper J2 controls the polarity of the intensity signal. In the POS position, an intensified character is signified by a logic high and a standard display by a ground. In the NEG position, logic high is used for the standard display and intensified characters are created by a ground.

- Jumper J4 controls the polarity of the horizontal sync. In the POS position the sync pulses are positive-going. In the NEG position the pulses are negative-going.

- Jumper J1 controls the polarity of the vertical sync. In the POS position the sync pulses are positive-going. In the NEG position the pulses are negative-going.

System Board Switch Settings

Sections 5 and 6 of switch 1 on the system board control which video format is used. In order for the Z-329 Card to operate, these switch sections must be in the proper position.

Figure 2.13 illustrates the location of switch 1 on the system board. Both sections 5 and 6 must be in the OFF position. Move the switches if necessary.

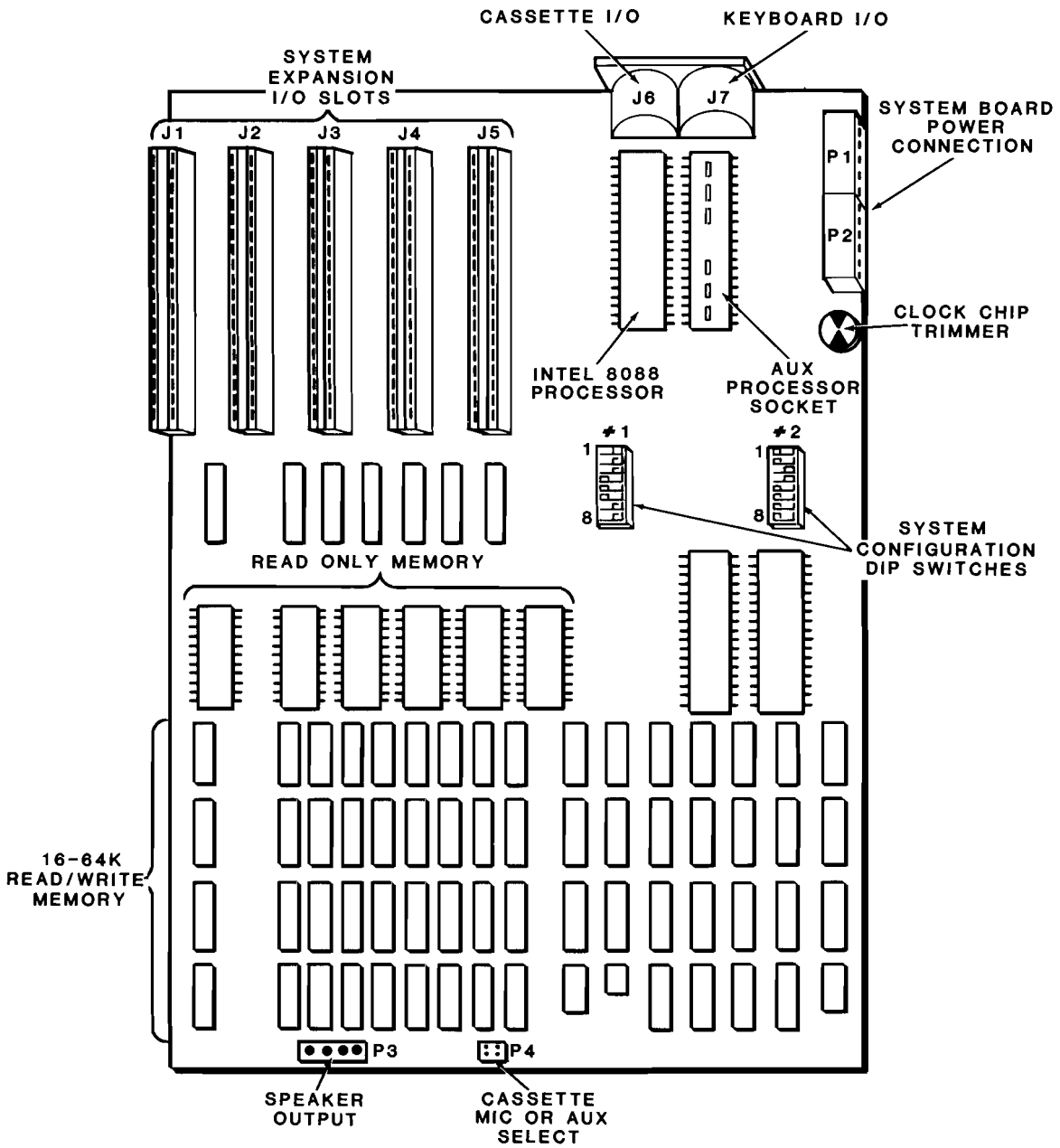


Figure 2.13. IBM System Board Component Layout

Installation of Video Card

- The new Z-329 Video Card may be installed in any unused expansion slot. Select any available slot (Figure 2.14).

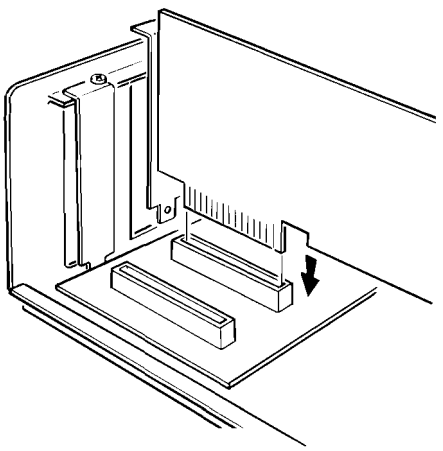


Figure 2.14. IBM PC Cabinet

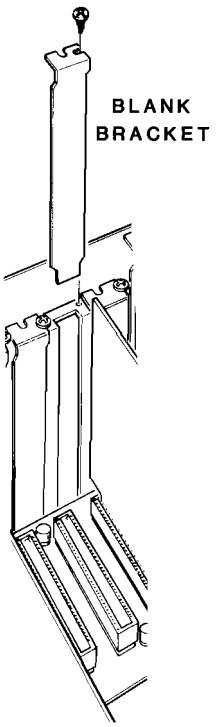


Figure 2.15. Blank Bracket

- Remove and save the blank bracket screw (Figure 2.15) from the blank bracket and then remove and discard the blank bracket.

Install the card as follows:

- Align the front edge of the card in the card guide.
- Insert the card into the card guide.
- Line up the card edge-connector with the backplane connector.
- Gently, but firmly push the card into the backplane connector until the card is fully inserted.
- Secure the card to the back of the computer with the screw removed from the blank bracket.

Reassembly

- Carefully place the cover in position (Figure 2.16).
- Slide the cover toward the back until it will go no further.
- Install the screws into the back panel of the computer (there are four screws on the PC-2 and PC-XT models, one in each back corner, and two screws in the PC-1, located in the lower-back corners).

Proceed to the checkout procedure.

Checkout

☐ Connect a monitor to the output from the Z-329 Card.

☐ Connect the computer and monitor to electrical power, and switch both units on.

☐ Load the system by booting the computer.

☐ A blinking cursor (or other messages, depending on the program used) should be displayed on the monitor. This signifies that the CRTC and most of the circuitry is operating correctly.

☐ Switch off the power to the computer and remove the power plug from the electrical outlet.

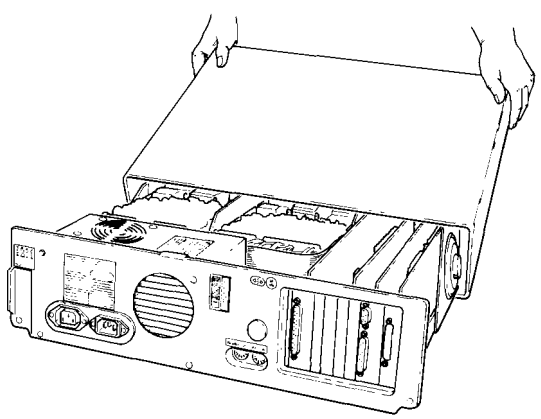


Figure 2.16. IBM PC Cover Installation

Chapter 3

General Theory of Operation

The Z-329 Monochrome Video Card produces 25 rows of 80 characters. The computer system transfers alphanumeric characters to the Z-329 Card in ASCII code. The character and an attribute byte are stored in the RAM on the Z-329 Card. When the character is to be displayed, the CRTC addresses the memory and a character ROM decodes the ASCII data into pixel lighting instructions.

Memory Organization

RAM

The memory supplied on the Z-329 consists of two 2K × 8 static RAMs. One RAM IC is used to store the character in ASCII code and the other stores the attribute associated with this character. The standard memory allows one page of text to be stored. The memory is arranged linearly (characters are stored sequentially in order of use) with no unused memory.

Optional 8K × 8 static RAMs may be installed, giving the Z-329 Card the capability of addressing up to two pages of text with an interlaced display.

The CPU addresses the RAM beginning at location B0000. The A0 bit is used to enable either the display RAM or the attribute RAM. This causes the display to be addressed using even numbers and the attribute RAM to be addressed with odd numbers. Example addresses are shown in Table 3.1.

Table 3.1. Character/Attribute Addressing

DISPLAY LOCATION	CHARACTER ADDRESS	ATTRIBUTE ADDRESS
1	B0000	B0001
2	B0002	B0003
3	B0004	B0005
4	B0006	B0007
-	—	—
80 (last in line 1)	B00A0	B00A1
81 (1st in line 2)	B00A2	B00A3
-	—	—
1975 (1st in line 25)	B0F5E	B0F5F
2000 (last on page)	B0FA0	B0FA1

Character ROM

The character ROM installed on the card at the factory is an 8K × 8 ROM which provides decoding of the ASCII code stored in the RAM into pixel on/off instructions. The standard ROM provides decoding for two 256 character fonts. An optional 16K × 8 ROM may be used to provide up to four fonts. The font in use is software selectable.

Character Generation

An alphanumeric character is generated by a matrix of pixels located inside a 9 × 14 field of pixels. Unused columns and rows provide spacing between the characters. Figure 3.1 shows the organization of the standard numeric character 7. The addresses are shown to indicate the bytes required to generate the number.

The character ROM generates the pixel lighting data based on the character stored in RAM and the address from the CRTC. Different fonts are possible by changing the character ROM. A second unsupported font may be contained on the standard ROM; this font may be addressed by changing bits 6 and 7 of the control register.

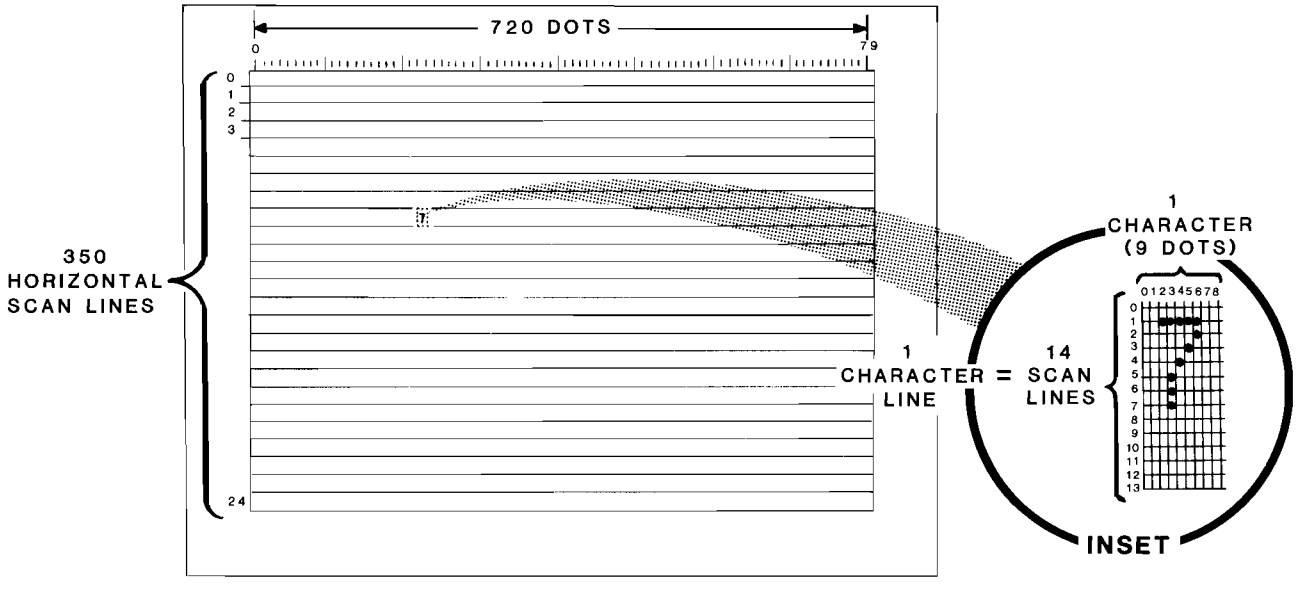


Figure 3.1. Character Generation

CRTC Addressing

The CRTC addresses the RAM and the character ROM using a character/line format. When the computer is turned on, the CPU initializes the CRTC's internal registers that define the number of characters in a line and the number of scan lines used to generate a character. In the Z-100 PC Series Computer, the character row is defined to be 80 characters long.

The CRTC increments the character address by one (1) each time the memory is addressed until character 80 is reached. The line address is then incremented by 1 and the character address is reset to 0. Note that the RAM is addressed by the character address and not by the line address. The character ROM is addressed by the output of the RAM (ASCII) and the line address.

Data Management

CRTC

The CRTC is the "manager" of the display and as such has priority over the CPU in accessing the RAM. The CRTC cannot write to the RAM, but controls the transfer from the RAM to the monitor. The CPU is allowed to write to the RAM (or read it) between the character display times of the CRTC. The CPU can, therefore, only access the RAM once every 512 nanoseconds.

The CRTC addresses a byte of data from the display RAM which is used to address the font ROM. Font ROM data is transferred into a parallel-in/serial-out shift register. The attribute byte is read by the decoder at the same time. The display data is shifted out of the register serially so that the data is presented to the monitor one bit at a time. The attribute byte is latched in a register and is present while all bits of the display data are shifted to the monitor. When all eight bits of the display data have been sent to the monitor, the next display and attribute bytes are transferred to the registers. The ninth bit of the display is controlled by external logic.

CPU Memory Access

The CPU cannot interfere with the transfer of data from the RAM to the registers (CRTC control), but must write all of the data into the RAM. The CPU is allowed access to the RAM for 245 nanoseconds of each 512 nanosecond access period. During this time, the CPU can write one byte of data into one of the RAMs. This means that to fill the screen, the CPU must write into the RAM 4000 times (80 character bytes and 80 attribute bytes by 25 lines).

To clear the screen, the CPU must write zeros to all attribute RAM locations. To scroll the screen, all data must be moved up one line position so that new data can be written to the last line.

CRTC Registers

The CRTC manages the memory and controls the display. The action of the CRTC is controlled by its 18 internal registers. All CRTC internal registers are set by the CPU at power up.

The internal registers are:

- **Address Register (AR)**—This 5-bit register is used to address the 18 internal registers. To gain access to any of the 18 registers, you must first write the number of the register (R0 through R17) to be modified into this register. If you write an address of 18 to 31, no register will be addressed.

- **Horizontal Total Register (R0)**—This 8-bit, write-only register sets the time (number of characters) between the starting points of character rows. This time, defined in character clock periods, includes all characters in a row, the delay before the horizontal sync pulse, the width of the sync pulse, and the retrace time. Since the first character is zero (0), you must enter the number of character clock signals you want minus 1. For instance, if you enter 112, there will be 113 character positions between the start of any 2 consecutive rows. The default value is 61H or 97 decimal.

- **Horizontal Displayed Register (R1)**—This 8-bit, write-only register selects the number of characters in each row that will be displayed on the screen. In normal operation, this register should contain the value 50H or 80 decimal.

- **Horizontal Sync Position Register (R2)**—This 8-bit, write-only register determines the position of the sync pulse in each scan line. Any value greater than the value stored in the horizontal displayed register (R1) and less than the value stored in the horizontal total register (R0) may be used. When the value programmed in R2 is increased, the display shifts to the left. When the value is decreased, the display shifts to the right. The default value is 52H or 82 decimal.

- **Sync Width Register (R3)**—This 8-bit, write-only register sets the pulse width of the sync pulse. The horizontal sync is controlled by the lower 4 bits, and the pulse width of the vertical sync by the upper 4 bits. Increasing this value lengthens the pulse. The default value is 0FH or 15 decimal.

NOTE: The sum of R1 + R2 + R3 must be less than or equal to the value in R0.

- **Vertical Total Register (R4)**—This 7-bit, write-only register and R5 are used to determine the refresh rate of the video monitor and the vertical retrace timing. This value is expressed in character rows (normally 14 scan lines). These values are based on a horizontal rate of 18,432 scan lines per second and are determined by the formula:

  value = horizontal scan lines per second/refresh rate × 1/scan lines per character.

NOTE: The scan rate of the monitor cannot refresh the display faster than 50 Hz.

Example for 50 Hz:

18,432/50 = 368.64 scan lines per frame
368.64/14 = 26.33
Note that the result of the above division is 26 with a remainder of 3.
Enter 25 (one less than the number desired) into register R4.

- **Vertical Total Adjust Register (R5)**—This 5-bit, write-only register is used to lengthen the vertical total time to account for the scan lines remaining when the value for R4 was determined. This value is expressed in scan lines. The correct value is 6 (06H).

- **Vertical Displayed Register (R6)**—This 7-bit, write-only register determines the number of character rows which will be displayed. This value cannot exceed, but may be equal to or less than, the value in R4. The default value is 19H (25 decimal).

- **Vertical Position Register (R7)**—This 7-bit, write-only register controls the position of the vertical sync expressed in character rows. This value should be less than or equal to the value of R4. Entering a lower number will move the display downward, higher values move the display upward. The default value is 19H (25 decimal).

NOTE: The illustrations on this page depict typical operation and not the actual display from the Z-329 Card.

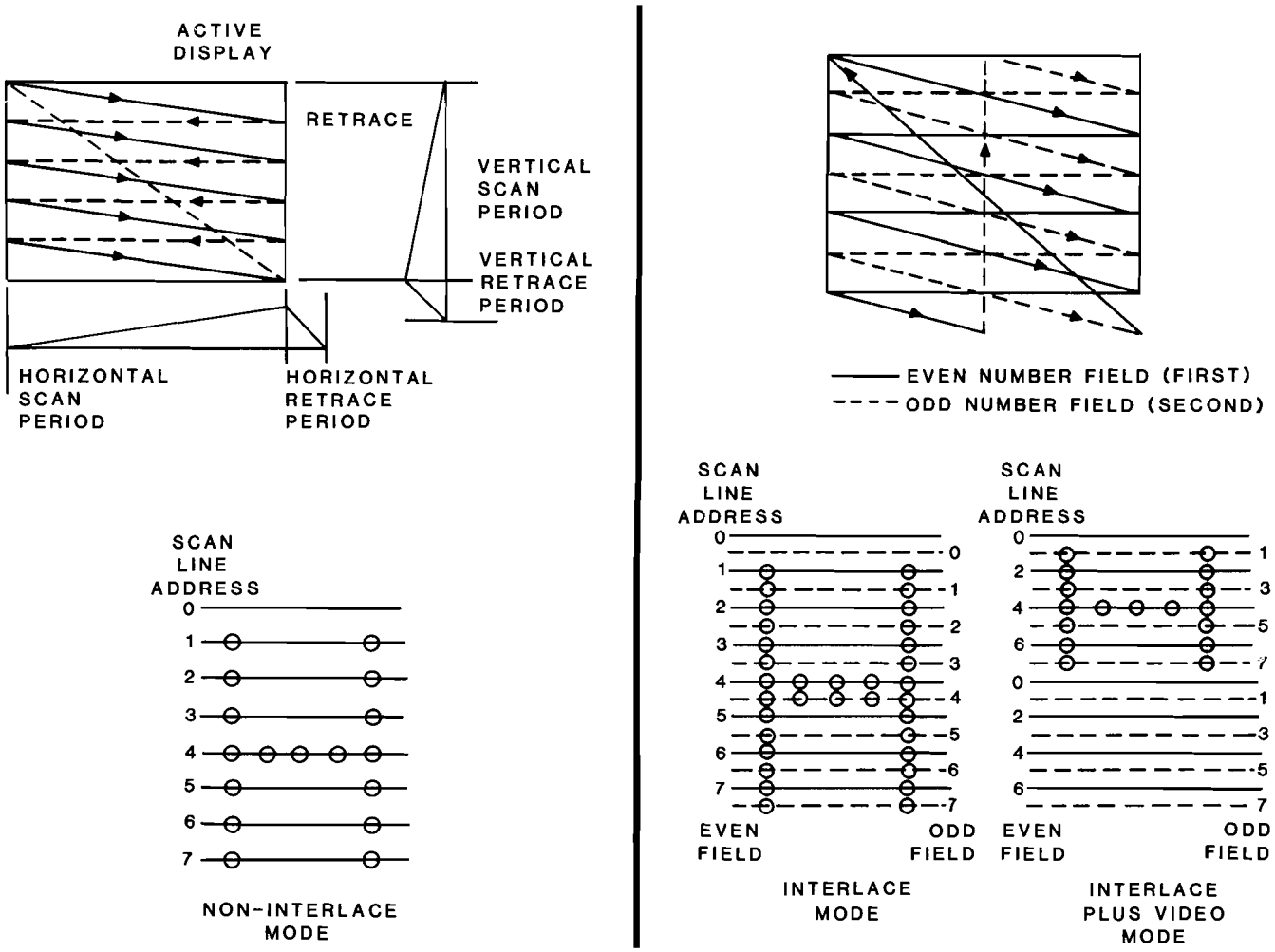


Figure 3.2. Interlace/Non-Interlace Modes

- **Interlace Mode and Skew Register (R8)**—This write-only register is used to control the interlace (2 modes) or non-interlace mode of the display (Figure 3.2), and the display enable offset (skew or delay) of the pixels. The mode is controlled by the 2 low-order bits, as shown in Table 3.2. The Z-329 Card normally is operated in the non-interlace mode. Bits 4 and 5 control the skew (delay) of the characters, and bits 6 and 7 control the skew of the cursor. Tables 3.3 and 3.4 define the function of these bits. The default value for this register is 02H (2 decimal).

Table 3.2. Interlace Mode Register

BIT 1	BIT 2	MODE
0	0	Normal sync mode (non-interlaced)
1	0	Normal sync mode (non-interlaced)
0	1	Interlace sync mode
1	1	Interlace sync and video mode

Table 3.3. Character Skew (Delay) Control

BIT 5	BIT 4	MODE
0	0	No character skew
0	1	1 character skew
1	0	2 character skew
1	1	Not available

Table 3.4. Cursor Skew (Delay) Control

BIT 7	BIT 6	SKEW
0	0	No character skew
0	1	1 character skew
1	0	2 character skew
1	1	Not available

- **Maximum Scan Line Address Register (R9)**—This 5-bit, write-only register controls the number of scan lines per character row. Since the first scan line is 0, the value you enter (15 maximum) must be 1 less than the number of scan lines used for each character. For example, for 9 scan lines per character, you would enter 8 (9 minus 1). The normal value for this register is 13 (14 scan lines). The default value for this register is 0DH (13 decimal).

- **Cursor Start Register (R10)**—This 7 bit, write-only register is used to define the beginning position of the cursor within the character field (scan line 0–15) and the blink rate of the cursor. The 5 low-order bits define the beginning scan line of the cursor. The size of the cursor is defined by both this data and R11. The high-order bits determine the blink rate of the cursor as shown in Table 3.5. The default value for this register is 0BH (11 decimal).

Table 3.5. Cursor Start Register

BIT 6	BIT 5	CURSOR DISPLAY MODE
0	0	Cursor on steady (used on this card)
0	1	No cursor is displayed
1	0	Cursor blinks at about a 4 Hz rate
1	1	Cursor blinks at about a 2 Hz rate

- **Cursor End Register (R11)**—This 5-bit, write-only register defines the last scan line occupied by the cursor. If you want a cursor to occupy the full character field, set the lower 5 bits of R10 to scan line 0, and R11 register to scan line 14 (14th line). Similarly, if a single line of the character space is to be used, both R10 and R11 would be set to the same scan line number. The default value for this register is 0CH (12H).

- **Start Address Registers (R12 and R13)**—These read/write registers contain the first address in RAM to be displayed (top-left corner of the display). If the optional 8K × 8 RAM chips are installed, this register can be used by the CPU to scroll the display. When the standard RAM is used, the bottom of the display is not addressable if this value is changed. R12 is the 6-bit, high-order address, and R13 is the 8-bit, low-order address.

- **Cursor Registers (R14 and R15)**—These read/write registers determine location of the cursor. Register R14 contains the 6-bit, high-order address, and R15 contains the 8-bit, low-order address.

- **Light Pen Registers (R16 and R17)**—These read-only registers locate the light pen strike. The Z-329 Card does not support this feature.

Chapter 4

Software Considerations

The Control Register

The control register provides a number of functions for the Z-329 Card. This register enables the CPU to communicate with the display RAM and attribute RAM, enables video data to be sent to the monitor, selects the font which is used, enables the blink attribute, and allows paging of the display when the optional 8K × 8 RAMs are installed.

To control all of these functions, a single 8-bit byte is written into the control register. The control register is located at I/O port 3B8H. The function of each bit is shown in Table 4.1.

Table 4.1. Video Control Register Functions

BIT NUMBER	SIGNAL NAME	BIT VALUE	FUNCTION
DB0	BRDEN	0	Prevents communication between the CPU and the display or attribute RAM. Data stored in RAM is displayed (if VIDEN is enabled) but cannot be changed.
		1	Enables communication between the CPU and the RAM. Data stored in RAM is displayed (if VIDEN is enabled). The RAM can be written to or read by the CPU.
DB1		X	Not used.
DB2		X	Not used.
DB3	VIDEN	0	Disables the display. The data stored in the display or attribute RAM is not changed but is not displayed. The RAM can be addressed by the CPU when the display is in this state (if the board is enabled).
		1	The display is enabled. Data stored in the display and attribute RAM is displayed.

Table 4.1 (continued). Video Control Register Functions

BIT NUMBER	SIGNAL NAME	BIT VALUE	FUNCTION
DB4	PAGE	0	This allows the first page of memory to be displayed.
		1	Pages the display to the second page of the display. This feature can be used only if the optional 8K × 8 RAMs are installed.
DB5	BLKEN	0	This allows the blink attribute bit in the attribute RAM to control the background intensity of the display.
		1	This allows the blink attribute bit to control the blinking of the character.
DB6/DB7	FONT 0/ FONT 1	X	These bits control the font in use FONT 1 by the display. The font selection follows a standard binary count (00 = font 0, 01 = font 1, 10 = font 2, 11 = font 3). Fonts 2 and 3 can be used only if the optional 128K ROM is installed.

To initialize the card, write the bits 0001XX1 into I/O port 3B8.

Writing Data to the Z-329 Card

NOTE: Bit 0 in the control register must be 1 to enable the write function. Before attempting to write to the memory, be sure this bit is properly set.

The display is treated by the CPU as RAM. The text and control data is written into the RAM on the Z-329 Card. The CRTC and hardware on the card manage the display. The programmer has a number of options in the way that data can be handled.

The programmer can alternately write data and control bytes to the display and attribute RAM, or fill the data into the display RAM and then fill the attribute RAM. The display RAM is enabled by a low on the CPU's A0 address line, causing all display RAM addresses to be even numbers. The attribute RAM is enabled by a high on the CPU's A0 address line so that all attribute addresses are odd numbers. The addresses are shown in Table 4.2.

Table 4.2. Character/Attribute Addressing

DISPLAY LOCATION	CHARACTER ADDRESS	ATTRIBUTE ADDRESS
1	B0000	B0001
2	B0002	B0003
3	B0004	B0005
4	B0006	B0007
-	—	—
80 (last in line 1)	B00A0	B00A1
81 (1st in line 2)	B00A2	B00A3
-	—	—
1975 (1st in line 25)	B0F5E	B0F5F
2000 (last on page)	B0FA0	B0FA1

In most cases, the attributes are changed in blocks. This means that the same attribute code is entered repetitively until the end of the block is reached. When whole blocks of data are moved to the screen, it may be faster to enter all of the characters and then the attributes. In cases where single characters are entered from the keyboard, it may be easier to enter the character and then the attribute.

Attribute Codes

The 8 bits of data stored in the attribute RAM are used to control the display of each character in the display. Six functions are available for each character and selected by the data in the attribute RAM. These functions are shown in Table 4.3, along with the code that generates them. In order to blink the character, the blink enable bit in the control register must be set as described earlier in this chapter.

Table 4.3. Attribute Codes

FUNCTION	ATTRIBUTE DATA BITS 7	6	5	4	3	2	1	0	CONTROL REGISTER DATA BIT 3
Not displayed	0	0	0	0	0	0	0	0	x
Intensify background	1	x	x	x	x	x	x	x	0
Blink	1	x	x	x	x	x	x	x	1
Underline	x	x	x	x	x	0	0	1	x
Intensify foreground	x	x	x	x	1	x	x	x	x
Reverse video	x	1	1	1	x	0	0	0	x

× = value does not affect attribute

Cursor Control

The cursor is generated by the CRTC. The current location of the cursor can be determined by reading the contents of CRTC registers R14 and R15. The cursor can be moved by writing a new location into the registers.

The value returned from this register will not be the same as the address the CPU uses to address the identical display location. The CPU must address the display and attribute memories at different locations. The CRTC addresses them at the same time. Bit 0 of the CPU address is used to select which of the two memories is being talked to. Since the CRTC addresses the two RAMs at the same time, there is no corresponding bit 0. Character address bit 0 from the CRTC is the same as address bit 1 from the CPU. The relationship of the addresses is such that the address from the CRTC registers must be shifted left one position to make them agree.

To reposition the cursor, do the following:

1. Determine the location you want the cursor to move to.

2. Write 0EH into I/O address 3B4H to address the high-order cursor address (CRTC index register R0).

3. Write the high-order value of the cursor address to I/O address 3B5H. Remember that the CRTC address is shifted to the right one position from the CPU address.

4. Write 0FH into I/O address 3B4H to address the low-order cursor address register (CRTC register R15).

5. Write the low-order address of the cursor to I/O address 3B5H.

Blanking/Clearing the Display

Blanking the display means that the characters stored in the character memory are not displayed on the CRT. The memory is not affected and can be read or changed while the screen is blanked. The display is cleared when all data stored in the RAM is erased.

The display is blanked through the video control register. To blank the display, write XXXX 0XX1 (for example, 01H) to I/O address 3B8H. No characters will be displayed on the CRT but the RAM may be changed at this time.

The display is cleared by writing 0s to all RAM locations.

Scrolling the Display

When the standard 2K × 8 RAMs are installed, the display must be scrolled by manipulating the data in the RAM. To scroll the display with the standard RAM, data from location 81 must be moved to location 1, etc. When the optional 8K × 8 RAM is installed, the programmer can use the flexibility of the 6845 CRTC to scroll the display.

With the optional RAM installed, the starting point of the display can be moved to a new location in the RAM without changing the RAM. This is done by writing 0CH into I/O address 3B4H to prepare the high-order register in the 6845 to accept data. Then write the high-order location to I/O address 3B5. The next step is to write 0DH to I/O address 3B4H and then the low-order location into I/O address 3B5H. The top-left corner of the display will now be the address specified. The programmer must exercise caution when addressing starting locations beyond the first page so that no addresses beyond the capability of the RAM are used at the end of the page.

Paging the Display

The standard RAM contains only enough memory to display one page of text. The optional RAM can display four pages of standard text or two pages in the interlace mode (the interlace mode cannot be used with standard memory). With the optional RAM, the programmer can page in one of two ways: using the CRTC address registers as described for scrolling (enter an address one page higher than the current address instead of one line higher), or through the video control register.

To use the video control register to page the text, write a 1 into bit 4 of the byte at I/O address 3B8H. Be careful not to change the other bits of this byte when using this procedure.

Character Font

The character font which is supported is shown in Table 4.4. The keycodes or data used to generate these symbols also are shown in Table 4.4.

Table 4.4. Character Font

DECIMAL VALUE	➡	0	16	32	48	64	80	96	112
⬇	HEXA-DECIMAL VALUE	0	1	2	3	4	5	6	7
0	0	BLANK (NULL)	►	BLANK (SPACE)	0	@	P	‘	p
1	1	☺	◄	!	1	A	Q	a	q
2	2	☻	↕	"	2	B	R	b	r
3	3	♥	!!	#	3	C	S	c	s
4	4	♦	¶	$	4	D	T	d	t
5	5	♣	§	%	5	E	U	e	u
6	6	♠	▬	&	6	F	V	f	v
7	7	•	↨	’	7	G	W	g	w
8	8	◘	↑	(	8	H	X	h	x
9	9	○	↓	)	9	I	Y	i	y
10	A	◙	→	*	:	J	Z	j	x
11	B	♂	←	+	;	K	[	k	{
12	C	♀	∟	,	<	L	\	l	¦
13	D	♪	↔	—	=	M	]	m	}
14	E	♫	▲	.	>	N	^	n	~
15	F	☼	▼	/	?	O	_	o	△

DECIMAL VALUE	➡	128	144	160	176	192	208	224	240
⬇	HEXA-DECIMAL VALUE	8	9	A	B	C	D	E	F
0	0	Ç	É	á				∝	≡
1	1	ü	Æ	í				β	±
2	2	é	FE	ó				γ	≥
3	3	â	ô	ú				π	≤
4	4	ä	ö	ñ				Σ	⌠
5	5	à	ò	Ñ				σ	⌡
6	6	å	û	a				μ	÷
7	7	ç	ù	o				τ	≈
8	8	ê	ÿ	¿				Φ	°
9	9	ë	Ö	⌐				⊖	•
10	A	è	Ü	¬				Ω	•
11	B	ï	¢	½				δ	√
12	C	î	£	¼				∞	η
13	D	ì	¥	¡				∅	2
14	E	Ä	Pts	«				∈	■
15	F	Å	f	»				∩	BLANK 'FF'

Status Register

The status register is a 4-bit, read-only register located at I/O port 3BAH. Bit 0 is the horizontal drive signal, bits 1 and 2 are the font number in use, and bit 3 is the video data. The programmer can look at bits 1 and 2 for font information and can use bits 0 and 3 for diagnostics, but data bits 0 and 3 are read "on the fly". These data bits may not meet the timing requirements to be read properly.

Quick Reference Charts

The following tables give the addresses and default values for the registers accessible to the programmer. Table 4.5 shows all the addresses which can be written to or read from and their use. Table 4.6 shows the CRTC registers and their default values.

Table 4.5. Register Addresses

I/O ADDRESS	FUNCTION	DESCRIPTION
3B4	CRTC Index Register	Used to select a CRTC register to write to. This register must be written to before data can be entered into the CRTC registers.
3B5	CRTC Data Register	Data written into this register is loaded into the CRTC register selected by writing into address 3B4.
3B8	CRT Control Register	This register controls the functions of the card including communication, video display, the page of the display, blink enable, and font selection. The function of these bits is shown in Table 4.1.
3BA	CRT Status Port	This port allows the programmer to look at the font selected, the video data, and the horizontal sync.

Table 4.6. CRTC Registers and Default Values

REGISTER #	REGISTER FILE	PROGRAM UNIT	80 × 25 MONOCHROME
R0	Horizontal Total	Characters	61H
R1	Horizontal Displayed	Characters	50H
R2	HSYNC Position	Characters	52H
R3	HSYNC Width	Characters	FH
R4	Vertical Total	Char Rows	19H
R5	VTOTAL Adjust	Scan Line	6H
R6	Vertical Displayed	Char Row	19H
R7	VSYNC Position	Char Row	19H
R8	Interlace Mode	—	02
R9	Max Scan Line Address	Scan Line	DH
R10	Cursor Start	Scan Line	BH
R11	Cursor End	Scan Line	CH
R12	Start Address (H)	—	00H
R13	Start Address (L)	—	00H
R14	Cursor (H)	—	00H
R15	Cursor (L)	—	00H
R16	Reserved	—	—
R17	Reserved	—	—

Chapter 5

Card/Circuit Description

This chapter describes the Z-329 Card from a hardware viewpoint. The components on the card and the operation of the circuit are described.

The Z-329 Monochrome Video Card produces 25 rows of 80 characters. The computer system transfers alphanumeric characters to the Z-329 Card in ASCII code. The character and an attribute byte are stored in the RAM on the Z-329 Card. When the character is to be displayed, the CRTC addresses the memory and a character ROM decodes the ASCII data into pixel lighting instructions.

Block Diagram

Figure 5.1 illustrates the block diagram of the Z-329 Card. Refer to this illustration for the following discussion.

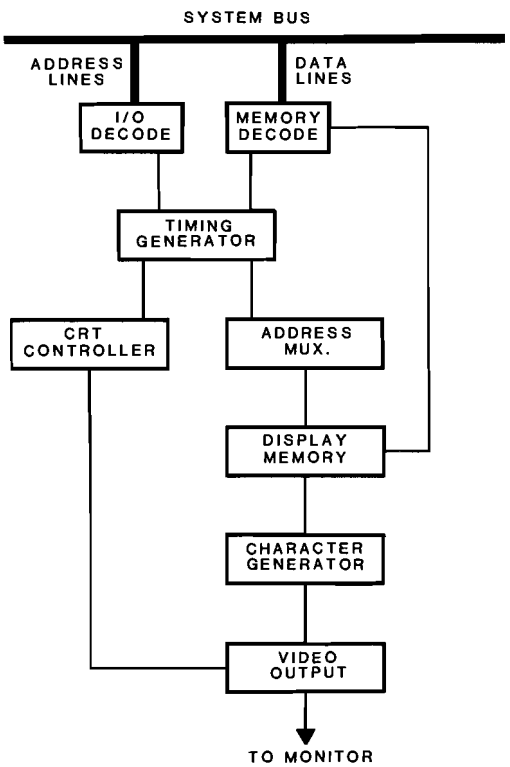


Figure 5.1. Z-329 Card Block Diagram

Card/Circuit Description

I/O Decode—The I/O decode circuit receives the incoming address from the CPU and decides if any part of the card is being addressed. This circuit enables the devices on the card which the CPU wishes to control.

Memory Decode—The memory decode circuit determines when the RAM on the Z-329 Card is being addressed, converts the bus signals into the correct logic for the RAM, and addresses the memory.

Timing Generator—The timing generator circuit controls arbitration of the memory so that only the CPU or the CRTC can access the memory at any time. This circuit also provides the proper timing of the transfer of data to and from RAM and to the video output.

CRTC—The CRTC provides the sync pulses for the monitor and address information to the RAMs during video cycles. The internal registers of the CRTC can be addressed to provide a number of functions.

Address Mux—The address mux (multiplexer) controls which device, the CPU or the CRTC, is in control of addressing the RAM.

Display Memory—These static RAMs are used to store the characters which are to be displayed on the CRT and the associated attribute. The standard memory devices are 2K $\times$ 8 but 8K $\times$ 8 ICs can be installed.

Character Generator—The character generator is a ROM. This device contains the font for the display memory. The data in the display memory is converted into pixel drive data by this device.

Video Output—The video output devices convert the parallel data from the character generator into serial data to drive a TTL input video monitor.

Circuit Description

Function and Timing Decoding

PAL U31, PAL U32, and PAL U26 provide decoding for most of the communication between the CPU, the CRTC, and the RAM. The inputs of U31 and U32 are connected to the CPU's control and address busses.

U31 decodes the incoming I/O addresses and I/O operations from the CPU and determines when one of the components on the card is being addressed. Based on the address and the states of the control signals, the read or write pulses are generated for the card.

U32 provides the system timing and decodes the video memory space. The /VIDEO output from this device is the character clock and has a 553 nanosecond period. This signal is used to control access to the display RAM. When this signal is low, the multiplexer connects the addresses from the 6845 to the RAM. When the /VIDEO signal is high, the CPU addresses are connected to the RAM. CRTC (6845) access time is 308 nanoseconds and CPU access time is 245 nanoseconds. When the CPU requests a memory access, U32 pulls the IOCHRDY (I/O Channel Ready) signal to the wait state, and then synchronizes the CPU access of the RAM to the correct time period. Because the CPU may not be done reading the data when the CRTC time slot occurs, the data from the RAM is latched into octal D latch U34 by the /DISCPU signal from U32.

The timing is provided by oscillator Y1 and U32. The output frequency from Y1 is 16.257 MHz. This signal is buffered by one NAND gate in U18. The output from U18 drives the clock input to U32 and is supplied to the shift register which converts the data bytes into pixel data (DOTCLK). Pins 13 (Q0) and 14 (Q1) of U32 provide a divide by 8 function for video timing (character clock). Both of these outputs are at a frequency of 2.0321 MHz, but the rising edge of Q1 is delayed 1 DOTCLK pulse from the rising edge of Q0.

Data Bus Communication

The CPU can read or write to the 6845 CRTC (U1), the character RAM (U2), or the attribute RAM (U23). The CPU can write only to the control register. The CPU can read only the status register. These functions are described in the following paragraphs.

The CPU data bus enters the card on backplane connector pins A2 through A9 (D7–D0). U33 is a 3-state buffer for the incoming data and U34 latches the data from the card onto the backplane bus.

The /WRITE signal from U31 enables the output from U33, allowing data from the CPU to enter the card when one of the devices on the card is addressed.

The /DISCPU signal (from U32) latches data from the card into U34 and the /READ signal (from U31) enables the output, allowing data to be sent to the CPU.

The 6845 CRTC (U1) has the most complex read/write procedure of all the devices on the monochrome video card because it requires one write cycle to address the register and a second cycle to actually write or read the register. Pin 25 (CS) must be brought high (/3BL from U31) to enable the data buffer in the chip, and pin 23 (E) also must be brought high to enable the registers (I/O from U31). The next process is for the CPU to select one of the registers. This is done by placing a low on pin 24 (RS) to select the desired register. This low is the A0 line from the CPU. The number of the register to be read from or written to is then presented on the data lines and the R/W* line is pulsed low. The selected register can now be addressed. The procedure is similar to the select procedure except that the A0 line (pin 24) is brought high to address the register.

CPU access to the RAM is less complicated, but requires that the CPU wait for the correct time to access the RAM. When the CPU wishes to write to (or read from) the RAM, the /BUSREQ signal from U31 places the CPU in a WAIT state. When the access time arrives, the /RDY signal from U32 cancels the WAIT. The address is allowed to connect to the RAMs through the 3 multiplexers (U4, U21, and U22). Which of the two RAMs is being addressed is determined by the A0 line. The output enable and write enable signals for the RAMs are generated by PAL U26. The CPU data bus is separated from the RAM data busses by octal transceivers U20 and U24. The enabling and direction of these transceivers are also controlled by signals from U26. The states of the transceivers are shown in Table 5.1. When a write function is done, U26 generates the write logic to the selected RAM. When a read function is performed, the data is latched into bus latch U34.

Table 5.1. Transceiver States

GAB STATE	GBA STATE	OPERATION
Low	Low	Transfer data from B lines to A lines
High	High	Transfer data from A lines to B lines
Low	High	Isolation (3-state)

Writing to the control register (U29) is straightforward. The /3BH signal from U31 enables decoder U28. The truth table for decoder U28 is shown in Table 5.2. Address lines A0, A1, and A2 then select a low at the addressed output. This low causes the data on the data bus to be latched into control register U29.

Table 5.2. Decoder U28 Truth Table

ENABLE INPUTS		SELECT INPUTS			OUTPUTS							
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Reading the status register also is straightforward. U28 selects the status register as described in the preceding paragraph. The low from U28 is ORed with the /IOR signal from the CPU by U19. This signal enables buffer U16, which places the video data and horizontal sync pulses (both from U15) on the bus along with the font select data from U29. Note that the data from U15 is read "on the fly" and may violate data stability bus timing requirements when read.

Converting Character Data To Pixel Drive Signals

The CRTC addresses the RAMs for conversion to pixel data. The CRTC acts as a counter, addressing the memory incrementally starting at 0 (or the address in its start register). There are two addresses used by the CRTC. The character location address is carried by the RMA0—RMA11 lines. These addresses locate one character in memory, but do not account for the several scan lines that must be sent to the display to form a character. The scan line address lines (RA0—RA3) are used to address the scan lines of the character. The count sequence starts with both addresses at 0. The character address is then incremented until the maximum count is reached. At that time the scan line is incremented and the character address is reset to the address of the first character in the line.

During its access time, the address from the CRTC is sent to the RAMs through multiplexers U4, U21, and U22. Both the character RAM (U2) and the attribute RAM (U23) are addressed in parallel. The character data output is latched into U3 by the /VIDEO clock. Note that the RAM is addressed by the CRTC's character addresses (RMA0—RMA11) only. The data from the latch is used to address the character ROM (U5). Note that the scan line addresses from the CRTC (RA0—RA3) are connected to the character ROM but not to the RAM.

The character RAM is addressed by character location and the ASCII data is latched into U3. This ASCII data and the scan line address from the CRTC address the ROM. This allows a different byte of pixel data to be sent from the ROM each time the character is addressed. Because of the way that the CRTC addresses the memory, the character RAM is addressed several times (once each scan line) until the character is formed.

The output from the character ROM is latched into U8. U8 is a universal shift/storage register which is used as a parallel-in/ serial-out shift register. U8 is described more fully at the end of this chapter, but only the parallel-in/ serial-out mode is used on this card. U8 is parallel-loaded by holding the S1 line high when the clock makes a low to high transition. This data is then clocked serially out of the IC by the DOTCLK. The data is gated by U13 and U14. U13 is a NAND gate which can be used to block the video data. U14 is an exclusive OR gate. If the other input to U14 is low, the gate acts as a noninverting buffer. If the other input is high, the gate acts as an inverting buffer. The data from U14 goes to the 1D input of U15 and is latched into the output by the DOTCLK. Jumper J3 is used to select either the 1Q output or the 1Q* output from U15. The output from the jumper is then buffered by U16 (the upper 4 bits of U16 always are enabled by grounding G1).

The output from the buffer is filtered by an RFI filter that is built into the 9-pin D connector and is then sent to pin 7 of the output connector.

Attribute Data Conversion

The attribute RAM (U23) is addressed in parallel with the character RAM. The byte contained in the attribute RAM then is decoded by PAL U25 into /GATE and /INVERT signals. The intensity bit goes directly to latch U30. These three signals are delayed by two /VIDEO pulses by U30. The first clock pulse latches these signals into the output of the latch which is connected to three other inputs in the latch. The second clock pulse then sends these signals to the rest of the system. The /GATE signal is used to block the video data. The /INVERT signal inverts the video data. The intensity bit is buffered by two gates of U19 and then passed through latch U15 in the same manner as the video data. The intensity bit is also buffered by U16 and filtered for RFI before being sent to the monitor on pin 6 of the output connector.

The BLINK bit from the attribute RAM is delayed by flip-flop U27 and then connected to U13 which gates the intensity bit into U15.

Sync

The horizontal and vertical sync pulses are generated by the CRTC. The horizontal sync is sent through U30, U15, and U16 just like the video data and connected to pin 8 of the output connector. The vertical sync is processed through the same chips and connected to the output connector at pin 9. The vertical sync pulses are also divided by U11 to provide the CURCLK and BLKCLK signals into PAL U25.

6845 CRTC

The 6845 CRT Controller provides the interface between the CPU and a raster scan CRT display. All inputs and outputs are TTL compatible.

The 6845 functions as a group of programmable counters. Each counter (register) is addressable by the CPU. These registers control all of the functions necessary to control the video memory and the CRT display. The registers and their operation is described in Chapter 4, "Software Considerations."

Typically, the CPU writes data into a memory which is dedicated to the display. The CRTC then controls the transfer of that data from the video memory to the display and provides the sync signals to the CRT.

The pinout of the 6845 is shown in Figure 5.2. The pins have the functions shown in Table 5.3.

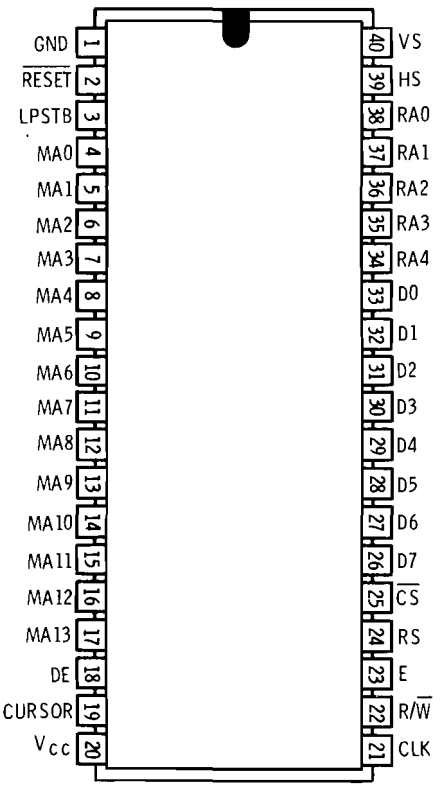


Figure 5.2. 6845 Pinout

Table 5.3. 6845 Pin Functions

PIN NO.	SIGNAL NAME	FUNCTION
1	GND	Provides VDD (ground) to the IC.
2	RESET*	A logic low on this pin forces the following action: The display operation is stopped and all counters are cleared (the control registers are not affected), all outputs are driven low.
3	LPSTB	A low to high transition on this pin latches the current address into the light pen strike register.
4–17	MA0-MA13	Memory address lines, defines the character line of the display. Normally each character line is made up of several scan lines.
18	DE	This output is a logic high when the 6845 is addressing memory. This signal can be used to enable memory and/or to provide input to memory access arbitration logic.
19	CURSOR	This output is used to light the cursor pixels at the correct address.
20	V_{cc}	+5 VDC must be supplied at this pin.
21	CLK	This input is used to synchronize all functions of the 6845 except the CPU interfacing. This signal should be the same frequency as the dot (pixel) clock.
22	R/W*	This signal determines whether the addressed register is being read from or written to. A logic low is used for the write signal.
23	E	When this pin is at a low logic level, the data bus is enabled.
24	RS	This signal from the CPU determines if the index register is being addressed (RS = 0) or the previously indexed register (RS = 1) is being addressed.
25	CS*	When this pin is at a low logic level, the internal registers can be addressed by the CPU.
26-33	D7-D0	These lines are bi-directional, 3-state data lines that carry the data between the 6845 and the CPU.

Table 5.3 (continued). 6845 Pin Functions

PIN NO.	SIGNAL NAME	FUNCTION
34-38	RA0-RA4	These outputs address the scan line of the memory. A character line is composed of several scan lines. The character line and the scan line address make up the complete address.
39	HS	This output is the horizontal sync to the monitor. This signal is derived from the clock signal. The frequency and pulse width of this signal can be programmed (by setting the number of clock pulses between these signals and the number of clock pulses that this signal will last).
40	VS	This output is the vertical sync to the monitor. It also is derived from the clock and can be programmed in the same way.

Shift/Storage Register

This device, U8, is a 74ALS299 universal shift/storage register with 3-state output; it may be used in several modes. Eight of its pins form a 3-state I/O port. These pins may be used for serial to parallel conversion or they may be 3-stated. The I/O pins may be used to input parallel data for parallel to serial conversion when they are in the 3-state output mode.

On the monochrome video card both the G1 and G2 pins are held high, causing the I/O port to be in its 3-state condition. This state allows parallel to serial conversion. Data is loaded in parallel into the I/O port and shifted out to the QH output.

Clearing the 74ALS299 is accomplished by bringing the S1 line low and then bringing the clear line low.

The hold mode (not possible because S0 is held high) is accomplished by bringing both S0 and S1 low. The clear line must remain high.

The shift right mode is accomplished by holding the S0 line high and the S0 line low. The leading edge of the clock pulse causes all data to be shifted to the right (output on the QH line). Data may be inputted serially, using the SR input.

Data may be shifted left by holding the S1 line high and the S0 line low. The leading edge of the clock pulse causes the data to be shifted left (output on the QL line). Data may be inputted serially, using the SL input.

The parallel load is accomplished by holding both S1 and S0 high. The leading edge of the clock pulse then loads the data on the I/O port into the registers.