DYNABYTE

Octaport
801957
Technical Manual

OCTAPORT

MAINTENANCE

CONTENTS PAGE

ILLUSTRATIONS PAGE

ILLUSTRATIONS PAGE

1. GENERAL

1.01 This manual provides a physical and functional description and the operating theory necessary for effective field service of four configurations of the Octaport.

(1) Octaport 801957 equipped with eight ports and two timers,

(2) Quadport 801876 equipped with four ports and two timers,

(3) Octaport 801995 equipped with eight ports and no timers,

(4) Quadport 802014 equipped with four ports and no timers.

Units 2, 3, and 4 are physical and functional equivalents of 1 except for having less ports or timers. The descriptions in this manual are confined to the Octaport 801957.

Features

1.02 The Octaport is a multiport serial input output (I/O) port device used in Dynabyte multi-user systems. Features of the Octaport include:

- Dynabyte S-100 Bus compatible.
- Eight EIA RS-232C serial ports.
- Full duplex asynchronous operation.
- 75 to 19,200 baud data rate.
- Interrupt controls. VI0 through VI7 supported.
- Two interval timers; 1/60 second TICK and one second real time clock (RTC). Both are ac line synchronous.
- Up to three Octaports per system.
- Solder masked pc board.
- Each printed circuit assembly (PCA) carries 30-day warranty on parts and labor.
- Each PCA is burned in for a minimum of 72 hours.

1.03 Dynabyte maintains hardware and software compatibility with the Dynabyte S-100 Bus only. The Octaport is designed for use with 4 MHz Phase 2 clock and, therefore, is not usable with 8080A type CPUs. Contact Dynabyte, Inc. for specific applications.

2. PHYSICAL DESCRIPTION

2.01 The Octaport is an integrated unit incorporating all the necessary components to provide the computer system with eight serial I/O ports, two timers and interrupt control. This printed circuit assembly (PCA) contains:

(1) Eight 8251/8251A Programmable Communication Interfaces. This device is referred to generally as a Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

(2) A baud rate generator.

(3) A latch to hold status information.

(4) Interrupt logic.

(5) Two timers.

(6) Data bus drivers and receivers.

(7) Voltage regulators for powering the Octaport logic.

Figure 2-1 illustrates the Octaport.

2.02 The pc assembly measures 5 inches by 10 inches. A 100-pin edge connector mates with the S-100 Bus connector of the 5100/5200 computer motherboard. This connector is offset by 5/8 inch from the pc board centerline, i.e., the Octaport cannot be inserted into the motherboard backward.

2.03 Distinctive white silkscreen marking has been provided on the component side of the Octaport.

(1) The card name, Dynabyte part number and a location for the serial number have been marked on the pc board. Some early Octaports have the serial number etched on the pc board.

(2) Component reference designators are marked where practical. They facilitate locating the individual part on the schematic or replaceable parts list. Refer to Part 7.

The Octaport integrated circuits and some major components derive their reference designations from the row-column matrix silkscreened onto the pc board. Refer to Figure 2-1. Rows are designated A through C and columns are designated 1 through 13. The integrated circuit located at the lower right corner is C13.

2.04 Four on-board regulators distribute dc voltage to the Octaport elements.

(1) U03 provides +12 Vdc to the board logic.

(2) U01 provides +5 Vdc to the board logic.

(3) U02 provides +5 Vdc to the USARTs.

(4) U04 provides -12 Vdc to the board logic.

If it becomes necessary to change one of these regulators, coat the mating surface with a thermal conductive cream. Secure the regulator to the surface with a screw and nut.

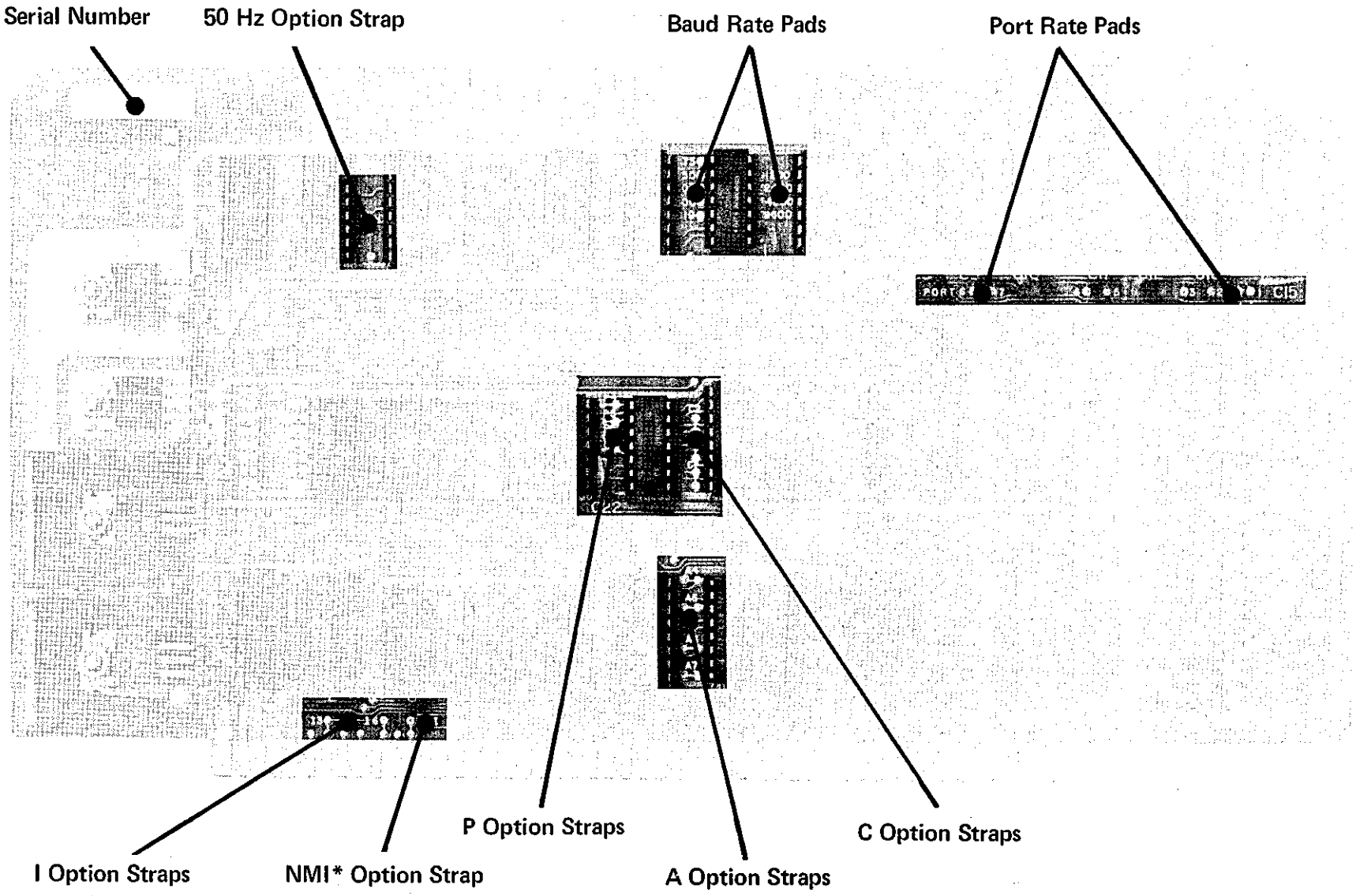

Figure 2-1 — Octaport — 801957

Option Straps

2.05 The Octaport PC Board has several positions for option straps. Refer to Figure 2-1.

(1) A4, A5, A6 and A7 strap options correspond to Bits 4, 5, 6 and 7 of the Octaport Address. Straps are installed for the particular installation.

(2) C1, C2 and C3 strap options correspond to the Octaport 1, 2 or 3 in the system and set the card interrupt. The Octaport is supplied with an etched strap at position C1.

(3) I3 and I6 strap options isolate Octaport RST3* and RST6* from the S-100 bus lines VI3 and VI6. Normally straps are not installed in these positions.

(4) NMI* strap option provides for activating S-100 Bus line NMI*, the non-maskable interrupt from the Octaport timer. Dynabyte software does not support the operation. Normally a strap is not installed in this position.

(5) P4, P5, P6 and P7 strap options provide for disabling the Port 4 to 7 logic when this board is configured as a Quadraport.

(6) 50 Hz strap option provides for operation of the one second timer from a 50 Hz ac line. Normally an etched strap connects the strap pads. The etched strap is removed for 50 Hz operation.

(7) Port Baud Rate strap options provide for setting each port to a different data rate. The Octaport is supplied with an etch trace from each port pad to the 9600 baud trace which is adjacent to each Port Pad. The port is changed by cutting the etch trace and installing a strap between the Port Pad and the appropriate Baud Rate Pad. The baud rate is silkscreened onto the pc board adjacent to the Baud Rate Pad.

2.06 The eight groups of I/O port signals are exchanged with the external terminals over a pair of 20-conductor connectors, J1 and J2, located along the top edge. The Octaport I/O cables, 803515, mate with these connectors and extend the signals to the Rear Panel of the 5100/5200 Computer Unit. These are 20-conductor flat cables.

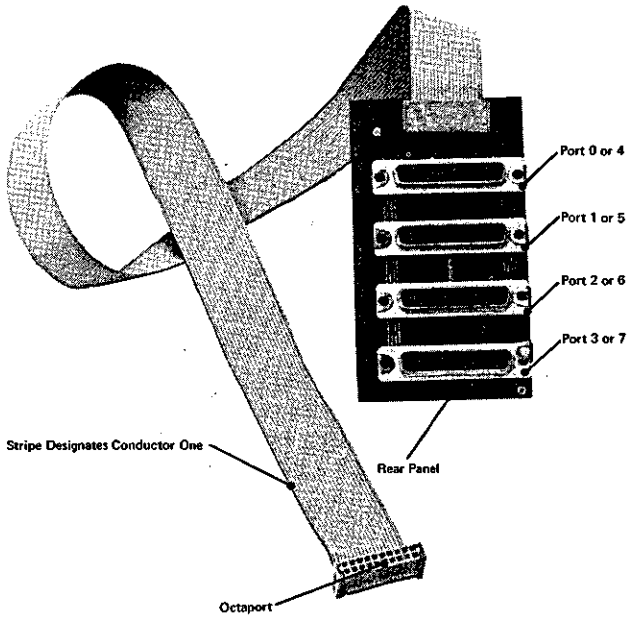

Figure 2-2 — Octaport I/O Cable — 803515

IMPORTANT

Multiconductor I/O cables are polarized with a painted strip on conductor one. This conductor is terminated at pin one of the cable connectors. This marking convention serves to polarize mating connectors.

Figure 2-2 illustrates an Octaport I/O Cable. This cable is terminated by a pc assembly which distributes the port signals to four DB-25S connectors. The port I/O pin assignments for these connectors are tabulated in Table 7-2.

3. FUNCTIONAL DESCRIPTION

3.01 The basic function of the Octaport is to provide eight full duplex asynchronous data communication line (DCL) interfaces for a 5100/5200 Computer Unit. Received serial data from the DCL is converted to eight-bit data words and transferred on to the S-100 Data Bus for processing. Eight-bit data words are transferred off the S-100 Data Bus, converted to a serial data character stream and transmitted out the selected port to the DCL. The DCL is terminated by a Video Display Terminal, Modem, Printing Terminal or other serial data device.

3.02 In addition, the Octaport is the master interrupt controller for multi-user operating systems. The interrupt functions on the Dynabyte Central Processing Unit (CPU) 803439 are disabled for multi-user systems equipped with an Octaport.

3.03 Figure 3-1 illustrates Octaport 801956 in block diagram and should be used in conjunction with the Octaport Logic Diagram in Part 7 for the description which follows. Table 3-1 tabulates the S-100 Bus signals used by the Octaport.

NOTE

A * suffix to a signal name indicates a logical NOT and active low.

Timing

3.04 The 4 MHz PHASE 2 is counted down to ten different data rates by the ***Baud Rate Generator.*** This provides data rates of from 75 to 19,200 baud for the eight ***USARTs***. The ***USARTs*** are supplied connected to 9,600 baud. A simple strap option will furnish any of the nine other data rates to an individual USART.

3.05 The Real Time Clock (RTC), Pin 55, of the S-100 Bus increments the ***Timer***. The ***Timer*** is used in multi-user operating systems to periodically generate an interrupt, VI6*, and to maintain the time of day.

(1) The S-100 Bus RTC is a 1/60 s or 16.6 ms clock supplied from the computer. This signal is buffered through a latch. The operating system monitors latch ***Status*** and resets the latch each time RTC sets it. The operating system designates this ***Timer*** output TICK.

(1) The S-100 bus RTC is counted down to one second. The operating system monitors this ***Status*** to determine the time-of-day. The operating system designates this ***Timer*** output as RTC.

IMPORTANT

The S-100 Bus RTC is 16.6 ms and the Operating System RTC is one second.

RTC or TICK generate VI6* to *Interrupt Control.*

3.06 A strap option also provides for RTC to generate a NMI* to the S-100 Bus. Dynabyte software does not currently support this option.

3.07 The CLOCK is supplied to each ***USART*** device clock line for device timing.

Addressing

3.08 The Octaport occupies an address space of 16 conventional ports. Eighteen ports are required to implement the desired functions. The extra ports are obtained by taking advantage of the Z80 μP I/O instructions which control the upper eight addresses during input-output. For example:

```
LD A,2
IN A,(0B0H)
```

will input from Port B0, low order address of B0, with 02 on the high order address lines.

3.09 ***Address Decode And Control*** decodes A9 and A8, as well as, A7 through A1. A0 is bussed to each ***USART*** Data-Control input. CE0 through CE7 selects the ***USART***. When A9 and A8 decode a:

(1) 0, the operation is ***USART*** data control.

(2) 1, the operation is check the ***USART*** received data status.

(3) 2, the operation is to check the ***Timer*** status and perform a reset.

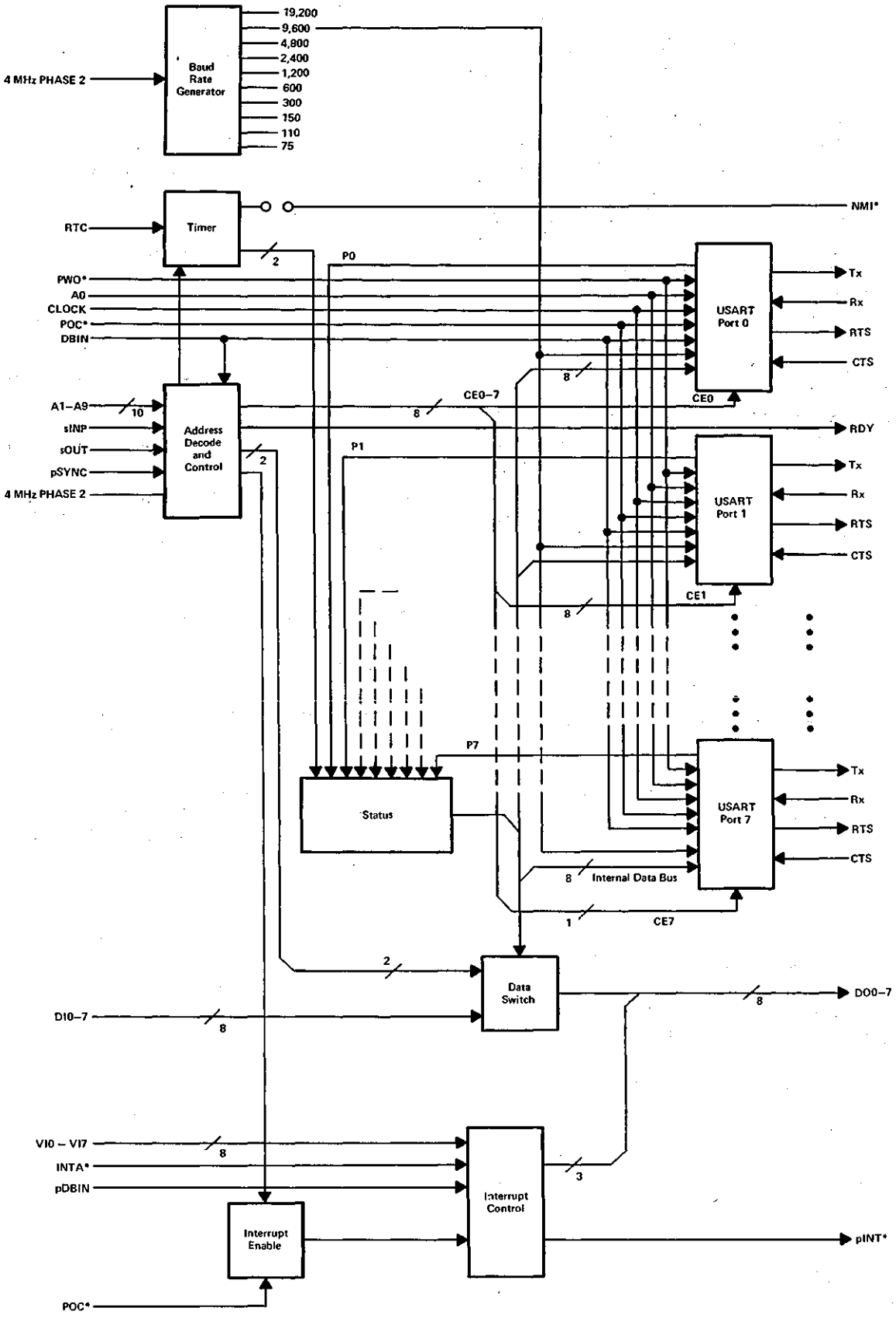

Figure 3-1 — Octaport Functional Block Diagram

Table 3-1 — The Octaport S-100 Bus Signals

Name	Pin	Function
4 MHZ PHASE 2	24	The master timing signal for the bus.
A0 - A15	Various	Address Bit 0 through Address Bit 15.
CLOCK	49	2 MHz (0.5%) 40 — 60% duty cycle Not required to be synchronous with any other bus signal.
DI0 - D17	Various	Data In Bit 0 through Data In Bit 7.
DO0 - DO7	Various	Data Out Bit 0 through Data Out Bit 7.
NMI*	12	Nonmaskable Interrupt.
POC*	99	The Master Reset signal. The Power-On-Clear signal for all devices. When this signal goes low, it must stay low for at least 10 ms.
RDY	72	One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true. Refer to Pin 3, XRDY.
RTC	55	Ac line frequency reference.
VI0* - V17*	Various	Vectored Interrupt line 0 through Vectored Interrupt line 7.
pDBIN	78	The control signal that requests data on the DI bus.
pINT*	73	The primary interrupt request bus signal.
pSYNC	76	The control signal identifying the beginning of a processor cycle.
pWR*	77	The control signal signifying the presence of valid data on the DO bus.
sINP	46	The status signal identifying the data transfer bus cycle cycle from an input device.
sINTA	96	The status signal identifying the bus input cycle(s) that may follow an accepted interrupt request presented on INT*.
sOUT	45	The status signal identifying the data transfer bus cycle to an output device.

3.10 The speed of the 8251/8251A USART is significantly slower than the CPU. It is, therefore, necessary for the Octaport ***Address Decode And Control*** to generate wait states from the 4MHz PHASE 2 Clock and pSYNC. The RDY line is held low during a wait state.

Table 3-2 — Octaport Address Space

Address High Order—Low Order	Description
0 - B0	In/Output Port 0 USART Data
0 - B1	In/Output Port 0 Status/Command
0 - B2	In/Output Port 1 USART Data
0 - B3	In/Output Port 1 Status/Command
0 - B4	In/Output Port 2 USART Data
0 - B5	In/Output Port 2 Status/Command
0 - B6	In/Output Port 3 USART Data
0 - B7	In/Output Port 3 Status/Command
0 - B8	In/Output Port 4 USART Data
0 - B9	In/Output Port 4 Status/Command
0 - BA	In/Output Port 5 USART Data
0 - BB	In/Output Port 5 Status/Command
0 - BC	In/Output Port 6 USART Data
0 - BD	In/Output Port 6 Status/Command
0 - BE	In/Output Port 7 USART Data
0 - BF	In/Output Port 7 Status/Command
1 - Bx (1)	Input - Receive data available status Bit n (n=0-7) = 1 for Port n data available. Output - not defined.
2 - Bx	Input - Bit 7: 1/60 second timer ready. (Active High) Bit 6: 1 second timer ready. Bit 5-0: Not defined Output - Bit 7: Reset 1/60 second timer ready. (2) (Active low) Bit 6: Reset 1 second timer ready Bit 5-0: Not defined.

Notes:

(1) x = any hexadecimal digit.
(2) Timers run continuously. Only the ready bits are set or reset.

3.11 The Dynabyte Operating System calls for the first Octaport in a system to be based at Address B0H, and the second at C0H. Octaports are supplied with a base address strapped at B0H. Strap Option A provides for changing this to any of 00H, 10H, 20H through F0H.

3.12 Table 3-2 presents the space occupied by an Octaport based at B0H. The table may be extended to any base by substituting the desired base for B.

Data Transfer

3.13 Octaport data communications is over a bi-directional internal data bus connected to:

(1) *USARTs,*

(2) *Status,*

(3) *Data Switch.*

The *Data Switch* transfers data between the internal data bus and the S-100 data in and out busses.

Interrupts

3.14 S-100 Bus VI0-VI7 are input to *Interrupt Control* to generate pINT*. POC* clears *Interrupt Enable* when the computer is turned on or reset. The operating system enables the *Interrupt Control.*

3.15 Four of the S-100 Bus vectored interrupts are dedicated to the Octaports. Each *USART* receive data ready (Rx RDY) line, P0 - P1, is extended to the *Status* and can be used to generate an interrupt.

(1) VI3 on Octaport 1

(2) VI4 on Octaport 2

Status of the *Timer* can be used to generate an interrupt.

(4) VI6 for timer on Octaport 1.

3.16 Table 3-3 defines the interrupts for the the Dynabyte multi-user operating system.

Table 3-3 —Octaport Multi-User Interrupt Assignments

Function	Interrupt	Call Address	Dynabyte S-100 Bus Pin
System	RST 0	0H	4
Winchester (1)	RST 1	8H	5
Diskette (1)	RST 2	10H	6
Octaport 1	RST 3	18H	7
Octaport 2	RST 4	20H	8
——— (2)	RST 5	28H	9
Clocks	RST 6	30H	10
System	RST 7	38H	11

Notes:

(1) Winchester Disk Storage 5011/13/15 and Diskette Storage 5200/5010 interrupts may be combined on RST 2 for some Dynabyte systems with RST 1 reserved for special applications.

(2) RST5 is not defined but reserved.

4. SPECIFICATIONS

4.01 Part 4 furnishes the user with information for shipping and installation and should be used to establish acceptance tests if they are performed. Minor deviations from the specifications tabulated in Table 4-1 which do not affect the computer performance are excluded from the Dynabyte warranty.

Table 4-1 — Octaport 801957 Specifications

PARAMETER	CHARACTERISTICS
Ports	
Number	Eight
Mode	Full duplex asynchronous
Data In	EIA RS-232C
Data Out	EIA RS-232C
CTS	EIA RS-232C
RTS	EIA RS-232C
Rate (2)	75 to 19,200 Baud. Strapped for 9600 Baud.
Interrupt	VI3, VI4 or VI5 for any data available.
Timers	
Number	Two
Interval	1/60 second and one second
Source	RTC signal at S-100 Bus Pin 55.
Indication	Each timer has status bit. VI6 for either timer.
Interrupt Controller	
Dedicated (1)	VI3, VI4 or VI5 strap optioned for Octaport. VI6 dedicated to Timers.
General	VI0, VI1, VI2 and VI7 are generated in response to appropriate S-100 Bus signal.
Power Requirements	
+16 Volt Bus	Regulated to +12 Vdc
+ 8 Volt Bus	Regulated to +5 Vdc
-16 Volt Bus	Regulated to -12 Vdc
Operating Temperature	10 C to 35 C (50 F to 95 F)
Relative Humidity	20% to 80%
Dimension, width	25.4 cm (10.0 inches)
, depth	1.5 cm (0.6 inch)
, height	12.7 cm (5.0 inches)
, weight	266.5 g (9.4 ounces)

Notes:

(1) Dedicated interrupts VI3, VI4 and VI5 can be connected to the corresponding S-100 Bus line through a strap option on the pc board.

(2) Octaports equipped with 8251 USARTs support rates to 9,600 baud. Octaports equipped with 8251A USARTs support rates to 19,200 baud.

5. INSTALLATION

5.01 Refer to the 5100/5200 Computer Unit Technical Manual for unpacking, inspection and return of material procedures.

WARNING

Hazardous voltages are present inside the cabinet. Disconnect ac power before removing the cabinet cover or assemblies.

5.02 The following hand tools are needed for installation and changing options.

(1) No. 3 Phillips screw driver,

(2) 11/32 socket or end wrench,

(3) 1/4 socket or end wrench,

(4) Knife or razor blade,

(5) Low wattage soldering iron.

NOTE

Some option straps are initially provided as etched traces between pc board pads. These should be cut for other strapping options.

Options

5.03 Refer to Figure 2-1. Check each set of option strap locations are correct for the system.

(1) A Option Straps. Refer to Table 5-1.

(2) C Option Straps. Refer to Table 5-1.

(3) I Option Straps. Normally vacant.

(4) NMI* Option Strap. Normally vacant.

(5) P Option Straps. Insure that four-port versions, 801876 or 802014, have straps at P4, P5, P6 and P7. Eight-port versions, 801957 and 801995, should be vacant.

(6) 50 Hz Option Strap. The etched trace should be cut if the ac line is 50 Hz.

Table 5-1 — Octaport Address And Interrupt Option Straps

Device	Address	A7	A6	A5	A4	Interrupt
Octaport 1 (1)	B0	Out	In	Out	Out	C1
Octaport 2 (2)	C0 (3)	Out	Out	In	In	C2 (4)

Notes:

(1) PC Assembly 801957, 801876

(2) PC Assembly 801957, 801995, 802014

(3) If A6 has an etched trace strap, remove it.

(4) If C1 has an etched trace strap, remove it.

(7) Baud Rate Option Straps. All port baud rates are set to 9600 baud. Any port can have it's rate changed by cutting a trace and adding a strap between the Port Rate Pad and the appropriate Baud Rate Pad. Cut the trace connecting the Port Rate Pad to the 9600 baud trace. Install a strap between the Port Rate Pad and the appropriate Baud Rate Pad at A7.

5.04 The Octaport can be installed in any of the 12 S-100 Bus positions which is not occupied. Select one which allows I/O cable(s) to form neatly.

STEP	PROCEDURE
1	Install Octaport I/O Cable(s) to the rear panel of the 5100/5200 computer Unit. The I/O interface is secured to the rear panel by the eight 4-40 DB-25S connector units.
2	Install the Octaport into the card cage.
3	Install Octaport I/O Cables to the Octaport. Be sure the cable connector Pin 1 mates with Pin 1 silkscreened onto the Octaport PC Board.

STEP	PROCEDURE
	NOTE *The 20-conductor I/O cables are polarized with a stripe at Pin 1.*

Operating System

5.05 The Dynabyte Operating System provides for integrating the Octaport. The installer should refer to the Operation Manual for the appropriate procedure.

6. MAINTENANCE

6.01 The Octaport is a result of several years of design, development and modern electronic manufacturing. The pc assembly is designed around the latest semiconductors and connectors. All components operate at relatively low power. Each assembly is burned in at the Dynabyte factory for 72 hours before shipment.

6.02 No routine maintenance should be performed to the Octaport.

Customer Support Service

6.03 Maintenance and procedures described in this manual should be performed in accordance with local instructions and the individual user's maintenance plan. Maintenance and repair of the Octaport during the warranty period should be limited to returning the pc assembly to Dynabyte, Inc. The Dynabyte Customer Support staff is available by telephone for assistance in troubleshooting and recommendations for repairs. All communications material should be directed to:

DYNABYTE, INC.
Customer Support
521 Cottonwood Drive
Milpitas, CA. 95035
(408) 263-1221
Telex 346-359

The 5100/5200 Technical Manual, Part 6, outlines the procedure for returning material.

NOTE

Dynabyte Authorized Service Centers (ASC) are staffed with factory-trained technicians that are supplied with technical manuals and routinely receive service bulletins and design change information on Dynabyte equipment.

7. REFERENCE

Schematics and Replaceable Parts Lists

7.01 Figure 7-1 will furnish the user with a schematic diagram of the Octaport. Table 7-1 is the Replaceable Parts List for the Octaport indexed by reference designator appearing on the respective schematic. Enough information is furnished so the maintenance technician should be able to purchase replaceable parts from a local supplier or make a substitution if necessary. Octaport PC Assemblies and I/O cables should be ordered directly from Dynabyte Customer Support Service.

Engineering Change Notices

7.02 Dynabyte makes changes to drawings and products through engineering change notices (ECN)s. Before a change to a product is approved or made:

(1) The implications to systems in the field are determined,

(2) Rework instructions are included for the equipment in the field when appropriate.

Dynabyte Customer Support Services receives copies of all ECNs and advises Dynabyte Authorized Service Centers through seminars and periodic bulletins.

7.03 There are no pertinent ECNs affecting the Octaport at the publication date.

Data Communication Lines

7.04 Table 7-2 tabulates the Rear Panel DB-25S receptacle pin assignments for the data communication lines.

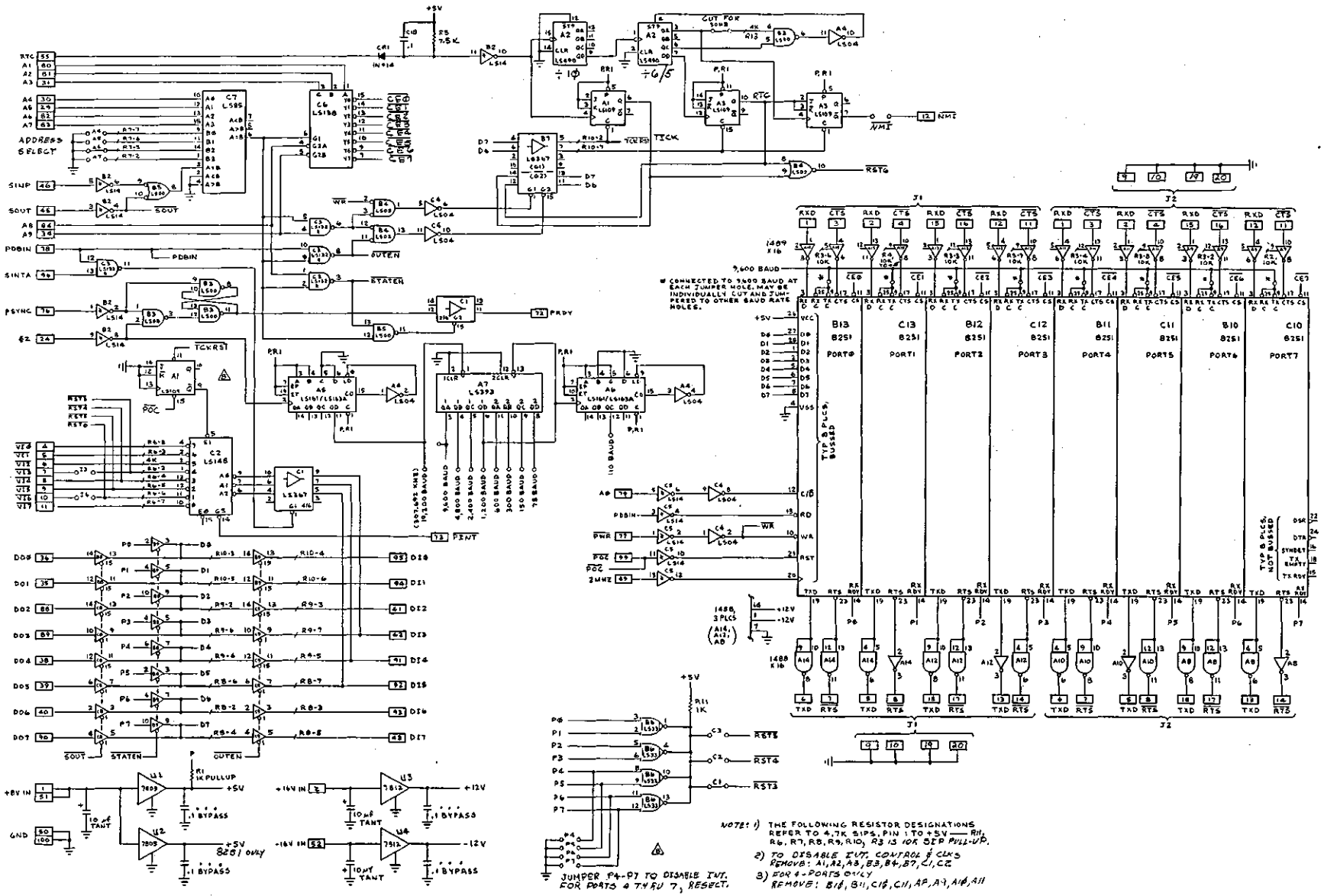

Figure 7-1 — Octaport Schematic

Table 7-1 — Octaport Replaceable Parts List

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
	PCA: OCTAPORT	DYNABYTE	801957	801957
	CABLE: OCTAPORT	DYNABYTE	803515	803515
C 01	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 02	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 03	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 04	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 05	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 06	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 07	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 08	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 09	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 10	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 11	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 12	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 13	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 14	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 15	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 16	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 17	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 18	C: FXD CER 10% 1KV 100PF	CENTRALAB	DD101	703978
C 19	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 20	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 21	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 22	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 23	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 24	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 25	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 26	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 27	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 28	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 29	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 30	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 31	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 32	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 33	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 34	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294

Table 7-1 — Octaport Replaceable Parts List (continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
C 35	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
CR 01	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
J 01	CONNECTOR: 20-CONDUCTOR	AP PRODUCT	929838-01-10	718108
J 02	CONNECTOR: 20-CONDUCTOR	AP PRODUCT	929838-01-10	718108
R 01	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 02	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 03	R: FXD SIP 7 X 10K OHM	BECKMAN	764-1-10K	703834
R 04	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 05	R: FXD CF 5% 0.25W 7.5K OHM	ROHM	R25J752	707272
R 06	R: FXD SIP 7 X 4.7K OHM	BECKMAN	764-1-4-4.7K	704716
R 07	R: FXD SIP 7 X 4.7K OHM	BECKMAN	764-1-4-4.7K	704716
R 08	R: FXD SIP 7 X 4.7K OHM	BECKMAN	764-1-4-4.7K	704716
R 09	R: FXD SIP 7 X 4.7K OHM	BECKMAN	764-1-4-4.7K	704716
R 10	R: FXD SIP 7 X 4.7K OHM	BECKMAN	764-1-4-4.7K	704716
R 11	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 12	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 13	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
U 01	IC: REGULATOR +5V	TI	7805C	703168
U 02	IC: REGULATOR +5V	TI	7805C	703168
U 03	IC: REGULATOR +12V	TI	7812C	701998
U 04	IC: REGULATOR -12V	TI	7912C	707344
U A01	IC: DUAL J-K FLIP FLOP	TI	SN74LS109N	703564
U A02	IC: DUAL DECADE COUNTER	TI	SN74LS490N	707074
U A03	IC: DUAL J-K FLIP FLOP	TI	SN74LS109N	703564
U A04	IC: HEX INVERTER	TI	SN47LS04N	704014
U A05	IC: SYNCH 4-BIT COUNTER	TI	SN74LS161N	707092
U A06	IC: SYNCH 4-BIT COUNTER	TI	SN74LS161N	707092
U A07	IC: DUAL 4-BIT BINARY COUNTER	TI	SN74LS393N	707110
U A08	IC: QUAD RS-232C LINE DRIVER	NATIONAL	DS1488N	707128
U A09	IC: QUAD RS-232C LINE RECEIVER	NATIONAL	DS1489N	707146
U A10	IC: DUAL J-K FLIP FLOP	TI	SN74LS109N	703564
U A10	IC: QUAD RS-232C LINE DRIVER	NATIONAL	DS1488N	707128
U A11	IC: QUAD RS-232C LINE RECEIVER	NATIONAL	DS1489N	707146

Table 7-1 — Octaport Replaceable Parts List (continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
U A12	IC: QUAD RS-232C LINE RECEIVER	NATIONAL	DS1489N	707146
U A12	IC: QUAD RS-232C LINE DRIVER	NATIONAL	DS1488N	707128
U A15	IC: QUAD RS-232C LINE RECEIVER	NATIONAL	DS1489N	707146
U A15	IC: QUAD RS-232C LINE DRIVER	NATIONAL	DS1488N	707128
U B02	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U B03	IC: QUAD 2-IN NAND	TI	SN74LS00N	703438
U B04	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U B05	IC: QUAD 2-IN NAND	TI	SN74LS00N	703438
U B06	IC: QUAD 2-IN NOR OC	TI	SN74LS33N	707182
U B07	IC: HEX BUFFER	TI	SN74LS367N	707200
U B08	IC: HEX BUFFER	TI	SN74LS367N	707200
U B09	IC: HEX BUFFER	TI	SN74LS367N	707200
U B10	IC: UART	NATIONAL	INS8251N	707218
U B11	IC: UART	NATIONAL	INS8251N	707218
U B12	IC: UART	NATIONAL	INS8251N	707218
U B13	IC: UART	NATIONAL	INS8251N	707218
U C01	IC: HEX BUFFER	TI	SN74LS367N	707200
U C02	IC: 8-TO 3-LINE OCTAL ENCODER	TI	SN74LS148N	707236
U C03	IC: QUAD 2-IN NAND SCHMIDTT	TI	SN74LS132N	703582
U C04	IC: HEX INVERTER	TI	SN47LS04N	704014
U C05	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U C06	IC: 3-TO 8-LINE DECODE / MUX	TI	SN74LS138N	707308
U C07	IC: 4-BIT MAGNITUDE COMPARE	TI	SN74LS85N	704068
U C08	IC: HEX BUFFER	TI	SN74LS367N	707200
U C09	IC: HEX BUFFER	TI	SN74LS367N	707200
U C10	IC: UART	NATIONAL	INS8251N	707218
U C11	IC: UART	NATIONAL	INS8251N	707218
U C12	IC: UART	NATIONAL	INS8251N	707218
U C13	IC: UART	NATIONAL	INS8251N	707218

Table 7-2 — I/O Port Pin Assignments

Pin	EIA	Description
1	AA	Protective or earth ground. (1)
2	BA	Data out or transmitted data.
3	BB	Data in or received data.
4	CA	Request to send.
5	CB	Clear to send.
7	AB	Signal common.

Notes:

(1) Pin 1 is a common pc bus to each DB-25S connector and is optionally connected to the computer chassis frame.


DYNABYTE