Cromemco

MAXIMIZER

Board Manual

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This manual was produced using a Cromemco System Three computer running under the Cromemco Cromix Operating System. The text was edited with the Cromemco Cromix Screen Editor. The edited text was proofread by the Cromemco SpellMaster Program and formatted by the Cromemco Word Processing System Formatter II. Camera-ready copy was printed on a Cromemco 3355B printer.

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Chapter 1

INTRODUCTION

Many scientific and engineering applications, particularly those involving complex video imaging, require large amounts of RAM and high-speed number-processing capability. The two-board Maximizer, consisting of the Maximizer Coprocessor (Max-C) and Maximizer I/O Coprocessor (Max-I), when used with Cromemco's DPU, provides an ideal solution to these applications requirements.

The Maximizer is a general-purpose, microprogrammable array coprocessor, capable of performing many functions in a fraction of the time required by the 68000 microprocessor.

HARDWARE SPECIFICATIONS

Microprocessor:

- 2901C microprocessor, using bit-slice internal ECL logic.
- Separate program and data paths.
- 16 general-purpose 2-port registers.
- 60 nsec, 16-bit multiplier.
- Double pipelined architecture.

Instruction Time:

62.5 to 125 nsec in four microcode-controllable steps; most instructions execute in 62.5 nsec.

Microcode Control Store:

- 4,096 x 48 bits of read/write RAM.
- 512 x 48 bits of PROM.

Data Storage:

16 Kbits x 8 bits of 55 nsec read/write storage.

Clock:

48 MHz system clock, phase-locked to the S-100 bus clock, variable from 32 to 60 MHz under microcode control.

Input/Output:

- I/O port addresses: F4h through F7h.
- S-100 DMA rate of 4 Mbytes/sec over full 16-Mbyte address space.
- S-100 and C bus DMA-controlled by I/O state machines.

Hardware:

- Two S-100 bus boards, with about 150 IC's.
- Two high-efficiency, switching, regulated 5-VDC power supplies, operating at 6 A.

SOFTWARE SPECIFICATIONS

The Maximizer operates with Cromemco's Cromix Operating System, and Cromemco's 256KZ and MCU (Rev K and up) boards. The Maximizer supports FORTRAN 77, Pascal, and C compilers to generate in-line code for the Maximizer with no changes to the source code. The operating environment allows multiple users to share the Maximizer's resources. Multi-tasking is supported without changes to the Cromix Operating System.

Microcode:

- Control Structures:
  - Microcode subroutines up to four levels.
  - Single-instruction looping.
  - Override for exiting multi-instruction loops.
  - 16 conditional tests.
  - Ability to flush microcode pipeline.
- Constant and computed addresses may be used for data storage and jump targets.
- Parallel control of input and output.
- Instruction time controllable by microcode.
- Multi-word shifting and arithmetic.

Development Software:

- Microcode assembler (written in C language) presents uniform register-transfer syntax.
- Microcode linker and loader.
- Microcode debugger is modeled after 68000 debugger.

APPLICATIONS

The Maximizer performs all basic arithmetic functions. In addition, it performs format conversions, square roots, logarithmic, and trigonometric functions. All floating-point arithmetic is handled according to the IEEE Standard, in single-precision (32-bit) or double-precision (64-bit) format, with dramatic speed improvements over normal DPU machines. The Maximizer also handles 16-bit and 32-bit integer operations.

Cromemco's Fast FORTRAN-77, Fast Pascal, and Fast C provide compiler support for the Maximizer. No knowledge of the Maximizer hardware or software is required to use the Maximizer with these languages. In addition, by recompiling and linking with the Fast software listed above, existing programs in 68000 FORTRAN, 68000 Pascal, and 68000 C can be used without modification.

Because of its high-speed number-processing and rapid DMA-accessing capabilities, many video graphics applications can also be run on the Maximizer.

Cromemco recommends that, because of the Maximizer's cooling requirements, this board set should only be installed in systems with adequate, positive fan cooling.

Chapter 2

INSTALLATION

The Maximizer boards are shown in Figures 2-1 and 2-2.

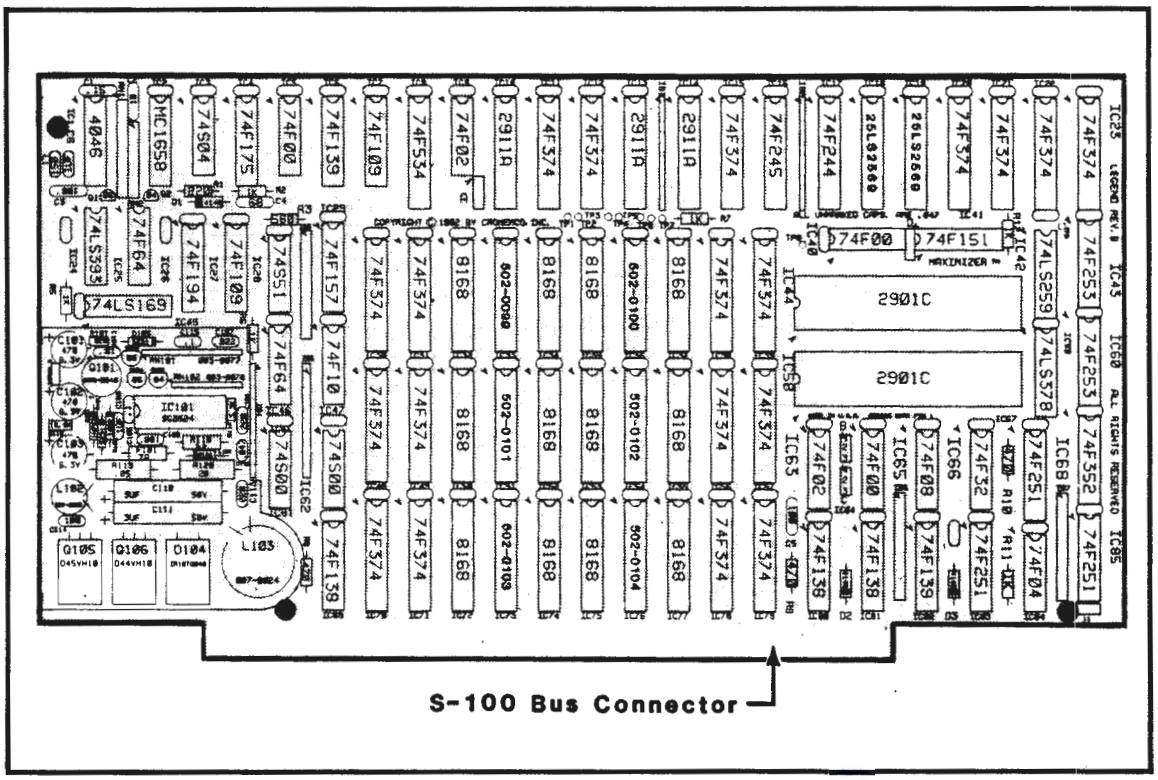


Figure 2-1: MAXIMIZER COPROCESSOR (MAX-C) BOARD

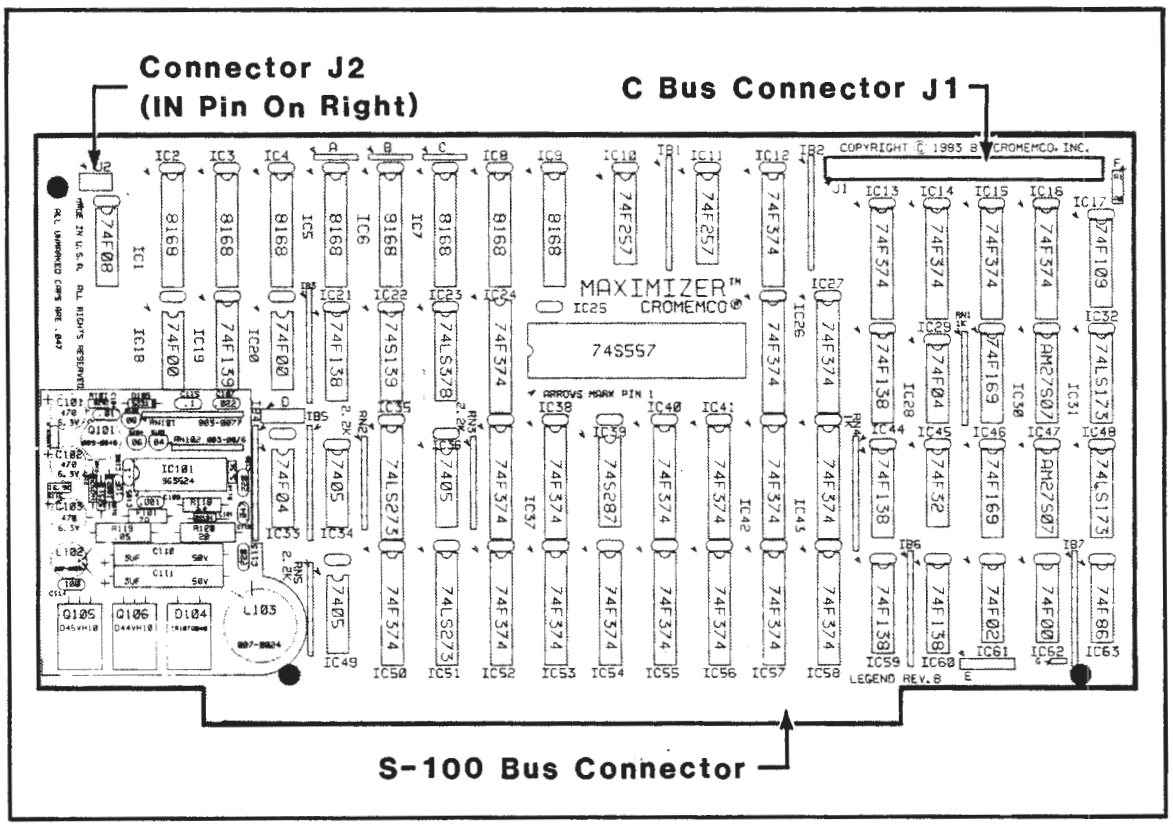


Figure 2-2: MAXIMIZER I/O COPROCESSOR (MAX-I) BOARD

JUMPERS

There are no user-configurable jumpers on either of the Maximizer boards. Do not change any of the jumpers on these boards.

CABLING

Two cables attach to the Maximizer--the DMA priority cable and the optional C bus cable. The DMA priority cable connects the IN pin (right pin) of connector J2 on the Max-I board to the OUT pin (~~right~~ pin) of connector J2 on the STDC board (or to the OUT pin (right pin) of connector J3 on the WDI-II board). The pin assignments and signals for the C bus connector, J1, are listed in table 2-1. The pin assignments and signals for the S-100 bus connector are listed in table 2-2.

Table 2-1: CONNECTOR J1 PIN ASSIGNMENTS AND SIGNALS

Pin No.	Signal	Input	Output	Pin No.	Signal	Input	Output
1	GND	-	-	26	A10	-	x
2	RESET	-	x	27	A11	-	x
3	Not Used	-	-	28	GND	-	-
4	GND	-	-	29	A12	-	x
5	WAIT	x	-	30	A13	-	x
6	D0	x	x	31	A14	-	x
7	D1	x	x	32	A15	-	x
8	D2	x	x	33	RD	-	x
9	D3	x	x	34	GND	-	-
10	D4	x	x	35	WR	-	x
11	D5	x	x	36	M1	-	x
12	D6	x	x	37	MREQ	-	x
13	D7	x	x	38	IORQ	-	x
14	GND	-	-	39	RFSH	-	x
15	A0	-	x	40	CPU DISCONNECT	x	-
16	A1	-	x	41	BUS AVAILABLE	x	x
17	A2	-	x	42	HALT	-	x
18	A3	-	x	43	GND	-	-
19	A4	-	x	44	INT	x	-
20	A5	-	x	45	NMI	x	-
21	GND	-	-	46	Not Used	-	-
22	A6	-	x	47	Not Used	-	-
23	A7	-	x	48	PRI 3	-	-
24	A8	-	x	49	Not Used	-	-
25	A9	-	x	50	GND	-	-

INSTALLATION PROCEDURE

Use the following procedure to install the Maximizer board set in your system:

1. Turn off the system power.

2. Insert the Maximizer board set into any adjacent pair of S-100 slots available.

3. Install the DMA priority cable between connector J2 on the Max-I board and connector J2 on the STDC (or connector J3 on the WDI-II board).

4. If your system has a C bus, install the C bus cable to connector J1 on the Max-I board.

5. Turn on the system power.

6. Boot the Cromix Operating System.

7. Perform the software installation procedures described in the manual accompanying the software you intend to run on the Maximizer.

IN CASE OF DIFFICULTY

The Maximizer adds a significant electrical load on the system power supply which may affect the selection of the proper line-voltage tap. Refer to the manual provided with your system should you need to change the line-voltage tap to accommodate the Maximizer.

Table 2-2: S-100 BUS CONNECTOR PIN ASSIGNMENTS AND SIGNALS

Pin No.	Signal	Input	Output	Pin No.	Signal	Input	Output
1	+8 VDC	-	-	51	+8 VDC	-	-
2	+18 VDC	-	-	52	-18 VDC	-	-
3	XRDY	-	x	53	Not Used		
4	Not Used			54	SLVCLR*	-	x
5	Not Used			55	Not Used		
6	Not Used			56	Not Used		
7	Not Used			57	Not Used		
8	Not Used			58	sXTRQ*	x	x
9	Not Used			59	A19	-	x
10	Not Used			60	SIXTN*	x	x
11	Not Used			61	A20	-	x
12	NMI*	x	x	62	A21	-	x
13	PWRFAIL*	x	-	63	A22	-	x
14	DMA3	-	x	64	A23	-	x
15	A18	-	x	65	MREQ*	x	x
16	A16	-	x	66	RFSH*	x	x
17	A17	-	x	67	MEMDSB*	-	x
18	SDSB*	-	x	68	MWRT	-	-
19	CDSB*	-	x	69	Not Used		
20	GND	-	-	70	GND	-	-
21	Undefined	x	x	71	Z80/68*	x	x
22	ADSB*	-	x	72	pRDY	x	
23	DODSB*	-	x	73	pINT*	x	x
24	phi 2	x	-	74	pHOLD*	x	x
25	pSTVAL*	-	x	75	RESET*	-	-
26	pHLDA	x	x	76	pSYNC	-	x
27	EXTAD*	x	x	77	pWR*	x	x
28	Undefined	x	x	78	pDBIN	x	-
29	A5	-	x	79	A0	-	x
30	A4	-	x	80	A1	-	x
31	A3	-	x	81	A2	-	x
32	A15	-	x	82	A6	-	x
33	A12	-	x	83	A7	-	x
34	A9	-	x	84	A8	-	x
35	DO1/D9	x	x	85	A13	-	x
36	DO0/D8	x	x	86	A14	-	x
37	A10	-	x	87	A11	-	x
38	DO4/D12	x	x	88	DO2/D10	x	x
39	DO5/D13	x	x	89	DO3/D11	x	x
40	DO6/D14	x	x	90	DO7/D15	x	x
41	DI2/D2	x	x	91	DI4/D4	x	x
42	DI3/D3	x	x	92	DI5/D5	x	x
43	DI7/D7	x	x	93	DI6/D6	x	x
44	sM1	-	x	94	DI1/D1	x	x
45	sOUT	x	x	95	DI0/D0	x	x
46	sINP	x	x	96	sINTA	-	x
47	sMEMR	-	x	97	sWO	-	x
48	sHLTA	-	x	98	ERROR*	-	x
49	CLOCK	-	-	99	POC*	-	-
50	GND	-	-	100	GND	-	-

Chapter 3

THEORY OF OPERATION

INTRODUCTION

The architecture of a traditional central processing unit is a trade-off between speed and flexibility. Most computers store data and instructions in the same memory space, and use a bi-directional bus to transfer information in and out of the central processing unit. This method provides a flexible, but slower than optimum, computer.

The Maximizer, on the other hand, is a computer designed to optimize memory-cycle time. Instructions and data are stored in separate memory locations. Separate buses into and out of the ALU are also provided for instructions and data. Separate memories and buses permit multiple data transfers to occur simultaneously.

Conventional microprocessor MOS logic has been replaced by pipelined bipolar logic, with a resulting speed improvement of 20 to 1 compared to the 68000.

The Maximizer circuits are placed on two circuit boards, interconnected by pin and socket connectors. A basic block diagram of the Maximizer is shown in figure 3-1. The processors and support circuits occupy the first board, called the Max-C. The companion board, called the Max-I, comprises the multiplier, data RAM, and bus interface registers. The architecture of the Maximizer and the functions of each section are discussed below. Where integrated circuit (IC) numbers are given, the heading of the section indicates on which board the circuit is located.

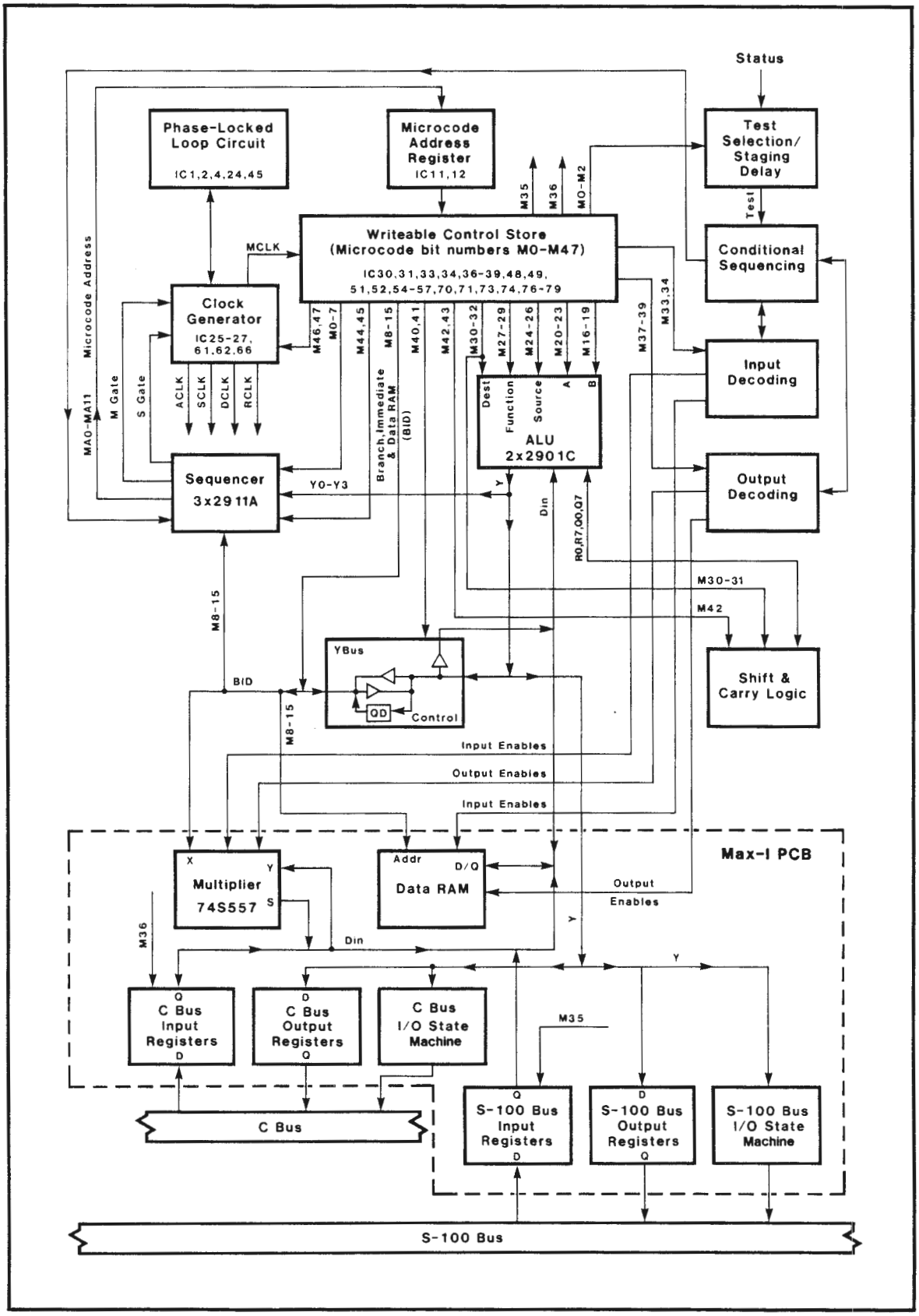


Figure 3-1: MAXIMIZER BLOCK DIAGRAM

DATA PATHS

The primary flow of data is along the D bus, which feeds the data input lines of the two 2901C bit-slice ALU's (Arithmetic Logic Unit). The output of the 74S557 multiplier drives the D bus, as do the outputs of the bus-interface registers. Both input and output circuits of the data RAM are connected to the D bus.

Another important path for data is the Y bus, which is driven by the data output from the 2901C ALU's. The Y bus supplies one operand to the multiplier, and provides data to the inputs of the bus-interface registers. It is also possible for the Y bus to drive the D bus, allowing the ALU to supply data to the data RAM or the BID bus to supply immediate values to the ALU. Also, the Y bus can be linked to the BID bus, described below.

The BID bus carries branch, immediate, and data RAM address information, supplied by one of the microcode fields in the WCS (Writeable Control Store). A bi-directional bus driver links the BID and Y buses. A temporary holding register, the Y register, can be used to gate a delayed sample of the Y bus information onto the BID bus.

ADDRESS PATHS

The Maximizer has separate paths for program addresses and data addresses. Program addressing is done by the 2911A instruction sequencer, described below, which provides information to the microcode address register. The output of this register is then applied to the microcode control store.

Data addressing is done by the ALU or the microcode control store; the information is passed along the BID bus, as described in the preceding section.

MICROCODE RAM AND ROM (MAX-C)

The microcode control store issues the 48-bit microinstructions required for operation of the Maximizer. The store is divided into a writeable section (IC's 32, 34, 35, 39, 50, 51, 53, 55, 72, 74, 75, and 77), which holds 4,096 entries in RAM, and a non-writeable section (IC's 33, 36, 51, 54, 73, and 76), which holds 512 entries in ROM. Registers are used at the input (IC's 11 and 12) and output (IC's 30, 39, 48, 57, 70, and 79) to store the microcode address and data, respectively. Microcode is loaded through registers (IC's 31, 38, 49, 56, 71, and 78) that connect to the Y bus. Microcode words are assembled one byte at a time, then written to the RAM during a load cycle.

INSTRUCTION SEQUENCER (MAX-C)

The instruction sequencer generates the microcode addresses that are supplied to the input register of the microcode control store. The sequencer uses three 2911A chips (IC's 10, 13, and 14) to obtain twelve bits of address. These chips provide a basic set of addressing modes, including sequential, skip-on-condition, loop, branch, and call-return along with a four-level stack for subroutine return and looping addresses. All branch, repeat, and skip operations use the test logic circuits to provide conditional sequencing. The branch instruction provides two fields, each of which can select one of sixteen branch options. The drop-through instruction, when combined with a branch instruction, makes it possible to execute a three-way branch. Control and input signals to the sequencer are latched by IC's 8, 21, and 23.

ARITHMETIC LOGIC UNIT (MAX-C)

The ALU is built from two 2901C bit-slice microprocessors (IC's 44 and 58). Together, these chips provide a 16-word by 8-bit two-port RAM, a high-speed ALU with eight functions, and associated shifting, decoding, and multiplexing circuitry. Seventeen bits of microcode control (M16-M32) are used to specify the ALU operation, ALU source and destination data, and two-port RAM addresses.

SHIFT, CARRY, LOOP AND TEST LOGIC (MAX-C)

Two four-input multiplexers (IC's 60 and 43) are used to complete the shift carry/borrow path around the ALU. The nature of the shift is determined by three microcode bits, M30, M31, and M42.

The carry-in bit to the ALU is supplied by a data selector, IC 41, which is controlled by microcode bits M32 and M42. Although the carry-in bit is normally the inverted microcode bit M43, the delayed carry-out from the preceding operation can be asserted when necessary.

Loop control is assisted by an eight-bit counter, IC's 18 and 19, which signals the ALU when the microcode has performed a specified number of instructions. The counter is loaded from the Y bus data when specified by microcode bits M39 through M37; the counter may be incremented, decremented, or cleared as specified by bits M7 through M5 of the microcode. The output of the counter (count-not-equal-zero) is sampled by the test logic.

The test logic works in conjunction with the sequencer to control the flow of the microprogram. Maximizer flags are sampled by IC's 83, 85, 87, and 68, and the selected test value is then sent to the sequencing logic.

DATA RAM (MAX-I)

Eight 4K x 4 static RAM's are used as a 16K x 8-bit data memory on the Maximizer. The array (IC's 2 through 9) is addressed by eight bits from the BID bus and six bits from address latch IC 23. The address latch is controlled by microcode bits M39 through M37, M16 through M18, and the Y bus. Chip selects are generated by decoder IC 22 operating on the outputs of address latch IC23.

The data lines are connected to the D bus. A write line from the ALU requires a bypass (IC 17 on Max-C) to gate data from the Y bus to the D bus. Data from other input devices can be written into the data RAM without involving the ALU or the Y bus.

MULTIPLIER (MAX-I)

In less than 60 nanoseconds, a high-speed multiplier, IC 25, multiplies two 8-bit unsigned or two's-complement signed numbers to form a 16-bit unsigned or signed product. The chip internally develops proper rounding for either signed or unsigned numbers, as specified by control register IC 24. The arguments for multiplier and multiplicand are supplied from the BID and Y buses; the product, latched when the multiplier is activated using microcode bits M37 through M39, is sent to the D bus through two data selectors, IC's 10 and 11.

FLAG AND SQUIRREL REGISTERS (MAX-C)

An addressable latch, IC 42, and flip-flop, IC 22, are used to generate control flags; selection of microcode RAM or ROM is done in this manner.

Eight selected status bits are latched by the squirrel register, IC 20, allowing momentary states of the Maximizer to be captured and examined at the proper time.

S-100 INTERFACE AND STATE CIRCUITS (MAX-I)

The interface between the Maximizer and the S-100 bus comprises input registers, output registers, and an I/O state machine. The input registers are used to read the state of the S-100 bus, including data signals (IC's 41 and 42) and handshake signals (IC's 37 and 38). The output registers are used to drive the bus signals when the Maximizer becomes a bus master. The data lines are driven by IC's 56 and 57; the address lines by IC's 50, 54, and 55; and the status/control lines are driven by IC's 35, 51, 52, and 58.

Some of the interface lines on the bus are driven directly from the I/O state machine, which uses a counter (IC 46) to drive a RAM (IC 47). The outputs of the RAM are latched and applied to the bus by IC 48. The contents of the RAM are loaded by the ALU, as specified by microcode bits M39 through M37. The counter is enabled and disabled by microcode bits M7 through M5.

I/O REGISTER CONTROL (MAX-I)

The I/O register control circuits make the Maximizer seem like an output port on the S-100 bus. A decoder PROM, IC 39, detects every I/O cycle in which the Maximizer is referenced, and generates a signal, ARCLK, which may be sampled by the microprogram. This signal clocks the middle byte of the S-100 address bus into input port IC 40, and bit A1 into flip flop IC 17 as another test condition.

C-BUS INTERFACE AND STATE CIRCUITS (MAX-I)

The interface between the Maximizer and the C bus comprises input registers, output registers, and an I/O state machine. The input registers are used to read the state of the C bus, including data signals (IC 26) and handshake signals (IC 12). The output registers are used to drive the bus signals when the Maximizer becomes a bus master. The data lines are driven by IC 27; the address lines by IC's 13 and 14; and the status/control lines are driven by IC's 15 and 16.

Some of the interface lines on the bus are driven directly from the I/O state machine, which uses a counter (IC 30) to drive a RAM (IC 31). The outputs of the RAM are latched and applied to the bus by IC 32. The contents of the RAM are loaded by the ALU, as specified by microcode bits M39 through M37. The counter is enabled and disabled by microcode bits M16 through M19.

CLOCK (MAX-C)

A phase-locked loop (IC's 1, 2, 4, 24, 45, and Q1 and Q2) generates the master clock, HCLK, for the Max-C using an ECL voltage-controlled oscillator and a CMOS phase detector. The signal ranges from 32 MHz to 60 MHz in eight microcode-controlled steps, and is locked to the S-100 bus clock signal, PHI2.

Several clock signals are derived from the master clock by IC's 25 through 27, 61, and 62. A field in each instruction chooses one of four cycle periods, lasting from three to six ticks of HCLK. MCLK is sent to the ALU; SCLK to the sequencer, RCLK to the data RAM, and ACLK to certain status decoders. These clocks may be gated off to allow control of the instruction pipeline. In addition, there is a DCLK clock which runs continuously.

POWER SUPPLY

Each board of the Maximizer uses a switching power supply to provide regulated 5-volt power at a maximum of 5 amperes. This supply draws its input power from the +18 volt bus line rather than the traditional +8 volt line; this reduces the input current requirement to a level that can be safely passed through the PC board edge connector. A 100-KHz, fixed-frequency, variable-duty-cycle waveform is generated by IC 101 and used to control the charging and discharging interval of L103 through Q103, Q105, Q106, D102, and D103. The flyback pulse is caught by Shottky diode D104.

The supply includes short-circuit protection (Q104 and Q102) and a crowbar circuit for overvoltage protection (D101 and Q101).

MICROCODE WORD DESCRIPTION

The Maximizer uses 48-bit words. These words are divided into seven basic fields. The bit positions of the fields are shown in figure 3-2. Each of the major basic fields and bit positions shown in figure 3-2 are summarized below. Additional detailed descriptions of each basic field follows the summaries.

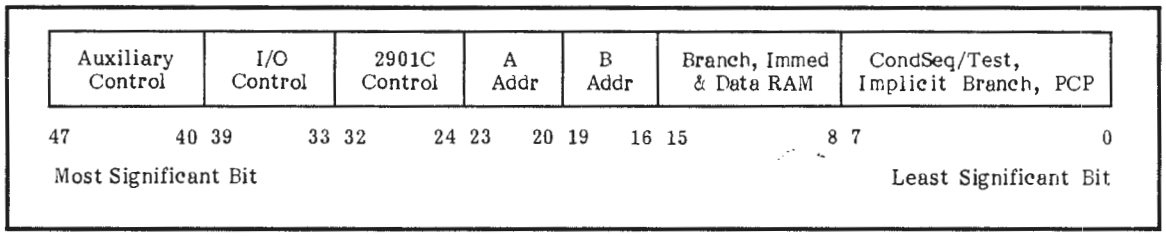


Figure 3-2: BASIC FIELDS AND BIT POSITIONS

Bits 40-47: Auxiliary Control Field

These eight bits are used to make up five small auxiliary fields that deal with instruction cycle-time selection, conditional sequencing and test modes, carry-in bit, shift modes, and immediate-field-to/from-Yout manipulations.

Bits 33-39: I/O Control Field

These seven bits provide fields for selectively storing input information from external buses, reading from various external registers into the 2901C microprocessor, and many other functions.

Bits 24-32: 2901C Control Field

These nine bits are sent to I0-I8 on the 2901C as source, function, and destination controls. Their effects include selection of shift types (along with the auxiliary shift mode field).

Bits 20-23: A Address Field

These four bits go to both the A address field on the 2901C and to selected input devices and decodes.

Bits 16-19: B Address Field

These four bits go to both the B address field on the 2901C and to selected output devices and decodes.

Bits 8-15: Branch, Immediate, and Data RAM Field

These eight bits always load into the D and R inputs of the 2911A and are clocked into the least significant byte of the microcode address register at the end of each instruction period. The bits can also load onto the Yout bus of the 2901C (YBUS) for particular instructions or can be replaced by the Yout field (as determined by the auxiliary control field).

In addition, these bits go to the least significant byte of the data RAM address, which, along with the 4-6 data RAM bank selection bits, determines the actual address used when the I/O control field calls for data RAM read or write.

Bits 0-7: Conditional Sequence/Test, Implicit Branch, and Processor Control Point

These eight bits are used to determine microprogram flow. They operate in three different modes, depending on the conditional sequence/test mode. In one mode, the bits select a test condition and provide for limited program redirection. In the second mode, the bits select a test condition to be used in the next instruction and provide special-purpose input and output functions. In the third mode, the bits provide two alternative control fields for the 2911A, thus allowing elaborate sequencing capabilities to be selected, depending on the outcome of a test of the previous instruction.

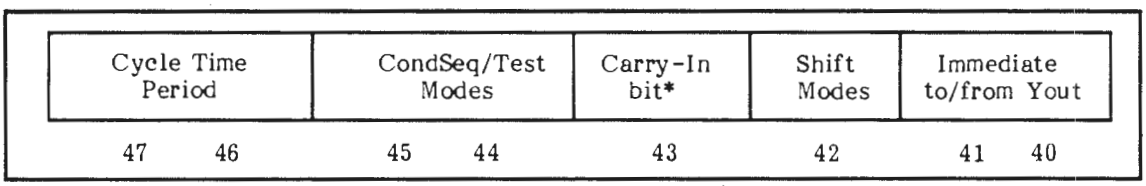


Figure 3-3: AUXILIARY CONTROL FIELD

Bits 46-47: Cycle Time Period

These two bits select the total time period allotted for the current cycle, using the following choices of bits 47 and 46:

Bit # 47 46		
0-0	125.0 nanoseconds	{TICK6}
0-1	104.2 nanoseconds	{TICK5}
1-0	83.3 nanoseconds	{TICK4}
1-1	62.5 nanoseconds	{TICK3}

Bits 44-45: Conditional Sequence/Test Modes

CondSeq/test modes, indexed by bits 45 and 44:

If = 0

The present instruction is one of the test mode instructions, in particular the **test/implicit branch** mode. In this mode, Bits 0-7 are divided into a test selection field (Bits 0-3) and an implicit branch field (Bits 4-7). The next instruction to be executed is determined by these two fields, and is limited to three possibilities: the next instruction in the pipeline, the instruction one later than the one in the pipeline, or the instruction in the writeable control store ("Replace") register. Refer to the section on Conditional Sequence/Test for additional information.

If = 1

The present instruction is also one of the test mode instructions, in this case the **test/processor control point (PCP)** mode. In this mode, bits 0-7 are divided into a test selection field (bits 0-3), a repeat-exit polarity field (bit 4), and a processor control point field (bits 5-7). The next instruction to be executed will be the next instruction in the pipeline (i.e., no effect on program sequencing). For further information, refer to the section on Test/Processor Control Points.

If = 2

The present instruction is a **conditional sequencer** mode instruction, which uses bits 0-7 to provide two alternate 4-bit choices of 2911A controls (depending on the value of the test flipflop, as set at the end of the last instruction) with:

Bits 0-3 used if TEST = 1
Bits 4-7 used if TEST = 0.

For further information, refer to the section on the Conditional Sequencer Field.

If = 3

The present instruction is also a **conditional sequencer** mode instruction, and is identical to the previous case, except that the microcode page (Bank) in two instruction-times is changed to that of the **pageN** register. The pageN register is located in the third 2911A (most significant nibble of microcode address), and is set by an I/O write. For further information, refer to the section on the Conditional Sequencer Field.

Note that four extra states are available for each of the 2911A control fields. These indicate Flush/NOP versions of four 2911A control choices (i.e., the next instruction in the pipe is effectively NOPied, by gating all clocks except those needed for the sequencer). The sequence state fed to the 2911A during this NOP is that of continue (i.e., the instruction executed two after the NOP will be taken from a microcode address one later than the address of the instruction immediately after the NOP). See details of conditional sequencer field.

Bit 43: Carry-In Bit (Inverted)

This bit is the inverted carry-in bit, unless a PCP (Processor Control Point) operation forces in an alternate one (using a logical OR).

Bit 42: Shift Modes

This bit selects the external carry structure for ALU shifts, with a great deal of influence from bits 30 and 31 (actually, bit 42 doubles the shift options for each direction already made possible by the 2901).

If bit 31 = 0

Right shift/rotates are done, with the following results for particular choices of bits 30 and 42 (with R0d meaning a one-clock-delayed R0):

Bit # 42	30			
0-0	R7 = C[t-1]	Q7 = R0	[Double RShift]	{DRS}
0-1	R7 = R0	Q7 = Q0	[Dual RRotate]	{DRR}
1-0	R7 = 0	Q7 = X	[Logical RShift]	{LRS}
1-1	R7 = R0d	Q7 = X	[Multprec RShift]	{MRS}

If bit 31 = 1

Left shift/rotates are done, with the following results for particular choices of bits 30 and 42 (with R7d meaning a one-clock-delayed R7):

Bit # 42	30			
0-0	R0 = Q7	Q0 = C[t-1]	[Double LShift]	{DLS}
0-1	R0 = R7	Q0 = Q7	[Dual LRotate]	{DLR}
1-0	R0 = 0	Q0 = X	[Logical LShift]	{LLS}
1-1	R0 = R7d	Q0 = X	[Multprec LShift]	{MLS}

Bits 40-41: Immediate To/From Yout

These two bits determine whether bits 8-15 will replace the normal output of the 2901 (i.e., Y bus) for its various loading activities, whether the Y bus bits will replace the normal output of microcode bits 8-15 (for loading the branch address into the 2911A and for addressing the data RAM), whether a delayed version of Y bus (Y register) will replace bits 8-15, or whether bits 8-15 and the Y bus are left uncoupled. These actions are for the following choices of bits 41 and 40:

Bit # 41 40	
0-0	Bits 8-15 drive Y bus
0-1	Y bus drives lines from bits 8-15
1-0	Normal (uncoupled)
1-1	Y register drives lines from bits 8-15

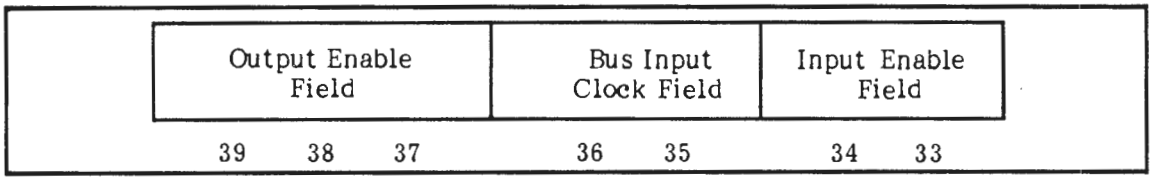


Figure 3-4: INPUT/OUTPUT FIELD

Bits 37-39: Output Clock Enables

The following are loaded from the Yout Bus at the end of the current cycle:

	Bit # 39 38 37		
	0-0-0	No load operation	(no address bits)
	0-0-1	Load data RAM	(M8-M15 as address bits)
	0-1-0	Load/update multiplier	(no address bits)
	0-1-1	Load loop counter	(no address bits)
(1)	1-0-0	Load I/O bus registers	(B0-B3 as address bits)
	1-0-1		
(2)	1-1-0	Load misc registers	(B0-B3 as address bits)
(3)	1-1-1	Load WCS registers	(B0-B2 as addr bits)

(1) Load I/O Bus Registers for both S-100 & C bus

	Bit # B3 B2 B1 B0		
	0-0-0-0	Load S-100 address bus bits 0-7	{SADDR0 =}
	0-0-0-1	Load S-100 address bus bits 8-15	{SADDR1 =}
	0-0-1-0	Load S-100 address bus bits 16-23	{SADDR2 =}
	0-0-1-1	Load S-100 data bus bits 0-7	{SDATA0 =}
	0-1-0-0	Load S-100 data bus bits 8-15	{SDATA1 =}
#	0-1-0-1	Load S-100 status lines	{SSTAT =}
#	0-1-1-0	Load S-100 control output lines	{SCTRLO =}
#	0-1-1-1	Load S-100 control input lines	{SCTRLI =}
#	1-0-0-0	Load S-100 DMA control lines	{SDMA =}
#	1-0-0-1	Load S-100 utility/reserved/non-defined	{SUTIL =}
	1-0-1-0		
	1-0-1-1	Load C bus address bus bits 0-7	{CADDR0 =}
	1-1-0-0	Load C bus address bus bits 8-15	{CADDR1 =}
	1-1-0-1	Load C bus data bus bits 0-7	{CDATA =}
#	1-1-1-0	Load C bus access lines	{CACCS =}
#	1-1-1-1	Load C bus mimic lines	{CMIMIC =}

Read Multiplier Product (Bit 42)

0	Read LS byte of product	{= PRODUCT0}
1	Read MS byte of product	{= PRODUCT1}

(2) Load Misc Registers

	B3 B2 B1 B0		
#	X-0-0-0	Load misc register (8 bits)	{MISC =}
	X-0-0-1	Load pageN (Bank) register (4 bits)	{PAGEN =}
#	X-0-1-0	Load flag register (4 bits, address latch)	{FLAGS =}
	X-0-1-1	Load ATEST selection reg. (3-6 bits)	{ATEST =}
	X-1-0-0	Load data RAM bank register (6 bits)	{DBANK =}
#	X-1-0-1	Load S-100 & C bus tri-state enable Reg.	{SCTRE =}
#	0-1-1-0	Load S-100 RAM-mapped I/O Control & RAM	{SIORAM =}
#	0-1-1-1	Load C bus RAM-mapped I/O Control & RAM	{CIORAM =}
#	1-1-1-0	Load S-100 RAM-mapped I/O Control	{SIOCTR =}
#	1-1-1-1	Load C bus RAM-mapped I/O Control	{CIOCTR =}

(3) Load WCS Registers

	Bit # B3 B2 B1 B0		
	X-0-0-0	Load WCS data bits 0-7	{WCS0 =}
	X-0-0-1	Load WCS data bits 8-15	{WCS1 =}
	X-0-1-0	Load WCS data bits 16-23	{WCS2 =}
	X-0-1-1	Load WCS data bits 24-31	{WCS3 =}
	X-1-0-0	Load WCS data bits 32-39	{WCS4 =}
	X-1-0-1	Load WCS data bits 40-47	{WCS5 =}
	X-1-1-0		
	X-1-1-1	Generate a load cycle (Next instruction)	{WCSLD =}

Read Misc Input Registers

	Bit # 3 2 1 0		
	0-0-0-0	Read S-100 data bus bits 0-7	{= SDATA0}
	0-0-0-1	Read S-100 data bus bits 8-15	{= SDATA1}
#	0-0-1-0	Read S-100 control lines	{= SCTRL }
#	0-0-1-1	Read S-100 utility/reserved/non-defined	{= SUTIL }
	0-1-0-0	Read C bus data bus bits 0-7	{= CDATA }
#	0-1-0-1	Read C bus control lines	{= CCTRL }
	0-1-1-0	Read Z80/68000 attention register	{= ATTREG}
	0-1-1-1		
	1-X-X-0	Read loop Control	{= LC }
	1-X-X-1	Read squirrel register	{= SQREG }

USING BIT-NUMBER AS ARGUMENT (unless otherwise stated):

Load Flag Register (Y3 = bit value and Y0-Y2 = bit-state address)
(addressable latch--only one bit at a time)

0	Flag1 (same processor)	
1	Flag2 (same processor)	
2	Flag3 (to other processor)	
3	Flag4 (to other processor)	
4	ForceWCS (1 = no microcode ROM)	
5	MC2 /	\
6	MC1 | Main clock phase-locked loop control	|
7	MC0 \	/

Load S-100 and C bus tri-state enable register {SCTRE =}

0	CXTS*	(C bus extra lines enable)
1	CHSTS*	(C bus heavy-signals enable)
2	CDBTS*	(C bus data bus enable)
3	CABTS*	(C bus address bus enable)
4	SXTS*	(S-100 extra lines enable)
5	SHSTS*	(S-100 heavy-signals enable)
6	SDBTS*	(S-100 data bus enable)
7	SABTS*	(S-100 address bus enable)

Load S-100 RAM-mapped I/O Control & RAM {SIORAM =, SIOCTR =}

0	Bit 0 of Control	
1	Bit 1 of Control	
2	Bit 2 of Control	
3	Bit 3 of Control	
4	pWR* bit of RAM	(S-100 pin 77)
5	sWO* bit of RAM	(S-100 pin 97)
6	pDBIN bit of RAM	(S-100 pin 78)
7	sMEMR bit of RAM	(S-100 pin 47)

Load C bus RAM-mapped I/O Control & RAM {CIORAM =, CIOCTR =}

0	Bit 0 of Control	
1	Bit 1 of Control	
2	Bit 2 of Control	
3	Bit 3 of Control	
4	WR* bit of RAM	(C bus pin 35)
5	MREQ* bit of RAM	(C bus pin 37)
6	RD* bit of RAM	(C bus pin 33)
7	[Not used]	

Load S-100 status lines {SSTAT =}

0	[Not used]	
1	sM1	(S-100 pin 44)
2	sINP	(S-100 pin 46)
3	sOUT	(S-100 pin 45)
4	[Not used]	
5	sINTA	(S-100 pin 96)
6	sHLTA	(S-100 pin 48)
7	sXTRQ*	(S-100 pin 58)

Load S-100 control output lines {SCTRLO =}

0	pSTVAL*	(S-100 pin 25)
1	pHLDA	(S-100 pin 26)
2	xRDY	(S-100 pin 3)
3	[Not used]	
4	[Not used]	
5	[Not used]	
6	[Not used]	
7	[Not used]	

Load S-100 control input lines {SCTRLI =}

0	pRDY*	(S-100 pin 72)	O.C.	
1	pINT**	(S-100 pin 73)	O.C.	[68000 interrupt]
2	NMI**	(S-100 pin 12)	O.C.	[68000 interrupt]
3	pHOLD**	(S-100 pin 74)	O.C.	
4	SIXTN**	(S-100 pin 60)	O.C.	[new RAM boards]
5	DMA3**	(S-100 pin 14)	O.C.	[undefined]
6	SLVCLR**	(S-100 pin 54)	O.C.	
7	ForceBAO*	(DMA priority pin 1)		

Load S-100 DMA control lines and miscellaneous lines {SDMA =}

0	ADSB**	(S-100 pin 22)	O.C.	
1	DODSB**	(S-100 pin 23)	O.C.	
2	SDSB**	(S-100 pin 18)	O.C.	
3	CDSB**	(S-100 pin 19)	O.C.	
4	MEMDSB**	(S-100 pin 67)	O.C.	[PHANTOM* by Standard]
5	ERROR**	(S-100 pin 98)	O.C.	[68000 bus error mode]
6	[Not used]			
7	TSRE (Tri-state register enable)			

Load S-100 utility/reserved/non-defined lines {SUTIL =}

0	NDEF	(S-100 pin 21)	
1	MREQ*	(S-100 pin 65)	[NDEF by Standard]
2	RFSH*	(S-100 pin 66)	[NDEF by Standard]
3	EXTAD*	(S-100 pin 27)	[RFU by Standard]
4	RFU	(S-100 pin 28)	
5	RFU	(S-100 pin 69)	
6	Z80/68*	(S-100 pin 71)	[RFU by Standard]
7	[Not used]		

Load C bus Access lines {CACCS =}

0	BUS-AVAILABLE*	(C bus pin 41)
1	M1*	(C bus pin 36)
2	IORQ*	(C bus pin 38)
3	[Not used]	
4	[Not used]	
5	[Not used]	
6	[Not used]	
7	[Not used]	

Load C bus mimic lines {CMIMIC =}

0	RESET*	(C bus pin 2)
1	RFSH*	(C bus pin 39)
2	HALT*	(C bus pin 42)
3	[Not used]	
4	[Not used]	
5	[Not used]	
6	[Not used]	
7	[Not used]	

Read S-100 control lines {= SCTRL}

0	pRDY	(S-100 pin 72)	O.C.	
1	pINT*	(S-100 pin 73)	O.C.	[68000 interrupt]
2	NMI*	(S-100 pin 12)	O.C.	[68000 interrupt]
3	pHOLD*	(S-100 pin 74)	O.C.	
4	SIXTN*	(S-100 pin 60)	O.C.	[new RAM boards]
5	PseudoBAI	(DMA priority pin 2)		
6	pHLDA	(S-100 pin 26)		
7	[Not used]			

Read S-100 utility/reserved/non-defined lines {= SUTIL}

0	NDEF	(S-100 pin 21)	
1	MREQ*	(S-100 pin 65)	[NDEF by Standard]
2	RFSH*	(S-100 pin 66)	[NDEF by Standard]
3	EXTAD*	(S-100 pin 27)	[RFU by Standard]
4	RFU	(S-100 pin 28)	
5	RFU	(S-100 pin 69)	
6	Z80/68*	(S-100 pin 71)	[RFU by Standard]
7	PWRFAIL*	(S-100 pin 13)	

Read C bus control lines {= CCTRL}

0	BUS-AVAILABLE*	(C bus pin 41)
1	PHI*	(C bus pin 3)
2	WAIT*	(C bus pin 5)
3	CPU-DISCONNECT*	(C bus pin 40)
4	INT*	(C bus pin 44)
5	NMI*	(C bus pin 45)
6	[Not used]	
7	[Not used]	

Bits 35-36: External Bus Input Clock Enables

Bit 35 causes all of the S-100 input information to be stored at the end of the current cycle, while bit 36 does the same for the C bus inputs. The following operations occur for bits 36 and 35:

Bit # 36 35	
0-0	Clock in neither S-100 nor C bus information
0-1	Clock in S-100 input information
1-0	Clock in C bus input information
1-1	Clock in both S-100 and C bus information

Bits 33-34: Input Enables

These two bits decode into input enables for loading onto the Din bus. The following are allowed to drive the bus using these values of bits 34 and 33 (address bits An mean the 2901 An bits, Bn mean the 2901 Bn bits, and Mn mean microcode bits 8-15, whether generated by the microcode address store, by Yout, or by Yreg):

	Bit # 34 33		
	0-0	Enable Yout-Din by pass	(no address bits)
*	0-1	Read multiplier product	(M42 as address bit)
	1-0	Read data RAM	(M8-M15 as address bits)
*	1-1	Read misc input registers	(A0-A3 as address bits)

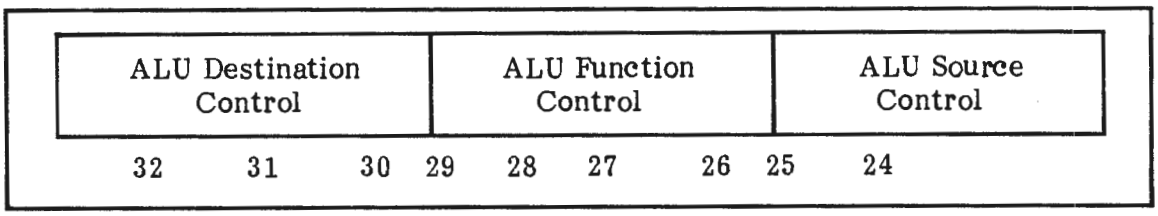


Figure 3-5: 2901C CONTROL FIELD

Tables 3-1, 3-2, and 3-3 list ALU destination and shift control, ALU function control, and ALU source control, respectively.

Table 3-1: ALU DESTINATION AND SHIFT CONTROL

Microcode Bits 32,31,30	RAM FCT		Q-reg FCT		Y	RAM SHIFTER		Q SHIFTER	
	shift	load	shift	load	OUTPUT	RAM0	RAM7	Q0	Q7
000 [0]	X	none	none	F->Q	F	X	X	X	X
001 [1]	X	none	X	none	F	X	X	X	X
010 [2]	none	F->B	X	none	A	X	X	X	X
011 [3]	none	F->B	X	none	F	X	X	X	X
100 [4]	down	F/2->B	down	Q/2->Q	F	F0	IN7 In(R7)	Q0	IN7 In(Q7)
101 [5]	down	F/2->B	X	none	F	F0	IN7 In(R7)	Q0	X
110 [6]	up	2F->B	up	2Q->Q	F	IN0 In(R0)	F7	IN0 In(Q0)	Q7
111 [7]	up	2F->B	X	none	F	IN0 In(R0)	F7	X	Q7

Table 3-2: CARRY BIT/FLAG AND OVR FLAG FOR VARIOUS ALU FUNCTIONS

Microcode Bits 29,28,27	ALU Function	Carry	OVR
000 [0]	R + S	C8 [ALU]	C7 XOR C8
001 [1]	S - R	same as for "R + S", using R* in defns	
010 [2]	R - S	same as for "R + S", using S* in defns	
011 [3]	R OR S	AnyZero[(R OR S)] v Cn	same as Carry
100 [4]	R AND S	AnyOne[(R AND S) v Cn]	same as Carry
101 [5]	R* AND S	AnyOne[(R* AND S) v Cn]	same as Carry
110 [6]	R XOR S	same as for "R XNOR S", using R* in defns	
111 [7]	R XNOR S	see 2901 specifications for logic eqns	

Notes: AnyZero [X v Cn] = 1 if any bit of X == 0 or if Carry == 1
AnyOne [X v Cn] = 1 if any bit of X == 1 or if Carry == 1

Table 3-3: SOURCE OPERAND AND ALU FUNCTION MATRIX

Bits 29, 28, and 27 ALU Function			Bits 26, 27, and 24 Source							
			000 [0]	001 [1]	010 [2]	011 [3]	100 [4]	101 [5]	110 [6]	111 [7]
			A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
	000 [0]	Cn=0 R + S Cn=1	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
	001 [1]	Cn=0 S - R Cn=1	Q-A-1 Q-A	B-A-1 B-A	Q-1 Q	B-1 B	A-1 A	A-D-1 A-D	Q-D-1 Q-D	-D-1 -D
	010 [2]	Cn=0 R - S Cn=1	A-Q-1 A-Q	A-B-1 A-B	-Q-1 -Q	-B-1 -B	-A-1 -A	D-A-1 D-A	D-Q-1 D-Q	D-1 D
	011 [3]	R OR S	AvQ	AvB	Q	B	A	DvA	DvQ	D
	100 [4]	R AND S	A.Q	A.B	0	0	0	D.A	D.Q	0
	101 [5]	R AND S	$\overline{A}$.Q	$\overline{A}$.B	Q	B	A	$\overline{D}$.A	$\overline{D}$.Q	0
	110 [6]	R XOR S	AxQ	AxB	Q	B	A	DxA	DxQ	D
	111 [7]	R XNOR S	$\overline{AxQ}$	$\overline{AxB}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{DxA}$	$\overline{DxQ}$	$\overline{D}$

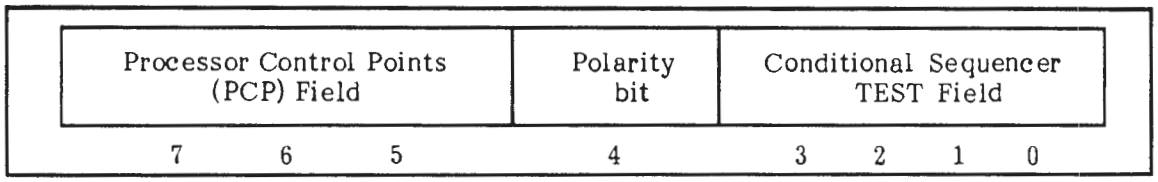


Figure 3-6: TEST AND PROCESSOR CONTROL POINTS FIELD OF CONSEQ/TEST MODES

Note: The following modes are **only** available when the CondSeq/Test field = 1. When this test mode is used, a Continue instruction is forced upon the 2911A, and these eight bits are available for other than 2911A control alternatives.

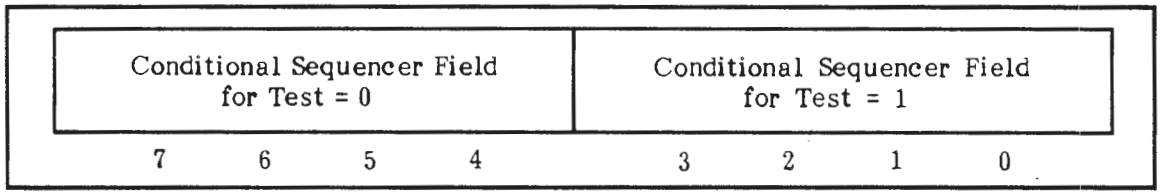


Figure 3-7: CONDITIONAL SEQUENCER FIELD

Note: The following modes are available when the Cond/Seq/Test field (bits 44 and 45) equals 2 or 3.

The following 16 conditional sequencing states are primarily the standard states from the 2911A, with bits 1 and 5 inverted with respect to the normal 2911A (i.e., S1, S0, FE*, and PUP); the four previously unused states are implemented, using NOP/FLUSH Mode options for Continue (i.e., SKIP) and Jump (i.e., JMP AR, JMP STK0, and JMP D). In the following list, the references are bits 3, 2, 1, and 0 and/or 7, 6, 5, and 4 and represent (approximately) S1, S0, FE, and PUP:

Microcode Bit # 3 2 1 0	2909/11	Mnemonic	Flush?	Action	Main Use
0-0-0-0	0 0 1 X	CONT	No	Continue	Continue
0-0-0-1	0 0 1 X	SKIP	Yes	Continue,Flush	Skip next Instr
0-0-1-0	0 0 0 0	POP	No	Cont,Pop Stack	End Loop
0-0-1-1	0 0 0 1	PUSH	No	Cont,Push uPC	Setup Loop
0-1-0-0	0 1 1 X	JMP AR	No	Jump to AR	Branch using AR
0-1-0-1	0 1 1 X	JMPF AR	Yes	JMP AR,Flush	Branch,NOP
0-1-1-0	0 1 0 0	RET AR	No	JMP AR,Pop Stk	End Subr
0-1-1-1	0 1 0 1	CALL AR	No	JMP AR,Push uPC	Jump Subr
1-0-0-0	1 0 1 X	JMP STK0	No	Jump to STK0	Loop Branch
1-0-0-1	1 0 1 X	JMPF STK0	Yes	LOOP,Flush	Loop,NOP
1-0-1-0	1 0 0 0	RET	No	LOOP,Pop Stk	Ret from Subr
1-0-1-1	1 0 0 1	CALL STK0	No	LOOP,Push uPC	
1-1-0-0	1 1 1 X	JMP addr	No	Jump to D	Branch using D
1-1-0-1	1 1 1 X	JMPF addr	Yes	JMP D,Flush	Branch,NOP
1-1-1-0	1 1 0 0	RET addr	No	JMP D,Pop Stk	End Subr
1-1-1-1	1 1 0 1	CALL addr	No	JMP D,Push uPC	Jump Subr

Bits 0-3: Conditional Sequencer Test Field

The following tests may affect the generation of the instruction 1, 2, or 3 time-slots later. The actual effect depends on the CondSeq/Test mode and the value of Test. The following selections use these choices of bits 3, 2, 1, and 0:

Bit # 3 2 1 0			
0-0-0-0	F=0	(set if 2901C ALU result = 0)	{ZERO}
0-0-0-1	CARRY	(carry out of 2901C)	{CARRY}
0-0-1-0	C[t-1]	(carry out delayed 1 clock)	{CDEL}
0-0-1-1	F7	(MS bit from 2901C ALU result)	{F7}
0-1-0-0	OVR	(arithmetic overflow)	{OVFL}
0-1-0-1	Cmid	(internal bit 3-to-4 carry)	{CMID}
0-1-1-0	Q0	(LS bit of Qreg, Rshifting	{Q0}
		Y6, Lshifting	{Y6}
		TEST[t-1], not shifting)	{TDEL}
0-1-1-1	Y0	(LS bit of Y bus)	{Y0}
1-0-0-0	LCNE0	(Loop counter != 0)	{LCNE0}
1-0-0-1	FLAG1	(from flag register)	{FLAG1}
1-0-1-0	FLAG2	(from flag register)	{FLAG2}
1-0-1-1	ARCLK	(Attention register clock)	{ARCLK}
1-1-0-0	INPCLK	(68000 input request clock)	{INPCLK}
1-1-0-1	ARFLAG	(Attention register A1 address bit)	{ARFLAG}
1-1-1-0	INT*	(Interrupt line)	{INTBAR}
1-1-1-1	FALSE		{FALSE}

These flags are tested at the end of the current cycle, using results from the present instruction.

Alternate Tests for Implicit Branch Determination

Alternate Test Selections.

If the Atest mode is chosen, one of the following tests is used, in conjunction with the polarity bit, to determine whether an implicit branch is to be taken. The three selections bits are preset by loading into the Atest register prior to calling for the results of the test. The following selections are common to both the I/O and arithmetic coprocessors, and use these choices of bits 2, 1, and 0 of the Atest register:

Bit # 2 1 0		
0-0-0	F=0	(set if 2901C ALU result = 0)
0-0-1	CARRY	(carry out of 2901C)
0-1-0	F7	(MS bit from 2901C ALU result)
0-1-1	LCne0	(Loop counter != 0, or != 0FFh)
1-0-0	FLAG1	(from flag register)
1-0-1	FLAG3	(spare input)
1-1-0	ARFLAG	(Attention register A1 address bit)
1-1-1	INT*	(Interrupt line)

These flags are tested at the end of the current cycle, using results from the present instruction.

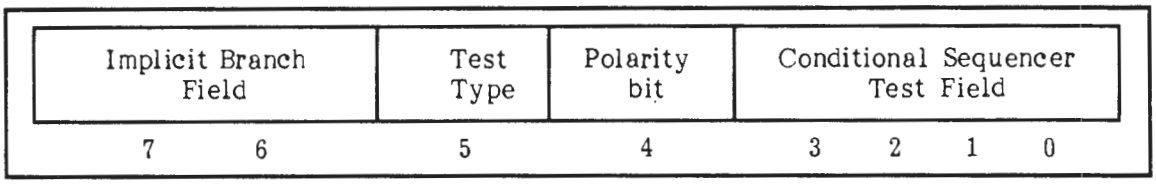


Figure 3-8: TEST & IMPLICIT BRANCH FIELD OF CONDSEQ/TEST MODES

Note: The following modes are **only** available when the CondSeq/Test field = 0. When this Test mode is used, a Continue instruction is forced upon the 2911A, and these eight bits are available for other than 2911A control alternatives.

Bits 6-7: Implicit Branch Field

These bits select one of the four types of implicit branches which may occur, assuming that the Test condition (as chosen by bits 4 and 5) calls for one. Bits 7 and 6 are used as indexes for the following:

Bit # 7 6		
0-0	Replace next instruction	{REPLACE }
0-1	Immediate Skip next instruction	{IMSKIP }
1-0	Repeat next instruction	{REPEAT }
1-1	Drop-through overrides next CondSeq instruction	{DROPTHRU}

Replace Next Instruction - If this mode is chosen, and the test is true, the Next instruction in line is replaced with the contents of the WCS register (which is assumed to have been set up to be the desired microcode instruction). The new instruction completely replaces the old instruction in the pipeline, including timing selection.

Immediate Skip Next Instruction - If this mode is selected, and the Test is true, the next instruction in line is immediately skipped (i.e., NOPied, in effect, by gating the clock to everything but the sequencing hardware). With this mode, both a Test and a limited CondSeq can be done in one instruction, instead of requiring one instruction to set up the test and one instruction to choose the CondSeq. If a NOP occurs, a Continue is forced upon the Sequencer during it; thus the instruction following the ImSkip target address directly follows it in time as well.

Note: The following are peculiar to a NOP cycle:

1. The timing selection (clock period choice) during a NOP is that of the instruction being ignored.

2. Test, C[t-1], R0d, and R7d are unchanged by the NOP (i.e., these flags appear the same, to the next instruction actually executed, whether or not the next instruction is skipped).

Repeat Next Instruction - If this mode is selected, and the Test is false, the next instruction is repeated until the test condition called for in it is true. If the Test is true, the next instruction in line is Imskipped. This instruction is more like "Imskip or repeat N times", while the actual Imskip instruction can be thought of as "Imskip or repeat Once". Thus, this presupposes that the next instruction is a test mode instruction. If the test/PCP mode is selected, the test field, along with the polarity bit, is used for exit determination. If the test/implicit branch mode is selected, the exit condition is the implicit test field (which may be test or ATEST). Upon exit, either a NOP is forced for the last repeat instruction (if test/PCP mode) or an implicit branch is done (if test/implicit branch mode). The comments made earlier about the NOP cycle hold here.

Drop-Thru Overrides Next CondSeq Instruction - If this mode is chosen, and the Test is true, the drop-through flipflop is set. This forces the next CondSeq instruction to be a Continue, despite what it may otherwise evaluate to be. This can be used in loops, for example, along with the loop counter decrement, to exit when the count reaches zero, irrespective of other tests going on.

Bit 5: Test Type

This bit chooses the type of test used to decide whether or not the implicit branch is executed.

If = 0

The main test field (Test) is used, with bits 0-3 providing the selection field.

If = 1

The alternate test MUX (ATEST) is used, with selection previously set by loading the alternate test selection register (ATEST register).

Bit 4: Polarity Bit

This bit selects the polarity of the test (as selected by bit 5) needed to execute the Implicit Branch.

If = 0

A False value will cause an implicit branch.

If = 1

A True value will cause an implicit branch.

Bits 5-7: Processor Control Points Field

These bits select one of eight processor control points, and require no operands. These actions are for the following choices of bits 7, 6, and 5:

	Bit # 7 6 5		
	0-0-0	Force Cin = Cin <or> Cin(delayed)	{+/- C}
	0-0-1	Clear loop counter	{LCCLR}
	0-1-0	Increment loop counter	{LCINC}
	0-1-1	Decrement loop counter	{LCDEC}
#	1-0-0	Update/load squirrel register	{LDSQR}
#	1-0-1	Toggle I/O RAM counter count-enable	{TIOCE}
	1-1-0	(spare)	{PCPSPARE}
	1-1-1	(no PCP operation)	

Update/load Squirrel Register - This enables the storing of the following flags, into a stable register, at the next clock; from there, they can be read into the 2901 using the proper I/O instruction. Using bit number as argument:

0	CARRY	(carry out of 2901C)
1	F=0	(set if 2901C ALU result = 0)
2	FLAG1	(from itself)
3	FLAG3	(from other Bipolar Processor)
4	Cmid	(2901C internal bit 3-to-4 carry)
5	LCne0	(Loop counter != 0, or != 0FFh if counting up)
6	OVR	(arithmetic overflow from 2901 ALU)
7	F7	(MSbit from 2901C ALU result)

Toggle I/O RAM Counter Count-Enable - When either I/O RAM Counter (one for the S-100 Bus and one for the C bus) is loaded, the count-enable flipflop is set. Thereafter, each successive Toggle alternates between stopping both counters and restarting them. Note that the effect of this instruction starts at different times, depending on whether the count-enable is about to be disabled or enabled. If the counter is about to be stopped, this instruction takes effect immediately (i.e., no count is made at the end of this instruction). If the counter is about to be restarted, it counts as of the next clock after the end of the present instruction.

Bit 4: Polarity Bit

This bit selects the polarity of the test (as selected by last instruction) needed to exit from the repeat loop.

If = 0

A false value will terminate the repeat loop.

If = 1

A true value will terminate the repeat loop.

Appendix A

PARTS LIST - MAX-C

Integrated Circuits

Designation	Cromemco Description	Part No.
IC1	CD4046B	011-0111
IC2	MC1658	010-0370
IC3	74S04	010-0123
IC4	74F175	010-0386
IC5	74F00	010-0372
IC6	74F139	010-0382
IC7	74F109	010-0380
IC8	74F534	010-0393
IC9	74F02	010-0373
IC10	2911A	010-0368
IC11-12	74F374	010-0392
IC13-14	2911A	010-0368
IC15	74F374	010-0392
IC16	74F245	010-0380
IC17	74F244	010-0340
IC18-19	25LS2569	010-0396
	Sckt 20 pin	017-0004
IC20-23	74F374	010-0392
IC24	74LS393	010-0141
IC25	74F64	010-0378
IC26	74F194	010-0387
IC27	74F109	010-0380
IC28	74S51	010-0171
IC29	74F157	010-0384
IC30-31	74F374	010-0392
IC32	8168/6168/IMS1420-45ns	011-0110
IC32-37	Sckt 20 pin	017-0004
IC33	PROM MAX-C	502-0099
IC34-35	8168/6168/IMS1420-45ns	011-0110
IC36	PROM MAX-C	502-0100
IC37	8168/6168/IMS1420-45ns	011-0110
IC38-39	74F374	010-0392
IC40	74F00	010-0372
IC41	74F151	010-0383

Integrated Circuits (Continued)

Designation	Cromemco Description	Part No.
IC42	74LS259	010-0137
IC43	74F253	010-0390
IC44	2901C	010-0367
	Sckt 40 pin	017-0006
IC45	74LS169	010-0144
IC46	74F64	010-0378
IC47	74F10	010-0376
IC48-49	74F374	010-0392
IC50	8168/6168/IMS1420-45ns	011-0110
IC51	PROM MAX-C	502-0101
IC50-55	Sckt 20 pin	017-0004
IC52-53	8168/6168/IMS1420-45ns	011-0110
IC54	PROM MAX-C	502-0102
IC55	8168/6168/IMS1420-45ns	011-0110
IC56-57	74F374	010-0392
IC58	2901C	010-0367
	Sckt 40 pin	017-0006
IC59	74LS378	010-0146
IC60	74F253	010-0390
IC61-62	74S00	010-0036
IC63	74F02	010-0373
IC64	74F00	010-0372
IC65	74F08	010-0375
IC66	74F32	010-0377
IC67	74F251	010-0389
IC68	74F352	010-0354
IC69	74F138	010-0381
IC70-71	74F374	010-0392
IC72	8168/6168/IMS1420-45ns	011-0110
IC73	PROM MAX-C	502-0103
IC72-77	Sckt 20 pin	017-0004
IC74-75	8168/6168/IMS1420-45ns	011-0110
IC76	PROM MAX-C	502-0104
IC77	8168/6168/IMS1420-45ns	011-0110
IC78-79	74F374	010-0392
IC80-81	74F138	010-0381
IC82	74F139	010-0382
IC83	74F251	010-0389
IC84	74F04	010-0374
IC85	74F251	010-0389
IC101	SG3524	010-0326

**Diodes/
Transistors**

Designation	Cromemco Description	Part No.
D1-3	1N4148/1N914	008-0002
D101	1N752A 5.6V	008-0056
D102	1N5231B 5.1V	008-0006
D103	UES1002 1A/100V 25ns	008-0071
D104	IR10TQ040	008-0072
D105	1N5231B 5.1V	008-0006
Q1	2N3906	009-0002
Q-2	2N3904	009-0001
Q101	SCRS2600	009-0048
Q102	2N3906	009-0002
Q103	2N3904	009-0001
Q104	2N3906	009-0002
Q105	D45VH10	009-0035
Q106	D44VH10	009-0047

Capacitors

Designation	Cromemco Description	Part No.
C1	0.15 uf 250V pycb	004-0131
C2	10 pf 1000V crdc	004-0001
C3	0.001 uf 50V card	004-0062
C4	68 pf crdc	004-0051
C5	100 pf 1000V crdc	004-0008
C6	1 uf 25V mono	004-0070
C101-103	470 uf 6.3V vari	004-0091
C104	0.01 uf 100V tcs	004-0037
C105	0.1 uf 10V crdc	004-0030
C106	220 pf 1000V crdc	004-0018
C107	0.022 uf 50V crdc	004-0036
C108	1 uf 25V mono	004-0070
C109	0.001 uf 1000V crdc	004-0022
C110-111	3.0 uf 50V pycb	004-0130
C112	0.047 uf 50V	004-0061
C113	220 pf 1000V crdc	004-0018
C114	100 pf 1000V crdc	004-0008
C115	0.1 uf 10V crdc	004-0030
-o-	0.047 uf 50V	004-0061

Resistors

Designation	Cromemco Description	Part No.
R1	220 ohm 1/4 5%	001-0010
R2	1 Kohm 1/4 5%	001-0018
R3	560 ohm 1/4 5%	001-0015
R5-7	1 Kohm 1/4 5%	001-0018
R8-10	470 ohm 1/4 5%	001-0014
R11-12	1 Kohm 1/4 5%	001-0018
R101	820 ohm 1/4 5%	001-0017
R114	3.3 Kohm 1/4 5%	001-0041
R115	16.9 Kohm 1/4 1%	001-0158
R118	3.9 Kohm 1/2 5%	001-0192
R119	0.05 ohm 3W 5%	001-0232
R120	20 ohm 3W 5%	001-0046

Resistor Networks

Designation	Cromemco Description	Part No.
RN1	9 pin Custom	003-0086
RN2	7 pin Custom	003-0085
RN101	10 pin Custom	003-0077
RN102	7 pin Custom	003-0076

Inductors

Designation	Cromemco Description	Part No.
L1	150 uH 0.5A	007-0027
L101	22 uH	007-0000
L102	30 uH	007-0025
L103	35 uH	007-0024

Miscellaneous

Designation	Cromemco Description	Part No.
	#6 split lock washer	015-0020
	4-40X1/4 ph slot cad	015-0076
	4-40X3/16X7/16 standoff	015-0083
	4-40X5/16 flat head	015-0182
	6-32X3/8 nylon	015-0183
	Heatsink 25W	016-0292
	Nutplate	016-0300
J1	Sckt wafer 2 pin	017-0009
IB1-7	10 pin Header	017-0384
F101	Fust 7A 125V	108-0039
	MAX-C PCB	020-0101
	3 Reg. sil-pad	021-0185
	Mounting pad	021-0186

Appendix B

PARTS LIST - MAX-I

Integrated Circuits

Designation	Cromemco Description	Part No.
IC1	74F08	010-0375
IC2-9	2168/8168/IMS1420-55ns	011-0110
	Sckt 20 pin	017-0004
IC10,11	74F374	010-0391
IC12	74F374	010-0392
IC16	74F374	010-0392
IC17	74F109	010-0380
IC18	74F00	010-0372
IC19	74F139	010-0382
IC20	74F00	010-0372
IC21	74F138	010-0381
IC22	74S139	010-0297
IC23	74LS378	010-0146
IC24	74F374	010-0392
IC25	74S557	010-0371
	Sckt 40 pin	017-0006
IC26,27	74F374	010-0392
IC28	74F138	010-0381
IC29	74F04	010-0374
IC30	74F169	010-0385
IC31	AM27S07	010-0369
IC32	74LS173	010-0119
IC33	74F04	010-0374
IC34	7405	010-0029
IC35	74LS273	010-0107
IC36	7405	010-0029
IC37,38	74F374	010-0392
IC39	PROM MAX-I	502-0098
	Sckt 20 pin	017-0004
IC40-43	74F374	010-0392
IC44	74F138	010-0381
IC45	74F32	010-0377
IC46	74F169	010-0385
IC47	AM27S07	010-0369
IC49	7405	010-0029

Integrated Circuits (Continued)

Designation	Cromemco Description	Part No.
IC50	74F374	010-0392
IC51	74LS273	010-0107
IC52-58	74F374	010-0392
IC48	74LS173	010-0119
IC59,60	74F138	010-0381
IC61	74F02	010-0373
IC62	74F00	010-0372
IC63	74F86	010-0379
IC101	SG3524	010-0326

Diodes/ Transistors

Designation	Cromemco Description	Part No.
D101	1N752A 5.6V	008-0056
D102	IN5231B 5.1V	008-0006
D103	UES1002 1A/100V 25ns	008-0071
D104	IR10TQ040	008-0072
D105	IN5231B 5.1V	008-0006
Q101	SCR S2600	009-0048
Q102	2N3906	009-0002
Q103	2N3904	009-0001
Q104	2N3906	009-0002
Q105	D45VH10	009-0035
Q106	D44VH10	009-0047

Capacitors

Designation	Cromemco Description	Part No.
C101-103	470 uf 6.3V	004-0091
C104	0.01 uf 100V tcs	004-0037
C105	0.1 uf 10V crdc	004-0030
C106	220 pf 1000V crdc	004-0013
C107	0.022 uf 50V crdc	004-0036
C108	1 uf 25V mono	004-0070

Capacitors (Continued)

Designation	Cromemco Description	Part No.
C109	0.001 uf 1000V crdc	004-0022
C110,111	3.0 uf 50V pycb	004-0130
C112	0.047 uf 50V	004-0061
C113	220 pf 1000V crdc	004-0013
C114	100 pf 1000V crdc	004-0008
C115	0.1 uf 10V crdc	004-0030
-o-	0.047 uf 50V	004-0061

Resistors

Designation	Cromemco Description	Part No.
R101	820 ohm 1/4 5%	001-0017
R114	3.3 Kohm 1/4 5%	001-0041
R115	16.9 Kohm 1/4 1%	001-0158
R118	3.9 Kohm 1/2 5%	001-0192
R119	0.05 ohm 3W 5%	001-0232
R120	20 ohm 3W 5%	001-0046

Resistor Networks

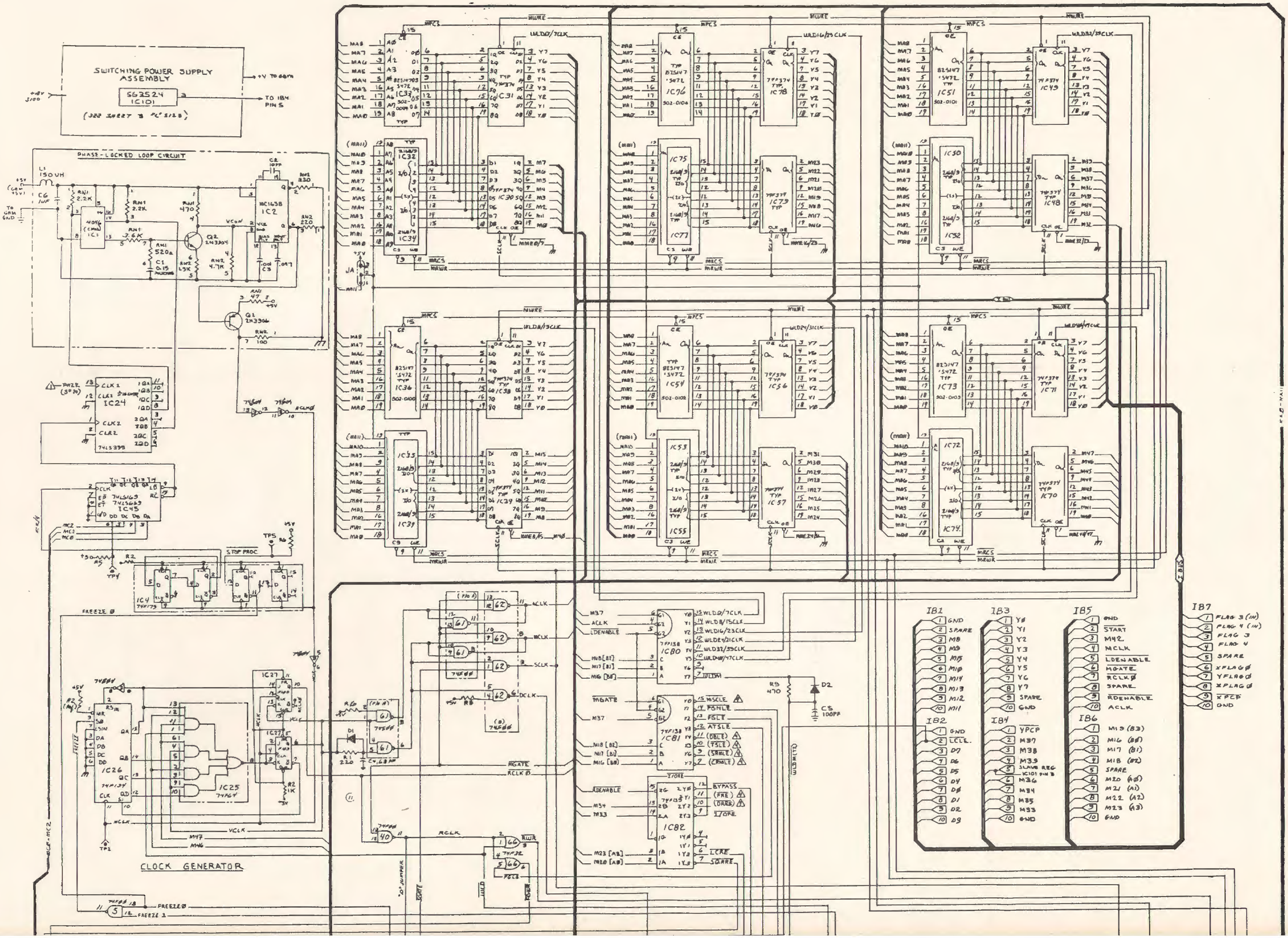
Designation	Cromemco Description	Part No.
RN1	1.0 Kohm 7R 8P	003-0007
RN2,3	2.2 Kohm 7R 8P	003-0008
RN4	1.0 Kohm 9R 10P	003-0011
RN5	2.2 Kohm 7R 8P	003-0008
RN101	10 pin Custom	003-0077
RN102	7 pin Custom	003-0076

Inductors

Designation	Cromemco Description	Part No.
L101	22 uH	007-0000
L102	30 uH	007-0025
L103	35 uH	007-0024

Miscellaneous

Designation	Cromemco Description	Part No.
	#6 split lock washer	015-0020
	4-40X1/4 ph slot cad	015-0076
	4-40X3/16X7/16 standoff	015-0083
	4-40X5/16 flat head	015-0182
	6-32X3/8 nylon	015-0183
	Heatsink 25W	016-0291
Htsnk Assy	Nutplate	016-0300
J2	Sckt wafer 2 pin	017-0009
J1	50 pin male connector	017-0033
IB1-7		017-0384
F101	Fuse 7A	018-0039
	MAX-I PCB	020-0100
	3 Reg. sil-pad	021-0185
	Mounting pad	021-0186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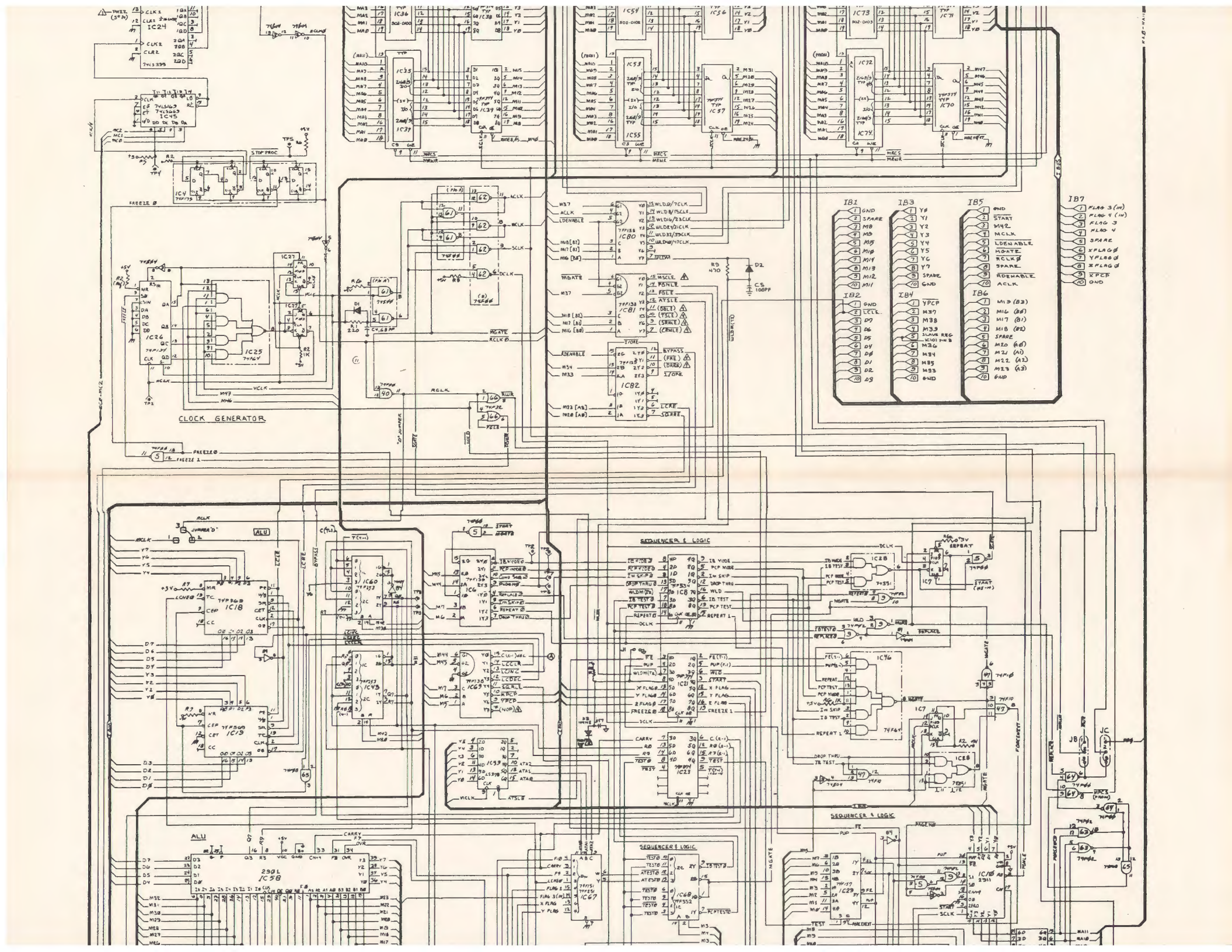
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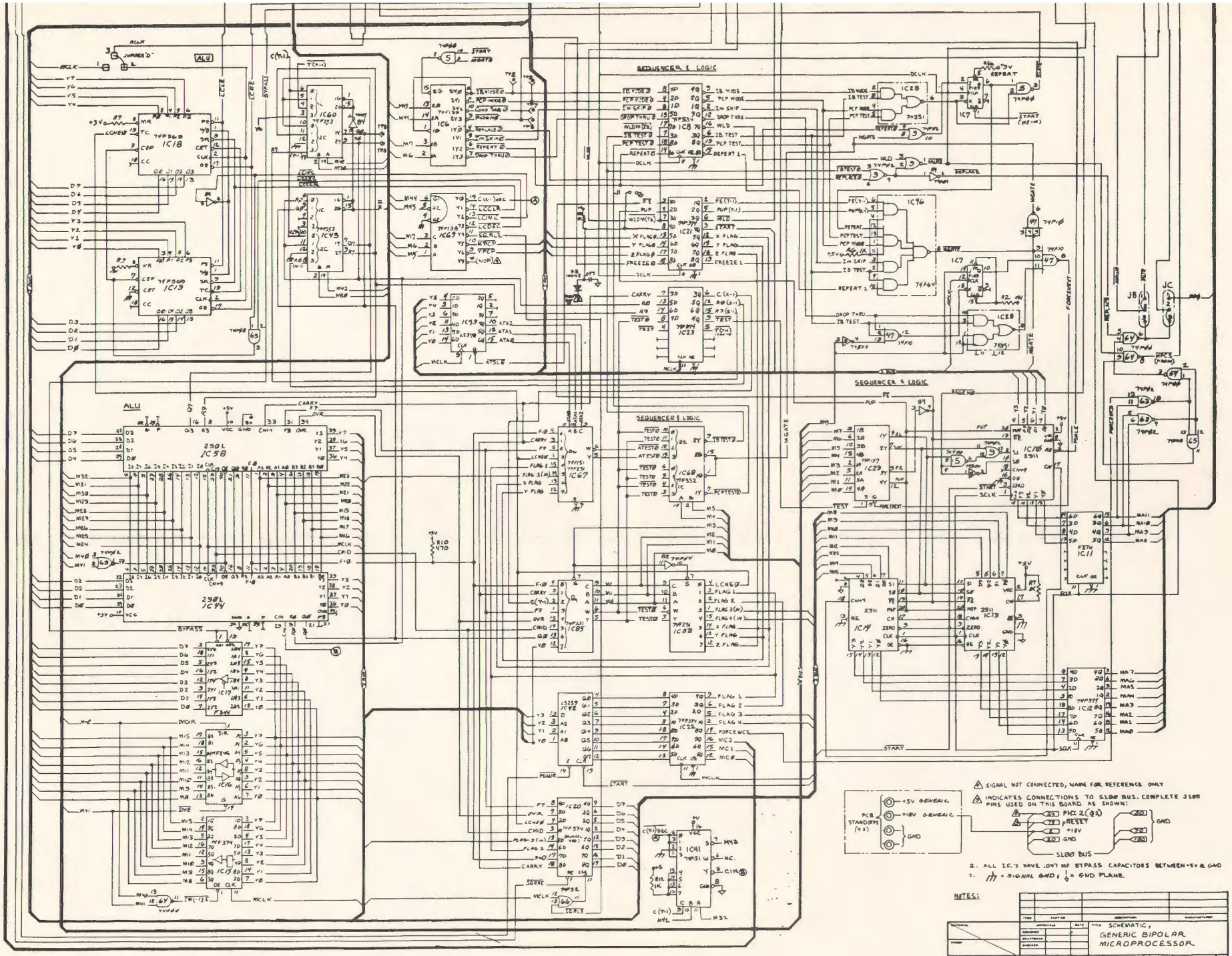
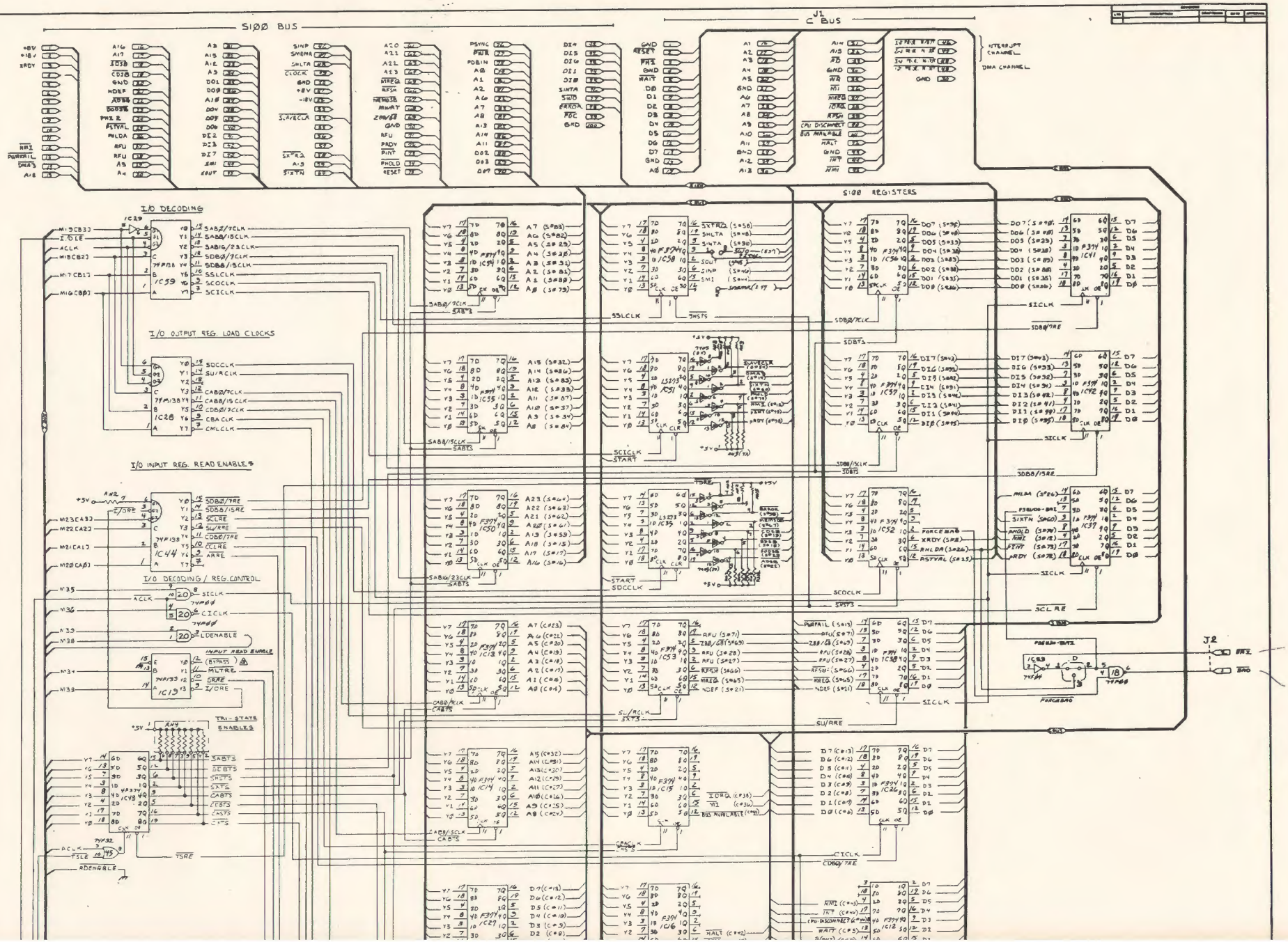
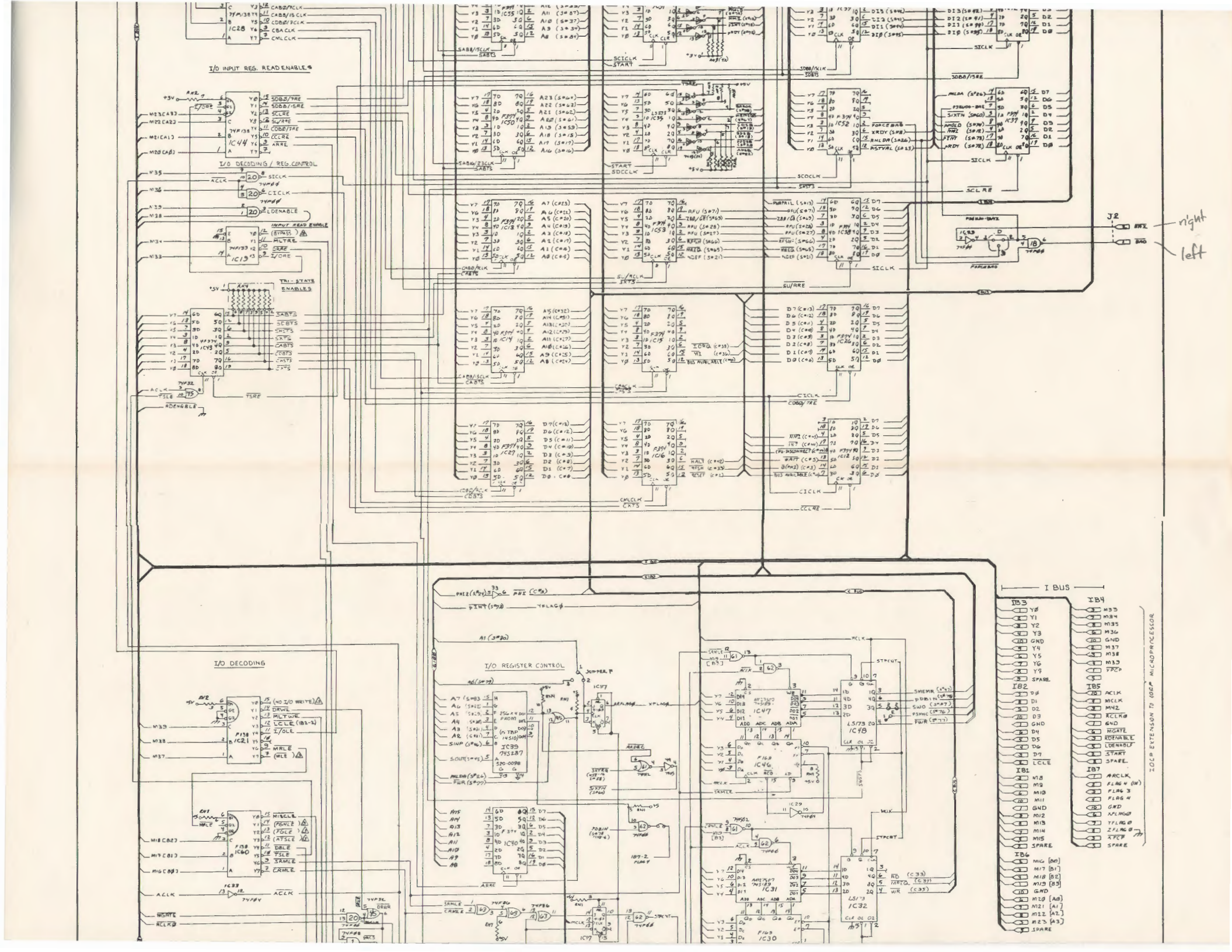
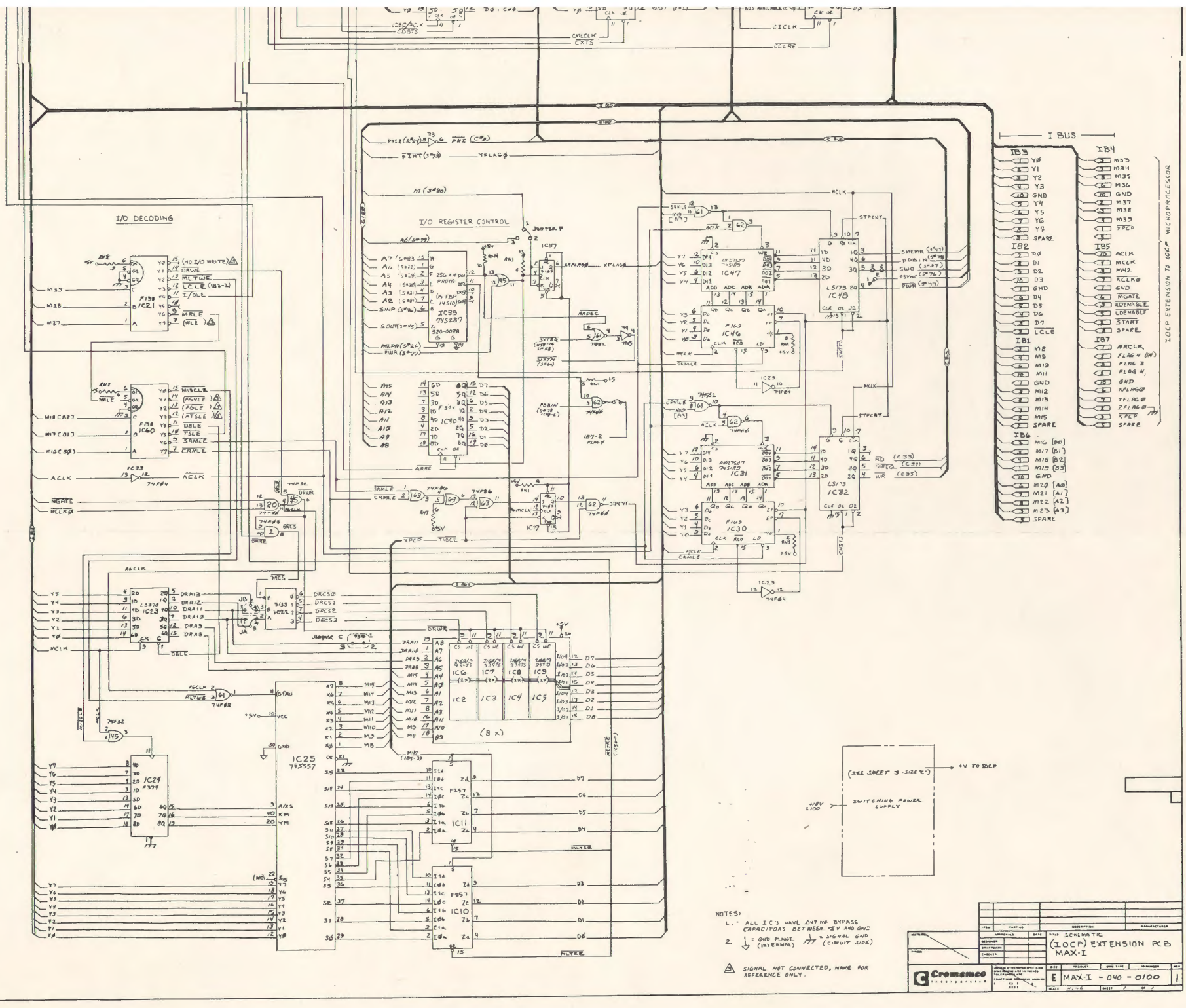

SEQUENCER & LOGIC
ALU
2901 IC58
2901 IC44
SEQUENCER & LOGIC
ALU
SEQUENCER & LOGIC
SCHEMATIC, GENERIC BIPOLAR MICROPROCESSOR
Cromemco
GBP - 040 - 0101
NOTES:
SIGNAL NOT CONNECTED, NAME FOR REFERENCE ONLY
INDICATES CONNECTIONS TO S100 BUS. COMPLETE S100 PINS USED ON THIS BOARD AS SHOWN:
SLOOB BUS
2. ALL I.C.'S HAVE .047 MF BYPASS CAPACITORS BETWEEN +5V & GND
1. = SIGNAL GND; = GND PLANE.


SIØØ BUS
J1
C BUS
I/O DECODING
I/O OUTPUT REG. LOAD CLOCKS
I/O INPUT REG. READ ENABLES
I/O DECODING / REG. CONTROL
TRI-STATE ENABLES
SIØØ REGISTERS
INPUT READ ENABLE
FORCEMAB
J2
right
left


I/O INPUT REG. READ ENABLES
I/O DECODING / REG. CONTROL
TRI-STATE ENABLES
I/O DECODING
I/O REGISTER CONTROL
I BUS
J2
right
left
I/O EXTENSION TO 68K MICROPROCESSOR


I/O DECODING
I/O REGISTER CONTROL
I BUS
IB3
IB4
IB5
IB2
IB1
IB6
IB7
IOCP EXTENSION TO IOCP MICROPROCESSOR
IC99 74S287
IC47
IC48
IC46
IC40
IC31
IC32
IC30
IC29
IC23
IC25 74S557
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IC11
(8 x)
(SEE SHEET 3 - SIZE C)
+V TO IOCP
SWITCHING POWER SUPPLY
NOTES:
1. ALL I.C.'S HAVE .047 MF BYPASS CAPACITORS BETWEEN +5V AND GND
2. = GND PLANE (INTERNAL) = SIGNAL GND (CIRCUIT SIDE)
SIGNAL NOT CONNECTED, NAME FOR REFERENCE ONLY.
SCHEMATIC
(IOCP) EXTENSION PCB
MAX-I
Cromemco
E MAX-I - 040 - 0100 1