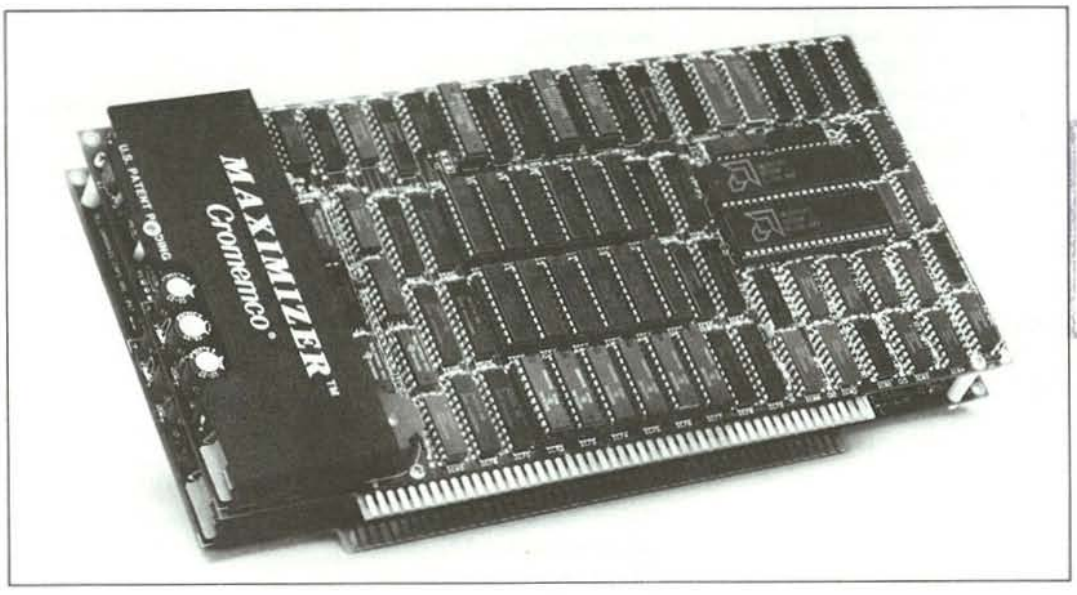
Cromemco®

MODEL MAXIMIZER
12 MIPS Microcoded Co-Processor



FEATURES

- ☐ High-Speed Co-Processor with On-Board Memory, I/O, and Bit-Slice ALU
- ☐ 12 Million Instruction Per Second (MIPS) Operating Speed
- ☐ Powerful Software Support:
  - IEEE Floating Point Package with Complete Set of Double Precision and Single Precision Functions
  - Microcode Assembler for User-Written Microprograms
- ☐ Works with Fast Languages — Fortran, Pascal and C
- ☐ Large On-Board Memories for Microprogram and Data
- ☐ High-Speed Access to Main Memory via 4 MB/S Direct Memory Access
- ☐ Typical Applications:
  - Signal Processing: Fourier Transform; Correlation; Digital Filtering
  - Graphics: 3-D rotation; Clipping; Scaling; Vector Generation
  - Engineering: Matrix Inversion; Polynomial Evaluation, Minimization/Maximization; Numerical Integration
  - Computer Science: Processor Emulation; Instruction Set Research; Multi-Processor/ Co-Processor Research; Algorithmic Execution Engine

PRODUCT DESCRIPTION

The Maximizer is a 12MIPS microcoded co-processor that can substantially increase the computational throughput of Cromemco 68000 Cromix systems. When used with the Cromemco Fast Fortran, Fast Pascal, or Fast C languages the Maximizer performs all IEEE double and single precision math functions. In addition, a microcode assembler is available which facilitates the writing of custom microcode for such applications as graphics primitives, matrix operations, or real-time cryptographic operations.

The Maximizer is ideally suited for use in computationally-intensive problems such as seismic analysis of geophysical resources, thermal transfer problems in mechanical engineering; circuit simulation in electrical engineering; and structural analysis in civil engineering. The key to the Maximizer's high speed is a 2900-series ECL technology bit-slice processor running at a 48 MHz master clock rate. The Maximizer has 16K bytes of high speed data memory, 16 dual-port registers, and 4K 48-bit words of downloadable microcode instruction store. Only 10 milliseconds are required to load the microcode from the host computer. This means that the personality of the Maximizer can be changed on-the-fly, by loading new microcode to suit the task at hand.

The Maximizer achieves very high speed operation by use of a 16 million operation per second multiplier chip, a doubly-pipelined instruction path, and state-machine controlled DMA transfers on the host bus. In addition, the clock period of the Maximizer adapts to the requirements of each microinstruction; most execute in 62.5 nanoseconds, but up to 125 nanoseconds are allowed for complex operations.

The microcode assembler model MAXASM allows the user to gain full control of the Maximizer hardware. Unlike conventional microassemblers, MAXASM frees the programmer from detailed consideration of individual fields within the microcode word. Assembler input takes the form of register transfer statements with several clauses on each line; MAXASM then partitions the buses and registers for optimum use, and, taking account of potential interactions between control fields, generates a microinstruction which satisfies the programmer's requirement.

TECHNICAL SPECIFICATIONS

Architecture:
Separate Processor and Interface boards comprising 2901C (ECL) bit sliced ALU; 16-bit high speed multiplier; separate program and data memories; writeable control store; high-speed I/O state machine for main bus DMA; high-speed state machine for C-bus interface; 2911 sequencers with extensive test selection logic; flexible triple-bus architecture; double-pipeline instruction path; microcode-selectable instruction timing.

Program Memory:
4096 words of 48 bits RAM (Writeable Control Store)
512 words of 48 bits PROM (Resident Microcode)
PROM/RAM overlay is microcode controlled
RAM downloaded from Host Via DMA

Data Memory:
16K bytes of 45 nSec RAM
Dual-ported 16 bytes RAM

Sequencing:
Two-branch conditional sequencing
Pipeline flush and repeat operations for three-way branch

S-100 Interface:
Occupies 2 locations in extended I/O space
I/O state machine controls 4 Megabyte/Second data transfer

C-bus Interface:
I/O state machine controls data transfer (4 MB/S maximum)

Instruction Cycle:
62.5-125 nSec, microcode controlled; phase-locked to system clock

Power Requirements:
+ 16 at 2 Amps maximum per board. On-card switching regulator for conversion to + 5 volts.

Bus:
S-100 (IEEE-696)

Operating System:
68000 Cromix

Software Support:
Fast Fortran
Fast Pascal
Fast C
(Note, languages above include IEEE Floating Point Microcode for Maximizer)
Microcode Assembler

Operating Environment:
0° to 55°C

Cromemco

Cromemco, Inc.
280 Bernardo Ave.
P.O. Box 7400
Mountain View, CA 94039
(415) 964-7400
TWX 910-379 6988

023-8285