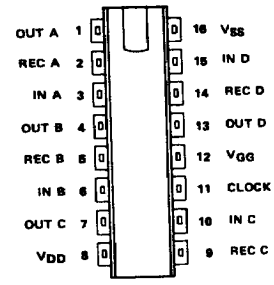
MOS
LSI

TMS 3409 JC, NC; TMS 3417 JC, NC
QUADRUPLE 80-, 64-BIT DYNAMIC SHIFT REGISTERS

BULLETIN NO. DL-S 7512266 REVISED NOVEMBER 1977

- 10-kHz to 5-MHz Operation
- Dynamic Configuration
- Single TTL-Compatible Clock
- Inputs and Outputs Fully TTL-Compatible
- On-Chip Recirculate Logic
- Power Supplies . . . 5 V, −12 V
- MOS Low-Threshold Self-Aligned-Gate Technology

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 3409 and TMS 3417 are quad 80-bit and quad 64-bit shift registers, respectively, with independent inputs, outputs, and recirculate controls for each register. A single external clock signal generates two internal clock phases to each register. The clock and all inputs can be driven from Series 74 TTL circuits and all outputs can drive TTL circuits without the use of external resistors.

P-channel enhancement-type low-threshold processing with self-aligned gates has been employed to reduce power dissipation and provide simple interfaces with bipolar circuits.

The TMS 3409 and TMS 3417 are offered in 16-pin dual-in-line ceramic (JC suffix) or plastic (NC suffix) packages designed for insertion in mounting-hole rows on 300-mil centers. These devices are characterized for operation from −25°C to 85°C.

applications

The TMS 3409 and TMS 3417 can be used in terminals, CRT displays, key-to-tape, key-to-disk, and card-punch applications.

operation

Transfer of data into and out of the shift register occurs on the high-to-low transition of the clock with output data becoming valid after a specified propagation delay following that transition. Input data must be set up a minimum time before the high-to-low transition and must be held for a minimum time after that transition.

Recirculate occurs on the high-to-low clock transition with the recirculate control high. The recirculate control level must be set up a minimum time before this transition and held a minimum time after the transition. Data is entered with the recirculate control low. During recirculation, data is continuously available at the outputs and data inputs are inhibited.

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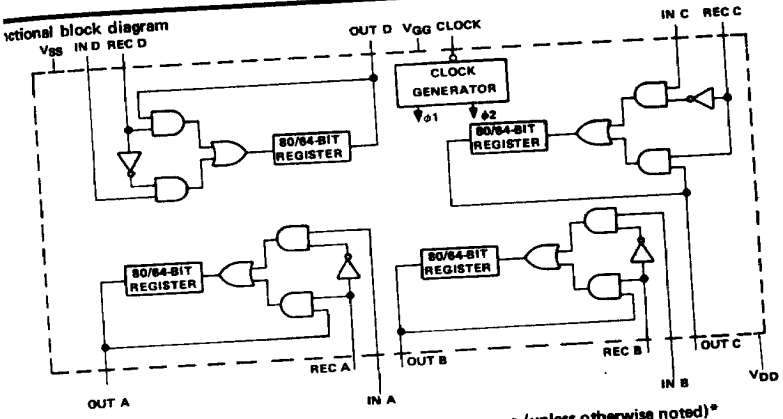
nctional block diagram



bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Clock input voltage (see Note 1)	−20 V to 0.3 V
Data input voltage (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most-positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Comment: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ecommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		0		V
Supply voltage, V_{GG}	−11	−12	−13	V
Supply voltage, V_{SS}	4.75	5	5.25	V
High-level input voltage, V_{IH}	V_{SS} −2		V_{SS}	V
High-level clock input voltage, $V_{IH(\phi)}$	V_{SS} −2		V_{SS}	V
Low-level input voltage, V_{IL}	0		0.8	V
Low-level clock input voltage, $V_{IL(\phi)}$	0		0.4	V
Pulse width, clock high, $t_{w(\phi H)}$	75		50000	ns
Pulse width, clock low, $t_{w(\phi L)}$	125		50000	ns
Data setup time, $t_{su(da)}$	50			ns
Recirculate setup time, $t_{su(rec)}$	200			ns
Data hold time, $t_{h(da)}$	50			ns
Recirculate hold time, $t_{h(rec)}$	100			ns
Clock frequency, f_{ϕ}	0.01		5	MHz
Operating free-air temperature, T_A	−25		85	°C

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electrical characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA	V_{SS} −1	V_{SS} −0.5	V_{SS}	V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		0.3	0.4	V
I_I	Input current (all inputs)	V_I = 0			−100	nA
I_{GG}	Supply current from V_{GG}	T_A = 25°C, f = 1 MHz		−10	−12	mA
I_{SS}	Supply current from V_{SS}			33	47	mA
P_D	Power dissipation			285	400	mW
C_i	Input capacitance, all inputs except clock	V_I = V_{SS}, f = 1 MHz			10	pF
$C_{i(\phi)}$	Clock input capacitance	$V_{I(\phi)}$ = V_{SS}, f = 1 MHz			25	pF

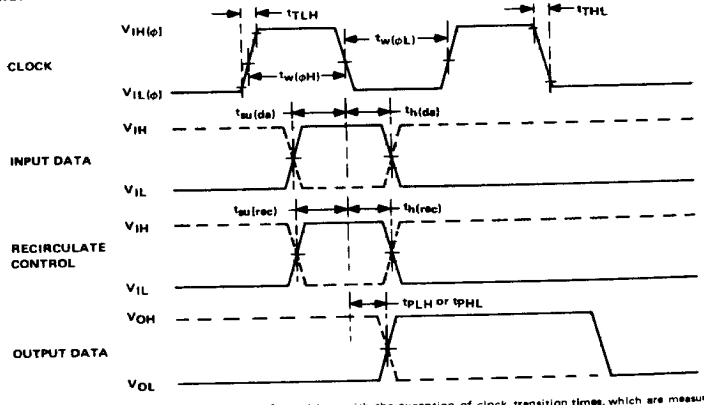
†All typical values are at T_A = 25°C.

switching characteristics under nominal operating conditions, T_A = −25°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	1 Series 74 TTL Load + 10 pF OR 10 MΩ + 10 pF (MOS Load) (see Note 2)		100	160	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			100	160	ns
t_{TLH}	Transition time, low-to-high-level output	1 Series 74 TTL Load + 10 pF (see Note 2)			60	ns
t_{THL}	Transition time, high-to-low-level output				50	ns

†All typical values are at T_A = 25°C.
NOTE 2: For final test purposes a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 10 MΩ and 10 pF. All loads are connected between output and V_{SS}.

voltage waveforms



NOTE 3. All timings are with respect to 50% points of transitions with the exception of clock transition times, which are measured at 90% (high) and 10% (low).

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