Cromemco

4KZ

Instruction Manual

Cromemco
incorporated
Specialists in computers and peripherals
2432 CHARLESTON RD., MOUNTAIN VIEW, CA 94043

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Introduction

The Cromemco 4KZ memory board incorporates 4096 8-bit memory locations with on-board address generation and a control port for memory bank select. The 4KZ mates with the Cromemco ZPU™ to provide virtually full speed operation at 4mHz with reliable low-power static RAM chips. The 4KZ is also compatible with 8080-based systems and may be used in any S-100 bus computer.

Initial Switch and Jumper Setup

Logical Address

The position of the 4KZ in memory is determined by the setting of the 4-place DIP switch in the upper right corner of the board. The switches, labelled $\frac{1}{5}, \frac{1}{4}, \frac{1}{3}, \frac{1}{2}$, control address bits A15 – A12 respectively. Setting a switch up or "on" conditions the board to respond to a high logic level in that address bit. There are 16 possible logical blocks which the 4KZ may occupy; Table 1 summarizes the switch settings for each.

Board Disable

When the Board Disable jumper is **inserted**, the 4KZ will go into a disabled state at POWER-ON-CLEAR or RESET. In the disabled state the memory may not be written or read. The bank select port must be used to reactivate the board. This jumper is used when several boards occupy the same logical address (on different banks) or for bootstrap arrangements. The jumper is above IC55.

Bank Select Enable

When the Bank Sel Enable jumper is **inserted**, the bank select port becomes operational. With the jumper out the board will not be affected by output to the bank select port. This jumper is located above IC50.

Wait Disable

If the 4KZ is used with a 2mHz 8080 system, no wait states are ever required and the Wait Disable jumper should be **inserted**. This prevents an occasional wait state during stack operactions. Do **not** insert this jumper when using a Cromemco ZPU™; the 4KZ senses the 2/4 mHz line and automatically eliminates wait states at 2mHz operation. This jumper is located above IC42.

Table 1

4K Block No.	1111 5432	Hex		Octal		Dec	
		Start	Finish	Start	Finish	Start	Finish
Ø	ØØØØ	0000	0FFF	000000	007777	0	4095
1	0001	1000	1FFF	010000	017777	4096	8191
2	0010	2000	2FFF	020000	027777	8192	12287
3	0011	3000	3FFF	030000	037777	12288	16383
4	0100	4000	4FFF	040000	047777	16384	20479
5	0101	5000	5FFF	050000	057777	20480	24575
6	0110	6000	6FFF	060000	067777	24576	28671
7	0111	7000	7FFF	070000	077777	28672	32767
8	1000	8000	8FFF	100000	107777	32768	36863
9	1001	9000	9FFF	110000	117777	36864	40959
A	1010	A000	AFFF	120000	127777	40960	45055
B	1011	B000	BFFF	130000	137777	45056	49151
C	1100	C000	CFFF	140000	147777	49152	53247
D	1101	D000	DFFF	150000	157777	53248	57343
E	1110	E000	EFFF	160000	167777	57344	61439
F	1111	F000	FFFF	170000	177777	61440	65535

Memory Bank

The 4KZ may occupy any combination of the eight levels in the memory bank. The 8-place DIP switch above the heat sink controls bank selection. Raise the switch corresponding to the Bank(s) desired. See paragraph for Bank Select Enable jumper wiring. Banks are controlled through output port 40H = 100Q = 64D. Each bank responds to its corresponding bit in the output word, e.g. Bank Ø is turned on by a "1" in bit Ø.

Theory of Operation

Address Anticipation

The Address Anticipation circuit supplies the address to the address pins of the 21L02 before the CPU does. The circuit operates in the following sequence:

1. The CPU begins a new cycle by transmitting a new address. On the 4KZ, the lower 12 bits are fed to comparators IC44-46, which check against the 12 bits currently latched in IC36-38. If these addresses agree, IC43 pin 6 goes low.

2. The CPU updates the status signals and transmits PSYNC to indicate the beginning of a machine cycle. If the status signals and A15-A12 are correct for a reference to the 4KZ, pin 3 of RN1 will go high, enabling read and write circuits.

3. The 4KZ strobes the PRDY line with PSYNC if IC43 pin 6 is not low when RN1 pin 3 is high. This will cause the CPU board "WAIT" flip flop to latch a wait-state request at the rising edge of Ø2 in machine state T2.

   If IC43 pin 6 is low during $\overline{\text{PSYNC}}$, no wait will be generated. This is the case for an anticipated address.

   Notice that there are two ways to defeat the PRDY driver IC54. The first is if the SSTACK line is low. This is the case for the Cromemco ZPU when operating at 2mHZ, so no wait states will be generated (at 4mHz SSTACK is high). The **WAIT DISABLE** jumper also defeats the PRDY driver and can be used to prevent waits when using an 8080 CPU where the SSTACK line is not always low.

4. The $\overline{\text{PRDY}}$ signal sets IC42 pin 8 during $\overline{\text{Ø2}}$. This signal is LOAD REQUEST. At the rising edge of Ø2, LOAD REQUEST is inverted and drives the $\overline{\text{LOAD}}$ inputs of IC36-38. As soon as the counters load the new address, IC43 pin 6 goes low, resetting the LOAD REQUEST latch.

   For anticipated addresses there is no LOAD REQUEST. (LOAD REQUEST occurs during Ø2 of T2 and is always followed by a TW wait state).

5. DBIN rises or MWRITE rises to cause IC33 pin 8 to rise or fall, respectively. If the address comparators don't yet have a match (i.e. IC43 pin 6 is not low) the MWRITE signal is held off until the addresses do agree. IC34 pin 11 goes low during DBIN or MWRITE.

6. After DBIN or MWRITE falls again IC34 pin 11 rises. This clocks the counters IC36-38. Since the addresses are inverted with respect to the CPU, the counters are decremented to match the CPU's increment. This occurs in T3, anticipating the address for the upcoming T1.

7. The next cycle is a repeat of the sequence above unless it is an M1 (instruction fetch). In this case, there is timing advance: Approximately 40 nanoseconds after SM1 rises, IC41 clocks in the status of U43 pin 6. If this is high, a $\overline{\text{LOAD}}$ signal is immediately applied to IC34 pin 9 to force the counters to load. This lets IC43 pin to go low but its previous state is retained by IC41 in order to generate a WAIT state with PSYNC. IC41 is reset at Ø2 in T2.

8. Simple DMA operation is allowed by using PHLDA to force IC36-38 into a LOAD condition. Max DMA rate is thus set by the 450 ns access time of the 21L02's.

Bank Select

During an output to port 40H = 100Q = 64, IC41 latches the OR of those bits selected by the BANK DIP switch. IC41 can pull down the Address and Status decoding node RN1 pin 3 and totally disable the board if none of the page bits it is connected to are high. IC41 is normally reset (pin 5 goes low) by $\overline{\text{POC}}$ or $\overline{\text{PRESET}}$ so that the 4KZ is enabled. The BOARD DISABLE jumper sets U41 during $\overline{\text{POC}}$ or $\overline{\text{PRESET}}$ so that the 4KZ is disabled. The clock signal is derived from A7-AØ, PWR and the Bank Enable jumper (which must be inserted).

Diagnostics

Hardware

Most of the address anticipation circuit can be directly observed with a four-trace oscilloscope. The simple program C3 ØØ ØØ (located at ØØØØH) should generate a wait during M1 only. Operation may be checked by following through **Theory of Operation** Section (Address Anticipation).

Software

With every 4KZ memory board Cromemco provides a paper tape listing of our 4KZ memory test program. Operation of the 4KZ memory test is described in the following section.

CROMEMCO Memory Test

The Cromemco Memory Test requires at least 2K of RAM starting at D800. The test program itself, however, can be loaded and executed at any other address. In particular, it can be stored and executed in one 2708 PROM at any address except the D-range. The program is compatible with both the Z-80 and the 8080 instruction sets.

The Memory Test includes the so-called bubble or ripple test. This part of the test checks crosstalk between memory cells. It also catches stuck bits and includes short-term and medium-term retention checks.

In the second division of the test, long-term memory retention is checked. Memory is filled with a pattern and then tested to see if it can retain the pattern for at least 6 seconds (at 4mHz). This, by the way, is six orders of magnitude longer than the short-term check mentioned above. Long-term retention is checked for each of several patterns.

How to Use the Test

Assume that the memory test resides in a PROM at EØØØ and that we wish to test memory cards addressed at 8ØØØ, 9ØØØ, AØØØ, BØØØ, and CØØØ hex.

Make sure that there is RAM at D000. Execute E400. When prompted with "CARDS:" type in the first and the last cards to be tested:

CARDS: 8 C (CR)

The program then responds with the prompt "TESTS:" If we answer by typing "10", for example, TESTS: 10 (CR) then 10 (hex) complete ripple tests followed by the long-delay test will be performed on each card. If any errors are detected then an error print-out occurs for that card. After all the cards have been tested the cycle begins again, starting with the first card (card 8 in our example).

One major use of the memory test is to burn-in new RAM chips by testing a card continuously for several days. In order to do this without reams of print-out an option is provided which performs the specified ripple tests on each card but omits the delay tests and error print-outs until the optional number of cycles through all the cards has been completed.

In the following case,

CARDS: A B (CR)
TESTS: 3 FE (CR)

there will be FE cycles. Each cycle consists of 3 ripple tests on Card A and 3 on Card B. Only on the last cycle, the FE-th, will the ripple tests be followed by the delay tests and a possible error print-out.

The sequence of FE cycles will repeat until the ESCAPE key is depressed.

Error Print-Out

If at least one error occurred during the testing of a card a card image is printed which indicates the RAM locations of the errors. The image is a mapping of the locations of the RAMs on the CROMEMCO 4KZ memory board.

```
(CARD 3)  0---- 1---- 2---- 3---- 4---- 5---- 6---- 7----
      0:  ********************************************************
      1:  ********************************************************
      2:  ************************************01 T5**************
      3:  ********************************************************
```

The four 1K segments of the card's address range are indicated along the side, and the eight bit positions are marked across the top. In the example above, errors occurred in bit 5 of row 2 (the 3rd K) of the card addressed at 3000 hex.

Note that there are two entries at this place in the image. The first entry is the number of the first test the RAM failed. The second entry indicates the last test it failed.

The ripple tests are numbered 01 through FE (hex). (An entry of FF as the number of tests or cycles is treated as infinity.) The long-delay tests are T0, TF, TA, T5, in the order of their occurrence.

Control Functions

Depressing CONTROL-P causes a print-out of the image of the card under test at the time. After print-out the test resumes at the point it was interrupted.

ESCAPE or CONTROL-SHIFT-K causes the print-out followed by termination of the test and prompting for a new test.

CONTROL-S causes the remainder of a print-out to be skipped. The test then resumes. This is useful primarily for skipping uninteresting print-outs when using slow consoles such as teletypes.

Loading the Paper Tape

The memory test program assumes that data transfer occurs on I/O port 1. Status flags are on input port 0. The data-available flag is on bit 6 of input port 0. The transmitter-buffer-empty flag is on bit 7 of input port 0. Both flags are active high.

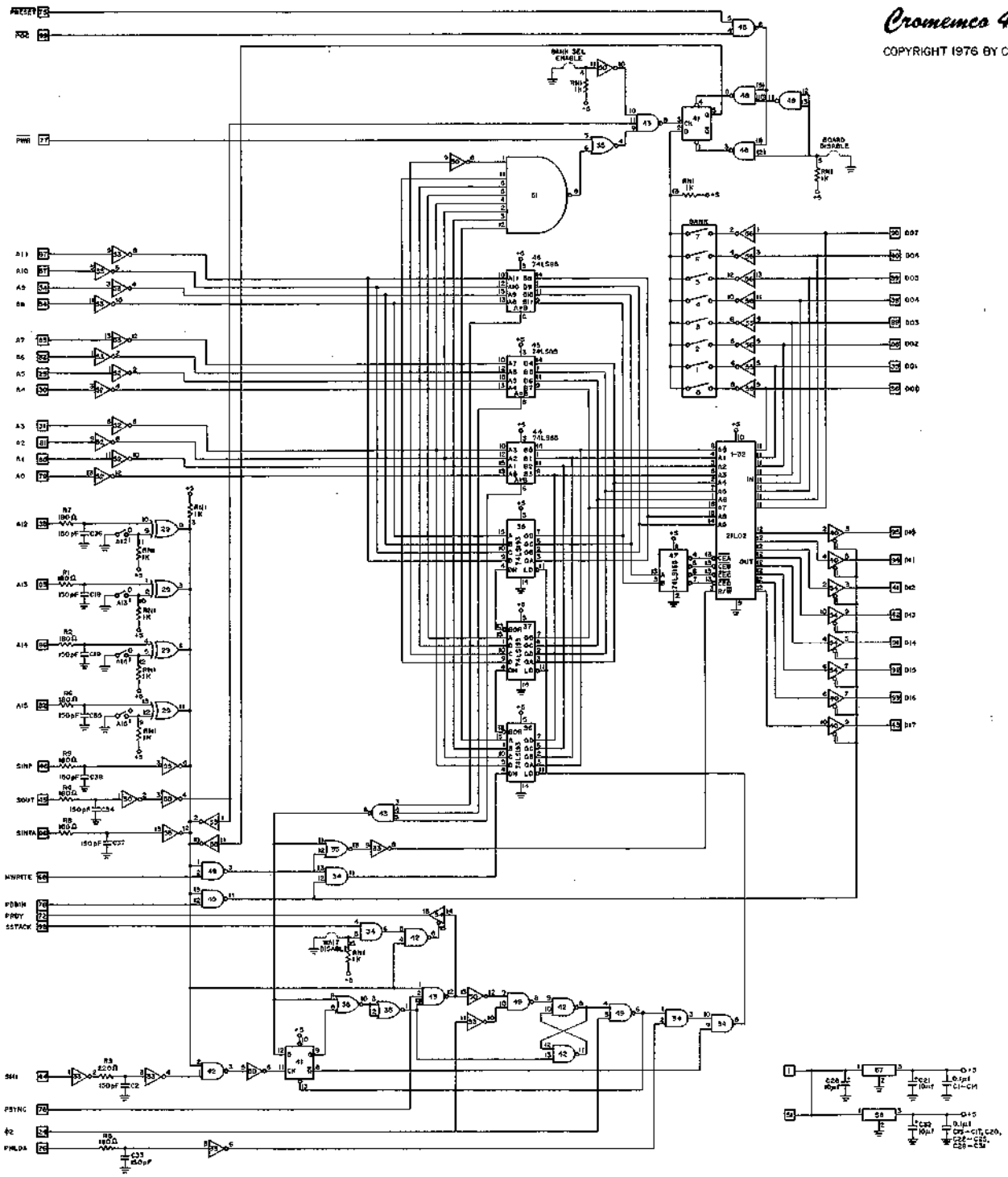
The following hex locations may be changed for different I/O conventions. (The addresses given are relative to the address of the PROM in which the test program is stored.)

Status port number (00): 0264, 0270, 028A, 0332
Input data port number (01): 026B, 0277, 0337
Output data port number (01): 0292
Input data-available mask (40): 0266, 0272, 0334
Output transmitter-buffer-empty mask (80): 028C

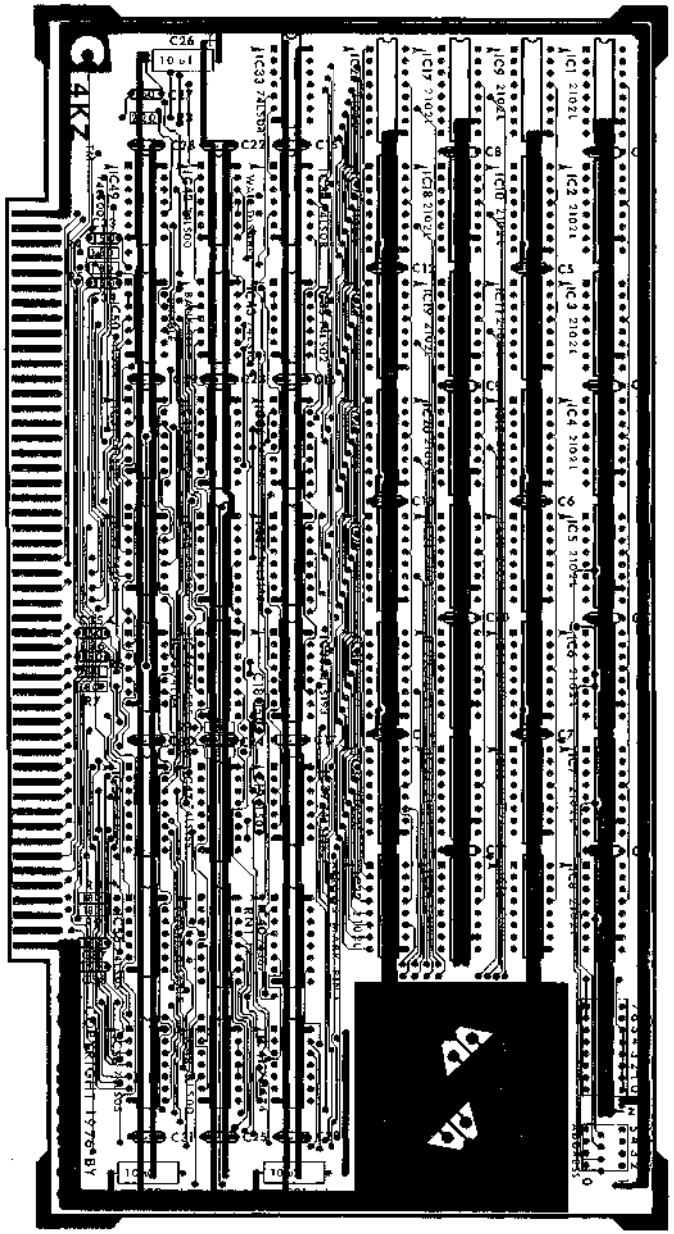
For active-low status flags change the following locations from CA hex to C2: 0267, 0273, 028D. Also change 0335 from C8 to C0.

The following program can be used to load the binary paper tape of the memory test into RAM at location 0 so that it can subsequently be programmed into PROM using a BYTESAVER. Recall that the memory test requires RAM at location D000 hex but it executes at any other address.

Address	Code		
1000	21 00 00		LD HL, 0
1003	DB 00	LOOP:	IN A, 0
	E6 40		AND 40H
	CA 03 10		JP Z, LOOP
	DB 01		IN A, 1
	77		LD (HL), A
	23		INC HL
	C3 03 10		JP LOOP



Schematic Diagram



Assembly Diagram

Parts List

Integrated Circuits

IC1 -	IC32	2102L
	IC33	74LS04
	IC34	74LS08
	IC35	74LS02
	IC36	74LS193
	IC37	74LS193
	IC38	74LS193
	IC39	74LS136
	IC40	74367
	IC41	74LS74
	IC42	74LS00
	IC43	74LS10
	IC44	74LS85
	IC45	74LS85
	IC46	74LS85
	IC47	74LS155
	IC48	74LS00
	IC49	74LS00
	IC50	74LS04
	IC51	74LS30
	IC52	74L04
	IC53	74L04
	IC54	74367
	IC55	74LS05
	IC56	74LS05
	IC57	LM340T-5 (7805)
	IC58	LM340T-5 (7805)

Capacitors

C1 -	C17	0.1 μF
	C18	150 pF
	C19	150 pF
	C20	0.1 μF
	C21	10 μF
	C22	0.1 μF
	C23	0.1 μF
	C24	0.1 μF
	C25	0.1 μF
	C26	10 μF
	C27	150 pF
	C28	0.1 μF
	C29	0.1 μF
	C30	0.1 μF
	C31	0.1 μF
	C32	10 μF
	C33	150 pF
	C34	150 pF
	C35	150 pF
	C36	150 pF
	C37	150 pF
	C38	150 pF

Switches

8 position bank select
4 position address select

Resistors

R1 180
R2 180
R3 220
R4 180
R5 180
R6 180
R7 180
R8 180
R9 180
RN1 1K DIP network

IC Sockets

42 - 16 pin sockets
15 - 14 pin sockets

Other

pc board
heatsink
4 6-32 X 3/8 screws
4 6-32 nuts
6 jumper pins
Instruction Manual
Paper tape listing of memory test program.

Warranty

Your factory-built 4KZ memory board is warranted against defects in materials and workmanship for a period of 90 days from the date of delivery. We will repair or replace products that prove to be defective during the warranty period provided that they are returned to Cromemco. No other warranty is expressed or implied. We are not liable for consequential damages.

Should your factory-built 4KZ memory board fail after the warranty period it will be repaired, provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse to repair any product that in our opinion has been subject to abnormal electrical or mechanical abuse. The service fee is currently $35 and is subject to change.

Your assembled 4KZ memory board kit will be repaired, provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse repair of any kit that in our opinion has not been assembled in a workmanlike manner or has been subject to abnormal electrical or mechanical abuse. Payment of the service fee must accompany the returned merchandise. The service fee is currently $35 and is subject to change.