CompuPro®

DISK 1A

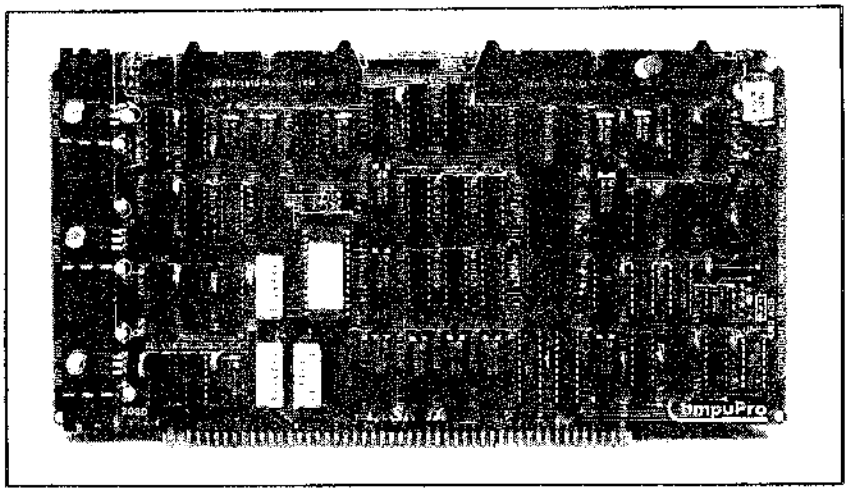
TECHNICAL MANUAL

A290

$20.00

DISK 1A

Technical Manual



HIGH PERFORMANCE FLOPPY DISK CONTROLLER
FOR 8" AND 5.25" DRIVES

DISK 1A TECHNICAL MANUAL

Hayward, CA 94545

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CONTENTS

OVERVIEW

The DISK 1A was specifically designed to give you one of the most powerful floppy disk interfaces available for the S-100 bus. Designed for full electrical and mechanical compatibility with the IEEE 696/S-100 bus standard, this board boasts several innovative features not found on many currently available disk controllers. These features include:

* 24 bit DMA data transfers with the ability to cross 64K boundaries

* priority arbitration for the on-board DMA circuitry that will allow up to 16 temporary bus masters to operate without conflict

* I/O mapped controls for uninterrupted memory space

* an advanced, 3rd generation floppy disk controller made by NEC or INTEL (765A or 8272)

* an advanced digital data separator for reliable data transfers and eliminates adjustments

* provision for running both 5.25" and 8" floppy drives at the same time

* on-board BOOT EPROM with the capability of supporting many different BOOT routines

Like all other CompuPro boards, the DISK 1A includes:

* on-board regulators

* low power Schottky TTL and MOS technology integrated circuits for reliable, cool operation

* sockets for all ICs go onto a four layer, solder masked circuit board with a complete component legend

HOW TO GET YOUR DISK 1A UP AND RUNNING WITHOUT READING THE MANUAL

This section is for those of you who are so anxious to see the DISK 1A running that you don't want to read the manual. This section will tell you how to set up the DISK 1A board so that it can run CP/M,® MP/M™ or Concurrent DOS™ 8-16™ in your system.

We strongly recommend that you relax and read the manual. If you don't, and you follow the directions in this section, and your system does not work, don't panic. Read the manual!

STEP 1. UNPACK DISK 1A BOARD.

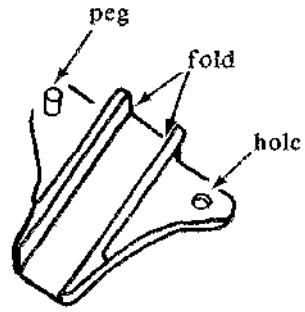
Along with the board, you will find an extra jumper shunt and two card ears in the plastic bag.

STEP 2. INSTALL CARD EARS.

a) Hold the board so the component side is toward you. (See diagram below.)

b) Insert the peg on the card ear into the hole in the right corner of the board. Fold the ear over the board's edge until the ear's hole snaps over the peg (make sure the long edge of the ear is along the top edge of the board.)

c) Repeat for left ear.



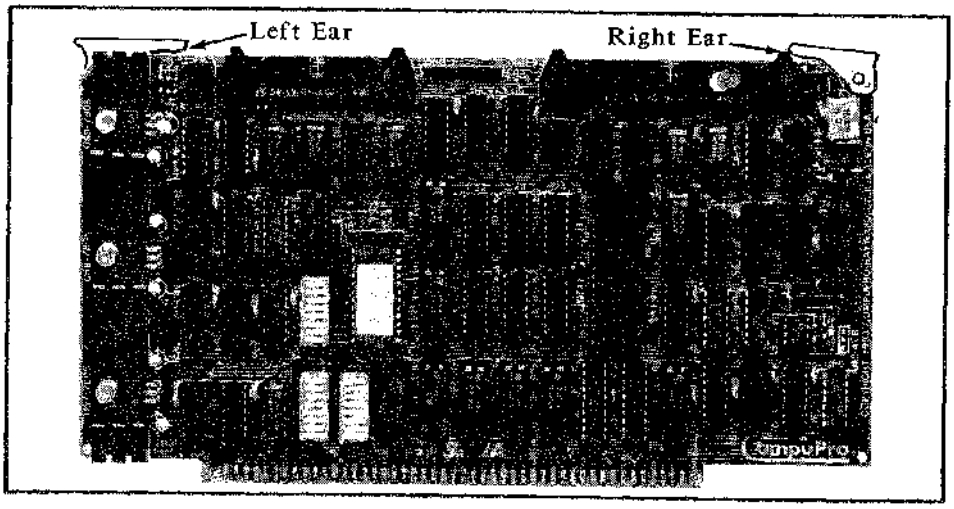
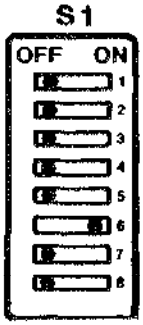


Figure 1. DISK 1A (Component Side)

STEP 3. SET SWITCHES. Check the DISK 1A switch settings (see figure on page 5 for the location of S1, S2 and S3.)

The black dot (•) shows which side of the switch should be down.

SWITCH 1:



POSITION	SET IT
1	OFF
2	*
3	*
4	*
5	*
6	OFF
7	ON
8	OFF

*Set S1 positions 2-5 as shown below depending on the type of CPU and console I/O device you are using.

BOOT ROUTINE*	SWITCH S1 POSITION 2	3	4	5	CPU
0	On	On	On	On	8085/8088/Z80
1	On	On	On	Off	8085/8088/Z80
2	On	On	Off	On	8085/8088/Z80
3	On	On	Off	Off	8085/8088/Z80
4	On	Off	On	On	8086/286
5	On	Off	On	Off	8086/286
6	On	Off	Off	On	8086/286
7	On	Off	Off	Off	8086/286
8	Off	On	On	On	68000
9	Off	On	On	Off	68000
10	Off	On	Off	On	68000
11	Off	On	Off	Off	68000
12	Off	Off	On	On	32016
13	Off	Off	On	Off	32016
14	Off	Off	Off	On	32016
15	Off	Off	Off	Off	32016

NOTE: In all the above cases, Switch 3, position 1 should be ON to use the System Support 1 as the console and OFF to use an Interfacer 3 or 4, user 7 as the console.

*The routine numbers are the ways the DISK 1A BOOT ROM works. An explanation of the routine numbers follows.

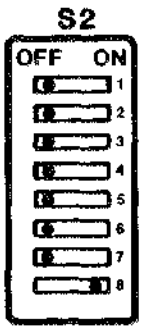
Routines 0, 4, 8, and 12 look for an 8" drive as drive 0. If it is ready, it will boot from it. If the 8" drive is not ready, it will try to boot from the DISK 3.

Routines 1, 5, 9 and 13 will always boot off of the DISK 3 and never look for any floppies.

Routines 2, 6, 10 and 14 will attempt to boot off an 8" drive as drive 0. If that is not ready, it will loop and look for a 5.25" drive as physical drive 2, if that is not ready it will go look for the 8", then the 5.25" drive.

Routines 3, 7, 11 and 15 will attempt to boot from a 5.25" drive as drive 0. If that is not ready, it will look for a DISK 3. It will contine to loop as in the first routine.

SWITCH 2:



POSITION	SET IT
1	OFF
2	OFF
3	OFF
4	OFF
5	OFF
6	OFF
7	OFF
8	ON

SWITCH 3:

POSITION	SET IT
1	*
2	ON
3	ON
4	ON
5	ON
6	OFF
7	OFF
8	ON

---

*NOTE: Set Switch 3, position 1 ON to use the System Support 1 as the console and OFF to use Interfacer 3 or 4, user 7 as the console.

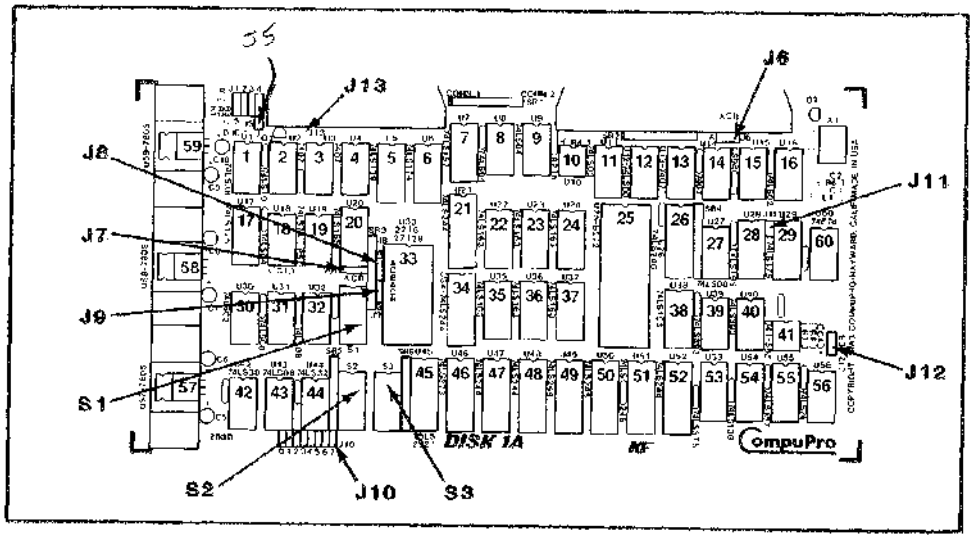


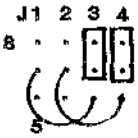
Figure 2. DISK 1A (jumper and switch location)

STEP 4. CHECK JUMPER SHUNT CONNECTORS

Make sure the jumper shunts are installed as listed below. (See Figure 2 for the location of jumper connectors.)

JUMPER SHUNTS

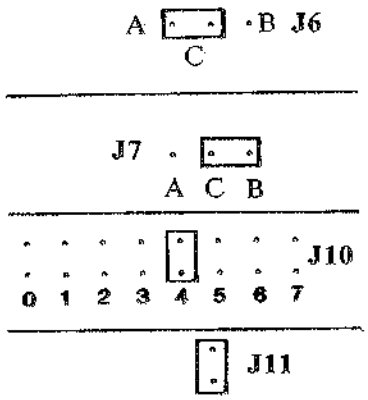
A jumper shunt is a small plastic part used to connect two pins on the jumper connector. Jumper shunts should be installed notch side up.



J1 and **J2** should be in position 8. (These may be in the "5" position for use with 5.25" drives.)

J3 and **J4** should be in position 5 for 5.25" drives; position 8 for 8" drives.

Remove **J5**.



J6 should be connected from A-C for all CompuPro drives.

Remove J7 if you are using CompuPro's 5.25" drives alone or with 8" drives, and connect it from B-C for 8" drives only.

Place a shunt on position 4 of J10.

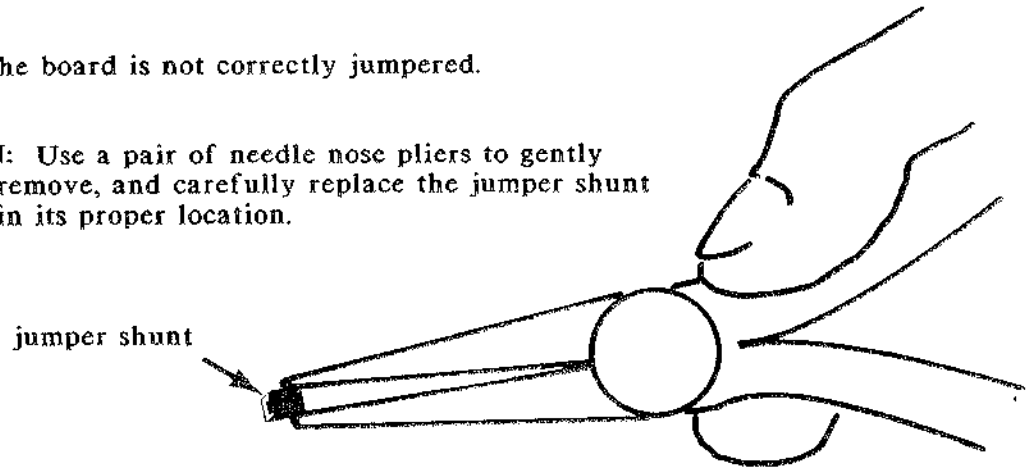
Install a shunt on J11.

You should have received the board with **J8** and **J9** both connected from B-C, and **J12**, and **J13** removed. Leave these jumpers set this way.

These settings select DMA arbiter priority 15, ports C0H-C3H, EPROM wait states enabled and the boot routine appropriate to the CPU selected by switch 1 positions 1-7.

IF: The board is not correctly jumpered.

THEN: Use a pair of needle nose pliers to gently remove, and carefully replace the jumper shunt in its proper location.



INSERT THE DISK 1A INTO THE MOTHERBOARD.

Place the board into the slot closest to the back of the enclosure. The edge connector is offset, so that the DISK 1A will fit only with the component side facing the front panel of the enclosure. PUSH DOWN GENTLY UNTIL THE BOARD IS FIRMLY INSTALLED.

CONNECT THE CABLES FROM DISK 1A TO THE FLOPPY DISK SUBSYSTEM.

Place your floppy disk subsystem near your computer enclosure. Make sure it is on a stable surface to reduce vibration when the computer is working. Make sure it is not located near telephones and magnetic fields (like those created by a generator). If you need to remove the cover from the computer, do not use a magnetic screwdriver.

CABLE INSTALLATION. Cables must be connected correctly. Be sure that when you assemble the cables the red stripe is always on the same side, and the connector plugs are inserted properly. You may connect these cables in any order.

DRIVE INTERFACE - 8 INCH DRIVES

Use a 50 pin cable plugged into CONN 2 to connect the DISK 1A to 8" floppy drives. Install and remove the jumper shunts listed below.

QUME TRAK 842

INSTALL (C,2S,DL,DSx)
REMOVE (T40,GND,DS,D,DC,Y,HA)

SHUNT: Cut HL and X, all others intact. Install terminator resistors on the last drive of the cable.

DRIVE INTERFACE - 5.25 INCH DRIVES

Use a 34-pin ribbon cable to connect the DISK 1A to 5.25" mini-floppies. Plug it into CONN 1.

Choose the proper drive select line on the programming shunt and leave it intact. If your minifloppy drive drives the READY* line (as CompuPro's Mitsubishi drives do), you must install a jumper between "C" and "A" of J6. If your minifloppy drive does not drive the READY* line, short B-C of J6.

Your DISK 1A is configured for drives that load the heads when a drive select occurs. For drives that use line 4 as HEAD LOAD, connect a wire between the pads of J13 and solder it on the back side of the board. This will bring the HEAD LOAD signal out to line 4.

MITSUBISHI DRIVE M4853

INSTALL HS, MM (DS 0, 1, 2 or 3 as appropriate)

Install terminator resistors on the last drive of the cable.

BOOT THE CONTROLLER

Before inserting your diskette, you should see the following:

1. Dimly glowing drive activity lights indicate that the floppy controller is scanning the drives.

2. The activity light of drive A flashing on and off approximately once a second (dependent on the CPU and it's speed), if the controller is trying to boot.

If you see both, insert your write protected diskette and listen. You should hear several clicking sounds from the drive and see the sign-on message. If both lights are on, your cable is installed backwards.

Your system should be up and running now. If it isn't, try repeating Steps 1-4. There is more detailed information in other parts of this manual if you need more specific help.

DISK INTERFACE PORT MAP

The DISK 1A interface uses a block of four port addresses for communication between it and the host processor. DISK 1A occupies no memory space of the host processor and performs all data transfers via DMA. The address of the first port is switch settable to any I/O address which is a multiple of four. The ports will be referred to as relative ports 0 - 3.

RELATIVE PORT	FUNCTION
0 READ	FDC Main Status Register
0 WRITE	Drive Select Register
1 READ	FDC Data Register
1 WRITE	FDC Data Register
2 READ	Drive Status Register
2 WRITE	DMA Address Register
3 READ	Not Used
3 WRITE	Motor Control Register

FDC Main Status Register (read only)

This is the main status register of the FDC chip. It may be read to obtain the status of the drives and the controller chip.

Drive Select Register (write only)

The Drive Select Register allows you to select a 5.25" or a 8" data rate, force the Two Sided Line when using double sided minifloppies, and invoke the alternate drive select and head load signals for the drive. The bit positions are shown in the following table.

BIT	FUNCTION
0	ALTERNATE UNIT SELECT BIT "0"
1	ALTERNATE UNIT SELECT BIT "1"
2	ALTERNATE SELECT (NORMAL = 0, ALTERNATE = 1)
3	FORCE TWO SIDED (NORMAL = 0, FORCE = 1)
4	ALTERNATE HEAD LOAD (LOAD = 1)
5	5.25"/8" DATA RATE SELECT (8" = 0, 5.25" = 1)
6	NOT USED
7	NOT USED

FDC Data Register

The FDC Main Data Register is the main communication path between the host system and the FDC chip. All command and result status pass through this register.

Drive Status Register (when read)

The Drive Status Register allows you to poll a drive's READY* status, view the drive's INDEX* pulse, check the FDC interrupt status, and read the board sense switch. The bit positions are shown in the following table.

BIT	FUNCTION
0	DRIVE READY STATUS (READY = 1)
1	DRIVE INDEX PULSE (PULSE = 1)
2	SENSE SWITCH S3-1 (ON = 0, OFF = 1)
3-6	NOT USED
7	FDC INTERRUPT STATUS (INTERRUPT ACTIVE = 1)

DMA Address Register (when written)

The DMA address register is actually a push-down stack of three one-byte registers. Load a three byte, twenty-four bit DMA address most significant byte first.

Motor Register (when written)

The Motor Register allows you to control the Motor Control Lines for drives that respond to these lines and disable the BOOT EPROM. When written with a "0" in bit D0, the BOOT EPROM will be disabled. A system reset is required to re-enable the BOOT EPROM. The Control Bits are described in the following table.

BIT	FUNCTION	
0	BOOT EPROM DISABLE (DISABLE = 0, SYSTEM RESET TO RE-ENABLE)	
1-3	NOT USED	
4	8" FLOPPY "0" MOTOR	(MOTOR ON = 1, MOTOR OFF = 0)
5	8" FLOPPY "1" MOTOR	(MOTOR ON = 1, MOTOR OFF = 0)
6	8" FLOPPY "2" MOTOR	(MOTOR ON = 1, MOTOR OFF = 0)
7	8" FLOPPY "3" MOTOR	(MOTOR ON = 1, MOTOR OFF = 0)
7	5.25" FLOPPY MOTOR	(MOTOR ON = 1, MOTOR OFF = 0)

NOTE: Bit 7 controls both 8" floppy #3 and 5.25" floppy motors.

COMPUPRO DRIVE INTERFACE ADDRESS

The current versions of all software packages written for the DISK 1A controller require that the base port address be set to C0H.

ACTUAL PORT	FUNCTION
C0	FDC Main Status and Drive Select Register
C1	FDC Data Register
C2	Drive Status and DMA Address Register
C3	Motor Control Register

PORT ADDRESSING

Use DIP switch S3, positions 2 thru 7 to select the base address of the four port block in a binary fashion as shown below:

SWITCH POSITION	ADDRESS BIT	
2	A2	
3	A3	
4	A4	"ON" = "0"
5	A5	"OFF" = "1"
6	A6	
7	A7	

EXAMPLE: To address this board at addresses C0H thru C3H for all CompuPro software, positions 6 and 7 would be "OFF" and positions 2 thru 5 would be "ON".

INTERRUPTS

The DISK 1A is capable of running in either a polled mode or an interrupt driven mode that is particularly suited for multi-user environments. The DRIVE STATUS port (relative port 2) allows you to run in the polled mode by sampling the interrupt output of the floppy disk controller on data bit 7. To run in an interrupt driven mode, the interrupt output of the floppy disk controller is driven onto one of the vectored interrupt lines (VI0* thru VI7*) of the S-100 bus. This is accomplished by installing a jumper shunt or a #30 wrap wire across the posts at jumper location J10, positions 0-7. Jumpers 0 thru 7 correspond directly to VI0* thru VI7*. Use the highest priority vectored interrupt to insure that it is not accidentally masked off. Currently, all CompuPro software uses VI4* for the floppy disk interrupt.

BOOT EPROM

The BOOT EPROM contains the software routines required to load the initial sectors of the disk operating system into memory for system startup.

On power-up, the BOOT EPROM will appear as 512 bytes of memory at the host CPU's reset address. If the CPU does not reset to a location on a 512 byte boundary, the BOOT EPROM will align itself on the nearest 512 byte page. For example, an 8085 or a Z-80 will reset to 0000H, which is on a 512 byte boundary. Therefore, in this case the BOOT EPROM will appear from 0000H to 01FFH. An 8088 or an 8086 resets to 0FFFF0H, which is not page aligned, therefore, the BOOT EPROM will appear from 0FFE00H to 0FFFFFH.

The DISK 1A requires that a minimum of 512 bytes of system RAM corresponding to the area of the processor's reset location be capable of responding to PHANTOM* by disabling itself. This RAM may be any amount equal to or greater than 512 bytes.

BOOT EPROM ROUTINE ADDRESSING

The BOOT EPROM is capable of holding up to 64 sets of switch selectable BOOT routines of up to 256 bytes each or 32 sets of switch selectable BOOT routines of up to 512 bytes each when a 27128 EPROM is installed. The standard configuration has a 2764 installed for 16 routines of 512 bytes each. Positions 2 thru 5 of switch S1 select one of the sixteen routines in a binary fashion corresponding to the EPROM address lines as shown in the following table.

SWITCH S1 POSITION						
2	3	4	5	CPU	EPROM STARTING ADDRESS	BOOT ROUTINE #
On	On	On	On	8085/8088/Z80	0000H	0
On	On	On	Off	8085/8088/Z80	0200H	1
On	On	Off	On	8085/8088/Z80	0400H	2
On	On	Off	Off	8085/8088/Z80	0600H	3
On	Off	On	On	8086/286	0800H	4
On	Off	On	Off	8086/286	0A00H	5
On	Off	Off	On	8086/286	0C00H	6
On	Off	Off	Off	8086/286	0E00H	7
Off	On	On	On	68000	1000H	8
Off	On	On	Off	68000	1200H	9
Off	On	Off	On	68000	1400H	10
Off	On	Off	Off	68000	1600H	11
Off	Off	On	On	32016	1800H	12
Off	Off	On	Off	32016	1A00H	13
Off	Off	Off	On	32016	1C00H	14
Off	Off	Off	Off	32016	1E00H	15

NOTE: In all the cases on the previous page, Switch 3, position 1 should be ON to use the System Support 1 as the console and OFF to use an Interfacer 3 or 4, user 7 as the console.

BOOT ROUTINE DESCRIPTION

As shipped, the BOOT EPROM contains routines for loading several sectors of track 0 into memory and passing on the value associated with the particular sense switch S3-1 routine. The value passed on allows the proper console I/O routine to be selected. In CompuPro single user operating systems, either the System Support 1 or the User 7 of an Interfacer 3 or 4 will be selected.

DISK 1A BOOT-ROM

There are routines for four different processor "families" CompuPro ships:

PROCESSOR	ROUTINE #S
Z80/8085	0 - 3
8088/8086/286	4 - 7
68000	8 - 11
32016	12 - 15

There are four routines per processor. Each processor has the same set of four routines, and setting Switch 1 positions 2 - 5 as listed on the previous page will select the routine described below.

The first set of routines (0, 4, 8 and 12) will look for an 8" drive as drive 0. If it is ready, it will boot from it. If the 8" drive is not ready, it will attempt to boot from the DISK 3.

The second set of routines (1, 5, 9 and 13) will always boot off of the DISK 3 and never look for any floppies.

The third set of routines (2, 6, 10 and 14) will attempt to boot off an 8" drive as drive 0. If that is not ready, it will loop and look for a 5.25" drive as physical drive 2, if that is not ready it will go look for the 8", then the 5.25" drive.

The fourth set of routines (3, 7, 11 and 15) will attempt to boot from a 5.25" drive as drive 0. If that is not ready, it will look for a DISK 3. It will contine to loop as in the first routine.

All routines will end with the number 2 plus the value of the sense switch S3-1 (0 or 1) in register "C" or equivalent. This determines whether the I/O console is the System Support 1 board or the Interfacer 4 user 7.

WAIT STATE ENABLE

The DISK 1A is capable of inserting wait states into the BOOT EPROM read as well as the I/O and DMA read or write cycles when fast processors are being used. The wait states become necessary when the access time of the BOOT EPROM and the floppy disk controller are longer than the fetch time of the host processor. The wait states are enabled by placing position 8 of switch S2 in the "ON" position. When enabled, the EPROM will have 5 wait states inserted, and the I/O and DMA cycles can have either 2, 3 or 4 wait states. With J7 in position "B", 2 wait states will be inserted, with J7 in position "A", 3 wait states will be inserted, and with J7 removed, 4 wait states will be inserted. (CompuPro recommends inserting 4 wait states when using 5.25" drives.)

BOOT ENABLE/INHIBIT

The BOOT EPROM may be enabled by putting position 8 of S3 in the "ON" position, and disabled by placing it in the "OFF" position. A possible reason for disabling the BOOT routine would be if two or more DISK 1A controllers were placed in the system at one time or the DISK 2 hard disk controller was the BOOTING device. In this case, more than one controller trying to boot would cause a system conflict.

Remember, the BOOT hardware on the DISK 1A board requires that a 256 or 512 byte page of memory respond to PHANTOM* at the host processor's reset address. If the memory residing at this address does not respond to PHANTOM*, a bus drive conflict will occur and possible damage could result.

ARBITER AND PRIORITY SELECTION

The DISK 1A controller allows multiple DMA devices to be active on the S-100 bus at one time. As long as a DMA board (temporary bus master) conforms to the IEEE 696 specifications concerning DMA arbitration and prioritization, up to 16 different bus masters may gain use of the bus in order of their assigned priority. Remember, there should never be more than one temporary bus master at the same priority level.

The priority of the DISK 1A board is selected in a binary fashion on positions 4 thru 7 on DIP switch S2 as shown below:

SWITCH POSITION (S1)	PRIORITY LEVEL	VALUE	
7	PRIORITY 3	8	
6	PRIORITY 2	4	"ON" = 0 VALUE
5	PRIORITY 1	2	"OFF" = VALUE
4	PRIORITY 0	1	

EXAMPLE:

1. For the highest priority (15), positions 4 thru 7 would be "OFF" (8+4+2+1=15).

2. For priority 9, positions 7 and 4 would be "OFF" and positions 5 and 6 would be "ON" (8+1=9).

3. For the lowest priority (0), positions 4 thru 7 should be "ON".

MOTOR CONTROL ENABLE

Four bits are provided in the Motor Control Register to control the four designated motor control lines for 8" floppies and the one designated motor control line for 5.25" minifloppies. (Your drives may not respond to these lines.) By controlling the contents of this register, any or all drives may have their motors turned "ON" or "OFF". In addition, this register has an automatic timeout feature that turns all the motors "OFF" approximately 15 seconds after the last access to the controller. Any access of the board resets this timer and the 15 seconds starts again. Since minifloppies have only one control line, data bit 7 will control 8" drive #3 and ALL minifloppies. You cannot turn each minifloppy "ON" and "OFF" individually. Jumper J11 is provided so that the minifloppies may be left with their motors "ON" at all times. If J11 is removed, the motors will stay on all the time. Otherwise, J11 should remain installed.

DISK 1A CONNECTOR PINOUT WITH 8 AND 5.25 IINCH DRIVES

DISK 1A CONN 2 PIN	8 INCH DRIVE SIGNAL	DISK 1A CONN 1 PIN	5 INCH DRIVE SIGNAL
2	LOW CURRENT		
4	MOTOR OFF 1		
6	MOTOR OFF 2		
8	MOTOR OFF 3		
10	TWO SIDED		
12	NC		
14	SIDE SELECT		
16	NC		
18	HEAD LOAD	2	OPTION LINE
20	INDEX (8")	4	HEAD LOAD
22	READY	6	DRIVE SELECT 4
24	MOTOR OFF 4	8	INDEX (5")
26	DRIVE SELECT 1	10	DRIVE SELECT 1
28	DRIVE SELECT 2	12	DRIVE SELECT 2
30	DRIVE SELECT 3	14	DRIVE SELECT 3
32	DRIVE SELECT 4	16	MOTOR ON
34	DIRECTION SELECT	18	DIRECTION SELECT
36	STEP	20	STEP
38	WRITE DATA	22	WRITE DATA
40	WRITE GATE	24	WRITE GATE

42	TRACK 00	26	TRACK 00
44	WRITE PROTECT	28	WRITE PROTECT
46	READ DATA	30	READ DATA
48	NC	32	SIDE SELECT
50	NC	34	READY

ALL ODD PINS GROUND ON BOTH CABLES.

PROGRAMMING CONSIDERATIONS FOR USING MINIFLOPPY DRIVES

Several things must be considered when using minifloppy drives with the DISK 1A, and these are listed below.

1) Most minifloppy drives use data rates that are 1/2 that of 8" drives, therefore, the clock frequency of the FDC and other circuitry must be reduced. This is accomplished by setting the 5/8* bit high in the Drive Select Register. After this is done, you must wait a while to let the FDC chip settle down, and then you must send new specify instructions to the FDC. Since the clock to the FDC is now 4 MHz instead of 8 MHz, you must adjust the values that you send it. (Refer to the data sheet)

2) Since almost all minifloppy drives have a Motor Control Line, you will need to make sure that you turn the drive ON and wait for it to come up to speed. The MOTOR REGISTER will automatically time out and shut off the drives after approx. 15 seconds. J11 will need to be installed if you wish to control the motor line, otherwise, the motors will be on at all times.

3) Some minifloppies have a READY line and some do not. If the drive does, simply connect A-C on jumper J6 and it will be used. If the drive does not use READY, you will need to connect B-C of J6 so that the READY line of the FDC is driven when 5/8* is set for 5.25" operation. This will make the FDC think that the drive is ready whenever the bit is set. You will not be able to tell if the drive is really ready without further checking.

4) Since minifloppy drives do not have a signal that tells the FDC that a floppy is single or double sided, this must be handled with external logic. This is accomplished by setting the Force Two Sided line (F2S) when a double sided floppy is used. The reason for this is that the FDC will not let you access the second side of a diskette that it thinks is single sided.

W A R N I N G !

Not all floppy disk controllers generate true IBM compatible 3740 and System 34 formats even though they claim to. Therefore, we strongly recommend that you do not use the DISK 1A to copy data onto a diskette that has been formatted by another controller! The proper procedure is to format diskettes using the DISK 1A, and copy the contents of other diskettes onto the newly formatted diskettes.

If you are sure that your controller generates a true IBM type format, or you are using diskettes formatted by IBM, you will not have to format new diskettes before using them with the DISK 1A.

SPECIFICATIONS FOR 8" FLOPPY DISK DRIVES

For the disk drives, the 50 pin cable connected into CONN 2 to connect the DISK 1A to 8" floppy drives is standard except that the stepper motors must be enabled at all times (not tied to drive select or head load). This causes the steppers to be powered at all times (they will get warm), and allows stepping without the lamp on the front of the drive being "ON" (so be careful). In addition, do not tie the head load signal to drive select since the 765A/8272 is always scanning the drives (this would result in a buzz). Use standard 50 pin ribbon cable to connect the drives to the controller, and terminate the last drive in the line as specified in the drive manual.

NOTE: Due to the steppers being enabled at all times, your disk power supply must be able to handle full load on the +24V line all the time and your drive enclosure must have adequate cooling.

SPECIFICATIONS FOR 5.25" MINIFLOPPY DISK DRIVES

If your minifloppy drive has a head load line, install the appropriate jumper to bring the head load out to pin 4. Jumper the minifloppy so the heads load on drive select. Set the drive select so READY is generated only when the drive is selected and a diskette is spinning in the drive.

THEORY OF OPERATION

The DISK 1A board can be broken down into six subsections. These six subsections correspond to the six pages of the schematic and include: the Bus Interface and Wait Circuitry, the BOOT Circuitry, DMA Counters and Address Drivers, the DMA Sequencing Logic and Priority Arbiter, the Disk Read/Write Circuitry and Data Separator, and the Floppy Disk Controller and Interface Circuitry. While reading this section it is suggested that you refer to the schematic and the data sheet on the controller chip.

THE BUS INTERFACE AND WAIT CIRCUITRY

This section includes the logic for the S-100 bus interface to the floppy controller, the strobe generators, the wait state circuitry and the the data bus interface. Octal bus latch U46 buffers and latches the address lines A0 thru A7 for on-board use by the strobe decoder (U54), the boot EPROM (U33), and the address decoder (U45). Octal comparator U45 uses DIP switch S3, address lines A2 thru A7, and sOUT and sINP* to decode a valid four port board select signal BDSEL*. BDSEL*, LA0 and LA1, OUTPUT* (which is sWO* buffered by U53), and BUS-STB (generated from pDBIN and pWR* by U12), are decoded by the 3 to 8 line decoder U54 to generate the strobes for the floppy disk controller chip and on-board registers.

Octal bi-directional bus drivers U50 and U51 buffer data to and from the controller board with steering from U2 and U27. When either a DMA bus cycle (BC*) or an OUTPUT* (command write to the FDC) occurs, U50 is enabled, and the DMA transfer line (XFER) determines the direction of the data. When XFER is high, data is transferred out of the board and onto the DO lines. When XFER is low, data is transferred from the DO bus onto the board (command write). When either a BDSEL*, PROM ENA* or a BC* occurs, the WEN line is asserted, and if BUS-STB and OUTPUT* are also asserted, U51 is enabled. When XFER* is high, the internal data is output onto the DI lines (PROM read, FDC read, or DMA write). When XFER* is low, the data goes from the DI lines to the FDC for a disk write operation.

A wait state is left pending in shift register U20 at all times, however it is gated onto the bus only when S2-8 is closed and WEN is high. After BUS-STB is asserted, U20 is allowed to shift its data once on each rising edge of PHI* during a bus strobe (BUS STB*- pDBIN or pWR*). The first low to inputs d-h of U20 will terminate the wait state after it has been shifted to Qh. Five cycles are required to terminate an EPROM wait state and 2, 3 or 4 cycles to terminate either an I/O or DMA wait state. The wait states are enabled only when switch S2-8 is closed (ON), and WEN is asserted (EPROM read, I/O operation, or DMA cycle).

THE BOOT CIRCUITRY

The boot circuitry consists primarily of "D" flop U56A and NOR gate U16. When boot is enabled by switch S3-8, INIT* presets the flop and when MEMR* goes low, BOOT and PROM EN* are generated. PROM EN* is used to enable the boot EPROM whenever a memory read occurs. The boot software is contained in EPROM U33. One of sixty-four routines within the EPROM is selected by positions 1-6 of switch S1. If 512 byte routines are desired, S1-7 will bring A8 from the bus into the EPROM with S1-6 "OFF". The data from the EPROM enters the internal data bus (D0-D7) and is buffered onto the S-100 bus by U51. Since PHANTOM* is generated by U1 whenever BOOT is asserted and a DMA bus cycle (BC*) is not occurring, and since system memory boards should be set to become disabled when PHANTOM* is asserted, the host CPU will read the BOOT EPROM during a boot sequence. When the boot is through, U56A is reset with D0=0 and MTR STB* and BOOT is released.

Three of the strobes from U54 are multiplexed by U55 along with WE, pDBIN to generate the strobes for the floppy disk controller (RD* and WR*) and the DMA clock (DMA CLK) depending on whether a DMA bus cycle (BC) is occurring or not. During a DMA cycle, WE and pDBIN generate the control strobes for the controller chip, and BC* clocks the DMA counters. During non-DMA cycles, U54 generates these strobes.

The FDC interrupt is buffered onto the VI* lines by U3 and the interrupt status (CINT), floppy drive status RDYS and IDXS, and sense switch S3-1 information are gated onto the internal bus by half of U34. The other half of U34 buffers A8, PHI, pHLDA, and pRESET for on board use. Regulators U57-59 provide 5 volts for the board.

DMA COUNTERS AND ADDRESS DRIVES

The six DMA counters (U22-24 and U35-37) form a parallel loading 24 bit counter for address generation during the DMA transfer cycle. When XFER is not asserted (low), and DMA CLK rises (from DMA STB*, non-DMA cycle), the counters are loaded from the internal data bus (U22, U35) or from the previous stage of counter (U23, U36 or U24, U37). When XFER is asserted (a DMA cycle), DMA CLK is generated by BC*, and the counters are incremented for the next byte transferred.

The address buffers (U47-49) drive the 24 bits of information from the DMA counters out onto the bus whenever BC* is asserted (during a DMA transfer). Since a full 24 bits of counter are present in this circuit, DMA transfers become independent of the 64K boundaries normally present in 8 bit processors. This allows 16 bit processors with up to 24 bits of direct addressing to be fully supported.

THE DMA ARBITER AND SEQUENCER LOGIC

A DMA cycle is initiated when the floppy disk controller asserts the data request (DRQ) line, the pHOLD* line is not asserted, and the hold acknowledge line (HLDA) is not asserted. After a delay of up to 1.6 uSEC through U2, U31, R5 and C1, U19A is preset and causes the assert priority line (APRIO) to be asserted along with the pHOLD* line. The priority is asserted onto the TMA0* - TMA3* lines as generated and checked by the logic of U42-44, and switch S2 positions 4 thru 7. The highest priority line DMA3* is asserted first depending on the switch setting, and if the DMA3* line agrees with the asserted priority (no one with higher priority is asserting the line), then the next lowest priority line (DMA2*) is asserted and checked as in the first case. This process repeats until either a priority mismatch occurs and the sequence is held or the IMHI line is asserted indicating that this board is the highest priority. U19A and the APRIO sequence is held while the processor acknowledges the hold by asserting HLDA line and the DMA cycle occurs. The sequence is terminated at the end of the DMA cycle with BC* and STB INH (U31) or when a reset occurs (INIT* - U32). As soon as HLDA and IMHI are asserted (U32), the transfer state is entered (XFER or XFER*) in U19B on the next rising edge of PHI*. This state causes the S-100 control strobes to be driven onto the bus in an IDLE state condition with all addresses, status, DO buffers, and control strobes disabled.

The transfer state is controlled by the sequencing logic of quad "D" latch U17, and the NOR gates of U30. Each new state is initiated on the meeting of several conditions and the rising edge of PHI. When XFER* is asserted, and STB INH is not, the bus cycle (BC, BC*) is initiated, the S-100 status lines (U52) and the DMA address lines (U47-49) are driven onto the bus. In addition, BC* is fed back to the FDC as an acknowledge signal (DACK), allowing the FDC to enter the data transfer mode. In the next state after BC is asserted, the STB ENA and STB ENA* lines are asserted. This causes the strobes to be switched from the IDLE state to either a read or write state depending on the WE* signal from the FDC. The strobes pDBIN* and pWR* are generated by U5A, pSYNC is generated from BC* and STB ENA in U30, and pSTVAL* is generated from pSYNC and PHI* in U31. The READY state is constantly being generated by pRDY* and is updated every cycle of PHI. When either READY is asserted or STB INH is asserted (U30), and STB ENA* is asserted, the strobe inhibit state (STB INH or STB INH*) is entered. This causes the strobes to be returned to the IDLE state as long as a wait state is not requested. If a wait state has been requested, the strobes will not be changed until the READY state occurs. STB INH also causes the APRIO line to be reset, and on the next rising edge of PHI, the bus cycle (BC) will be terminated causing the status and address lines to be removed from the bus. As soon as pHOLD* is released and HLDA stops being asserted, the next edge of PHI* will cause the termination of the transfer state (XFER) and the removal of the S-100 strobes and the IDLE state on the bus.

DISK READ/WRITE CIRCUITRY AND DATA SEPARATOR

The master clock for the FDC is generated by a 16 MHz crystal oscillator consisting of X1, L1, and U15. This clock is divided by 2 by half of U60 and fed to counter U39 and multiplexer U38 where one output drives the FDC clock input and the other output with U56 generates WRITE CLK at the proper frequency determined by the signal MFM from the FDC and 5/8* the data rate select line. WRITE CLK is a 250 nSEC pulse for use by the FDC.

WRITE DATA and the two write precompensation signals PS0 and PS1 are fed and gated (U11) into write precomp shift register U28 where the WRITE DATA (WRD*) is clocked out with the proper precomp delay. This delay will be 250 nSEC. per clock cycle for the alteration of EARLY to NORMAL to LATE precompensation.

A digital data separator (U10) is fed with the raw read data (RAWD), MFM, and CLK 8/4 to yield separated read data (RDD) and the window reference clock. Counter U40 is fed with a low speed clock from timer U41 and generates timeout register clear signals DSCLR and MTRCLR if not cleared by the ACTIVITY signal.

The Drive Select Register U6 controls the data rate select line 5/8*, the force two sided line F2S, and 4 other lines that control the alternate head load and drive select signals. In the normal state, multiplexer U7 passes through the FDC's own head load and unit select signals. If bit 2 of the register is set, bits 0, 1, and 4 of the register will then control those lines.

The clock select line 5/8* is synchronized by half of U60 and CLK4* to insure that transients are not sent to the FDC during clock change-over.

THE FLOPPY DISK CONTROLLER AND INTERFACE CIRCUITRY

The floppy disk controller chip (U25) provides for the bridging of the previous five sections to the disk interface circuitry and the disk drives. The FDC is reset by INIT, and is connected to the internal data bus through D0-D7. The FDC interface to the internal bus is controlled by LA0, WR*, RD*, and XFER, which leave the FDC enabled at all times except during a transfer state, and steer the data with WR*, and RD*. DRQ initiates the DMA cycle, and BC* initiates the FDC data transfer. CLK and WCK are pulled up by SR4 to achieve a greater voltage swing for the internal clocking logic of the FDC. WINDOW describes the data cell time of the RD DATA pulse from the data separator, VCO ENA is not used, and MFM describes whether the FDC is expecting single or double density data. WRITE DATA feeds the write precompensation circuitry with PS0 and PS1 describing the amount of precomp needed for the particular data pattern. The WE and WE* (inverted by U9) lines control the enabling of the write circuitry and are used to determine the direction of the data transfers to and from the FDC. The INT output from the FDC is the general interrupt signal that is fed to inverter U18 and buffer U3 for driving the vectored

interrupt lines (VI0-VI7) if jumpered. INT is also buffered by Tri-state buffer U34, which gates the interrupt status onto D7 when a STATUS STB* occurs.

The Drive interface signals are decoded and buffered as described below. The HD line is inverted by U9 and buffered by U3 and U13 to drive the SIDE SELECT* line to determine which head of a double sided drive to use. HDL is fed to the mux and inverted and used to drive the HEAD LOAD* line of the drive. The IDX signal from both connectors are NANDed (U12) and fed directly to the FDC. The RDY signal from the 8" connector and the SRDY signal are NANDed to generate RDYS for the FDC. The unit select lines US0 and US1 are fed to multiplexer U7 and are decoded by decoder U5B to decode the one of four drives possible with this controller, and these four signals are buffered by four sections of U4 and fed to jumpers J1-4 to drive the DR SEL0* through DR SEL3* lines of the drives. The four signals WP/TS, FLT/TR0, FR/STP, and LCT/DIR each have two functions which are determined by the RW/SK line (read-write/seek). During a read or write operation, the drive signal WRITE PROT* is inverted and fed to the FDC line WP and the FDC line LCT is inverted (U26) and buffered (U13) to drive the LOW CURRENT* drive line. During a seek operation, the drive signals TWO SIDED*, and TRACK 0* are ANDed from the connectors, inverted and fed to the FDC lines TS* and TR0* and the FDC lines STP* and DIR* are inverted (U26) and buffered (U14 and U3) to drive the STEP* and DIRECTION* drive lines. These changes are controlled by the RW/SK line which determines which half of U26 will be enabled. The WRD* line is buffered (U13 and U3) to drive the WRITE DATA* line and the READ DATA* lines are NANDed and fed directly to U10. The MOTOR CONTROL signals are latched in U29 and buffered by U14 to drive the 8" motor lines. MOFF3* is run through disable jumper J11 and buffered to feed the MTR ON line on the minifloppy drives. All lines coming from the floppy drives are terminated by 150 ohm resistors, and jumper J6 is used to select either MRDY or inverted 5/8* to drive SRDY for ready status to the FDC. The WE* is buffered by U13 and U4, and fed to transistors Q1 and Q2. The transistor, resistor, Zener diode circuit kills the WRITE GATE signal if the power supply drops below a certain threshold. This inhibits accidental writes when the floppy diskette is left in the drive during power-down.

TROUBLESHOOTING

If you are having problems getting your DISK 1A up and running and you have read the previous sections of this manual, read on. The following section may help you solve your problem.

PROBLEM: ONE OR MORE OF YOUR DRIVE ACTIVITY LIGHTS STAYS "ON" BRIGHT ALL THE TIME.

Solution: This almost always indicates that the drive cable is backwards at either the drive box connector or at the drive. This may be verified by removing the 50 pin cable from either the board or the box. If the lamp goes off, the cable is reversed. However, the light on the fourth drive connected to the DISK 1A will glow brightly when no other disk activity is going on. This is normal, and shows that your controller is working properly.

PROBLELM: ACTIVITY LAMPS DO NOT GLOW DIMLY NOR FLASH BRIGHTLY

Solution: This generally indicates that the drive is jumpered wrong or there is a controller fault. Make sure that the drives are jumpered correctly and that the activity lamp is activated by drive select and not head load. Make sure that the drive has all of the different DC voltages that it requires. If the lamp still does not light, there could be a problem in either the controller or an open in the 50 pin drive cable.

PROBLEM: ACTIVITY LAMP GLOWS DIMLY BUT DOES NOT FLASH

Solution: This typically indicates either that the CPU is not executing the code in the BOOT EPROM due to the memory not being phantomed OFF, or that the host CPU does not have its jump-on-reset circuit turned off. The lamp will flash even if there is nothing in the system but the CPU and the DISK 1A board (no RAM!). Try removing everything but the CPU and the DISK 1A and verifying that the lamp flashes. If it does not, either of these boards could be at fault. Review your switch settings. You may have incorrectly selected a boot routine for a different CPU.

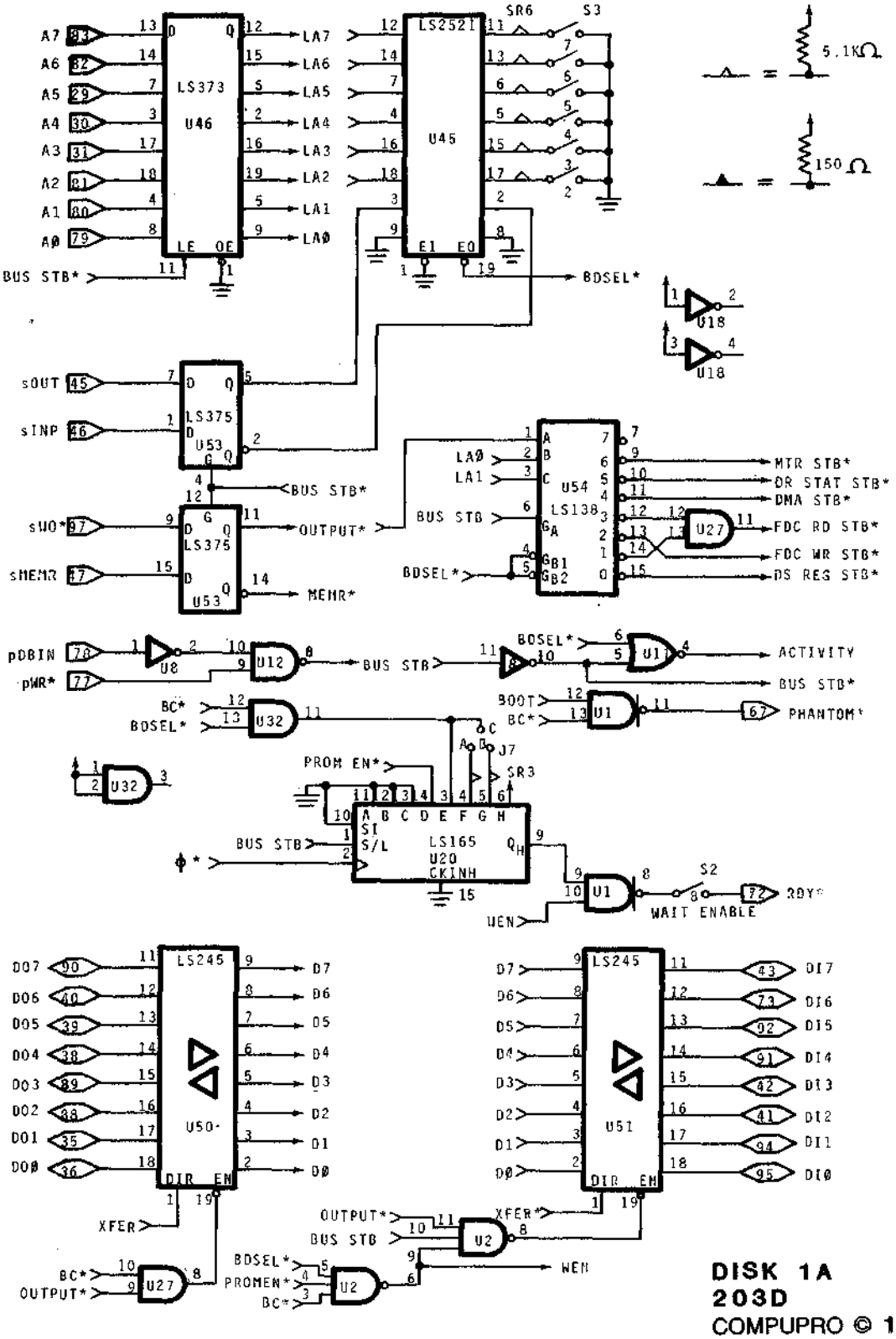
PROBLEM: DRIVE LOADS HEAD THEN UNLOADS AND REPEATS

Solution: If the board clicks and then pauses, and then repeats itself, this is typically an indication that the controller is unable to read the data from the drive. This could be from the data on the diskette being bad, the DMA cycle being inhibited by the CPU, or a hardware problem on either the drive, the cable, or the DISK 1A board. Try to isolate the problem by substitution if possible, otherwise check switch settings and drive hardware for proper configuration.

PROBLEM: DRIVE LOADS HEAD ONCE THEN STOPS

Solution: A single loading of the head and then nothing generally indicates that the controller is reading the first several sectors OK but either the data is transferred into memory improperly or the system memory is either bad or misaddressed. Improper transfer into memory generally occurs only with dynamic RAM boards that rely on specific CPU timing. If you have dynamic memory, make sure that it can handle DMA and that it generates its own refresh timing. Otherwise, make sure that the RAM is addressed properly, and there is the proper amount of RAM. Remember that for CP/M-80 you need 64K, for CP/M-86 and CP/M 8-16 you need at least 128K, for MP/M 8-16 you need at least 192K, and for Concurrent DOS 8-16, you need at least 256K. If you can run a RAM test, verify that that your memory is OK. Another possibility is that your operating system does not match your CPU. For example, CP/M 68K will not run with an 8086/87 CPU board.

LOGIC DIAGRAM 1 of 6



DISK 1A
203D
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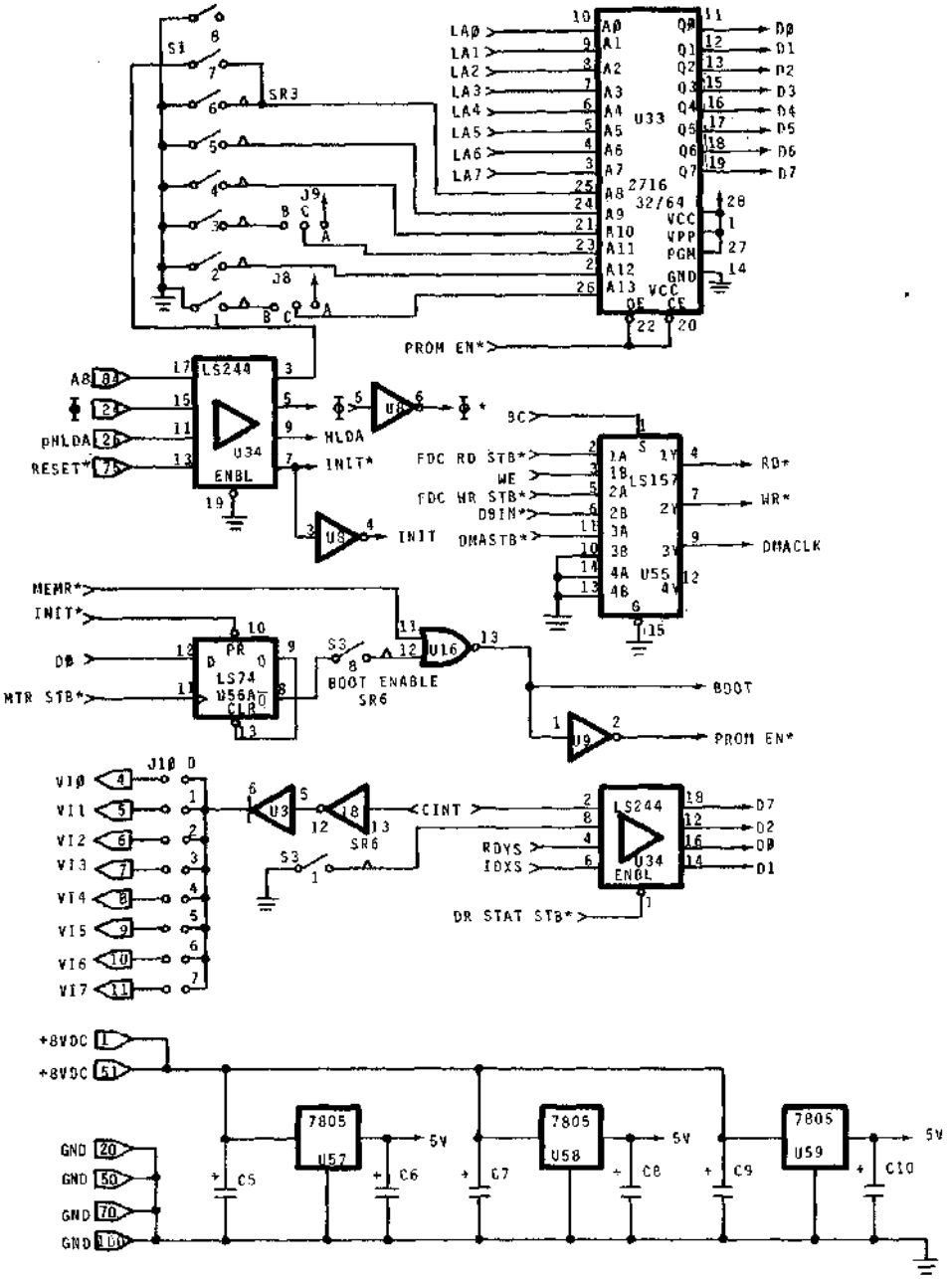

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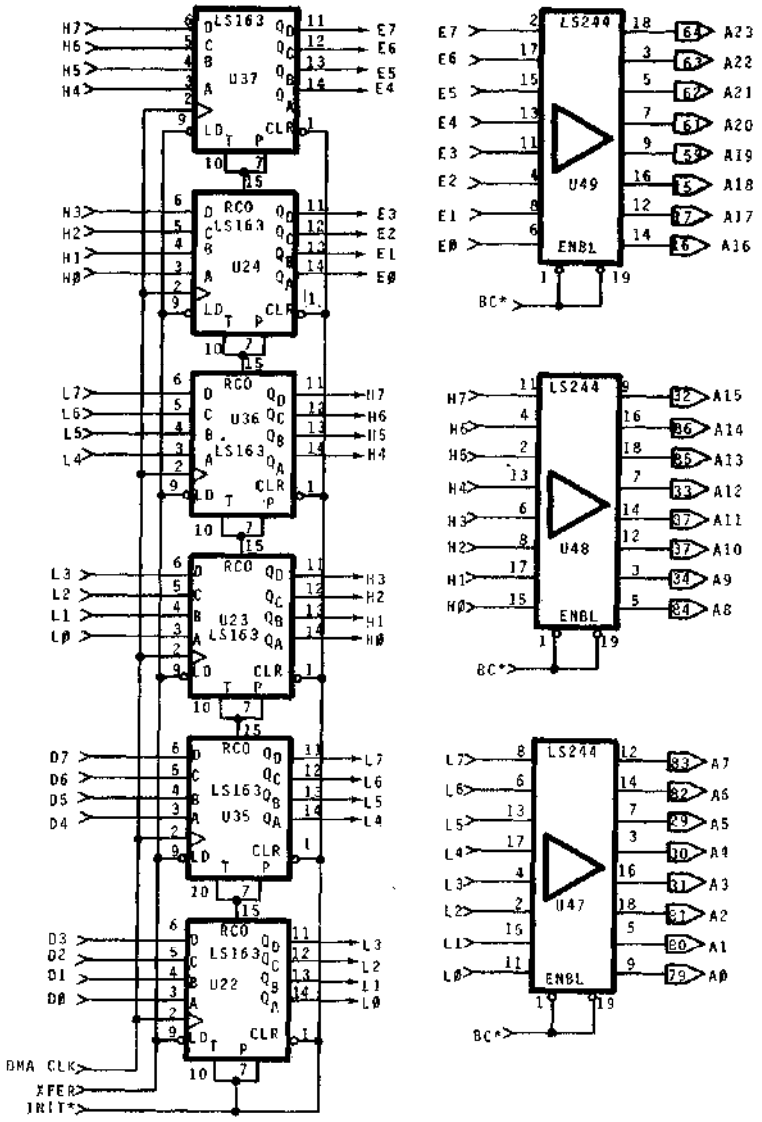
203D
COMPUPRO © 1984



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203D
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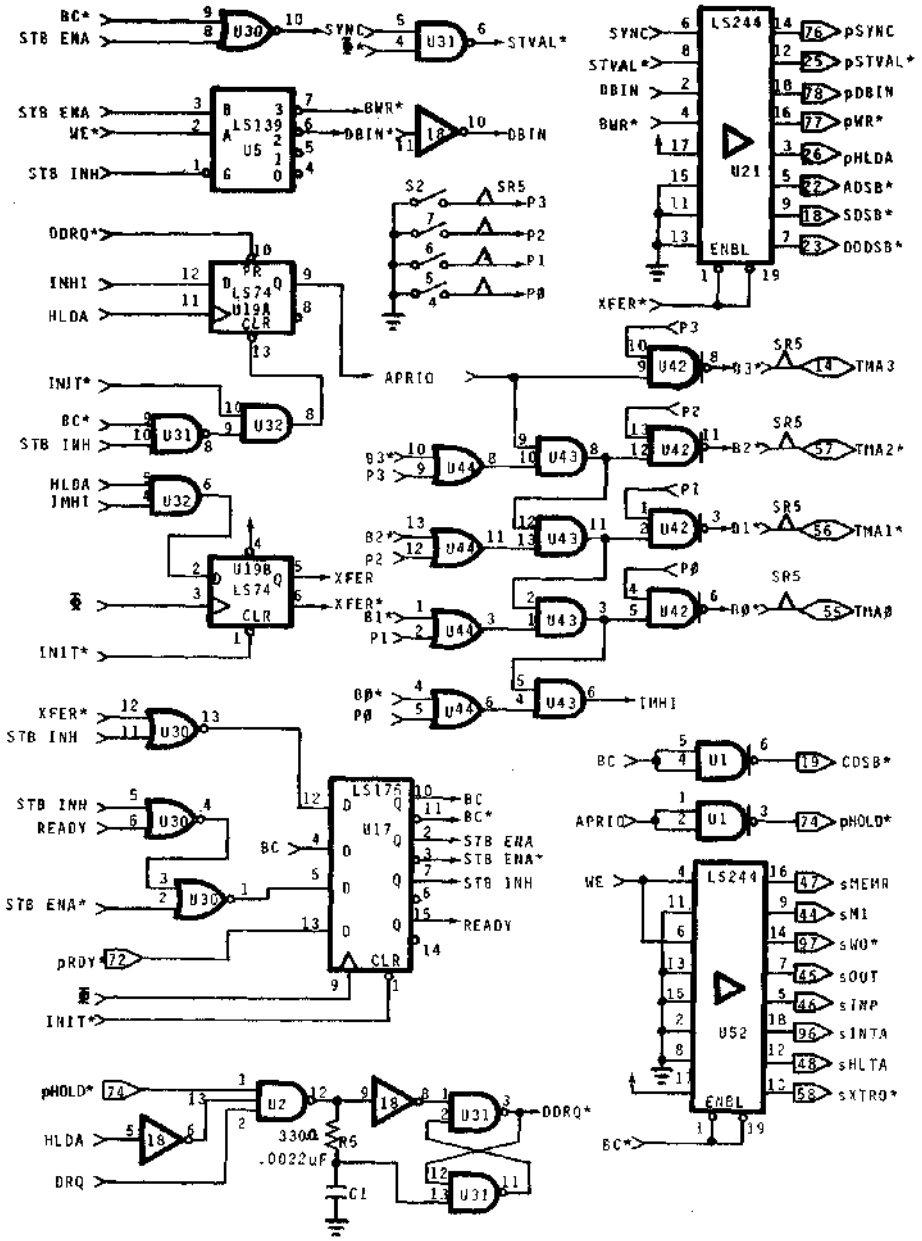

DISK 1A
203D
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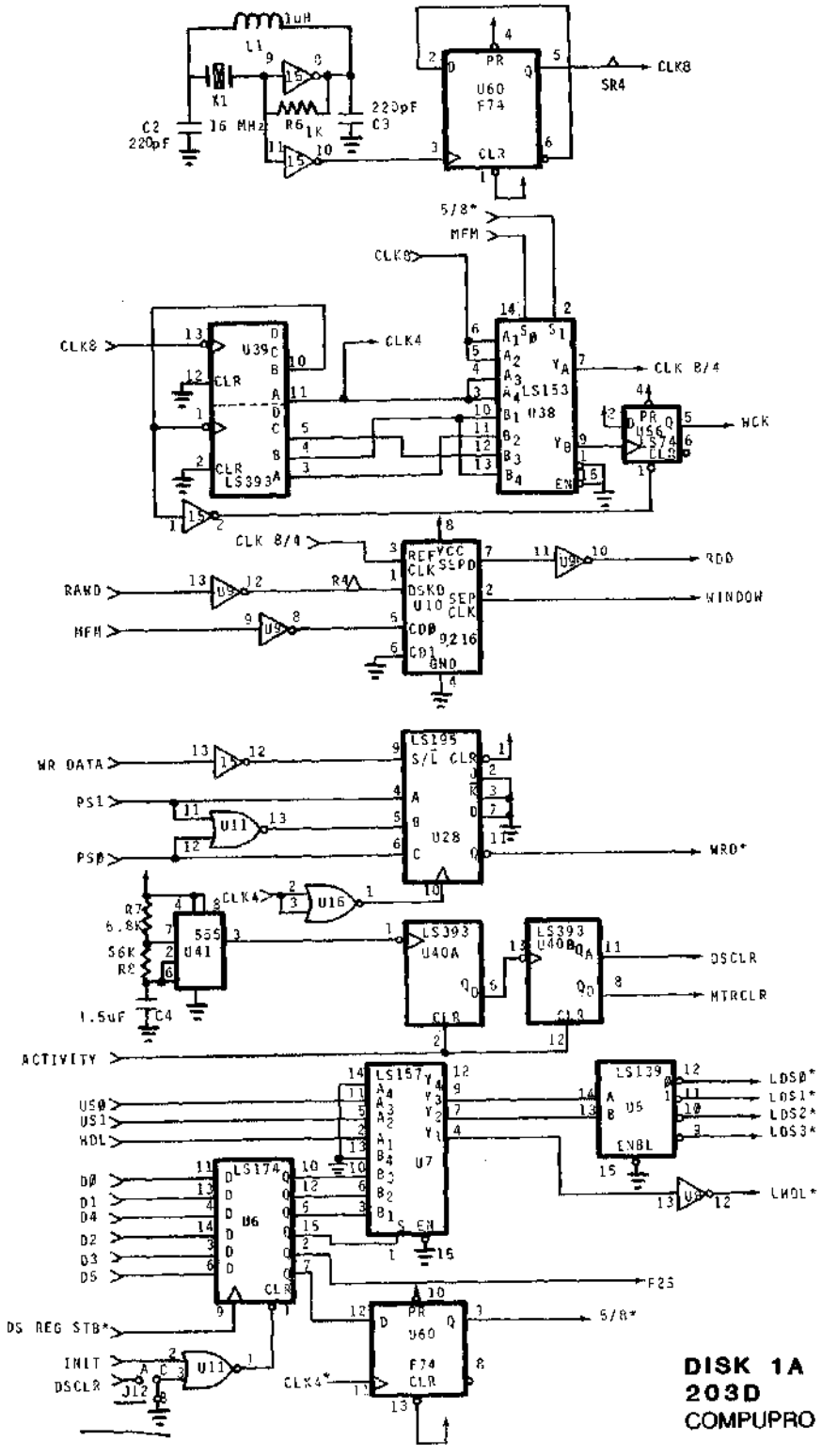
1uH
L1
X1
16 MHz
R6 1K
C2 220pF
220pF C3
U60 F74
PR
CLR
CLK8
SR4
5/8*
MFM
CLK8
CLK4
U39 LS393
CLR
CLK 8/4
LS153 U38
WCK
U56 LS74
REF CLK
DSKD U10 9216
SEP CLK
VCC SSPD GND
RDD
WINDOW
RAWD
MFM
R4
WR DATA
PS1
PSØ
LS195 S/L CLR
U28
WRD*
U11
U16
CLK4
R7 6.8K
R8 56K
555 U41
1.5uF C4
LS393 U40A
LS393 U40B
DSCLR
MTRCLR
ACTIVITY
LS157 U7
US0
US1
HDL
LS139 U5
ENBL
LDSØ*
LDS1*
LDS2*
LDS3*
LHDL*
LS174 U6
DØ
D1
D4
D2
D3
D5
F25
DS REG STB*
INIT
DSCLR
U12
CLK4*
5/8*
DISK 1A
203D
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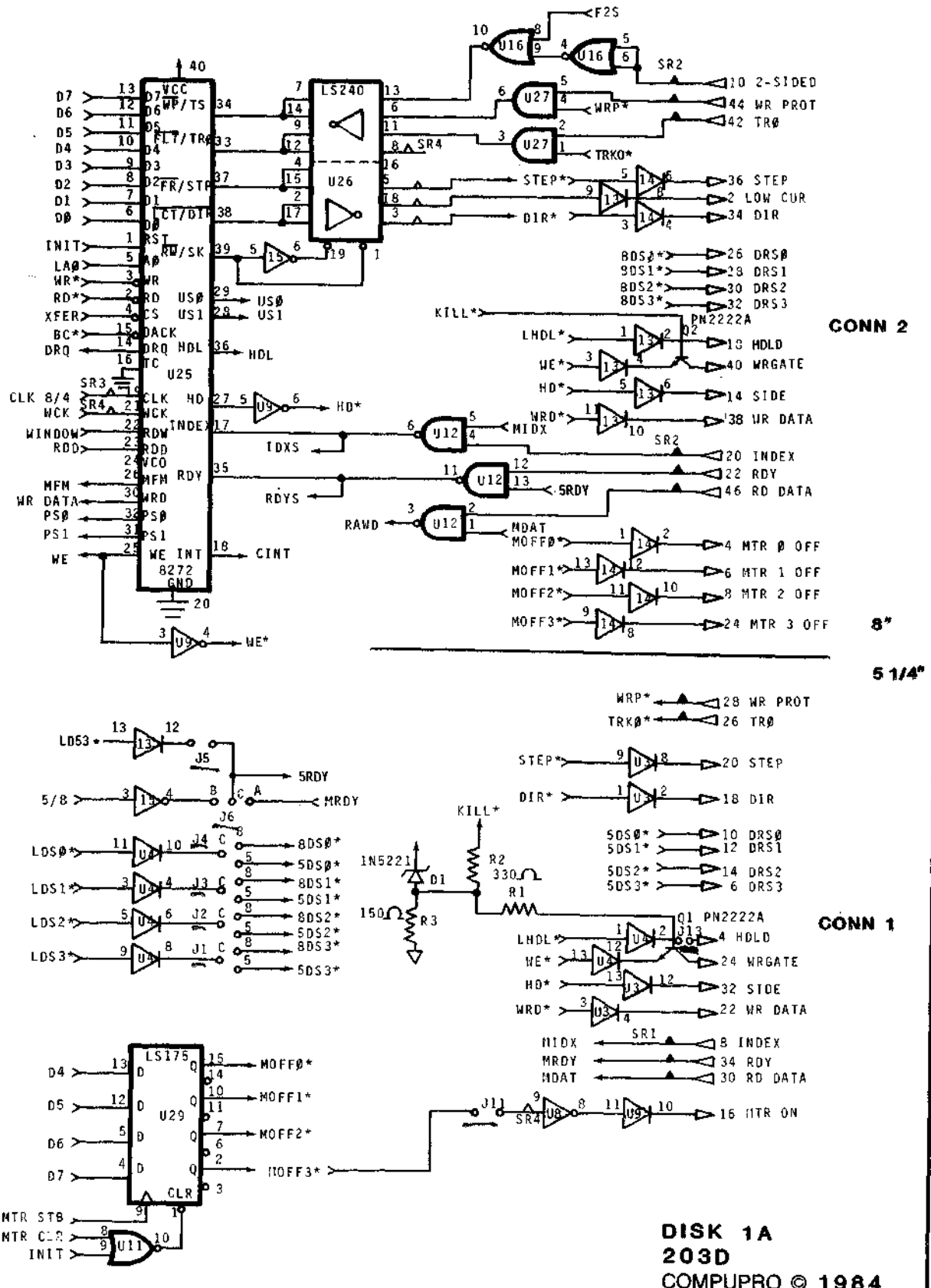
F2S
U16
SR2
10 2-SIDED
U27
WRP*
44 WR PROT
42 TRØ
TRKØ*
LS240
U26
STEP*
36 STEP
2 LOW CUR
DIR*
34 DIR
BDSØ*
BDS1*
BDS2*
BDS3*
26 DRSØ
28 DRS1
30 DRS2
32 DRS3
KILL*
PN2222A
CONN 2
LHDL*
18 HDLD
WE*
40 WRGATE
HD*
14 SIDE
WRD*
38 WR DATA
U25
8272
INDEX
IDXS
MIDX
20 INDEX
RDYS
SRDY
22 RDY
46 RD DATA
RAWD
MDAT
MOFFØ*
4 MTR Ø OFF
MOFF1*
6 MTR 1 OFF
MOFF2*
8 MTR 2 OFF
MOFF3*
24 MTR 3 OFF
8"
5 1/4"
WRP*
28 WR PROT
TRKØ*
26 TRØ
STEP*
20 STEP
DIR*
18 DIR
LD53*
J5
5RDY
5/8
MRDY
J6
LDSØ*
LDS1*
LDS2*
LDS3*
8DSØ*
5DSØ*
8DS1*
5DS1*
8DS2*
5DS2*
8DS3*
5DS3*
1N5221
D1
R2
330
R1
150
R3
5DSØ*
10 DRSØ
5DS1*
12 DRS1
5DS2*
14 DRS2
5DS3*
6 DRS3
Q1 PN2222A
CONN 1
LHDL*
4 HDLD
WE*
24 WRGATE
HD*
32 SIDE
WRD*
22 WR DATA
MIDX
8 INDEX
MRDY
34 RDY
MDAT
30 RD DATA
LS175
U29
MOFFØ*
MOFF1*
MOFF2*
MOFF3*
J11
16 MTR ON
MTR STB
MTR CLR
INIT
U11
DISK 1A
203D
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PARTS LIST

SEMICONDUCTORS

D1	1N5221
Q1,2	PN2222
U1,42	74LS38
U2	74LS10
U3,4,13,14	7407
U5	74LS139
U6	74LS174
U7,55	74LS157
U8,9,15,18	74LS04
U10	SMC9216B
U11,16,30	74LS02
U12,31	74LS00
U17,29	74LS175
U19,56	74LS74
U20	74LS165
U21,34,47,48	
U49,52	74LS244
U22-24,35-37	74LS163
U25	8272/765A FDC
U26	74LS240
U27,32,43	74LS08
U28	74LS195
U33	BOOT EPROM
U38	74LS153
U39,40	74LS393
U41	555
U44	74LS32
U45	25LS2521
U46	74LS373
U50,51	74LS245
U53	74LS375
U54	74LS138
U57-59	7805 REGULATOR
U60	74F74

CAPACITORS

C1	.0027 uF
C2,3	470 pF mica
C4	1.5 uF 10V tant.
C5-10	tant bypass
UNMARKED	.01 uF disc

RESISTORS

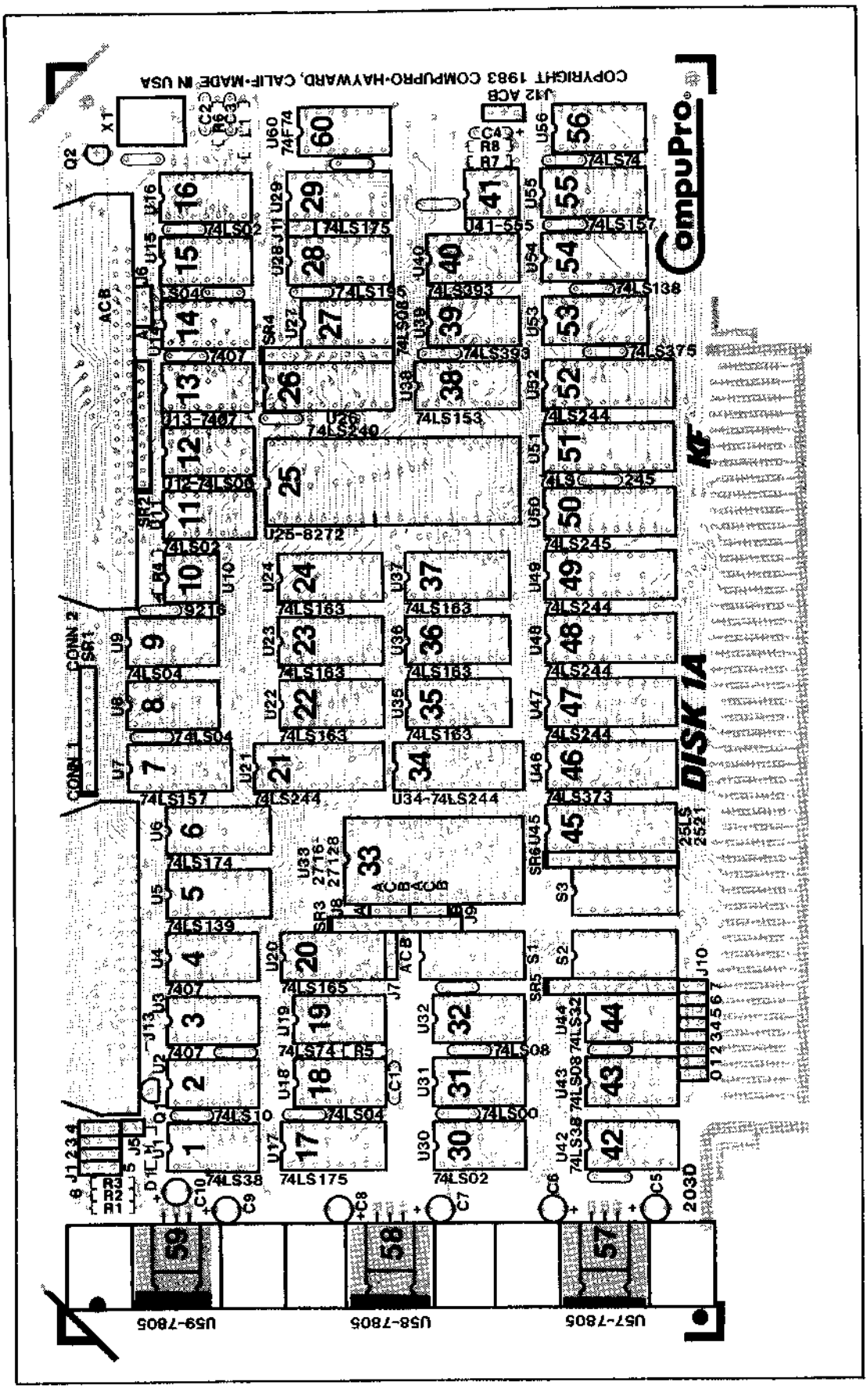
R1,2,5	330 OHM
R3	150 OHM
R4	2.7 K OHM
R6	1.0 K OHM
R7	6.8 K OHM
R8	56 K OHM

SIP RESISTORS

SR1,2	150 OHM
SR3-6	5.1 K OHM

MISCELLANEOUS

L1	1 uH Inductor
X1	16.0 MHz Crystal
S1-3	8 position DIP Switch
CONN 1	34 PIN CONNECTOR
CONN 2	50 PIN CONNECTOR
(3)	HEATSINKS
(3)	SETS OF #6 HARDWARE
(2)	CARD EXTRACTORS
(2)	2X3 PIN POSTS (J1-4)
(2)	1X2 PIN POSTS (J5,11)
(2)	1X3 PIN POSTS (J6,7)
(1)	1X6 PIN POST (J8,9)
(1)	2X8 PIN POST (J10)
(2)	8 PIN SOCKETS
(24)	14 PIN SOCKETS
(17)	16 PIN SOCKETS
(11)	20 PIN SOCKETS
(1)	28 PIN SOCKET
(1)	40 PIN SOCKET
(1)	PRINTED CIRCUIT BOARD #203



COMPONENT LAYOUT

LIMITED WARRANTY

COMPUPRO warrants this computer product to be in good working order for a period of one (1) year, (two [2] years CSC and six [6] months for disk drives) from the date of purchase by the original end user. Should this product fail to be in good working order at any time during this warranty period, COMPUPRO will, at its option, repair or replace the product at no additional charge except as set forth below. Repair parts and replacement products will be furnished on an exchange basis and will be either reconditioned or new. All replaced parts and products become the property of COMPUPRO. This limited warranty does not include service to repair damage to the product resulting from accident, disaster, misuse, abuse, or unauthorized modification of the product.

If you need assistance, or suspect an equipment failure, always contact your COMPUPRO System Center or dealer first. COMPUPRO System Center technicians are factory trained to provide prompt diagnosis and repair of equipment failures. If you prefer, or if you are not satisfied by the actions taken by your System Center/dealer, you may return the product to COMPUPRO for warranty service. Please call COMPUPRO at (415) 786-0909 to obtain a **Return Material Authorization (RMA)** number, or, write to COMPUPRO at 3481 Arden Road, Hayward, California 94545, Attn.: RMA. Be sure to include a copy of the original bill of sale to establish purchase date. If the product is delivered by mail or common carrier, you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the warranty service location (System Center or COMPUPRO) and to use the original shipping container or equivalent. Contact your COMPUPRO System Center/dealer or write to COMPUPRO at the above address for further information.

ALL EXPRESS AND IMPLIED WARRANTIES FOR THIS PRODUCT, INCLUDING THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO A PERIOD OF ONE (1) YEAR FROM THE DATE OF PURCHASE, AND NO WARRANTIES, WHETHER EXPRESS OR IMPLIED, WILL APPLY AFTER THIS PERIOD. SOME STATES DO NOT ALLOW LIMITATIONS ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS MAY NOT APPLY TO YOU.

IF THIS PRODUCT IS NOT IN GOOD WORKING ORDER AS WARRANTED ABOVE, YOUR SOLE REMEDY SHALL BE REPAIR OR REPLACEMENT AS PROVIDED ABOVE. IN NO EVENT WILL COMPUPRO BE LIABLE TO YOU FOR ANY DAMAGES, INCLUDING ANY LOST PROFITS, LOST SAVINGS OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OF OR INABILITY TO USE SUCH PRODUCT, EVEN IF COMPUPRO OR A COMPUPRO FULL SERVICE SYSTEM CENTER HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, OR FOR ANY CLAIM BY ANY OTHER PARTY.

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES FOR CONSUMER PRODUCTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU.

THIS WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, AND YOU MAY ALSO HAVE OTHER RIGHTS WHICH MAY VARY FROM STATE TO STATE.

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Note: This warranty supersedes all previous warranties, and all other warranties are now obsolete.