CompuPro®
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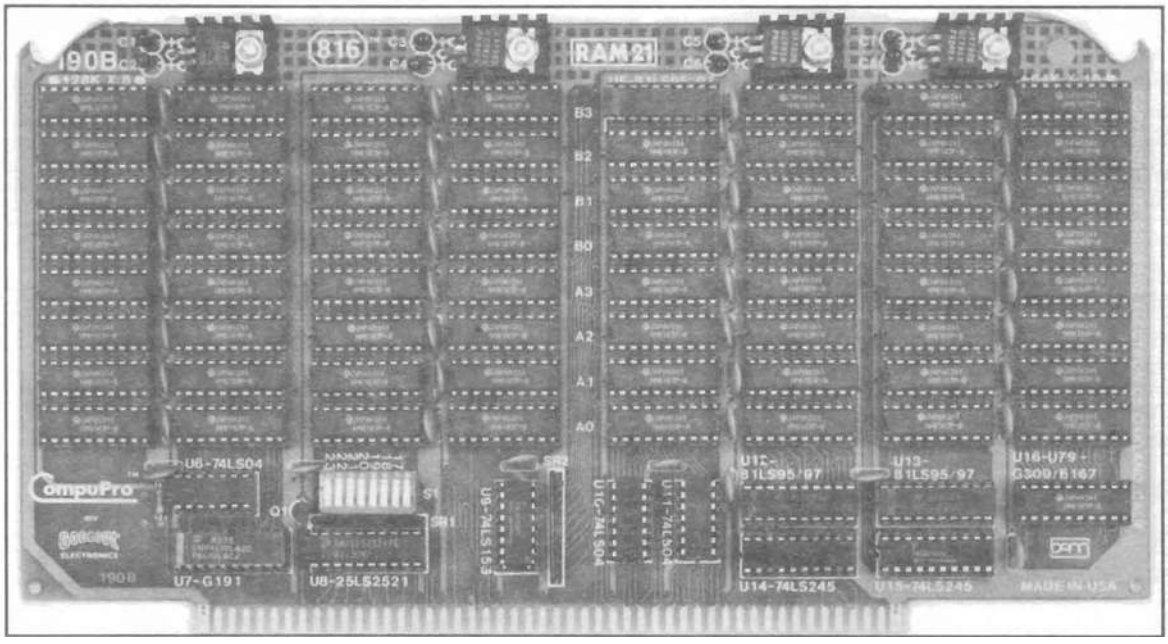
# RAM 21™

## Technical Manual

IEEE 696/S-100




## STATIC MEMORY

## 128K x 8 or 64K x 16

$10.00

A173

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## ABOUT RAM 21™

The RAM 21 from CompuPro represents one of the most advanced RAM boards ever produced for the IEEE 696/S-100 Bus. Combining state of the art static MOS RAM technology with CompuPro's design excellence makes the RAM 21 the most versatile, efficient and reliable RAM available today. The RAM 21 works as a "byte-wide" memory in 8 bit systems and automatically switches to "word-wide" mode for today's newer 16 bit systems. The RAM 21 is the choice of professionals for scientific, industrial and commercial applications where the emphasis is on full speed operation with the advanced CPUs of today and tomorrow while maintaining downward compatibility with 8 bit CPUs.

## TECHNICAL OVERVIEW

The RAM 21 uses sixty-four high performance 16K X 1 MOS RAM chips to provide a total of 128K bytes or 64K words of storage. The RAM 21 is addressable on any 128K byte boundary in the 16 megabyte address space specified by the IEEE 696 standard.

The RAM 21 also dynamically switches between "byte-wide" or "word-wide" modes per the state of the sXTRQ* signal on the S-100 Bus (see the Theory of Operation section for a complete discussion of how this protocol works).

The RAM 21 was designed to work with 8086/88 type processors at speeds exceeding 10 MHz. It also handles DMA flawlessly, a feature few boards can boast.

To reduce the number of support ICs required to pack all this function and capacity onto a standard height S-100 board, a PAL (programmable-array-logic) element is used. The PAL selects the proper memory chips and controls the complicated data bus switching scheme required to mix 8 and 16 bit operations.

## IMPORTANT NOTES:

NOTE 1. Due to the critical timing requirements of the 6 MHz CPU-Z and the internal architecture of the RAM 21 being optimized for 16 bit CPUs, a memory request wait state (S1-3) may be required when running this board at 6 MHz with CPU-Z. This board will run fine with 6 MHz 8085 and 8 MHz 8088 or 10 MHz 8086 type CPU without wait states.

NOTE 2. Active termination of the IEEE/696 S-100 standard states: "All bus lines except the power and ground lines may be terminated

to reduce bus noise..." We suggest that for most reliable operation of CompuPro products the user ensure the use of an actively terminated motherboard. This will both create an optimal bus environment and provide pull-up for the PHANTOM line. All CompuPro motherboards and enclosures comply with this recommendation.

## HOW TO CONFIGURE THE RAM 21 FOR YOUR SYSTEM

The RAM 21 requires only that the starting address of the board be set using switch S1. **All other features such as PHANTOM and byte** (8 bit)/word (16 bit) transfers are handled automatically by on-board logic. This board responds to the upper eight address lines (A16-23) as provided for by the IEEE 696/S-100 standard.

The starting address of the board is selected by setting the first seven paddles of dip-switch S1. S1 is located near the bottom left-hand corner of the board. The address is set in a binary fashion with each paddle of S1 representing an address bit. An "ON" paddle represents a binary "zero" and an "OFF" paddle represents a binary "one". The paddle to address bit relationship is shown in the following table:

**SWITCH SETTINGS FOR S1 - ADDRESS SELECTION**

| ADDRESS BIT | PADDLE NUMBER | |
|---|---|---|
| A23 | 1 | |
| A22 | 2 | |
| A23 | 3 | ON = 0 |
| A20 | 4 | OFF = 1 |
| A19 | 5 | 8 = NC |
| A18 | 6 | |
| A17 | 7 | |

EXAMPLE: If this is the first RAM board in your system and you want 128K starting at address 000000H, set paddles 1 through 7 of S1 ON.

EXAMPLE: If this is the second 128K board in the above system and you want it addressed at 020000H set paddles 1 through 6 ON and paddle 7 OFF.

EXAMPLE: If you want this board to reside at the top of the first megabyte of address space (i.e., starting address 0E0000H), set paddles 1 through 4 ON and paddles 5 through 7 OFF. Incidentally, this would put the board at the highest 128K address which an 8086 or an 8088 can directly address.

The RAM 21 is designed to work in 8 and 16 bit systems per the protocol established by the IEEE 696/S-100 standard. The DATA IN and DATA OUT busses operate as a bidirectional 16 bit data path when word transfers are performed. The two busses remain unidirectional during byte operations.

Here's how the protocol works: The bus master requests a 16 bit transfer by asserting sXTRQ* (line 58 low). If the slave (in this case the RAM 21) is capable of performing word transfers, it acknowledges this fact to the master by asserting SIXTN* (line 60 low). **Sometimes, even a 16 bit master may only want to transfer** one byte rather than a whole word. In this case, the master does not assert sXTRQ* but instead uses the data busses as an 8 bit master would, that is: data from the master would be transferred on the DO bus and data to the master would be transferred on the DI bus.

The RAM 21 handles this multiplexing of the data busses with two bi-directional bus buffers (U14 and U15) and three intermediate buffers (U5, U12 and U13). Both U14 and U15 are enabled for all word transfers. Both U5 and U12 are enabled for word read operations. When byte writes occur with A0=0, U14 only is enabled. When byte writes occur with A0=1, U14 and U13 are enabled. When byte reads occur with A0=0, U12, U13 and U15 are enabled. When byte reads occur with A0=1, U5 and U15 are enabled.

This complicated algorithm is executed by PAL (programmable array logic) element G191 (U7). The PAL also selects the proper array decoder(s), U9, for 8 or 16 bit transfers. The RAM is configured as two arrays of 64K by 8 bits, A and B. The bit/address decode scheme is covered in the next section. The PAL also generates the signal ENM*, which enables the decoder (U9) only during memory reference operations. This feature, coupled with the use of RAM chips which power down when not selected makes the RAM 21 consume less power than most dynamic RAM designs while providing the speed of operation and reliability that only static RAM delivers.

The base address of the board is set with dip-switch S1. Octal comparator (U8) generates signal BSEL* when the address present on bus lines A17 through A23 matches that set in S1-1 through S1-7. Position 8 of S1 is not used.

ESXT* is the signal generated in the PAL which causes the RAM 21 to acknowledge requests for word transfers when the board is selected. Transistor Q1 provides the open collector output required to drive bus signal SXTN* (line 60).

## LOCATING RAM ICs BY ADDRESS AND BIT

The COMPONENT LAYOUT on the next page may be used as a map to locate RAM ICs by address and bit. Bit numbers are shown at the top of each column of RAM IC's with bit 0 at the right through bit 7 on the left. Row numbers A0 through B3 are arranged vertically in the center of the RAM array. Note the dual bit numbers in row A3; the right hand number is the bit number when the RAM 21 is operating in the word or 16 bit mode. In the word mode two rows of RAMs are selected. The low order byte is in array B and the high order byte is in array A. Row selection is the binary decode of system bus lines A15 and A16. For example, to select rows A0 and B0 both A15 and A16 would have to be in the zero state.

In the byte or 8 bit mode one row of RAMs is selected. All even bytes, A0 in the zero state, are in array A. All odd bytes, A0 in the one state, are in array B. Row number selection is the binary decode of lines A15 and A16 as above with the addition of the state of A0 determining whether that row is in array A or array B.

## PARTS LIST

SEMICONDUCTORS

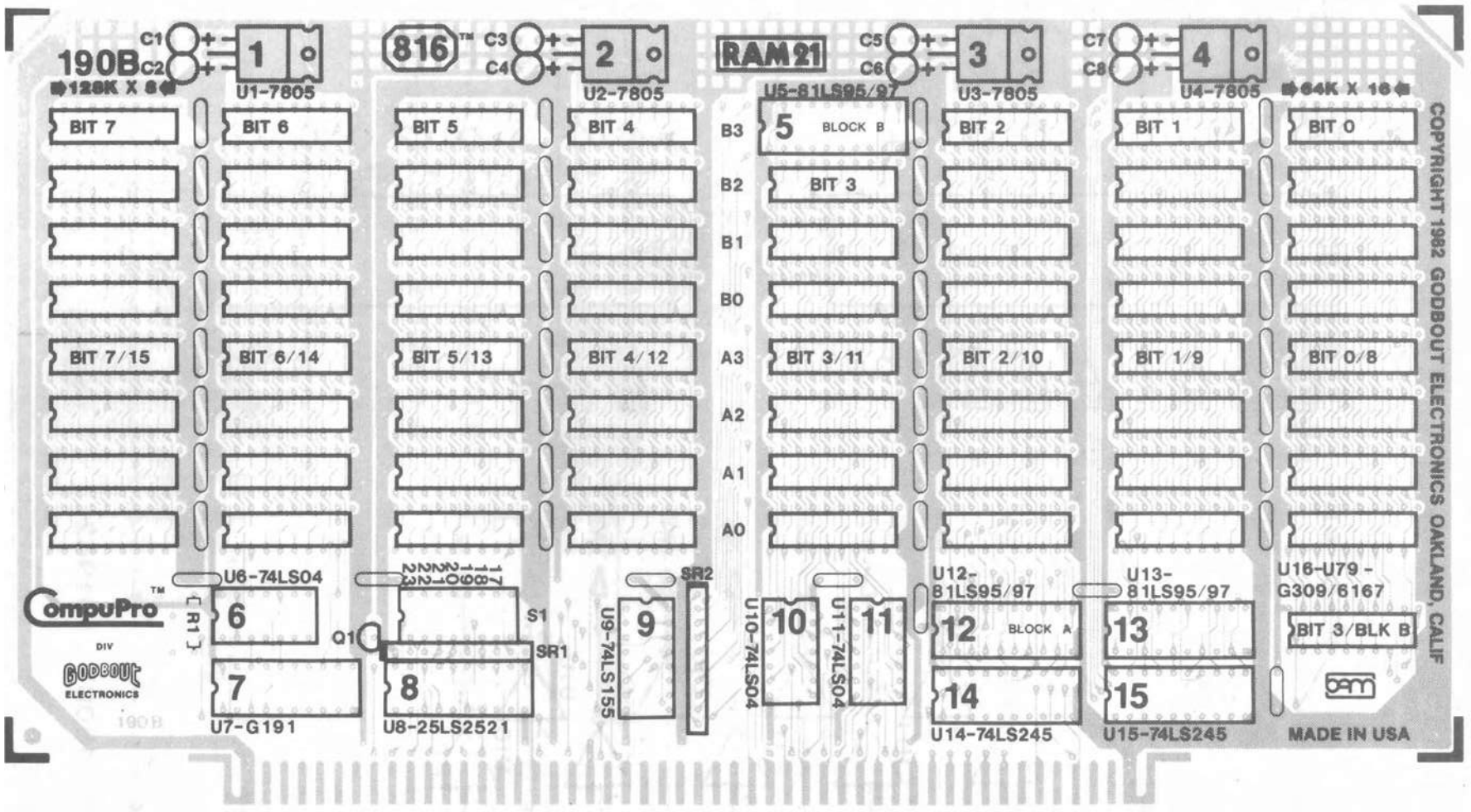
| | |
|---|---|
| Q1 | MPS 3646 |
| U1-4 | 7805 |
| U5, | 81LS2521 |
| U6, | 74LS04 |
| U7 | G191 |
| U8 | 25LS2521 |
| U9 | 74LS155 |
| U10-11 | 74LS04 |
| U12-13 | 81LS2521 |
| U16-79 | GBT1400/HM6167 |

CAPACITORS

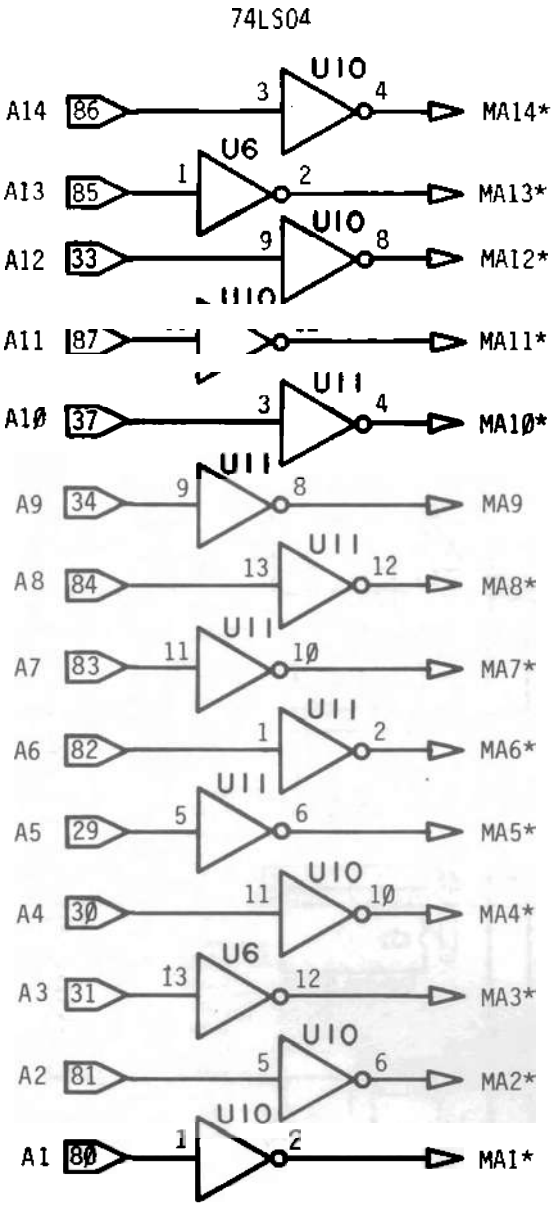
| | |
|---|---|
| C1-8 | 10V/higher dipped tant. |
| C9 | 68 pF dipped mica |
| (38) | bypass capacitors |

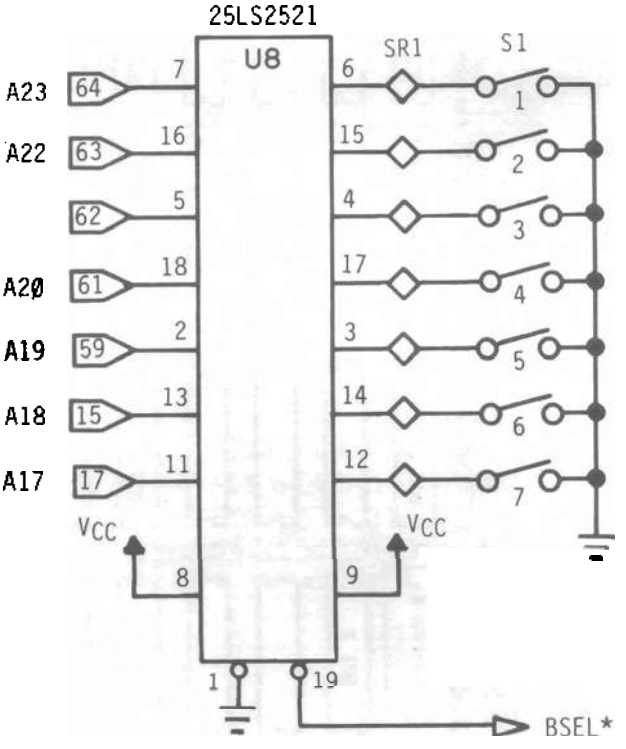
RESISTORS

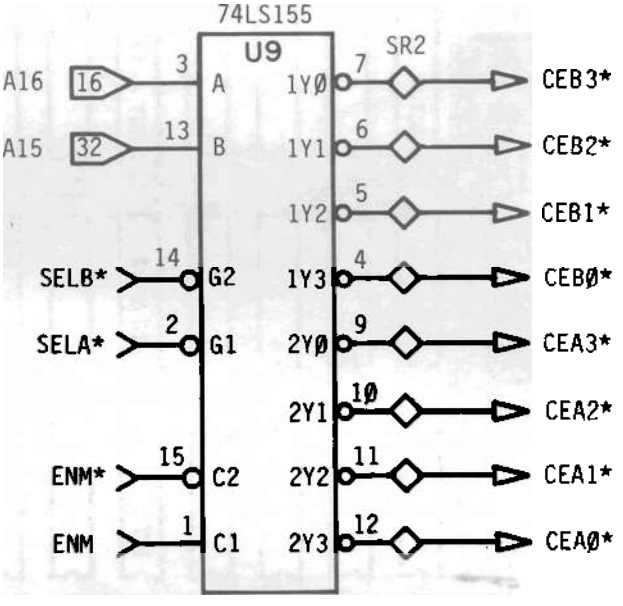
| | |
|---|---|
| R1 | 1.5 K Ohm |
| S1 | 8 position DIP switch |
| SR1,2 | 5.1K Ohm SIP - 10 pin |




COMPONENT LAYOUT

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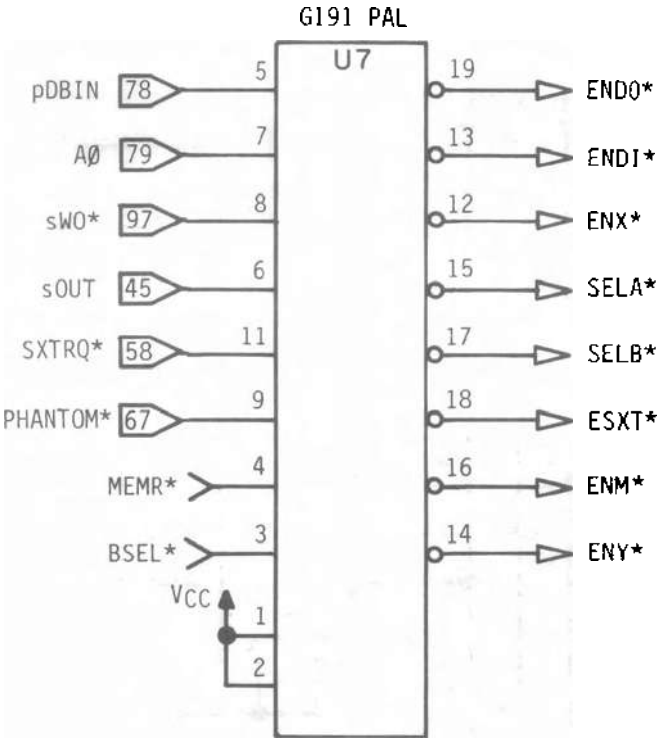
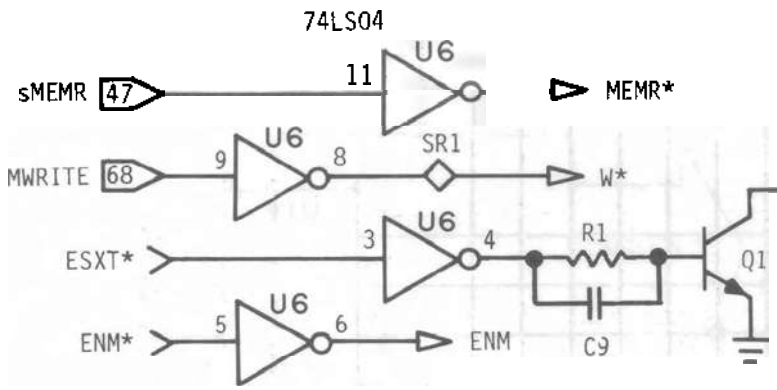
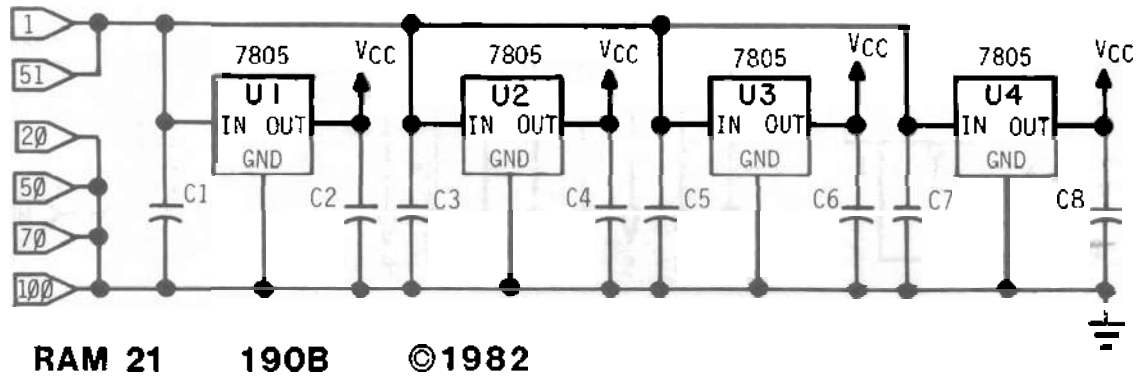



◇ = SIP PULL-UP RESISTOR = VCC SR X

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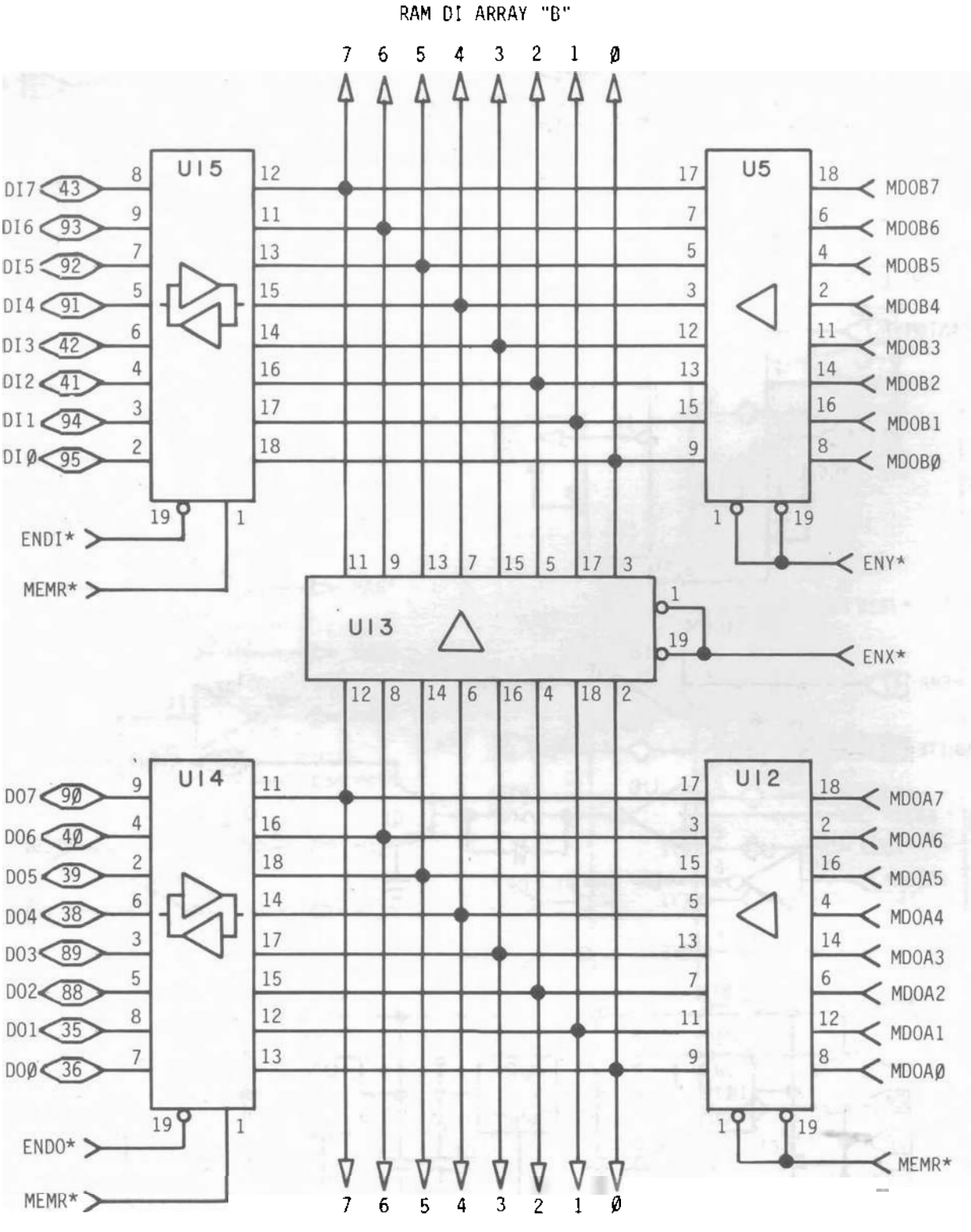


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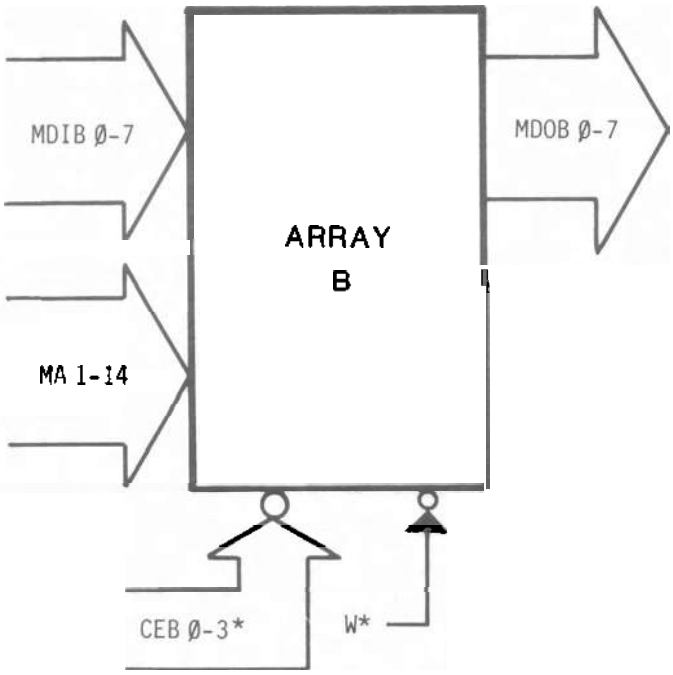


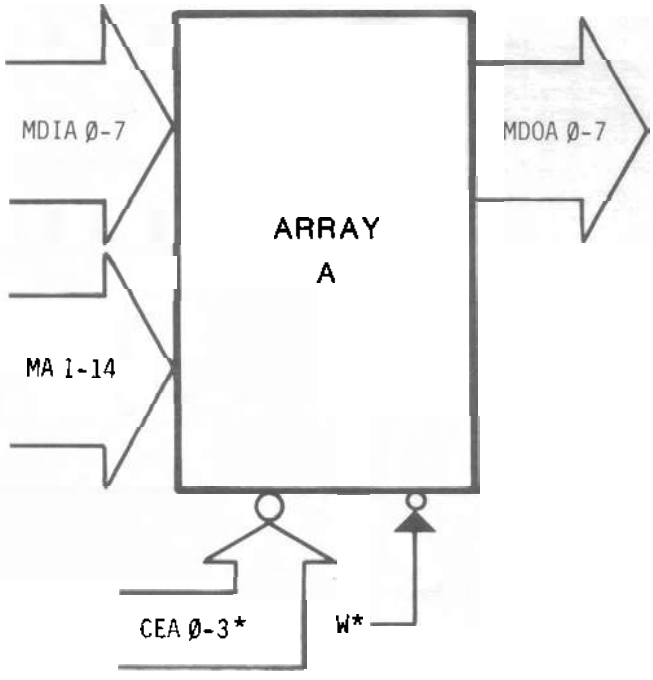


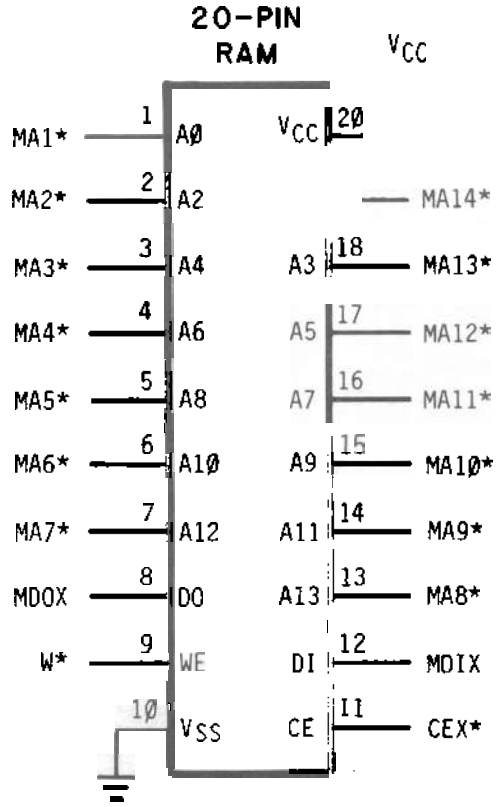


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