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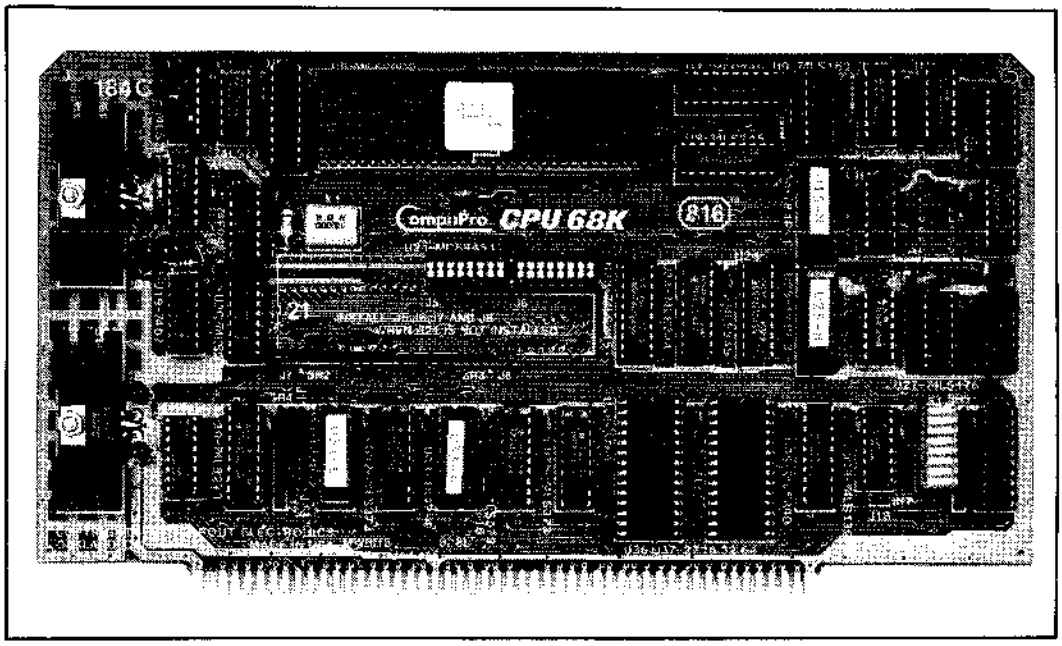
CPU-68K™

Technical Manual

IEEE 696/S-100



16 BIT 68000

with provisions for MMU and up to 16 K bytes of ROM

Clock Rates to 10 MHz

$20.00

A196

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ABOUT CPU 68K

The **CompuPro CPU 68K**™ board is a central processing unit based on the 68000 microprocessor. Another member of the CompuPro product family, the CPU 68K will upgrade any 8-bit system to a very powerful 16-bit system without requiring a complete system change. The CPU 68K will work with older IEEE 696/S-100 8-bit memory boards as well as with newer 16-bit memory boards, or any mix of the two. The CPU 68K also features a flexible interrupt handling system, two sockets for up to 16K bytes (8K words) of on-board ROM, a jump-on-reset feature to allow system operation to start anywhere in the memory space, and wait circuitry to add up to 5 waits for any type of machine cycle. Other features include 24-bit addressing, and provisions for an optional Memory Management Unit. The 16 megabyte addressing range includes a 64K block of I/O port addresses. Any combination of 8- and 16-bit memory and peripheral devices may be used.

The assembled and tested version of the CPU 68K includes an 8 MHz 68000 and may be operated at either 4 or 8 MHz. The CSC version features a 10 MHz 68000 and will operate at either 5 or 10 MHz. The CPU 68K is fully IEEE 696/S-100 compatible when operated within the 6 MHz range defined by the specifications.

The S-100 bus is the professional level choice for commercial, industrial and scientific applications. This bus provides for ready expansion and modification as the state of the art improves. We believe that this board, along with the rest of the CompuPro product line, is one of the best boards available for the S-100 Bus. CompuPro continually strives to create products with superior performance, the finest quality components and unprecedented reliability. P.Q.R. synonymous with CompuPro.

TECHNICAL OVERVIEW

Clock Rate Selection

The standard 68000 is an 8 MHz CPU (10 MHz for the CSC version). The board may be operated at either full or half speed as selected by J1. The 2 MHz bus CLOCK signal is derived by division of the oscillator frequency as controlled by J2 and J3. The board speed can be determined by looking at the crystal below the 68000 chip. A 20 MHz crystal should be installed for 10 MHz operation, and a 16 MHz crystal for 8 MHz operation.

CPU 68K (assembled and tested 16 MHz crystal)

4 MHz Operation		8 MHz Operation	
J1	A-C	J1	C-B
J2	OFF	J2	OFF
J3	OFF	J3	OFF

CPU 68K (CSC, 20 MHz crystal)

5 MHz Operation		10 MHz Operation	
J1	A-C	J1	C-B
J2	ON	J2	ON
J3	OFF	J3	OFF

MEMORY SOCKETS

The CPU 68K has two sockets (U36 and U37) for a pair of ROMs. Jumper options allow the use of 2716, 2732 or 2764 type EPROMs for ROM capacities of 2K, 4K or 8K words respectively. Because of the word organization (even bytes in U36, odd bytes in U37), ROMs must always be used in pairs. The base address for the ROM is provided partially by a DIP switch (for high order bits through A15) and partially by a PAL (U31 determines the extended address page for the ROMs). As shipped, the ROM resides in extended page FD0000 (hex) of PROGRAM space. When 2716 or 2732 type EPROMS are used, they must be installed in the lower 24 pins of the 28 pin sockets. J17 must also be set appropriately for each type of EPROM as shown below.

	2716	2732	2764	
SW1-2	ON	ON	OFF	
SW1-3	ON	OFF	OFF	
SW1-4	ON	ON	ON	
SW1-5	A15	A15	A15	
SW1-6	A14	A14	A14	ON = "0"
SW1-7	A13	A13	OFF	OFF = "1"
SW1-8	A12	OFF	OFF	
J17	A-C	C-B	C-B	

To disable sockets completely, turn SW1-4 OFF.

POWER-ON-JUMP (POJ) - The 68000 will fetch two double words from memory address zero following a RESET. This data is used to initialize the stack pointer and program counter. In systems with a DISK 1, the DISK 1's boot ROM will usually be used to provide this data. If a DISK 1 is not available, the CPU 68K may self boot using its own ROMs to provide the initialization data.

If the CPU 68K POJ feature is enabled by installation of a shorting plug at J4 (near U12), a BOOT flip flop will be set by bus RESET. When set, the BOOT flip flop makes the local ROM global (i.e.: the ROMs repeat[modulo] their length throughout the address space). BOOT will enable the ROMs in this way regardless of the state of the ROM enable switch SW1-4. When the 68000 makes its first two double word fetches, the data will be obtained from the first eight bytes of local ROM. This data is used to initialize the stack pointer and program counter as mentioned above. A useful initial value for the program counter is address 000008 (hex), the next location in the ROM. Location 000008 (hex) may then contain a JSR instruction which will send the 68000 to wherever it is to continue. The BOOT flip flop is cleared by any memory write operation. When the JSR is executed, the 68000 will push the current PC onto the stack before going to the new address. This push resets BOOT, limiting the local ROM to its normal address range and allowing access to external memory. If the JSR points to address FD000E (hex), execution would continue in the local ROM at the location following the JSR.

I/O - The CPU 68K has memory mapped I/O at a location determined by PAL U31. The PAL which is labeled 184P-2A maps the I/O into extended page FF0000 - FFFFFF (hex) of DATA space providing 64K ports. To a program, all I/O devices will appear as memory, however, accessing any of these addresses will result in S-100 bus I/O cycles. Since most I/O devices only decode an 8-bit address (0-FF (hex)), the programmer should be aware that if the program accesses location FF0100 (hex) it will usually get the same I/O device as location FF0000 (hex). Although the CPU 68K can access up to 64K I/O devices, very few I/O devices have 16-bit addressing capability.

MWRT - The CPU 68K board is capable of generating the MWRT bus signal on pin 68. Jumper J14 (below U32) should be installed if the CPU 68K is to generate the MWRT signal. The IEEE 696/S-100 standard requires that MWRT be generated in only one place in the system, and usually a front panel generates the signal. If there is not a front panel in the system then the shorting plug for J14 should be installed. As shipped the CPU 68K has the shorting plug installed, but this should be removed if there is a conflict with another source.

PHI-DSB - The CPU 68K is capable of tri-stating the PHI bus signal on bus pin 24. This capability is reserved for future slave processor boards which want to take over the bus and run at a completely different bus speed. By installing a shorting plug on jumper J15 (below U33) the CPU 68K will tri-state its PHI clock driver in response to PHI-DSB*, an active low signal on bus pin 21. PHI on the bus will be enabled or disabled on rising edges of the internal PHI clock after PHI-DSB* is asserted or removed. As shipped the CPU 68K has the shorting plug removed.

pDBIN - The CPU 68K provides two different sources for the bus signal pDBIN. These two sources, controlled by jumper J16 (between U33 and U34), may provide either a synchronous or asynchronous read strobe pDBIN. The synchronous version (J16 A-C) will assert pDBIN on the rising edge of the bus clock which ends pSYNC. This version of pDBIN will meet all IEEE 696/S-100 specifications. The asynchronous version (J16 C-B) will assert pDBIN one gate delay after pSTVAL which occurs at the falling edge of the bus clock within pSYNC. While this may not meet the minimum delay specified for pSTVAL to pDBIN, it causes no problems for static RAM and allows higher speed operation without wait states. For bus speeds above 6 MHz the asynchronous pDBIN is preferred, because it provides a longer read strobe, but to meet the IEEE 696 standard the clocked version of pDBIN is available. As shipped the CPU 68K uses the asynchronous pDBIN (J16 B-C).

MMU - The CPU 68K will accept a 68451 Memory Manager Unit (optional). Use of the MMU will add two clock states to each bus cycle. Since these states are inserted before the bus cycle begins to allow time for address translation, system speed is lowered as if they were wait states, but no additional strobe width is provided.

To install the MMU, remove jumpers J5, J6, J7 and J8. Install the 68451 at location U21 and 74LS245s at U7 and U8.

If a board is to be revised to use a MMU return the board to the factory for the modification and testing of the MMU. Contact CompuPro for current pricing.

WAIT-STATES - The CPU 68K has very versatile wait state generation hardware to provide compatibility with a broad range of hardware which does not share its speed. The user may select from zero to five wait states independently for I/O cycles, ROM cycles and M1 cycles. In addition, the same range of waits may be asserted for all cycles. Each of the functions (M1, ROM, I/O or ALL) has a control pin which may be left open for zero wait states or jumpered to one of the five wait lines (1W, 2W, 3W, 4W or 5W). The longest applicable wait selected will apply. For example, an instruction fetch from local ROM will be subjected to the number of waits programmed for ALL, but may be subjected to an even greater number of waits programmed for M1 or ROM cycles. The bus ready lines XRDY and pRDY may of course extend the cycles even more.

J9-A	5W	J10-A	I/O
J9-B	4W	J10-B	ROM
J9-C	3W	J10-C	M1
J9-D	2W	J10-D	ALL1
J9-E	1W		

Each functional line may be connected to one wait line or left open for zero waits. Shorting plugs may be used to jumper straight across, or 30 gauge wire-wrap wire may be used to scramble wire the waits.

INTERRUPTS - The 68000 microprocessor has hardware built in to support a seven level prioritized interrupt structure. This feature is used to implement the IEEE 696/S-100 bus non-maskable interrupt line NMI* and six of the vectored interrupt lines VIn. The bus NMI line is latched on the CPU 68K since this line may be pulsed and the 68000 requires that the line be asserted until serviced. The latched NMI is connected to interrupt level 7, the highest priority. The remaining six levels will normally be used for bus lines VI0 through VI5.

The 68000 internal interrupt structure allows interrupts with priorities below any desired level to be masked OFF by software. This allows the implementation of fully nested interrupt schemes.

A jumper option will allow the CPU 68K to assert the bus INT* line when an interrupt is pending. This is a signal for temporary masters to release the bus for interrupt processing.

If the CPU 68K user wishes to use another interrupt controller such as a System Support 1 board, the level 6 priority input may be jumpered to INT* instead of VI0. Lower priority lines which are physically connected must be masked OFF by software if desired.

To process interrupts on the CPU 68K without the use of any external controller, SW1-1 should be turned ON enabling the 68000 "auto vector" mode. In this mode, an interrupt vector is determined by the priority level of the interrupt. If the board is to be used with an external controller which is capable of providing a vector, SW1-1 should be left OFF. When the 68000 responds to an interrupt, it fetches a word from which it extracts the lower byte which is used to enter a table. If the external controller can provide only a byte response, then a shorting plug should be installed on jumper J18 (below U39). This will prevent the CPU 68K from performing two consecutive byte reads on an interrupt acknowledge cycle even though the interrupt controller fails to assert the 16-bit acknowledge line SIXTN. The single byte received on the DI bus will be used as the vector. The data on the DO bus (which is not driven in this case) is the byte which is thrown away. This jumper should be left OFF when using a System Support 1 board to provide the vector since it expects to provide two consecutive bytes on an interrupt acknowledge and to have the first byte discarded.

NOTE: THE "D" revision 68K board will not operate properly in AutoVector mode. A modification can be made at the factory for those users who need this capability in their system.

Interrupt Input Lines:

J12-1	VI-7	
J12-2	VI-6	
J12-3	VI-5	(Tied to Level 1)
J12-4	VI-4	(Tied to Level 2)
J12-5	VI-3	(Tied to Level 3)
J12-6	VI-2	(Tied to Level 4)
J12-7	VI-1	(Tied to Level 5) (IRQ from MMU)

Interrupt processing without an independent controller:

S1-1	ON	Enable "Auto Vector" mode.
J13	C-D	Ties VIO To Level 6.
J13	A-B	To assert INT* on pending interrupt.

Interrupt acknowledge to expect vector:

S1-1	OFF	Disable "Auto Vector" mode.
J13	C-B	INT* to Level 6.
J18	ON	Single byte acknowledge response.
J18	OFF	Word acknowledge response.

Note: Jumpers J12 and J13 are between U30 and U31

THEORY OF OPERATION

CLOCK CIRCUITRY - The LC oscillator consisting of L1, C5 and C6 is constrained to a precise frequency by the crystal X1. Half of U4 (74LS74) is used to divide the oscillator frequency by two. The jumper J1 selects whether the input of a second divide by two in U4 is obtained from the first divide by two or from the oscillator directly. The second binary provides a clock for the 68000 and the bus of 1/2 or 1/4 of the crystal frequency.

Bus PHI (pin 24) is driven by U13 and will be tri-stated if the PHI-DSB* jumper is installed and the signal is asserted. The flip-flop in U3 is used to synchronize the enabling and disabling of the clock on the bus so that clock on the bus will always be in the high state when one is enabled and the other disabled.

The 2 MHz bus clock signal is derived by dividing the oscillator frequency by 8, 10, 12 or 14. The divisor is selected with J2 and J3. The counter U9 actually loads at a 4 MHz rate. Since the top stage loads its complement through the inverter U11, a symmetric 2 MHz is obtained.

POC* and pRESET* - According to the IEEE 696/S-100 standard bus signal POC* should occur on every power-on and after PWRFAIL* goes away. POC* should also generate pRESET* and SLAVECLR* bus signals. This is accomplished by circuitry shown on page 6 of the schematic using Q1, C7, D1, and some other buffers along with a flip-flop in U3 (74LS74). Upon initial power-on C7 will charge through R4. The collector base junction of Q1 will be reverse biased, isolating it from the circuit. When the bus signal PWRFAIL* is asserted and subsequently goes away, the flip-flop will be clocked low and cause Q1 to discharge C7 and cause another POC*, which will preset the flip-flop again.

DATA BUS - The S-100 allows byte addressing of memory and peripherals. 8-bit transfers are allowed to any address, 16-bit transfers to even addresses only. The 68000 is a word addressing processor. It provides separate strobes for the upper and lower halves of its data bus and so may perform byte operations by inhibiting one of the two strobes. To operate the 68000 on the S-100 bus, an A0 is derived from the upper and lower data strobe signals.

The S-100 specification also defines a handshake which allows CPUs capable of 16-bit data transfers to function with either 8- or 16-bit memory and I/O. A CPU capable of 16-bit data transfers and wishing to access a word will assert the 16 request status line sXTRQ* along with the word address. If the addressed memory or peripheral device is capable of the 16-bit operation, it will assert the acknowledge signal SIXTN* as an indication to the CPU that all 16 bits of data will be transferred in a single bus cycle. If an 8-bit device has been addressed, it will ignore sXTRQ* and not assert SIXTN*. If the bus cycle is a write operation, only the data on the DATA-OUT bus will be transferred on the current cycle. The state machine consisting of U15 and U25 will generate a

second bus cycle to write the odd addressed byte. The data previously asserted on the DATA-INPUT will be asserted on the DATA-OUT bus. If the attempted word operation was a read, only the data on the DATA-INPUT bus from the even addressed byte will be received on the first cycle. The state machine will perform a second read from the odd addressed byte to obtain the balance of the word. The operations of the bus state machine are transparent to the 68000 since the cycle is not acknowledged until all bytes have been transferred.

POWER-ON-JUMP (POJ) - The CPU 68K can use the first 8 bytes in the on-board ROM to get the initial Program Counter and Stack Pointer. This function is controlled by a latch consisting of parts of U10 and U12, and U31. If Jumper J4 is installed then upon receiving a reset the latch will assert the BOOT signal and U31 will assert the ROM-SEL signal. This will select the ROM chips throughout the memory map until the first write operation. The R/W signal will clear the latch when it goes low and cause BOOT to go away. The ROM-SEL signal will then only be asserted when the proper address is selected. The POJ usage is explained in the Technical Overview Power-On-Jump section.

ROM SOCKETS - Sockets for either 2716, 2732, or 2764 EPROMs are provided by U36 and U37. These sockets are addressed partially in a PAL (U31) and partially by U40 (25LS2521). U31 has the 8 high order address lines (A16-A23) and ROM-RANGE as inputs as well as status signals from the 68000. This allows the sockets to be addressed in extended page FD (hex) PROGRAM space only. U40 decodes lower address lines by comparing switch inputs with the address lines coming into the comparator. When the address matches the selected address ROM-RANGE will be asserted and go to PAL U31. When using 2732's or 2764's, more address lines must go to the EPROMs to access the larger amount of memory, and hence these address lines must not go to the comparator U40. These address lines are disconnected from the comparator by switching SW1 positions 2 and 3 to OFF. When these switches are OFF the corresponding switch on the other side of the comparator must also be OFF. Switch settings are explained in the Technical Overview.

INTERRUPT CIRCUITRY - Page 4 of the schematic shows the interrupt circuitry and the J12 jumper positions. These jumper positions can be used to allow VI6 or VI7 to be jumpered to any of the other VI lines if needed. Jumper J13 is used to allow the INT bus line (pin 73) to be either an input or an output or allow VI0 to be an input to the vector generation circuitry. Latch U30 (74LS273) is used to latch any pending interrupt and present the interrupts to the priority encoder U29 (74LS148). The encoder then sends the highest priority vector to the 68000 chip and the interrupt will be serviced if the software will allow it. The NMI signal is latched by U20 and will cause the highest priority interrupt to the 68000 chip.

WAIT CIRCUITRY - Page 3 of the schematic also shows the wait generation circuitry. U27 (74LS175) and U28 (74LS151) are the heart of the wait circuit. Jumpers J9 and J10 can be connected to cause up to 5 waits for any type of operation. At the end of each operation the signal STB-ENA goes away clearing the wait counter U27. When the next operation starts the counter will start to count and if any of the waits are selected the appropriate outputs will be low until a certain count (up to 5) is received. The multiplexor U28 will allow only one input to go out depending on the type of operation, and if the selected operation has a low input the processor will wait until the input goes high. This will occur for every type of operation depending on the jumper configuration. Any operation can have any number of waits, or all operations can have the same number of waits. Wait selection is explained in the Technical Overview Wait section.

MEMORY MANAGEMENT UNIT - The CPU 68K has the provisions for adding the companion memory management unit (MMU) 68451 to allow for dynamic memory allocation. Using this chip adds two clock cycles to each memory operation which is required to translate the virtual address coming from the 68000 to the new physical address which will go out to the bus. When the MMU is initially reset, it comes up in a transparent mode which passes the virtual address straight through to the bus. To send commands to the MMU U7 and U8 (74LS245) must also be installed. U31 looks at the upper 8 address lines and the function codes (FC0-FC2) from the 68000 and will generate the MMU-SEL signal when extended page FE is selected in the SUPERVISOR DATA mode. When the MMU is initialized, it will remap addresses as assigned and abort certain operations depending on the modes selected in the MMU. For more details on the MMU, consult the data sheet for the 68451.

When the MMU is not installed, jumpers J5-J8 must be installed to allow the address bus from the 68000 to drive the address bus drivers and connect the address strobe from the 68000 to the rest of the board which can use either the strobe from the 68000 or the 68451.

ADDRESS BUS - The S-100 address bus is driven by U32, U34, and U35 (74LS373). These devices are transparent latches used as bus drivers when the MMU is not installed and used as latches when the MMU is installed. The different usages come about because the MMU drives the physical address bus for only a short period of time then floats the bus, the latches grab the address and holds it for the proper length of time. When the MMU is not installed the 68000 directly drives the address buffers through jumpers J5 and J6 and the latches remain transparent due to a pullup resistor on the HAD signal line.

STATUS BUS - The status signal on the S-100 bus are driven from U38 (74LS240). These signals are decoded from U39 (74LS139), and one gate in U16 (74LS27), as well as some signals directly from the 68000. These signals will be floated when the SDSB* signal is asserted on the bus.

CONTROL BUS - Four of the control signals come from U33 (16R4), and the other control signal, pSYNC, comes from U15 (16R4). These devices are programmable array logic (PAL) chips which are factory programmed to generate the proper S-100 bus timing for these signals. The pDBIN signal is jumper selectable (J16) to use one of two signals coming from U33. The two signals are slightly different in that output 19 is a gate output and will come out one gate delay after the pSTVAL* signal, and output 14 is a clocked output making the pDBIN come out with the rising clock edge occurring when the pSTVAL* signal is asserted. These signals are both generated to allow a longer read strobe which may not meet the IEEE 696/S-100 standard, and the clocked output which will always meet the standard. When the CPU 68K is used at speeds above 6 MHz the IEEE 696/S-100 standard is no longer binding, and the asynchronous pDBIN signal is recommended to allow for more time for the read strobe. This is achieved by having jumper J16 in the B-C position. The control bus will be floated when the CDSB* signal is asserted on the bus.

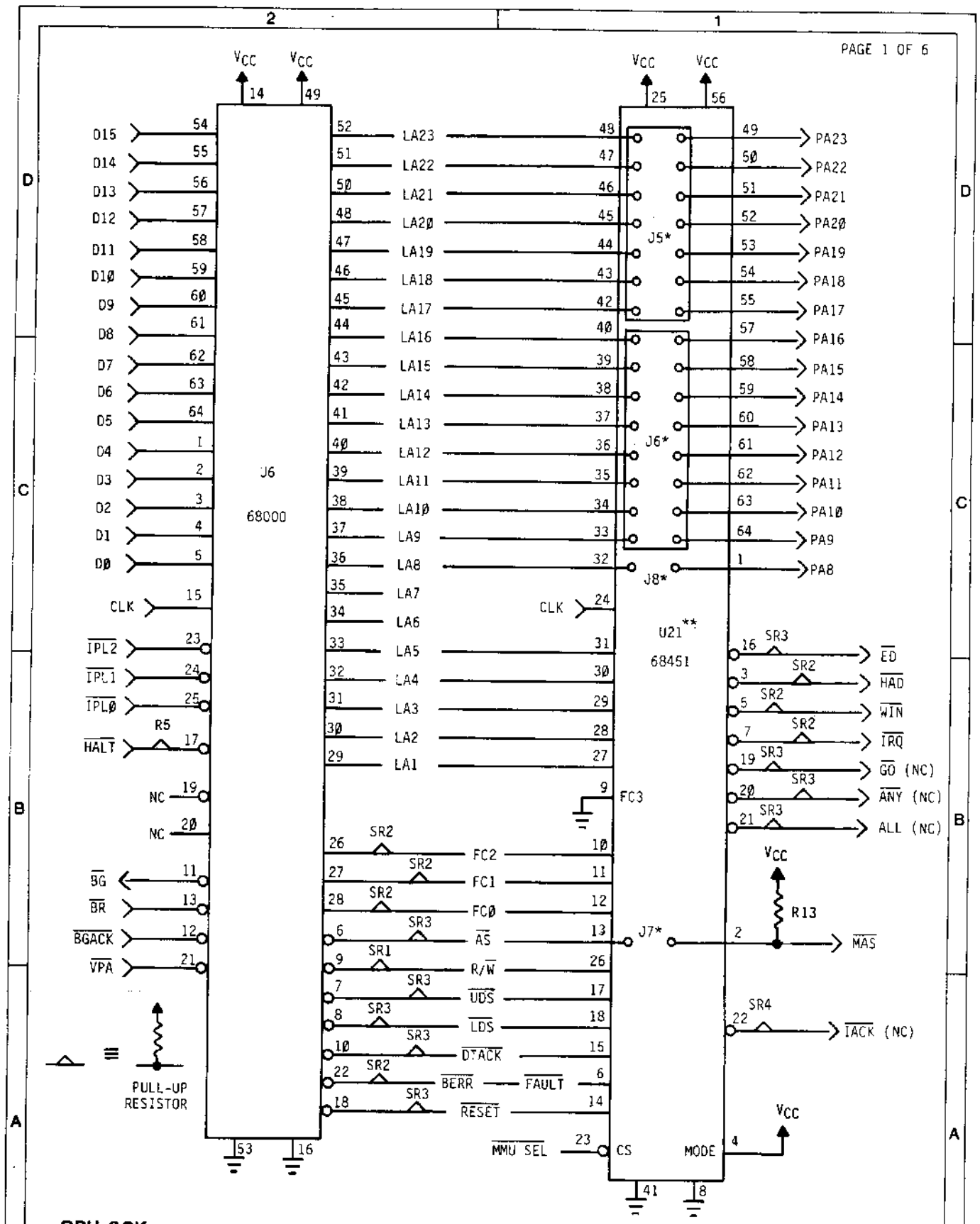
STATE MACHINE - The CPU 68K performs the byte fetching sequence by making the 68000 wait while two bus cycles occur. This is accomplished by the state machine in U15 (16R4). Inputs for this PAL come mainly from the 68000 and the gate used to determine if one or two bus operations are needed. If two operations are needed the state machine synchronizes the signals with the clock input and generates all the proper strobes, and increments address line A0. Then the processor is released from waiting and allowed to complete the operation. If jumper J18 is not installed, the two cycle operation will also be performed during an interrupt acknowledge operation. This is required for proper operation with the System Support board because the interrupt circuitry on the System Support sends two bytes of information during the interrupt acknowledge operation.

JUMPER and SWITCH SUMMARY

The following summary of jumpers and switches explains the function of each option, the location, and the manual page with the detailed explanation for usage.

JUMPERS	FUNCTION	BOARD LOCATION	PAGE
J1	CLOCK SPEED	BETWEEN U4 & U5	5
J2	2 MHz	BETWEEN U7 & U9	5
J3	2 MHZ	BETWEEN U7 & U9	5
J4	POWER-ON-JUMP	BETWEEN U11 & U12	6
J5	MMU OPTION	IN U21 OUTLINE	7
J6	MMU OPTION	IN U21 OUTLINE	7
J7	MMU OPTION	BELOW U21	7
J8	MMU OPTION	BELOW U21	7
J9	NUMBER OF WAITS	BETWEEN U27 & U28	8
J10	MACHINE CYCLES	BETWEEN U27 & U28	8
J11	DELETED REV.D		
J12	INTERRUPTS	BETWEEN U30 & U31	9
J13	BUS INT PIN	BETWEEN U30 & U31	9
J14	MWRITE	BELOW U32	7
J15	PHI-DSB	BELOW U33	7
J16	pDBIN	BETWEEN U33 & U34	7
J17	ROM ADDRESS	BETWEEN U36 & U37	6
J18	INTERUPT ACK.	BELOW U39	9
SW1 POS 2-8	ROM ADDRESS	BETWEEN U39 & U40	6
SW1 POS 1	AUTO VECTOR	BETWEEN U39 & U40	8

HARDWARE SECTION



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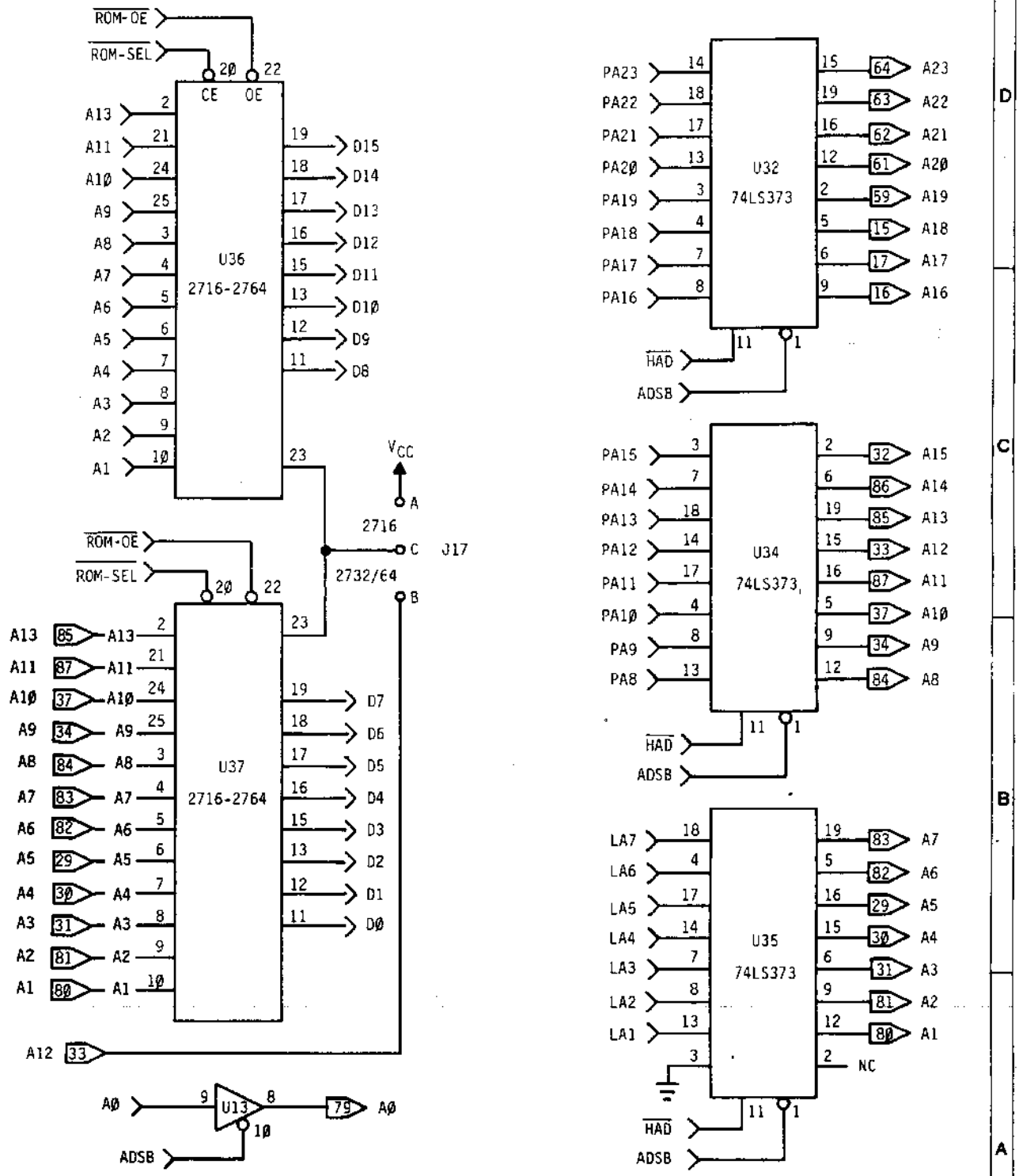

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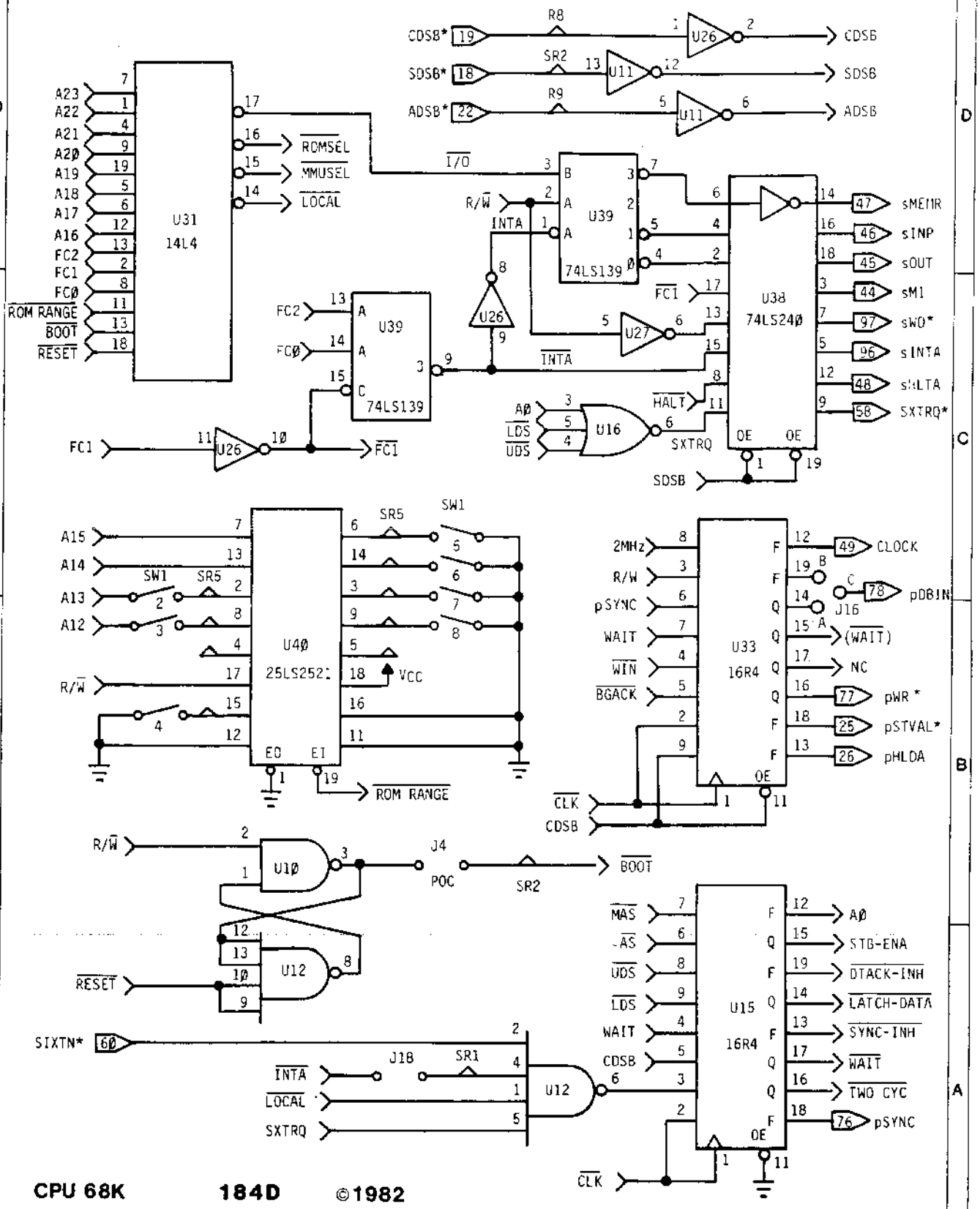

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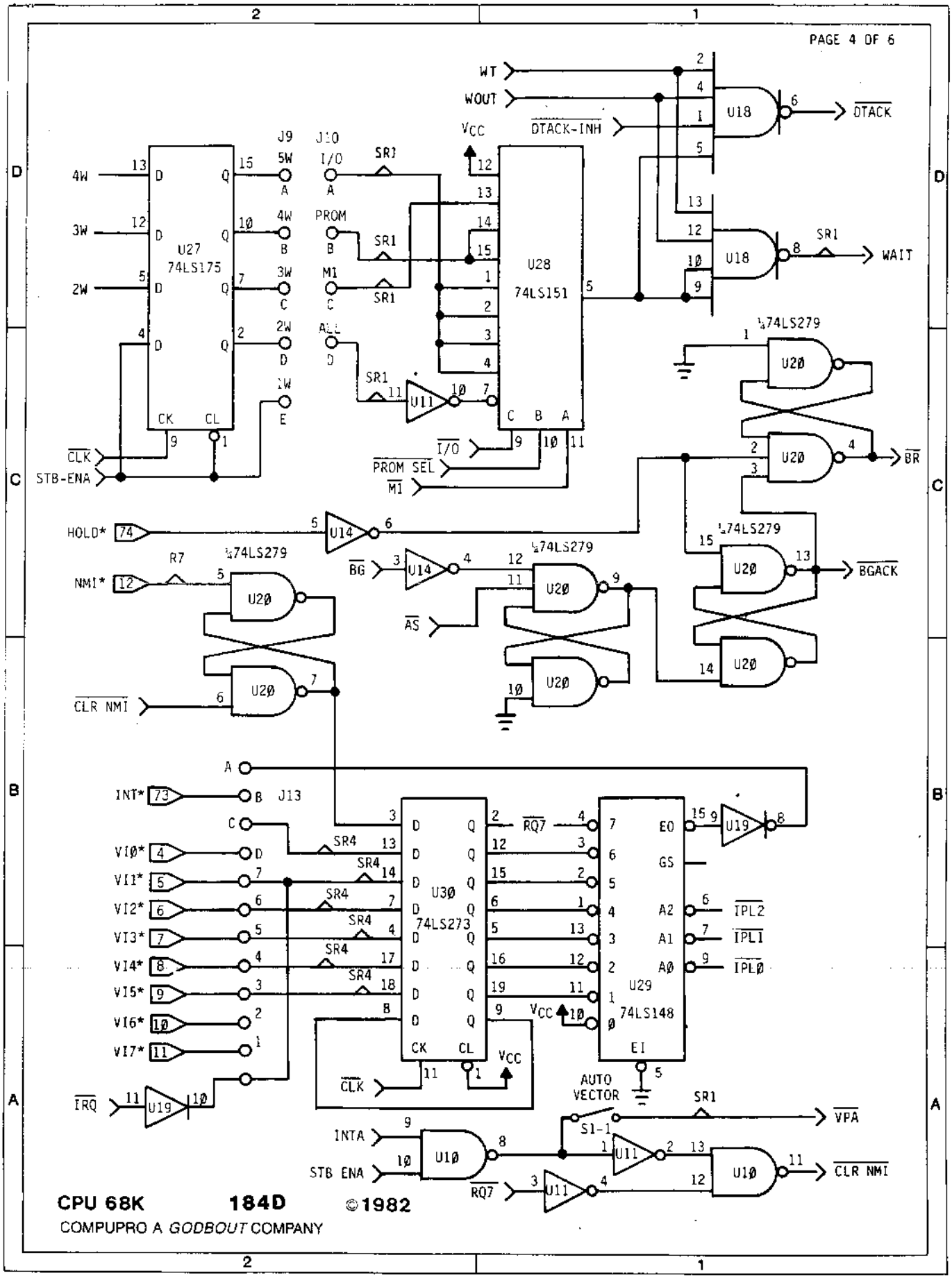
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WT
WOUT
DTACK-INH
U18
DTACK
WAIT
SR1
VCC
J9
J10
5W
4W
3W
2W
1W
I/O
PROM
M1
ALL
U27
74LS175
U28
74LS151
U11
CLK
STB-ENA
I/O
PROM SEL
M1
¼74LS279
U20
BR
HOLD*
U14
R7
NMI*
BG
AS
BGACK
CLR NMI
INT*
J13
VI0*
VI1*
VI2*
VI3*
VI4*
VI5*
VI6*
VI7*
SR4
U30
74LS273
RQ7
U29
74LS148
EO
GS
A2
A1
A0
IPL2
IPL1
IPL0
EI
IRQ
U19
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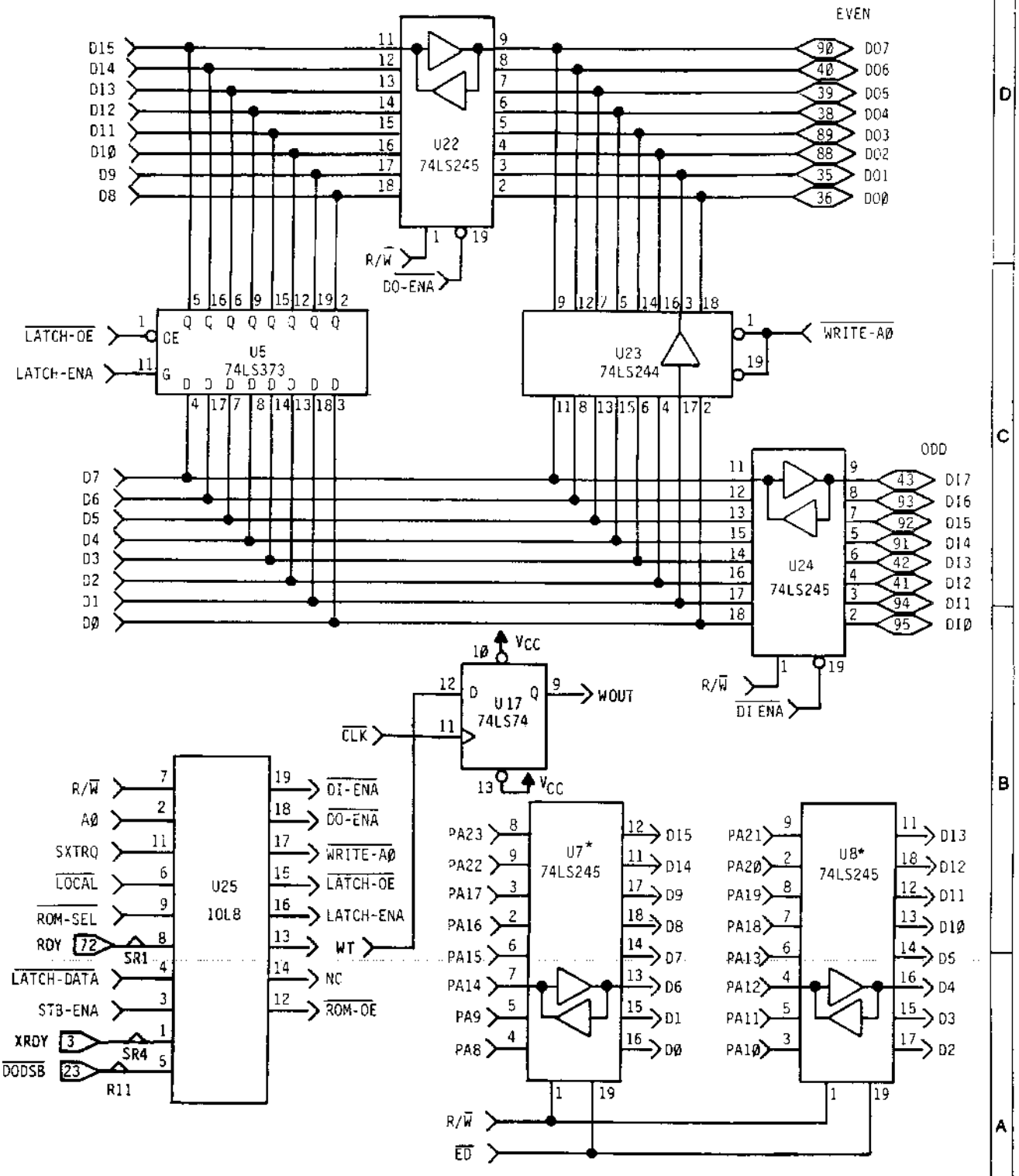

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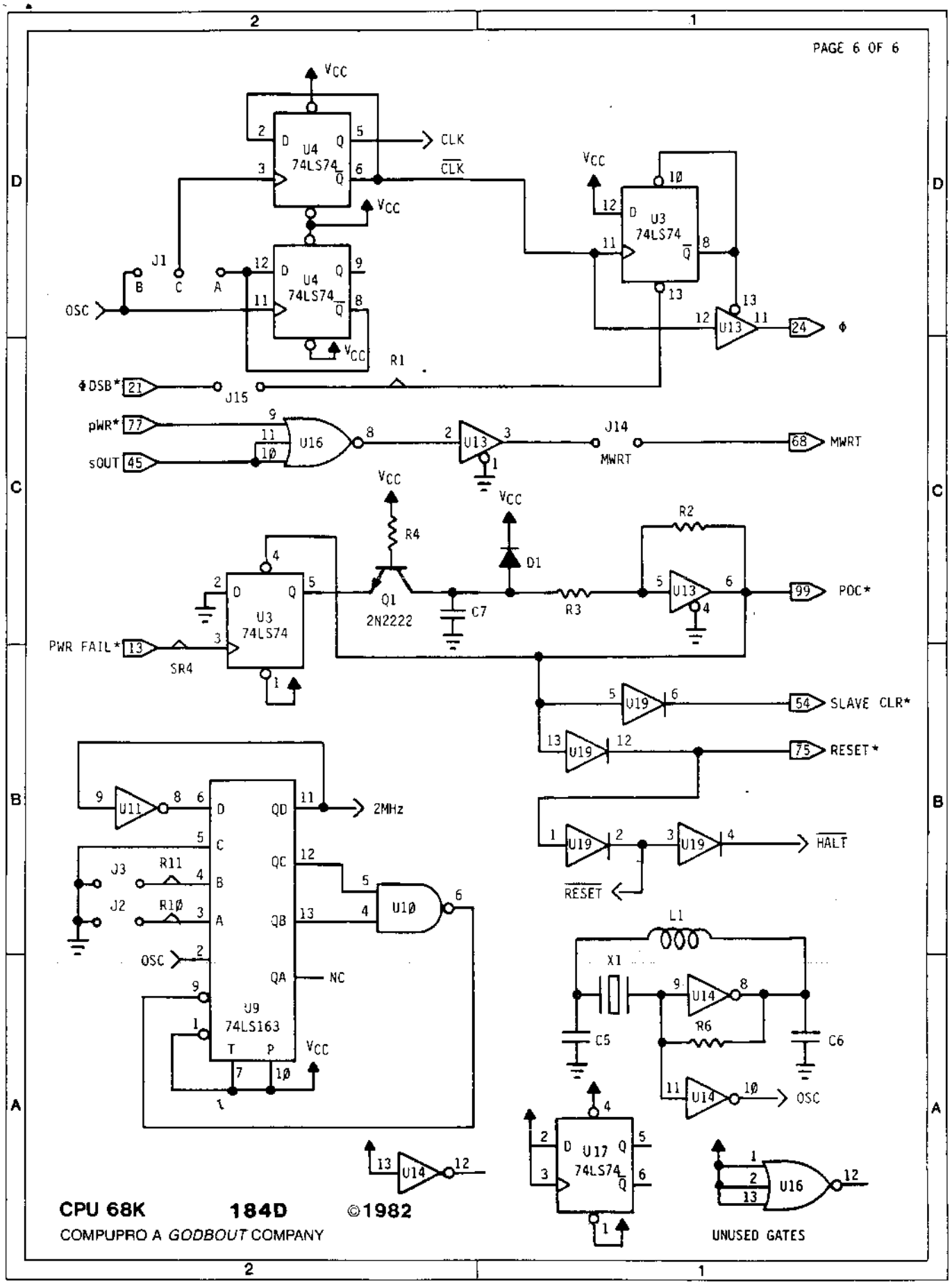
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VCC
U4
74LS74
CLK
CLK
U3
74LS74
J1
B
C
A
OSC
U13
Φ
R1
ΦDSB*
J15
pWR*
sOUT
U16
J14
MWRT
R4
D1
R2
Q1
2N2222
C7
R3
POC*
PWR FAIL*
SR4
U19
SLAVE CLR*
RESET*
HALT
RESET
U11
2MHz
J3
R11
J2
R10
U10
U9
74LS163
NC
L1
X1
U14
R6
C5
C6
U17
UNUSED GATES
CPU 68K
184D
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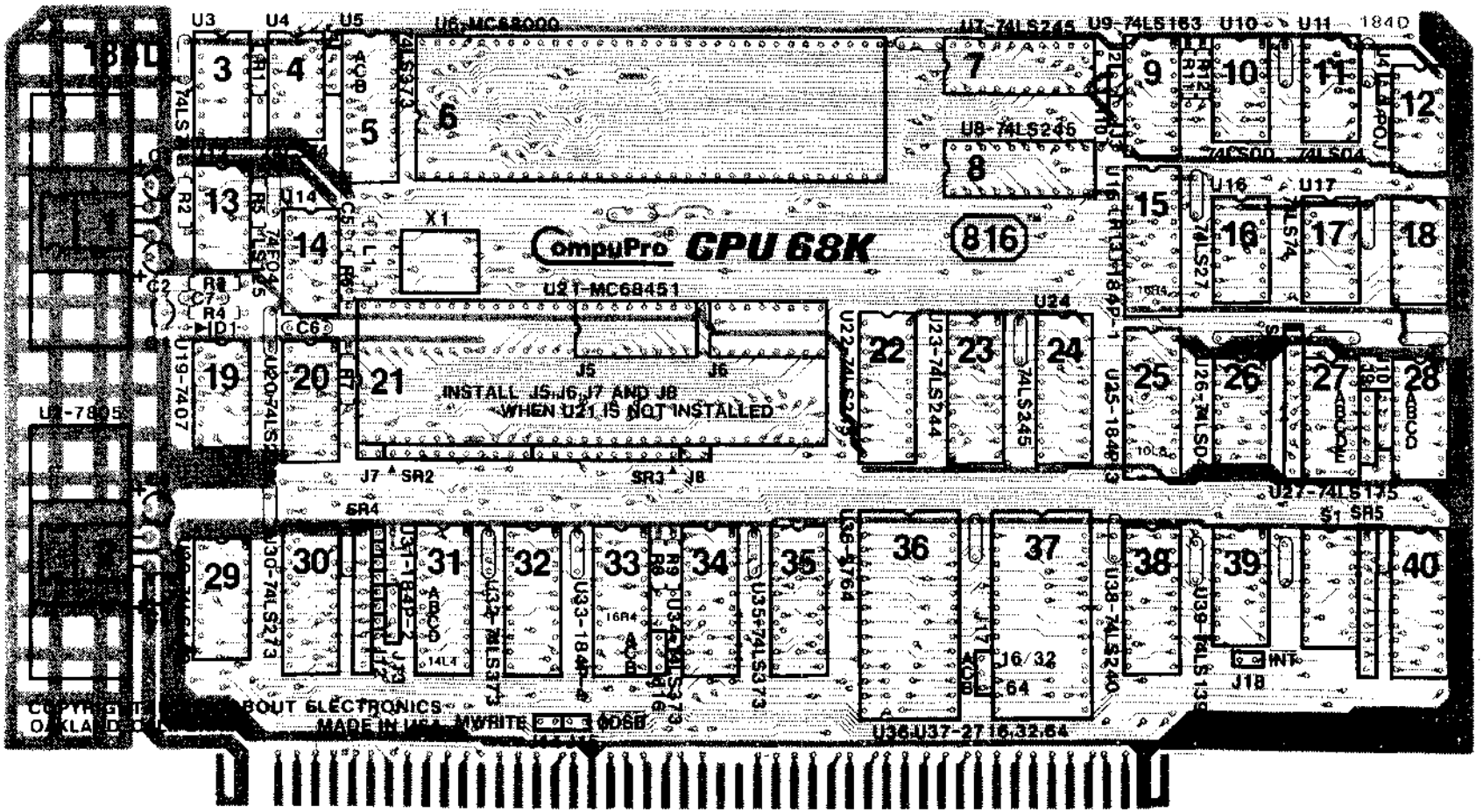
COMPUPRO A GODBOUT COMPANY

PARTS LIST

INTREGRATED	CIRCUITS	RESISTORS	VALUE
U1-U2	7805	R1	1.5K ohm
U3-U4	74LS74	R2	3.3K ohm
U5	74LS373	R3	1K ohm
U6	68000	R4-R5	5.1K ohm
U7-U8	74LS245	R6	1K ohm
U9	74LS161/163	R7-R9	1.5K ohm
U10	74LS00	R10	5.1K ohm
U11	74LS04	R11	1.5K ohm
U12	74LS20	R12-R13	5.1K ohm
U13	74LS125	SR1,SR2,SR4	1.5K ohm
U14	74F04	SR3,SR5	5.1K ohm
U15	G184P-1A (16R4)		
U16	74LS27		
U17	74LS74	CAPACITORS	
U18	74LS22	C1-C4	bypass (dip Tant.)
U19	7407	C5-C6	150 pF (dipped Mica)
U20	74LS279		120 pF (on CSC boards)
U21	68451 - (optional)	C7	47 uF (dip Tant.)
U22	74LS245	(23)	0.01 uF disc
U23	74LS244		
U24	74LS245		
U25	G184P-3A (10L8)	CRYSTAL	
U26	74LS04	X1	16 MHz
U27	74LS175		20 MHz (on CSC boards)
U28	74LS151		
U29	74LS148	INDUCTOR	
U30	74LS273	L1	1.0 uH
U31	G184P-2A (14L4)		
U32	74LS373		
U33	G184P-4A (16R4)	TRANSISTOR	
U34-U35	74LS373	Q1	PN2222
U36	2716,32,64		
U37	2716,32,64		
U38	74LS240	SIGNAL DIODE	
U39	74LS139	D1	
U40	25LS2521		



COMPONENT LAYOUT