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Product Manuals
User Manuals
1975-1980

CompuPro™
OAKLAND AIRPORT, CA 94614

division of GODBOUT ELECTRONICS

Product User Manuals

1975-1980

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OAKLAND AIRPORT, CA 94614

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GODBOUT ELECTRONICS
P.O. BOX 2355
OAKLAND AIRPORT, CA 94614

FOREWORD

This book represents the principal computer related products manufactured by Godbout Electronics from 1975 through 1980 - starting out with one of the very first boards for the S-100 Bus (then called the Altair Bus); our 4Kx8 static RAM board, all the way through our state-of-the-art CPU 8085/88 dual processor board, the first board to bring 16 bit power to the S-100 bus in a usable and affordable configuration.

This book is basically a compilation of all the user's manuals for all these products, but we have thrown in a few extra goodies. One of these is a discussion of the IEEE-696 S-100 Bus standard (written by none other than Bill Godbout himself!) that is not intended to replace the IEEE document, but is useful as a supplement to it. A copy of the IEEE document was printed in Issue #1 of S-100 Microsystems magazine. Back issues are available for $5.00 from: Microsystems, P.O. Box 789-M, Morristown, NJ, 07960. We also recommend a subscription to this journal as it often contains useful information and product reviews.) We have also included schematics that have had all errors corrected (to the best of our knowledge) as well as different schematics for the various revisions of a product. We have also tried to correct all known errors in the documentation itself.

You may also notice that our name has been slowly changing over the years. First it was just Godbout Electronics. Then the CompuKit logo appeared, and now that this is much more than a hobbyist oriented industry, CompuKit was replaced by CompuPro. Now the CompuPro name is getting bigger and the Godbout Electronics logo is getting smaller.

This book covers our products from 1975 through the end of 1980, thus not all of our current product line is represented in this volume. Volume 2 will contain products from 1981 on, and it will be out as soon as we get enough new products out for a whole volume (which should be pretty soon at the rate we're growing!).

Thanks for adding this volume to your technical library. We hope it will be an education to those who bought it just for reference, and a handy aid to those dealers and technicians who see our products through their shops all the time, or only occasionally. Enjoy!

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IEEE 696/S-100

Modular Microcomputer Bus

A bus provides a defined set of paths for data, address, and control signals for a system. Additionally, provision must be made for power and any other utility signals a system may require. The IEEE 696/S100 proposed bus standard provides the definitions noted above in addition to defining bus signal timing and handshake conventions for DMA devices. The standard also specifies the form factor and dimensions of the S100 board. (See Appendix A, page 94). The form factor of the board which was originally produced by MITS in 1975 has been retained. This provides mechanical compatibility among boards produced by the hundreds of different manufacturers of S100 board products. Electrical compatibility is not as easily assured. Hopefully the outline of the electrical specification of the bus will aid the reader in design of new S100 products and evaluating existing products.

In the opinion of this writer, the systems architect for the S100 bus was not MITS but rather the designer of the Intel 8080. The logic signals present on the original bus are those of the 8080. The 8080 possesses many of the attributes of earlier large machines. The fortuitous result of this fact, whether by chance or design, is a logical structure which provides almost all of the control and status signals required for any microprocessor regardless of the size of data and address words. The influence of the 8080 has been so profound upon the design of later microprocessors that the IEEE 696/S100 bus can accommodate virtually any 8 or 16 bit processor. There are schemes under consideration for getting 32 bit machines on the bus sometime in the mid 80's.

The physical bus consists of 100 lines. These will be considered by function without regard to actual line or pin numbers. (See Appendix B, page 110, for actual pin assignments) All signal names which include reference to signal direction are made relative to the CPU or master, i.e. permanent master/"host processor" or temporary master such as a DMA device, whichever happens to be controlling the bus at the time the signal is referenced.

1. DATA 16 Lines

8 DI=Data In 8 DO=Data Out

In an 8 bit application the DO lines are usually driven by the bus master and the DI lines are driven by bus slaves such as memory or I/O. These lines are then considered uniderectional since data is always only received or transmitted on those lines by any particular board, master or slave. This mode of data transfer is also used by 16 bit processors such as the 8088 which performs 8 bit data transfers only. This transfer mode is also used by properly designed 16 bit CPU's when exchanging data with 8 bit slaves. Microprocessors such as the 8086 have both 8 bit and 16 bit transfer modes. The S100 bus contains provisions for signalling the bus master whether a particular device is capable of performing a 16 bit "word" transfer. If, for example, an I/O port is set up to handle only 8 bit "byte" transfers, then the 16 bit master should have a default mode which will perform 16 bit transfers in byte serial fashion. This means a system owner does not have to replace all the 8 bit memory and I/O in a system just to use a new 16 bit CPU.

In 16 bit applications the DO and DI lines are driven by both bus masters and slaves. The 16 data lines operate in a bi-directional mode. In this mode the 8 DO lines contain the least significant byte and the 8 DI lines contain the most significant byte. Word parallel data transfers are performed in this fashion between 16 bit masters and slaves. 16 bit slaves such as memory and I/O should include a default mode capable of performing byte serial transfers with 8 bit masters. The sections on Status and Control signals contain details about 16 bit transfers. 32 bit transfers could be accomplished between 16 bit devices by performing 16 bit word serial transfers.

2. ADDRESS 24 Lines
Memory 16/24 I/O 8/16

The 8080 and the original MITS bus provided only 16 address lines. Initially this was considered more than adequate. With the cost of RAM as high as it was, and in the virtually absence of software, 4K bytes were quite adequate and 8K bytes were heavenly! This state of affairs did not last for long. Many operating systems now occupy more than 16K and some interpreters require a minimum of 64K for proper operation. Multi user applications require considerably more. Initially an I/O scheme called "bank select" was devised to permit 8 bit processors to access more than the 64K which they could directly address. This scheme was cumbersome at best. The advent of newer MPU's with more than 16 address lines, v.g. the 8088 has 20, there was no need for bank select but the bus did need more address lines. The S100 standards committee added 8 address lines to the 16 already on the bus. The term IEEE extended addressing now refers to devices capable of decoding the full 24 bits of an address. The capability of directly accessing up to 16 Megabytes of RAM should fill just about any needs for the foreseeable future. All new designs should include extended addressing.

I/O addressing with the 8080 was 8 lines providing for up to 256 I/O devices. The proposed IEEE 696 contains extended I/O addressing using 16 lines to provide for up to 64K I/O devices. I/O addresses are asserted on the low order S100 address lines.

3. STATUS 8 Lines

The status lines are used to specify the type of bus cycle to be performed. Status should be asserted as early in a bus cycle as is possible. The first seven are 8080 originals; the last two are newly defined in IEEE 696.

A. sMEMR, status MEMory Read, is asserted whenever the current bus cycle is a memory fetch.

B. sM1, status Op-code fetch, is asserted along with sMEMR to identify a memory read cycle where the current bus master is calling an instruction from memory.

C. sINP, status INPut, is asserted whenever the current bus master is reading data from an I/O port.

D. sOUT, status OUTput, is asserted whenever the current bus master is writing data to an I/O port.

E. sWO*, status Write Out, is asserted whenever the current bus master is writing data to either memory or I/O.

F. sINTA, status INTerrupt Acknowledge, is asserted by the current bus master to indicate that it is prepared to service an interrupt request previously issued to it by a bus slave.

G. sHLTA, status HaLT Acknowledge, is asserted by the current bus master to acknowledge that a halt instruction has been executed.

H. sXTRQ*, status siXteen bit data Transfer Request, is asserted by the current bus master to ascertain if the currently addressed bus slave can perform 16 bit (word) transfers. If the request is not acknowledged by the slave the master should perform byte serial data transfers. This signal permits both byte and word organized slaves to operate on the same bus.

I. sMW, status Memory Write-a ninth status signal for which there is no bus line-is defined as sMW=(-sOUT).sWO.

4. Control Output 5 Lines

The control output signals establish the timing and movement of data during all bus cycles. These five are original 8080 signals. However, in the author's opinion there is a sixth signal, MWRT, memory write, which should have been included in this section of IEEE 696. This signal is covered in the utilities section of this

paper in order to maintain correspondence with IEEE 696. Designers and users should include MWRT in any consideration of timing and control relating to the S100 bus.

A. pSYNC, SYNChronize, indicates the start of each bus cycle.

B. pSTVAL*, STatus VALid (analogous to phi 1 on the 8080) signifies, in conjunction with pSYNC, that status and address are stable on the bus and ready for use. Proper assertion of pSTVAL requires that there be only one negative transition on pSTVAL during pSYNC.

C. pDBIN, Data Bus IN, is the general read strobe which gates data from an addressed slave onto the bus. Address signals must be held stable before, during and after assertion of pDBIN. Data from the slave must be stable on the bus sufficiently prior to the end of pDBIN to meet the read data access time requirements of the master asserting pDBIN.

D. pWR*, WRite, is the general write strobe which gates data from the bus into an addressed slave. Data and address signals must be held stable before, during and after assertion of pWR*.

E. pHLDA, HoLD Acknowledge, is asserted by the permanent bus master to indicate to the temporary master with highest priority that the permanent master is relinquishing control of the bus. Note that only the permanent bus master can issue pHLDA.

Timing diagrams of typical bus masters, an 8 bit Z80 and a 16 bit 8088, are contained on pages 232 and 233 of this manual.

5. Control Input 6 Lines

The control input signals provide the means by which bus slaves may synchronize bus masters with the timing requirements unique to the slaves. They also provide the means for slaves to request interrupt or hold operations from the permanent bus master.

A. RDY, ReaDY, is the general ready line for bus slaves. When not ready is asserted the bus master is stalled or caused to issue wait states until the slave removes the not ready signal. In this fashion slaves with slower access times than the bus masters can synchronize data transfers with those masters. RDY is an open collector line and should be terminated by an appropriate pull-up on the bus permanent master.

B. XRDY, eXternal ReaDY, is functionally redundant with RDY. XRDY is specified as a totem pole driven line so it cannot be used by more than one device without conflict. XRDY should not be used in new designs. XRDY was formerly used on the front panels of firms which are now defunct. The line was not deleted at the time IEEE 696 was originated because there were still a significant number of these front panels in use. The XRDY line is a candidate for future reassignment.

C. INT*, INTerrupt, is an open collector general interrupt service request line. The INT* line is often used with a slave device which services the 8 vectored interrupt lines defined in section 7. Interrupt requests are asserted on INT* as a level and when accepted by the bus master it will acknowledge with sINTA. INT* may be masked by internal software operations on the bus master.

D. NMI*, Non Maskable Interrupt, is An open collector interrupt service request line which cannot be masked of by the bus master. NMI* is asserted as a negative transition on the line and need not be acknowledged by a sINTA cycle.

E. HOLD*, HOLD request, is an open collector line used by temporary bus masters to request control of the bus. HOLD* may be software maskable by the Host Processor. HOLD* is acknowledged by an sHLTA cycle. Hold requests always take priority over interrupt requests. (See 7)

F. SIXTN*, SIXTeeN acknowledge, is an open collector signal line used by bus slaves to respond to sXTRQ* that 16 bit data transfers are possible. An absent or delayed SIXTN* should cause a bus master

to default to byte serial data transfer mode.

6. DMA Control 8 lines

DMA control is probably the least understood and most maligned part of IEEE/S100 specsmanship around. Well sports fans I'm sure that some of you have got your "skinnin knives" out by now and the rest of you poor souls who have worked your way through my stilted prose are just waiting to get in your shots. First, let me assure you that successful DMA design and operation are no more difficult than playing poker with some of the local fauna out here around Silicon Gulch. Some of the card sharks in the computer business make the Vegas kids look like slow third graders! So, what's the secret? First, you gotta know the rules, COLD. Second, you gotta know the odds, er, I mean priorities. Third, you must have good timing; ever try to run a bluff only to be murdered because your timing was bad? Proper timing in DMA operation is critical.

A. DMA0*, DMA1*, DMA2*, DMA3*, Direct Memory Access, 0 through 3 are open collector lines which carry the encoded priorities of up to 16 temporary bus masters. The priorities asserted on these lines are used to simultaneously arbitrate requests for bus control.

B. ADSB*, Address DiSaBle; DODSB*, Data Out DiSaBle; SDSB*, Status DiSaBle and CDSB*, Control DiSaBle; are open collector DMA control lines asserted by temporary bus masters to disable the address, data, status and control signals of the permanent bus master/Host Processor. also other bus masters

DMA operations are controlled by the 8 DMA control lines working in conjunction with HOLD* and pHLDA. A temporary master begins a DMA cycle by asserting HOLD*. It may do so ONLY when HOLD* and pHLDA are not true on the bus. No temporary master may request control when the permanent master is not in control of the bus. We shall assume that this HOLD request is the only one present on the bus. The Host Processor grants the request by asserting pHLDA. Only the permanent bus master/Host Processor may assert pHLDA. NESTED DMA OPERATIONS ARE NOT PERMITTED ON THE S100 BUS. The temporary master will continue to assert HOLD* until it relinquishes control of the bus to the Host Processor. Upon receipt of the bus grant, pHLDA, the temporary master asserts ADSB*, SDSB* and DODSB* while enabling its control outputs as shown below.

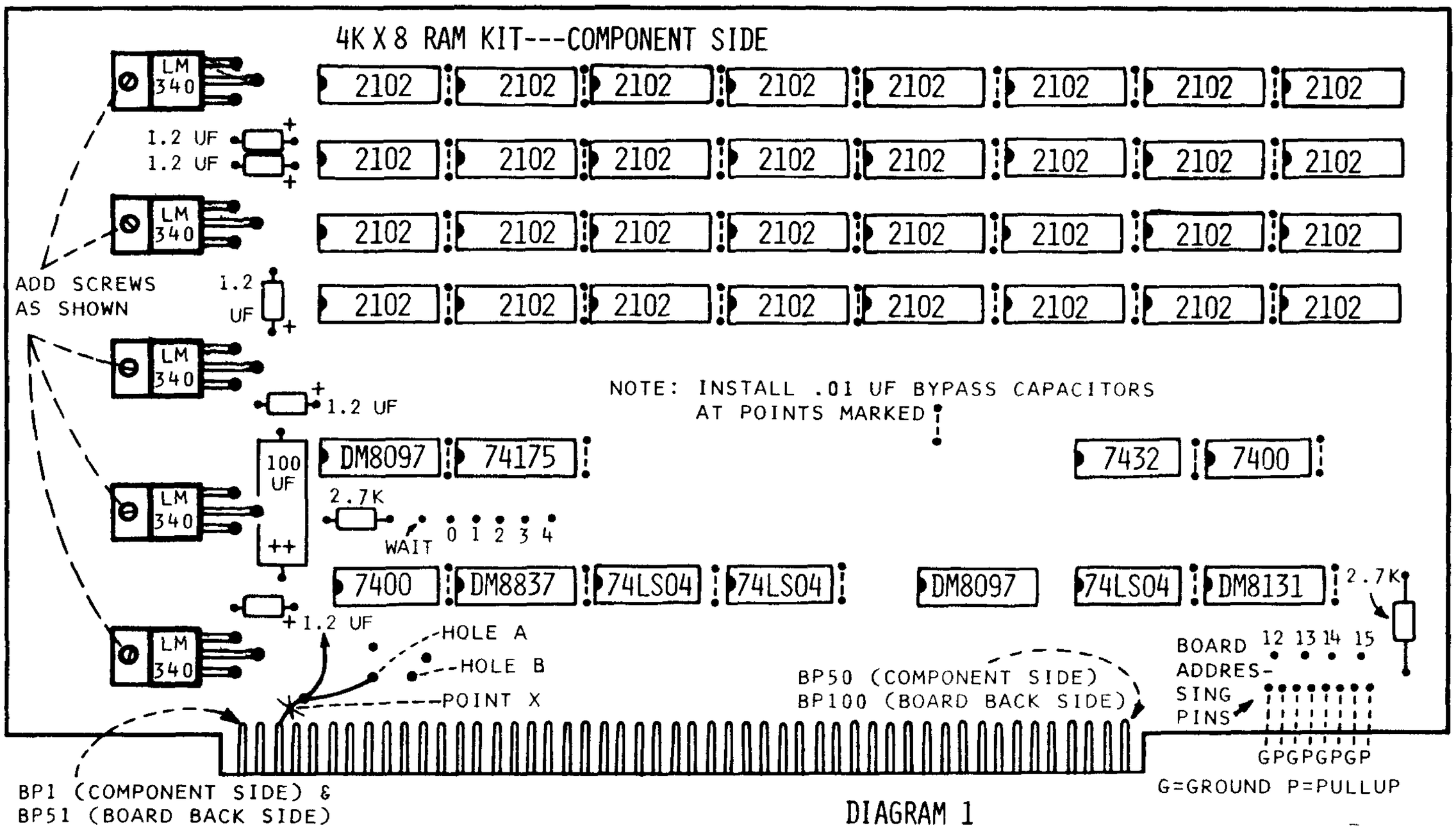
SIGNAL	LOGIC STATE
pSYNC	False
pSTVAL*	False
pDBIN	False
pWR*	False
pHLDA	True

The control signal outputs from both the Host Processor and the temporary master should match with both driving the bus.

The transfer between Host Processor and temporary master is completed by the temporary master asserting CDSB* and enabling its address, data and status outputs. Note the importance of overlapping drive on the control bus. pSYNC and pDBIN are active high signals. If the control signals were allowed to float for a few nanoseconds during transfer, one or more devices on the bus could see the slice (we are dealing with reasonably fast logic) and cause an unwanted reaction. Unwanted reaction is spelled CRASH or, worse yet, something so subtle that it does not appear until many lines of code have been executed. The control lines must not be allowed to float. Performing transfer of control as described above insures that the control lines will not float. The temporary master now has control of the bus. IEEE 696/S100 imposes no limit to the number of bus cycles a temporary master may perform before returning control to the Host Processor. This provides much flexibility for software system design. Transfer of system control from Host Processor to temporary master is called transfer state one, XS I. Transfer of system control from temporary master to Host Processor is called transfer state two, XS II. Performing the steps described for XS I in

CONTINUED ON PAGE 26

4K X 8 RAM KIT



NOTE: INSTALL .01 UF BYPASS CAPACITORS AT POINTS MARKED

DIAGRAM 1

CAVE graphx

ASSEMBLY INSTRUCTIONS

1) First solder in all sockets 2) Insert all 2102 ICs 3) Insert bypass capacitors between 2102s as indicated in diagram 1. Please note. in our experience, some of the .01 bypass caps are not quite thin enough to fit comfortably between the 2102s Should you come across a capacitor like this, put it aside and use it elsewhere on the board. 4) Install other ICs and other bypass caps as indicated in diagram 1. 5) Install LM340/5s on board, using silicone heat sink grease between the sink side of the LM340 and the board Fasten tight with a nut and bolt, but don't overtighten to prevent cracking the board 6) Mount and solder capacitors, observing polarity as indicated. 7) Mount and solder resistors. 8) Solder wirewrap pins (optional) into board addressing holes (see diagram 1).

WAIT STATE WIRING: This board is designed to work with 0 wait states at 25°C. To operate board in this manner, add a jumper from hole "wait" to hole "0" and remove the 74175 (saves about 45 ma of current drain) For longer wait states, re-insert the 74175 and add a jumper from hole "wait" to the other appropriate-numbered hole

BOARD ADDRESSING PIN WIRING: This determines which one of 16 possible blocks of addressable memory this board will occupy. The four pins (12, 13, 14, 15) represent a 4 bit binary number that selects the block, pin 12 is the least significant bit, pin 15 is the MSB For example, to select the first block use the binary number 0000, connecting pins 12, 13, 14, and 15 to "G" or ground pins To select the second block (bytes 4096 to 8091), ground pin 12 while connecting pins 13, 14, and 15 to "P" or pull-up. If you want to select the last block of 4096 bytes, pins 12, 13, 14 and 15 go to "P"

SPECIAL NOTE TO ALTAIR OWNERS: PCC (People's Computer Company) has suggested a modification to the Altair 8800 wherein its control panel READY signal is disconnected and reconnected to XRDY. If your Altair has been changed in this manner, then you need to do the following things

1) Looking at the board from the component side, cut the trace between BP3 and the first hole it meets at point "X", as illustrated in diagram 1

2) Connect a jumper from hole "A" to hole "B".

DIAGRAM 2 SHOWS HOW TO PLUG THE GODBOUT MEMORY BOARD INTO YOUR ALTAIR.

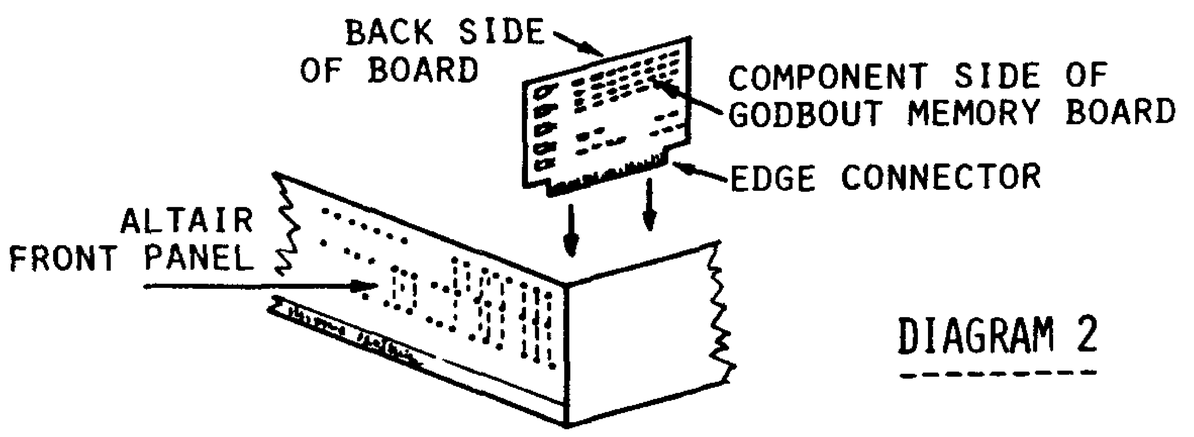
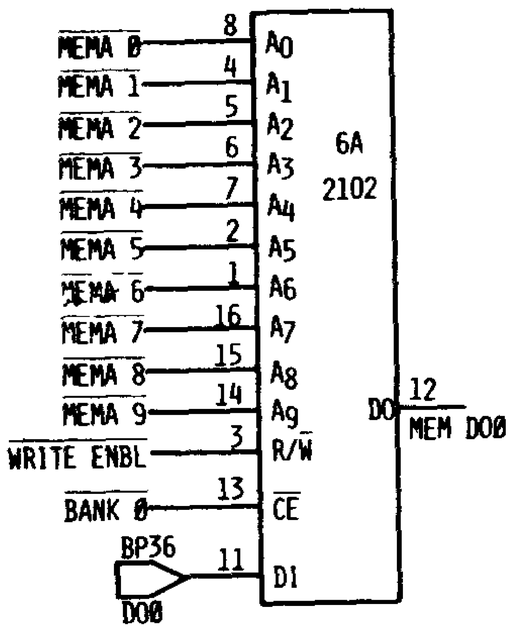
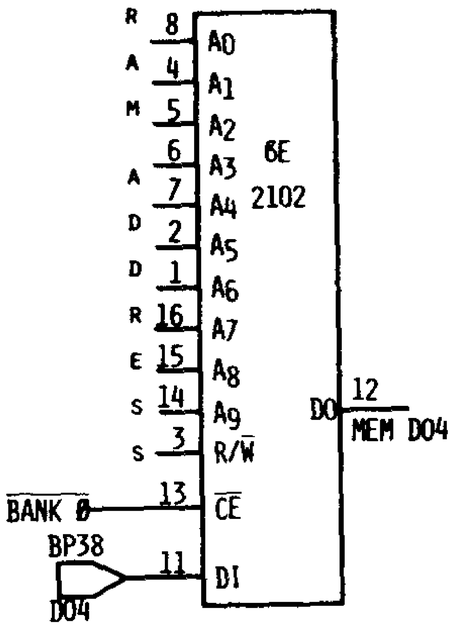


DIAGRAM 2

GODBOUT

BILL GODBOUT ELECTRONICS
BOX 2355, OAKLAND AIRPORT, CA 94614


MEMA 0
MEMA 1
MEMA 2
MEMA 3
MEMA 4
MEMA 5
MEMA 6
MEMA 7
MEMA 8
MEMA 9
WRITE ENBL
BANK 0
BP36
DO0
6A
2102
MEM DO0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6E
2102
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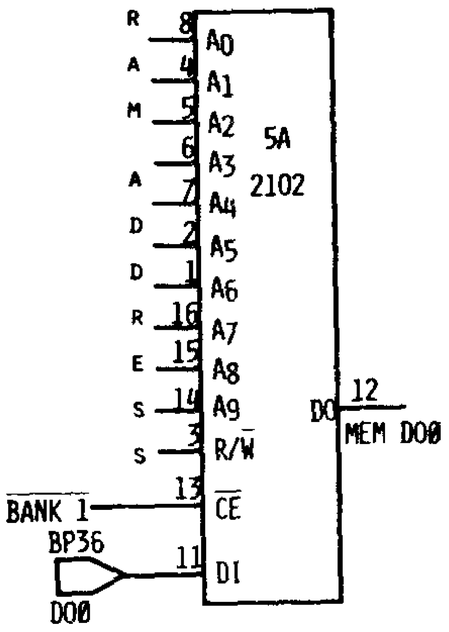
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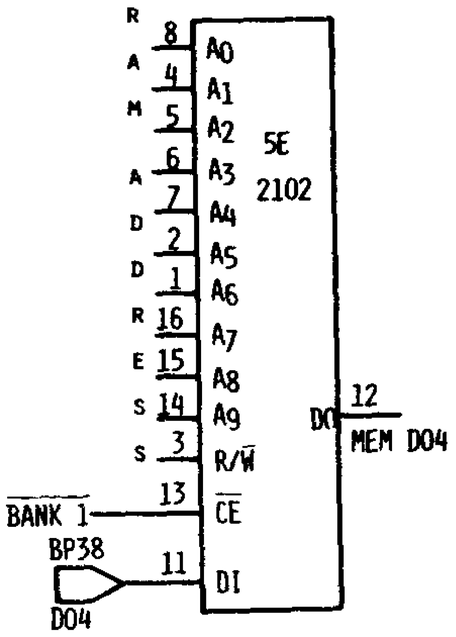
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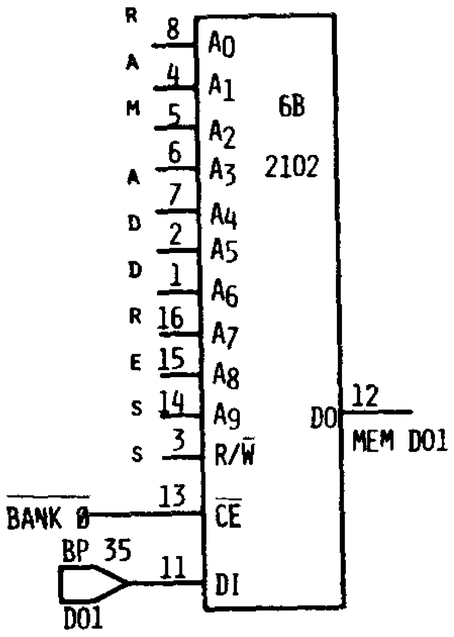
5E
2102
MEM DO4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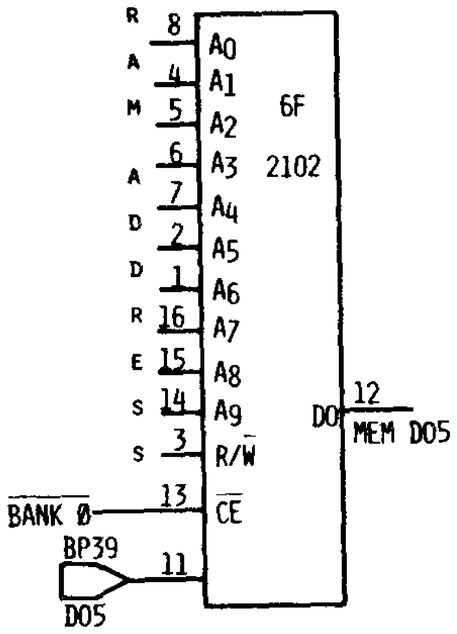
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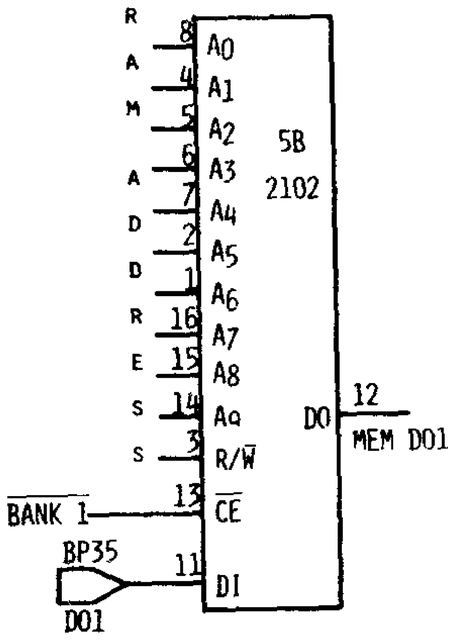
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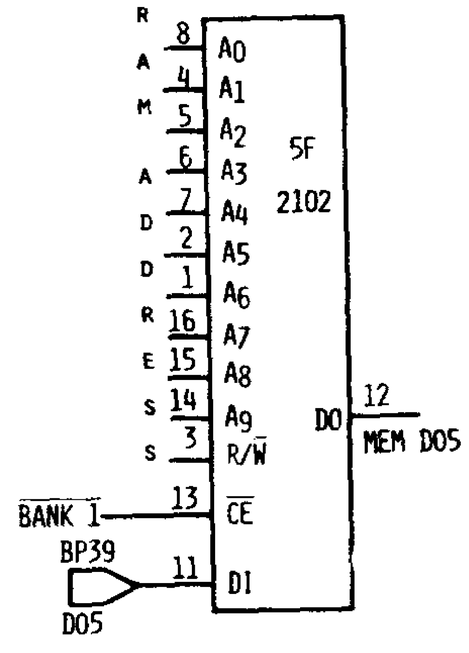
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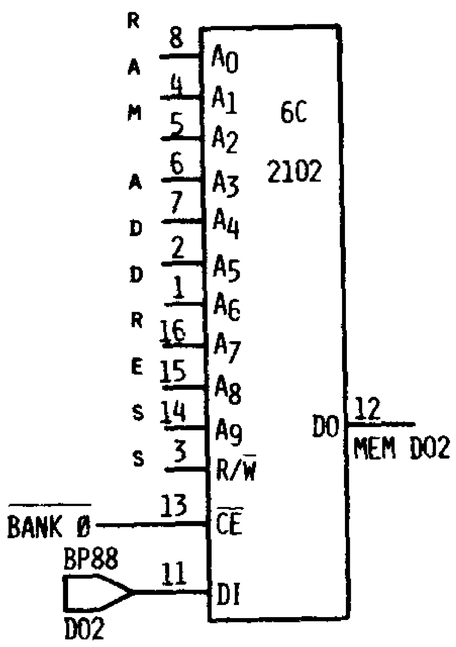
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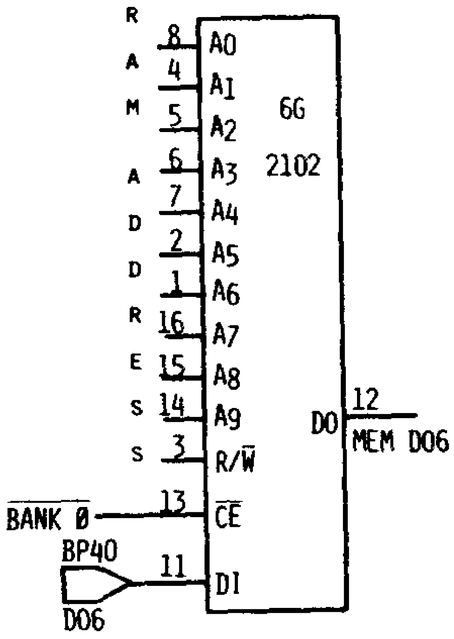
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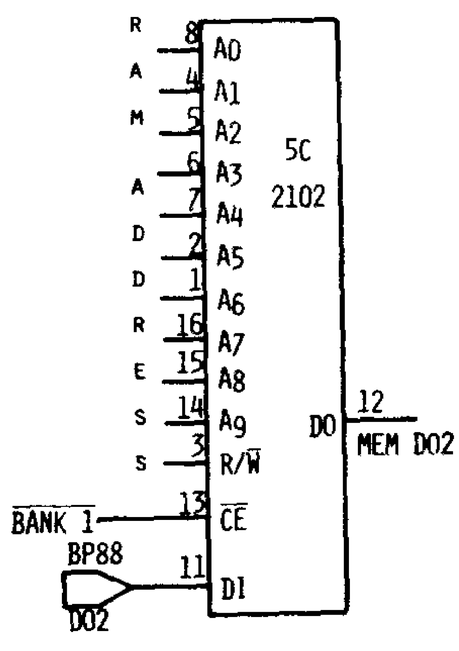
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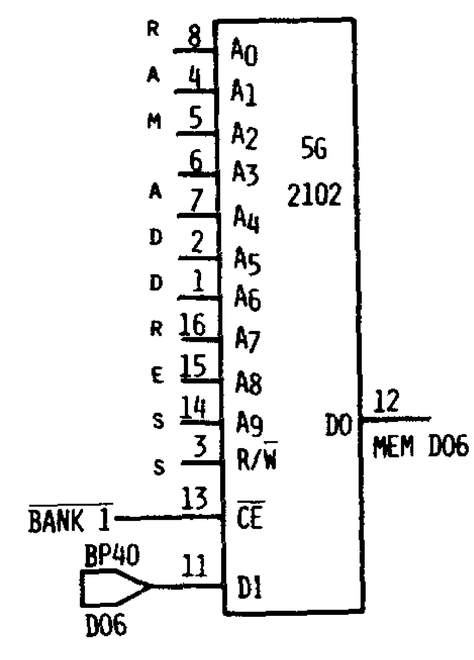
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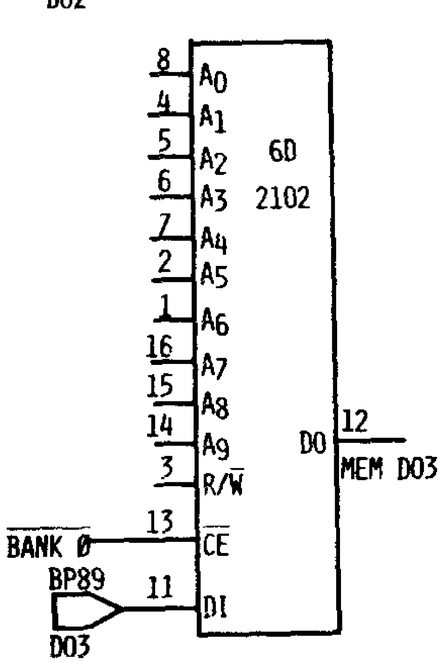
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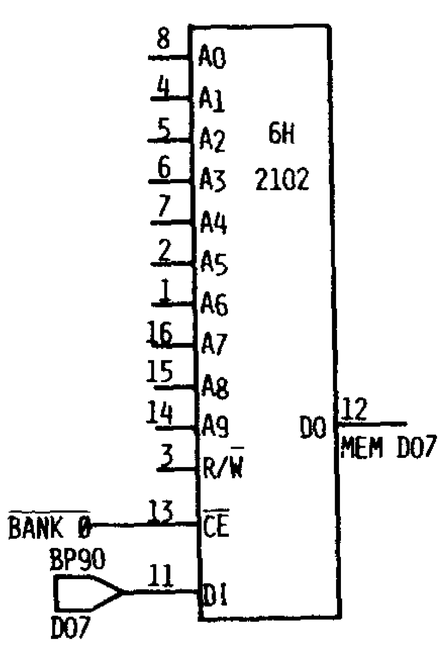
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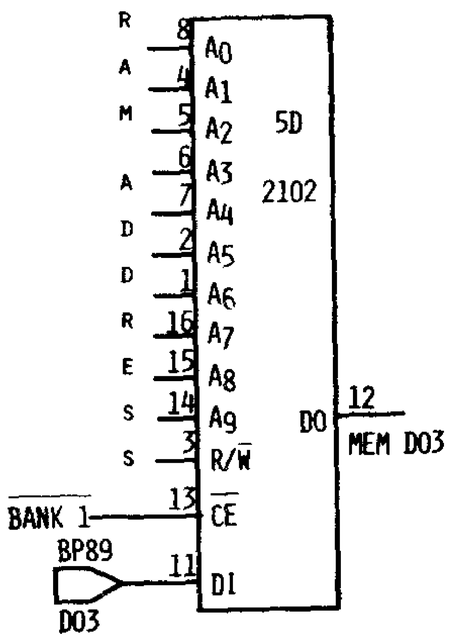
MEM DO7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5D
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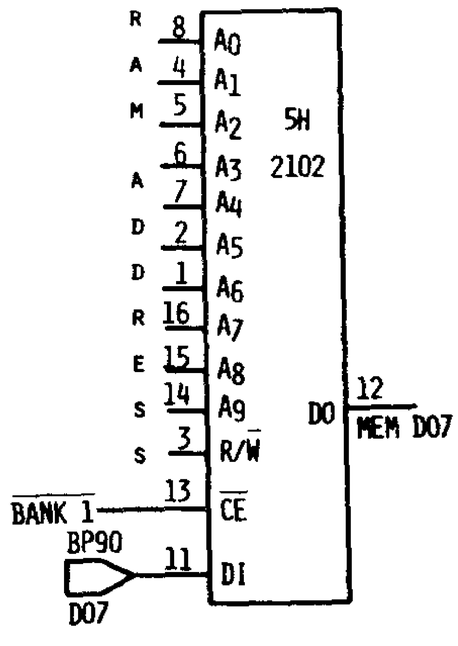
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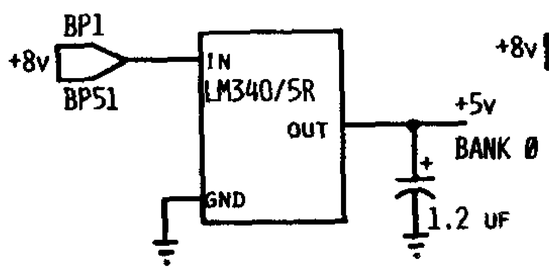
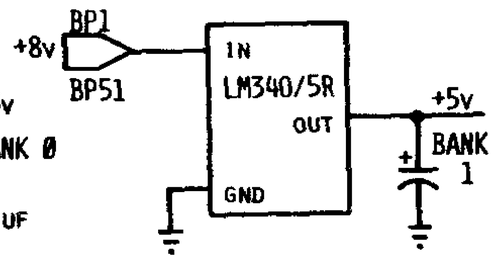
DO7
5H
2102
MEM DO7


+8v
BP1
BP51
IN
LM340/5R
OUT
GND
+5v
BANK 0
1.2 UF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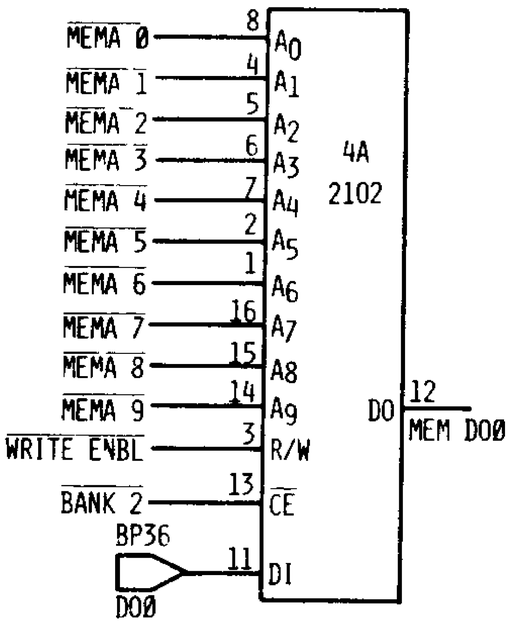
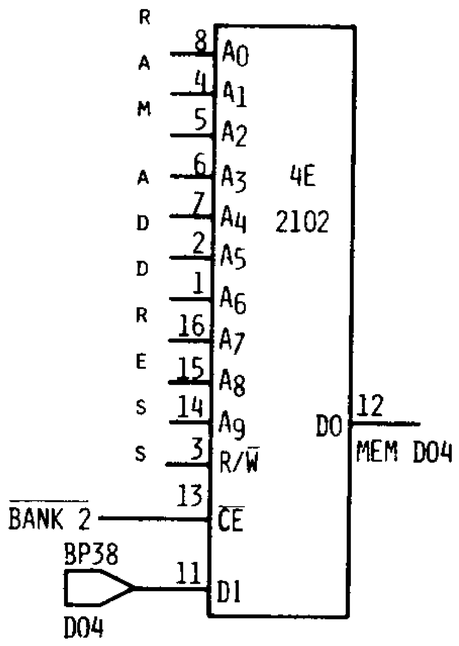
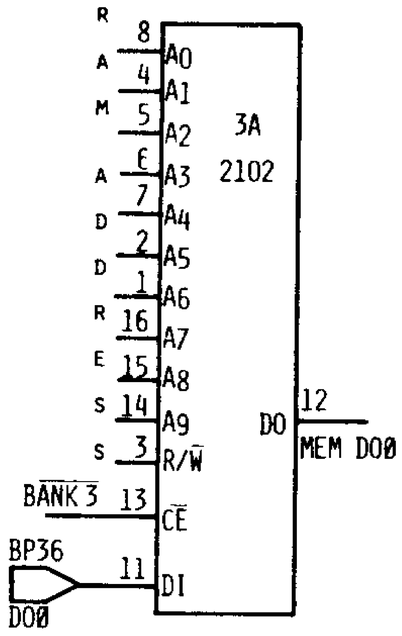
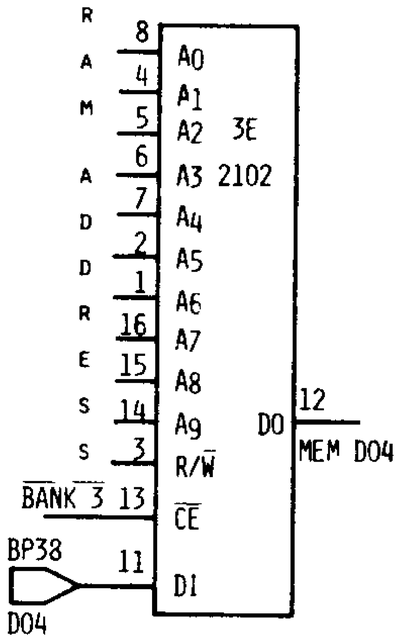
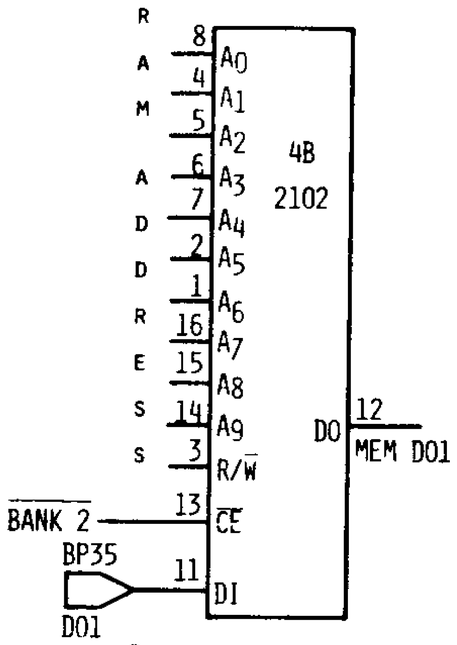
BP1
BP51
IN
LM340/5R
OUT
GND
+5v
BANK
1

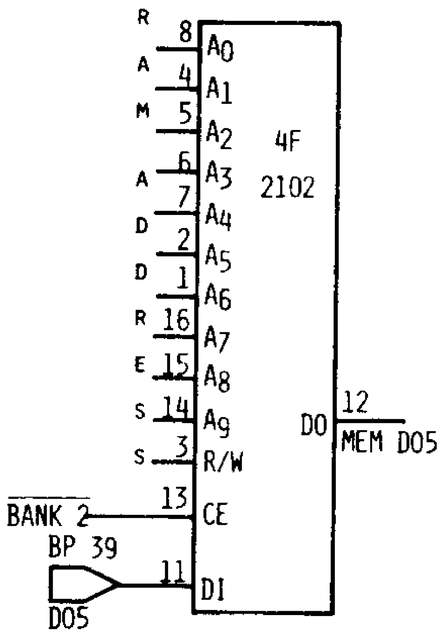


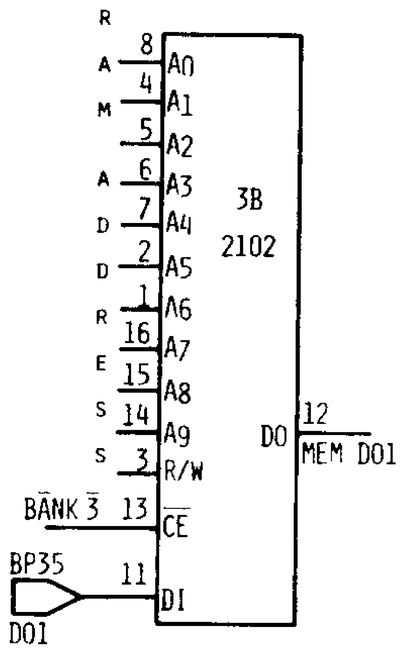


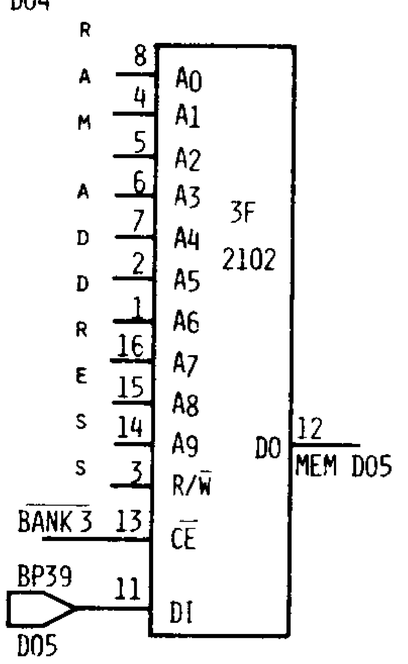


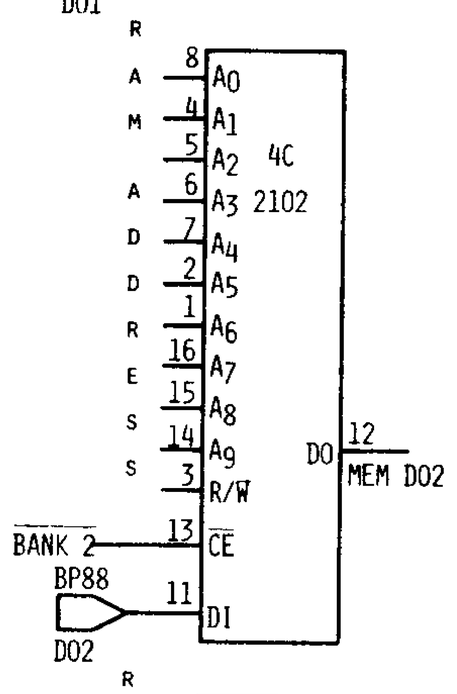


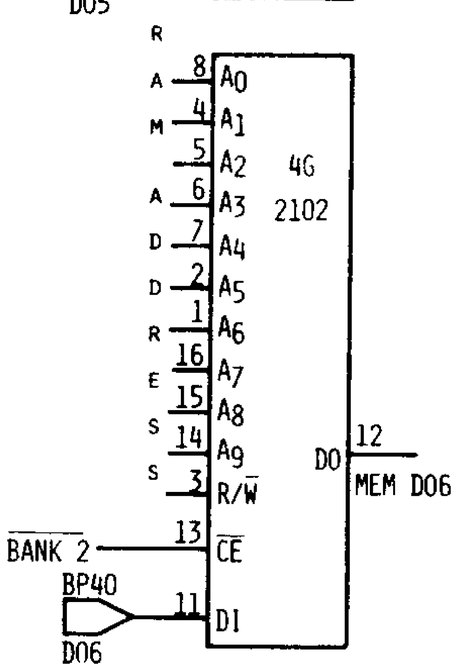


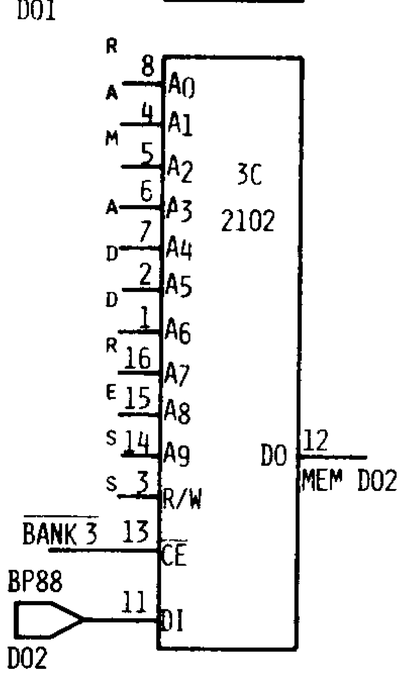


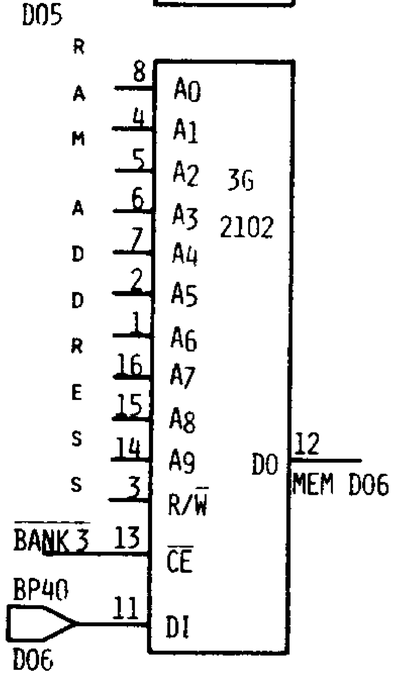


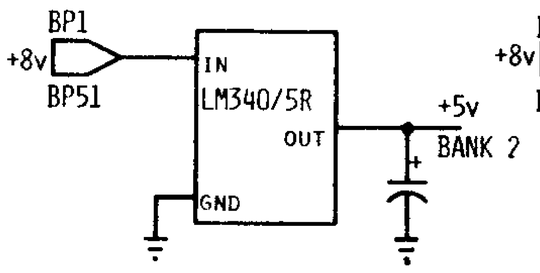


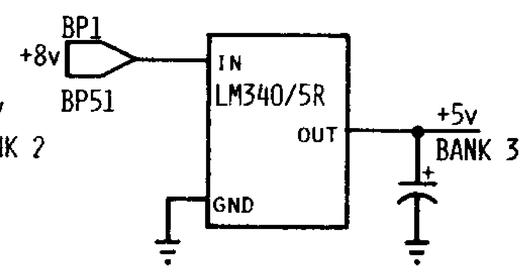












GODBOUT

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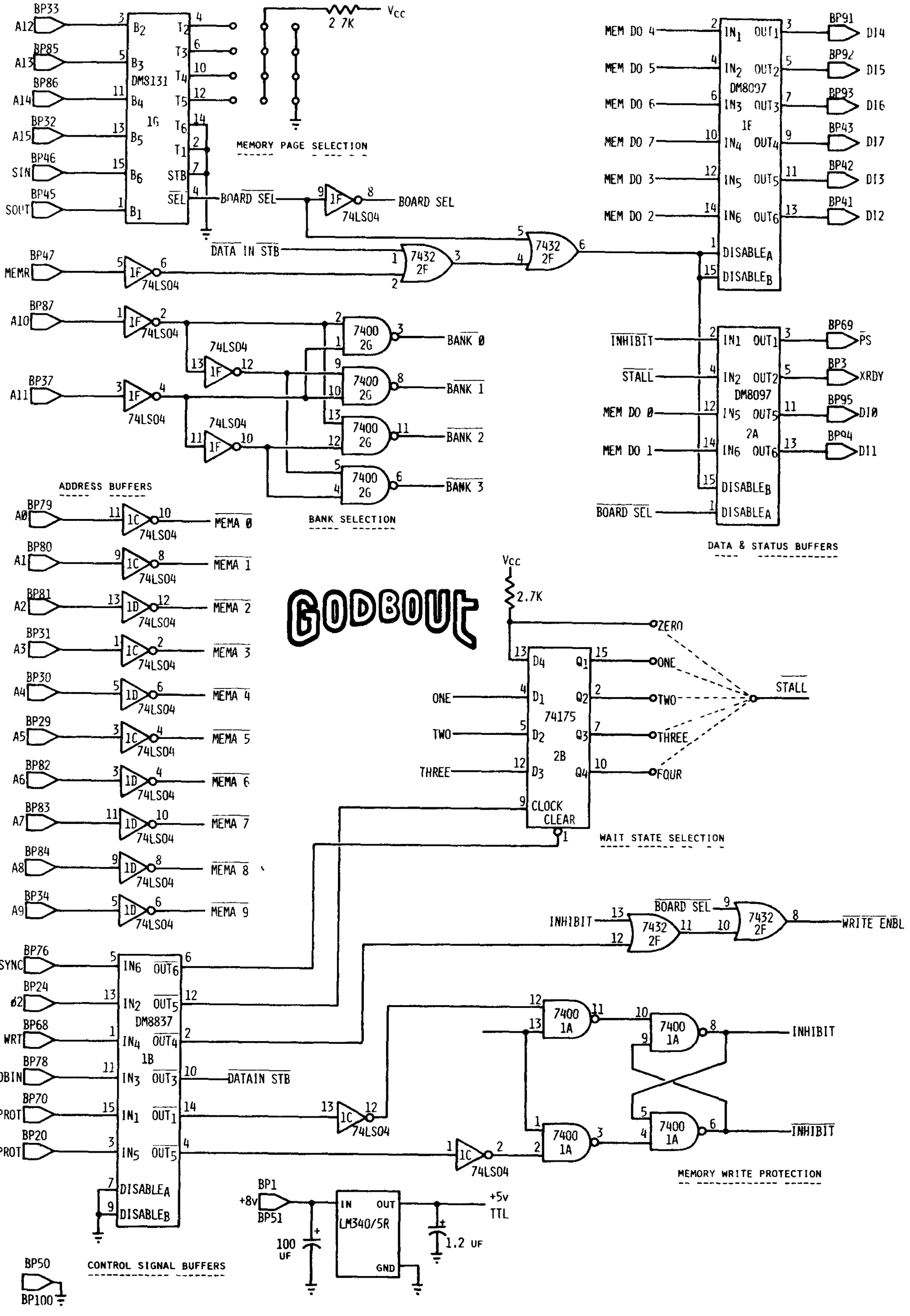

BP33
A12
BP85
A13
BP86
A14
BP32
A15
BP46
SIN
BP45
SOUT
DM8131
1G
B2
B3
B4
B5
B6
B1
T2
T3
T4
T5
T6
T1
STB
SEL
MEMORY PAGE SELECTION
Vcc
2.7K
BOARD SEL
74LS04
BOARD SEL
DATA IN STB
7432
2F
BP47
MEMR
BP87
A10
BP37
A11
7400
2G
BANK 0
BANK 1
BANK 2
BANK 3
BANK SELECTION
ADDRESS BUFFERS
BP79
A0
BP80
A1
BP81
A2
BP31
A3
BP30
A4
BP29
A5
BP82
A6
BP83
A7
BP84
A8
BP34
A9
MEMA 0
MEMA 1
MEMA 2
MEMA 3
MEMA 4
MEMA 5
MEMA 6
MEMA 7
MEMA 8
MEMA 9
BP76
PSYNC
BP24
ø2
BP68
MEM WRT
BP78
PDBIN
BP70
PROT
BP20
UNPROT
DM8837
1B
DISABLEA
DISABLEB
DATAIN STB
CONTROL SIGNAL BUFFERS
BP50
BP100
BP1
+8v
BP51
LM340/5R
IN
OUT
GND
100 UF
1.2 UF
+5v
TTL
MEM DO 4
MEM DO 5
MEM DO 6
MEM DO 7
MEM DO 3
MEM DO 2
MEM DO 0
MEM DO 1
DM8097
1F
2A
DISABLEA
DISABLEB
BP91
D14
BP92
D15
BP93
D16
BP43
D17
BP42
D13
BP41
D12
BP95
DI0
BP94
DI1
INHIBIT
STALL
BP69
PS
BP3
XRDY
BOARD SEL
DATA & STATUS BUFFERS
Vcc
2.7K
ZERO
ONE
TWO
THREE
FOUR
74175
2B
D4
D1
D2
D3
Q1
Q2
Q3
Q4
CLOCK
CLEAR
STALL
WAIT STATE SELECTION
INHIBIT
BOARD SEL
7432
2F
WRITE ENBL
7400
1A
INHIBIT
INHIBIT
MEMORY WRITE PROTECTION

GODBOUT

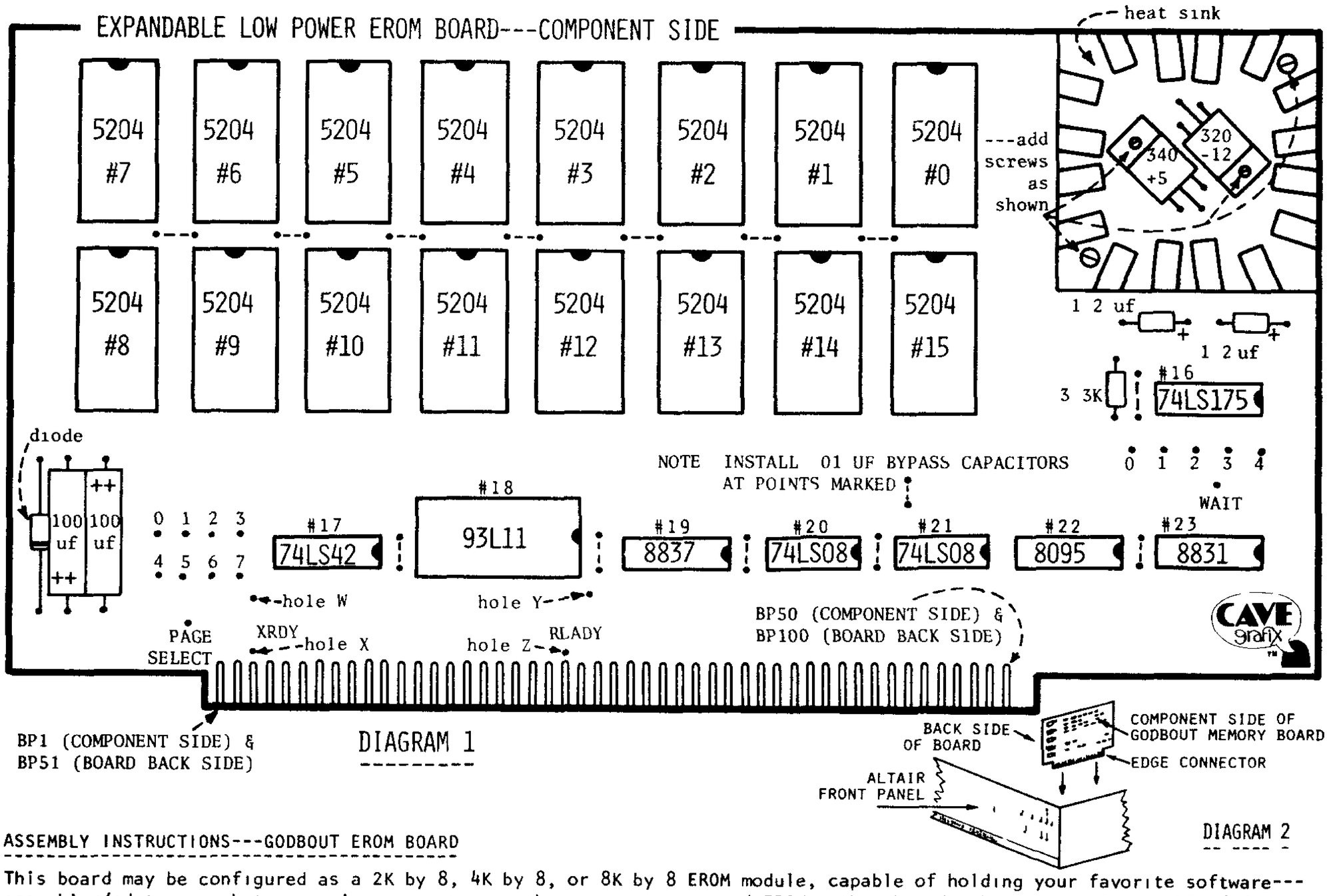


DIAGRAM 1

DIAGRAM 2

ASSEMBLY INSTRUCTIONS---GODBOUT EROM BOARD

This board may be configured as a 2K by 8, 4K by 8, or 8K by 8 EROM module, capable of holding your favorite software---assembler/editor or whatever In conjunction with our pre-programmed EROMs, this board makes an ideal assembler/editor for the 8080 microprocessor in the 4K by 8 configuration

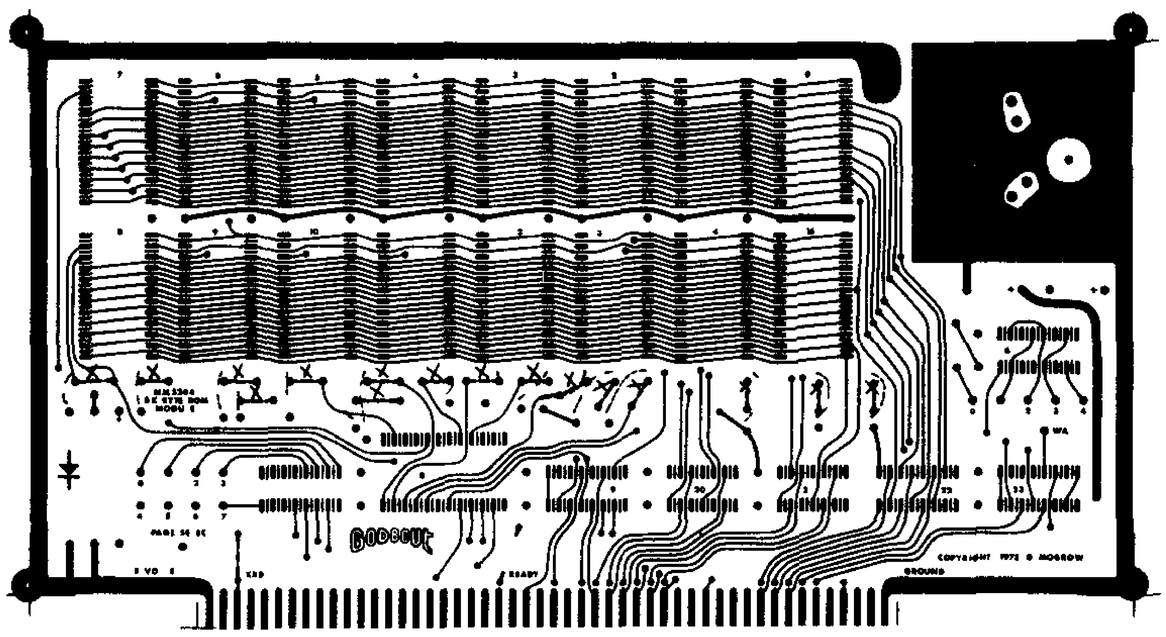
***ASSEMBLY 1) First solder in all sockets 2) Install heat sink into place on circuit board, and attach with two screws Do not overtighten screws to prevent cracking the circuit board 3) Install regulators on top of the heat sink, using silicone grease Note that a mica insulator installs under the LM320T/-12, also note that the LM340T/5 may be house numbered as SL00100 Again, attach with two screws, do not overtighten screws 4) Mount and solder the diode, 3 3K resistor, and 1 2 uf capacitors 5) Mount and solder the 01 uf bypass capacitors 6) Observing polarity, mount & solder the 100 uf electrolytics 7) Solder wirewrap pins (optional) into the holes for PAGE SELECT and WAIT 8) Look over your work, noting the polarity of the electrolytic capacitors and the diode Check for solder bridges or shorts 9) Plug in the non-EROM ICs (all ICs except 5204s)

***PLUGGING IN EROMS The EROMs should be handled as little as possible and should be stored in conductive foam. Plugging in a 24 pin IC, however, requires a bit of careful handling to avoid bending or otherwise damaging the pins We recommend lining up one side of the EROM with the socket holes (while holding the EROM over the socket), then running your thumbnail along the other side until the EROM pins line up with the socket holes. If necessary, do this for both sides of the EROM When the EROM pins are lined up with the socket holes, push the EROM in---all pins at the same time. The 2K version comes with 4 EROMs, which may go into any 4 sockets on the board, whether you want them in the upper block of memory, the lower block, or scattered is up to you Plugging in this board commits 8K of address The 4K version comes with 8 EROMs, which similarly may be placed in any 8 EROM sockets The 8K version comes with 16 EROMs, which fill up all the sockets The 8080 assembler/editor board comes with 8 EROMs, 7 of which are dedicated to the software These EROMs have numbers on the top (8 through 14), and must go into the matching numbered sockets on the EROM board The 8th EROM is shipped unprogrammed, in case you want to add custom EROM information to the software.

***PAGE SELECT This board may occupy any one of 8 pages of memory, add a jumper from PAGE SELECT to the appropriate number page For the 8080 assembler/editor software board, the jumper must connect to page 7

***WAIT STATE SELECTION Since editor/assemblers are intrinsically I/O bound, this board was designed to sacrifice speed somewhat to gain significant power savings At 25°C, this board should work with 2 wait states, it is guaranteed to work with 3 wait states over the normal temperature range To select the desired wait state, add a jumper from WAIT to the appropriate number Should you desire a faster board, it is possible to achieve 1 wait state operation by following directions (given elsewhere on this sheet) on modifying your board The penalty is an increase in power consumption

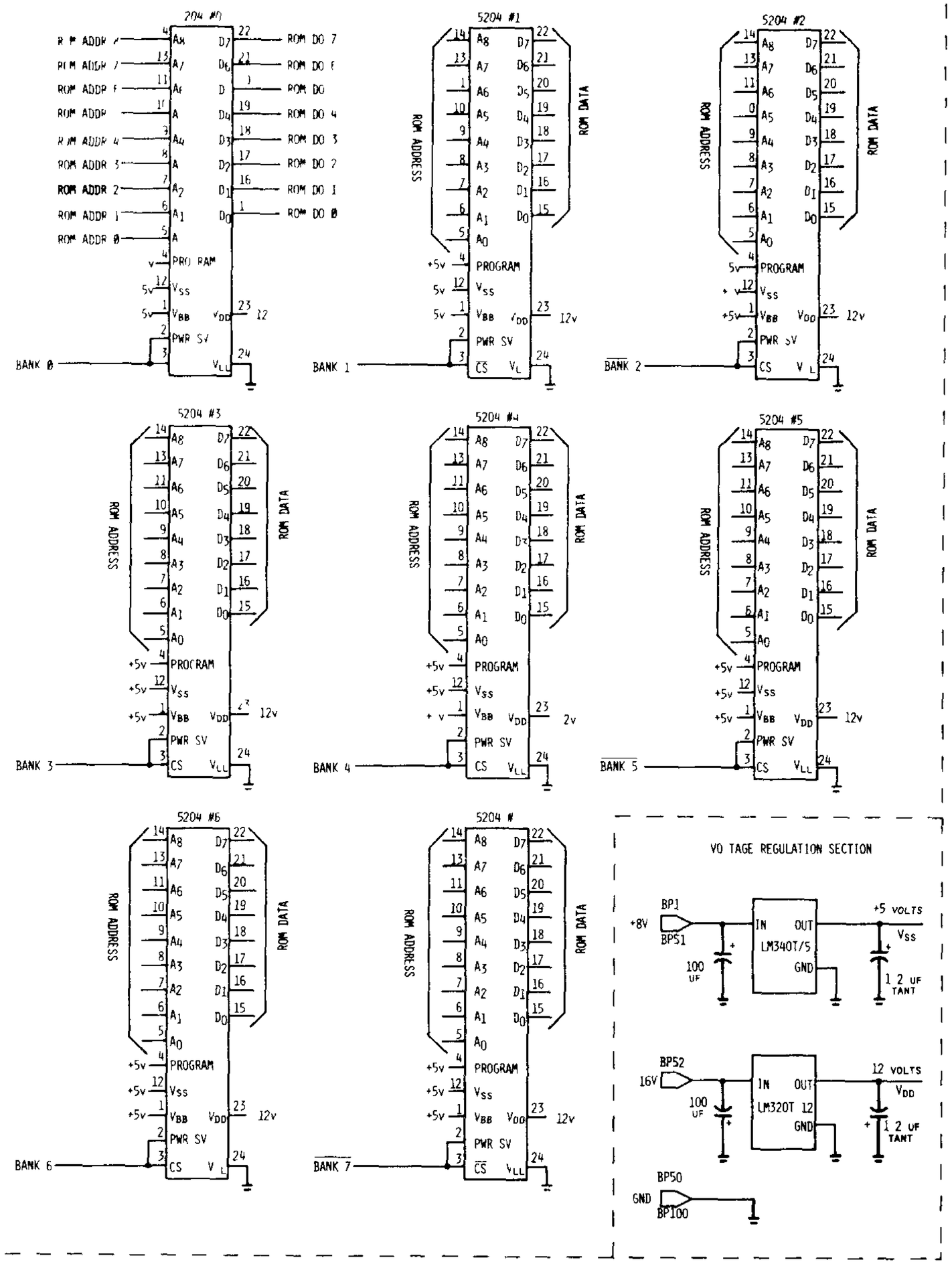
***SPECIAL NOTE TO ALTAIR OWNERS PCC (People's Computer Company) has suggested a modification to the Altair 8800 wherein its control panel READY signal is disconnected and reconnected to XRDY If your Altair has been changed in this manner, then you need to do the following referring to diagram 1, cut the trace between hole W and hole X, then, add a jumper between hole Y and hole Z Diagram 2 shows how to plug the Godbout EROM board into your Altair

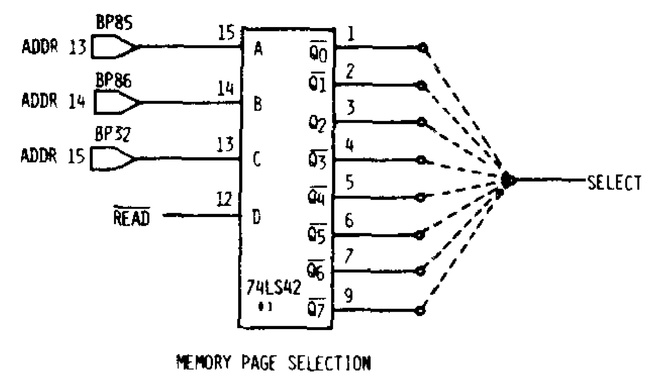


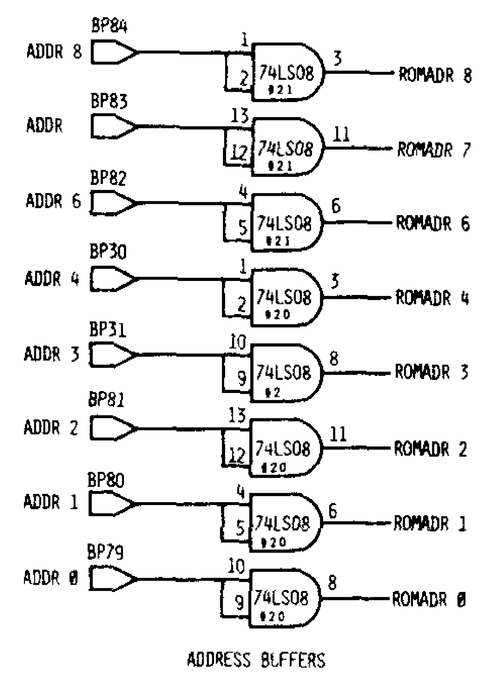
The diagram on the left shows the component side of the EROM board By cutting traces at the points marked (X), and adding the jumpers shown with dotted lines, it is possible to achieve one wait state at 25°C, and a guaranteed 2 wait states Bear in mind, though, that running at the faster speed adds approximately 22 ma per 5204 on the board for a savings of approximately 800 ns in terms of time

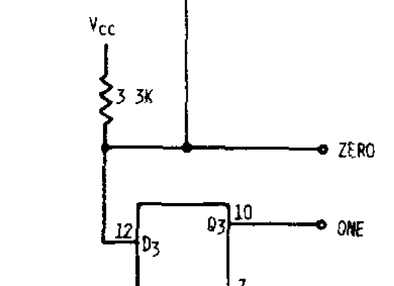
When cutting traces, use a knife to cut the trace at the two thin points-then use your knife to lift up the trace between the two thin points

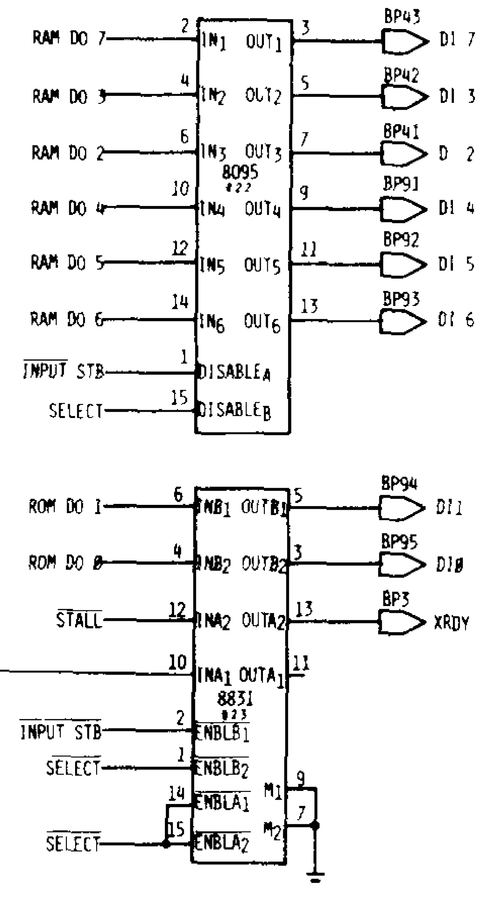
EROM BANK #0 THRO H #7 EROM BANK #8 THROUGH #15 ARE IDENTICAL AND ARE NOT SHOWN)

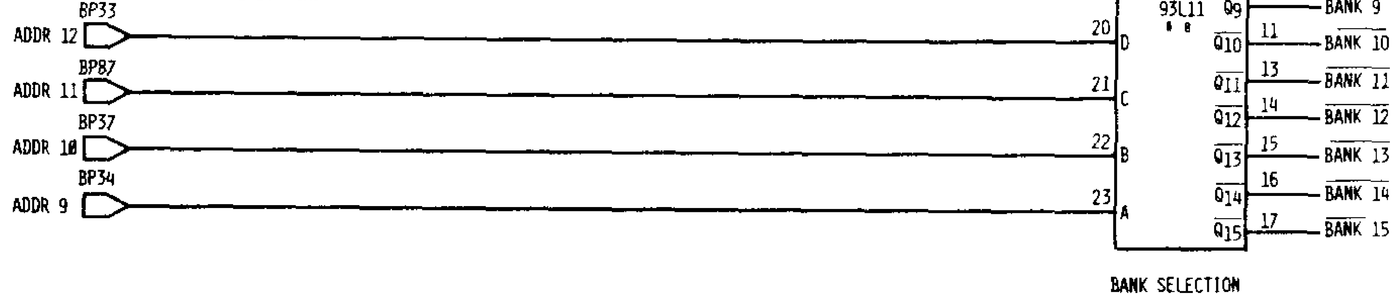




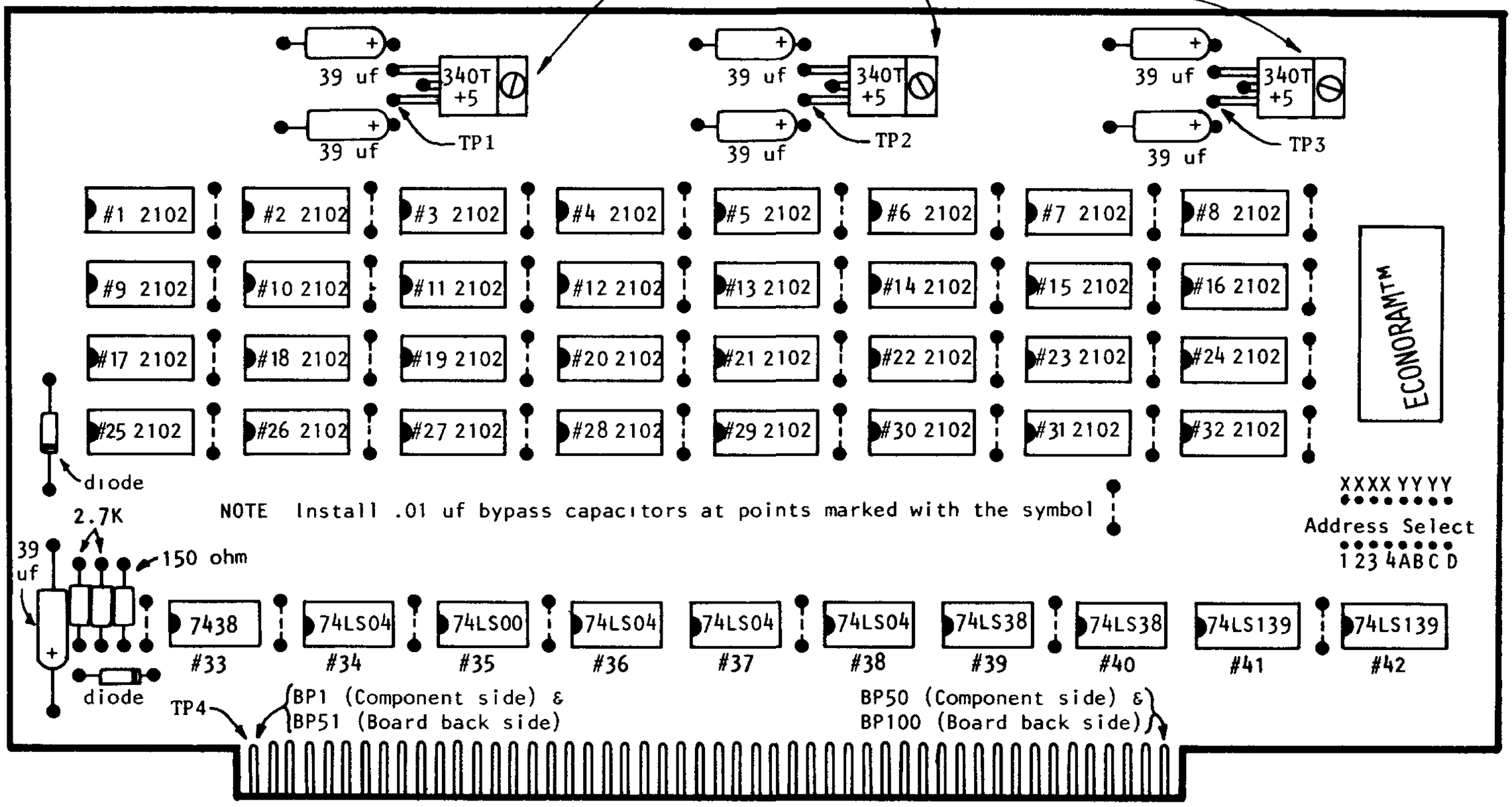








"ECONORAM" 4K X 8 KIT, COMPONENT SIDE



4Kx8 RAM KIT ECONORAM

ASSEMBLY INSTRUCTIONS

**PRELIMINARIES First, check off the parts in your kit against the parts shown on the component layout to familiarize yourself with the various components Note that the rounded ends of the 39 uf tantalum capacitors are the (+) ends
**SOLDERING. Use a fine tip soldering iron, rated at about 25 watts Use only rosin core solder, using any other type of solder invalidates the warrantee Solder every pin of every socket
**ORDER OF ASSEMBLY

1 Mount the sockets and solder them To prevent the sockets from falling out as you turn the board over to solder, put a piece of cardboard over the top of the sockets, and turn the board over while holding the cardboard against the sockets to keep them in place
2 Solder the optional DIP switch into the address select part of the board (the DIP switch mounts as if it were an IC)
3 Check TP1 by taking a VOM and setting it to its highest resistance scale, then connect one probe to ground and one probe to TP1. The reading should read infinite ohms or very close to it If not, check for solder bridges or a possible (but not very probable) board short
4. Follow this same test procedure for TP2, TP3, and TP4
5 Put in all capacitors, noting the polarity of the tantalum types
6 Check TP1 through TP4 again, but this time with the VOM set on its lowest ohms range There should be a "kick" on the meter while the capacitors charge, and then the readings should drift up to a much higher setting.
7. Install the 3 resistors and the two diodes (observe polarity)
8 Mount the LM340T/5 regulators on the board, using silicone grease between the sink side of the LM340T and the board Fasten tight with a nut and bolt, but don't overtighten to prevent cracking the board This completes assembly

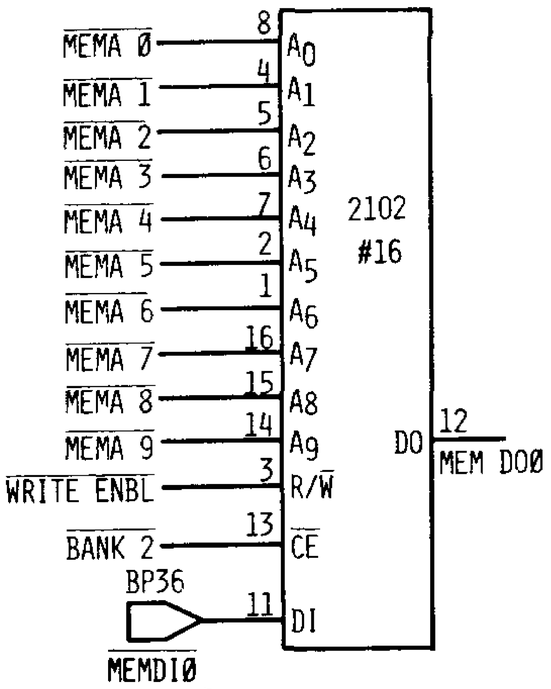
**ADDRESS SELECT This memory board can occupy 1) any of four 16K blocks in your machine, and 2) any 4K block within that 16K Connecting address select hole A to any one of the Y holes selects the first 16K of memory, B jumpered to Y selects the second 16K of memory, C jumpered to Y selects the third 16K of memory, D jumpered to Y selects the fourth 16K of memory Similarly, hole 1 jumpered to any hole X selects the first 4K of the 16K block previously selected, hole 2 jumpered to to hole X selects the second 4K block, hole 3 jumpered to hole X selects the 3rd 4K block, hole 4 jumpered to X selects the fourth 4K block This jumpering may be implemented with wire jumpers or a DIP switch

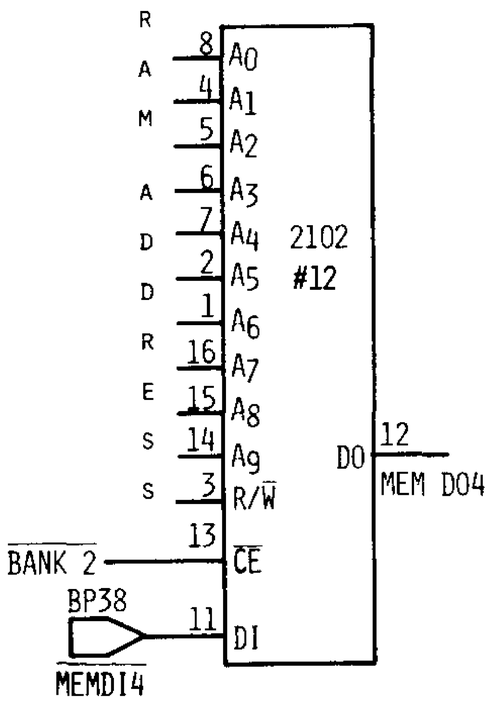
WE HOPE YOU ENJOY ASSEMBLING AND USING "ECONORAM", AND ENJOY GETTING FEEDBACK FROM USERS ON ITS OPERATION AND APPLICATION

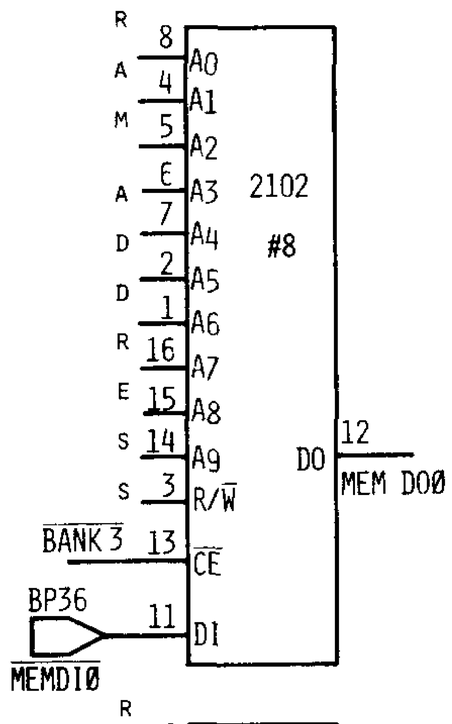
GODBOUT
BILL GODBOUT ELECTRONICS
BOX 2355, OAKLAND AIRPORT, CA 94614

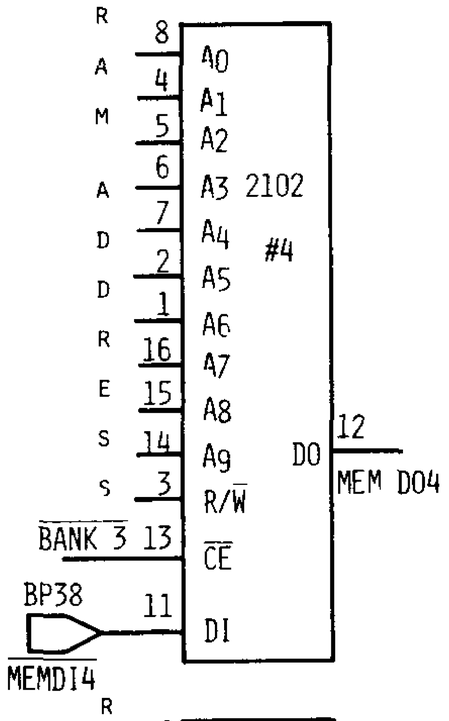
Plug ECONORAM into your ALTAIR, IMSAI, Polymorphic, etc computer so that the component side of the board faces the same direction as the component sides of any other boards plugged into your microcomputer system

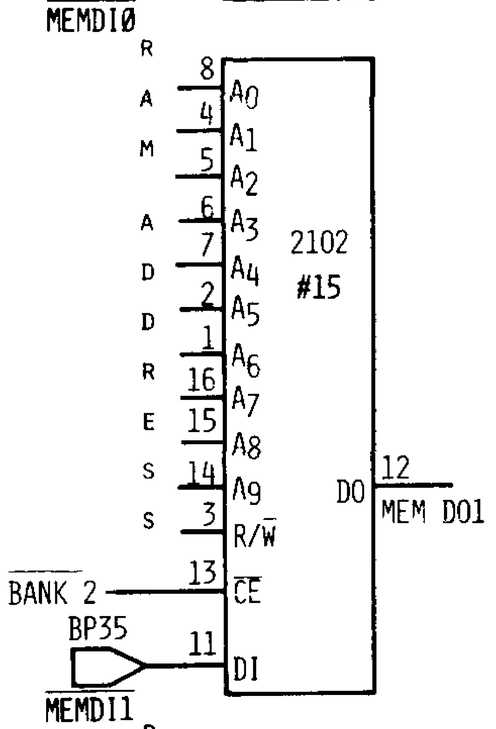
CAVE graphx

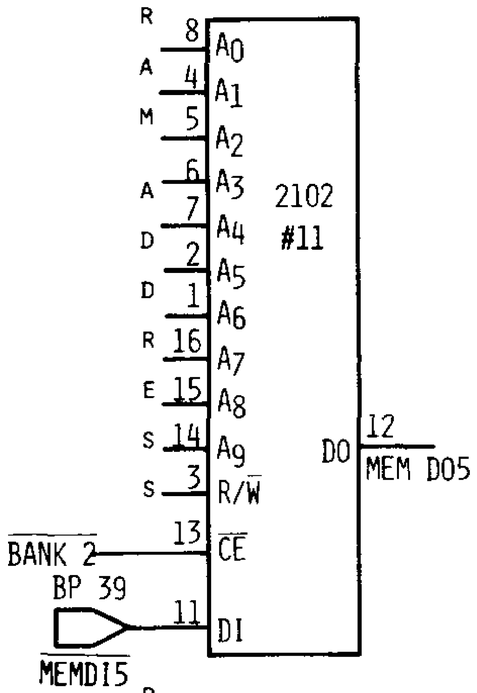

MEMA Ø
MEMA 1
MEMA 2
MEMA 3
MEMA 4
MEMA 5
MEMA 6
MEMA 7
MEMA 8
MEMA 9
WRITE ENBL
BANK 2
BP36
MEMDIØ
2102
#16
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
R/W
CE
DI
DO
MEM DOØ

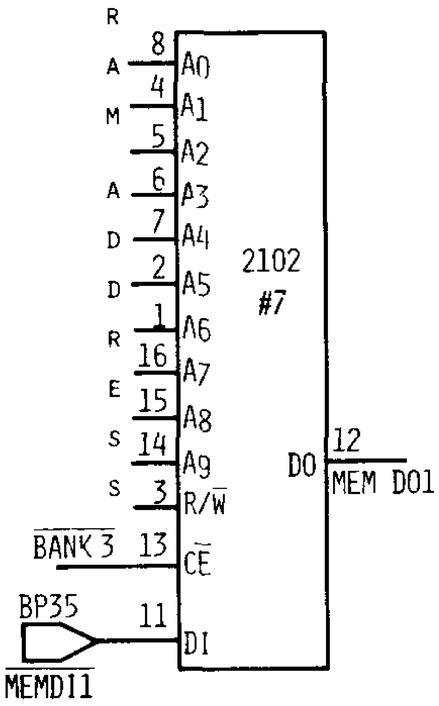

BANK 2
BP38
MEMDI4
2102
#12
MEM DO4

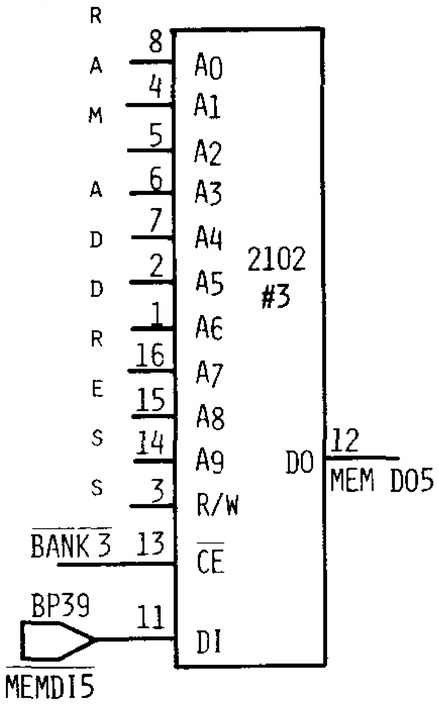

BANK 3
BP36
MEMDIØ
2102
#8
MEM DOØ

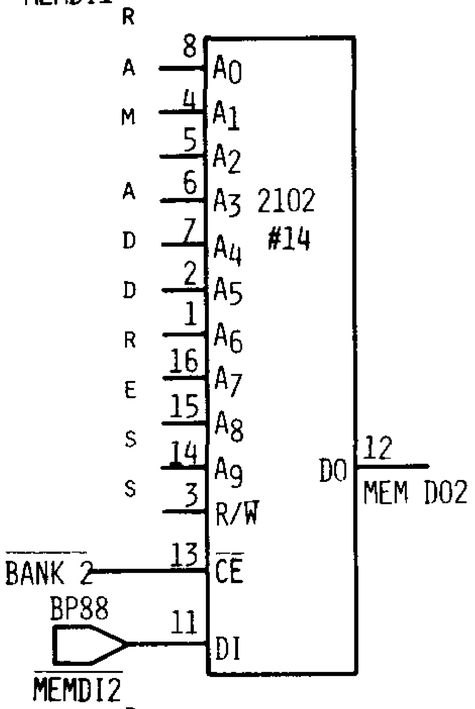

BANK 3
BP38
MEMDI4
2102
#4
MEM DO4

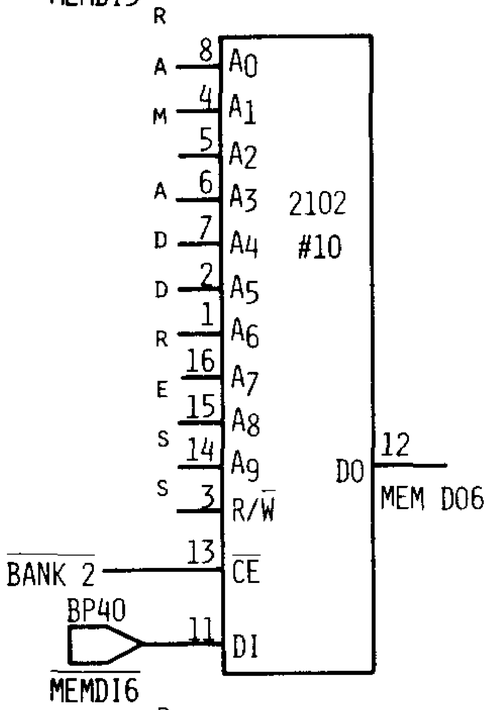

BANK 2
BP35
MEMDI1
2102
#15
MEM DO1

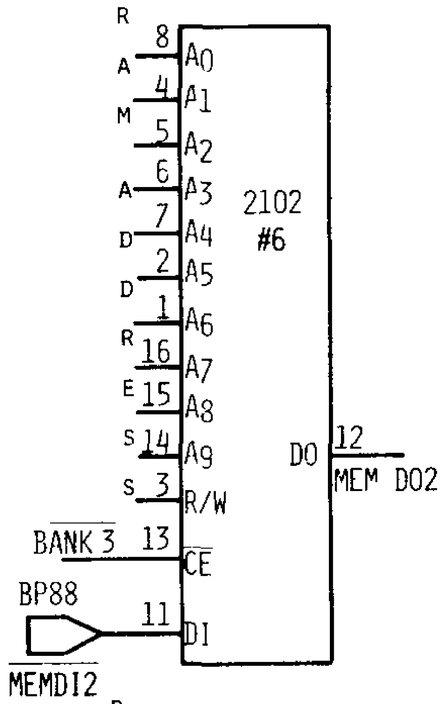

BANK 2
BP 39
MEMDI5
2102
#11
MEM DO5

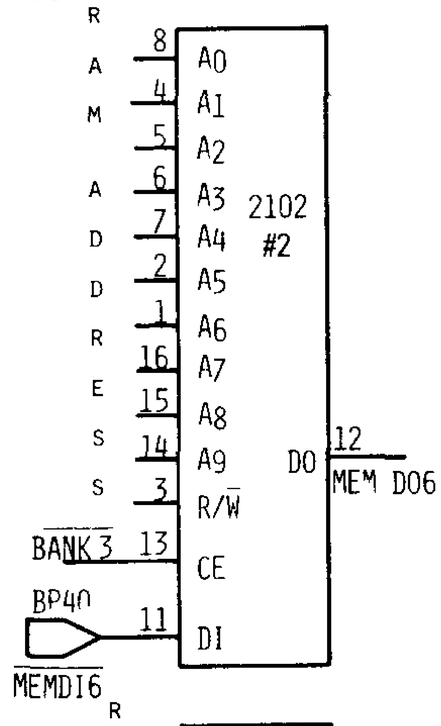

BANK 3
BP35
MEMDI1
2102
#7
MEM DO1

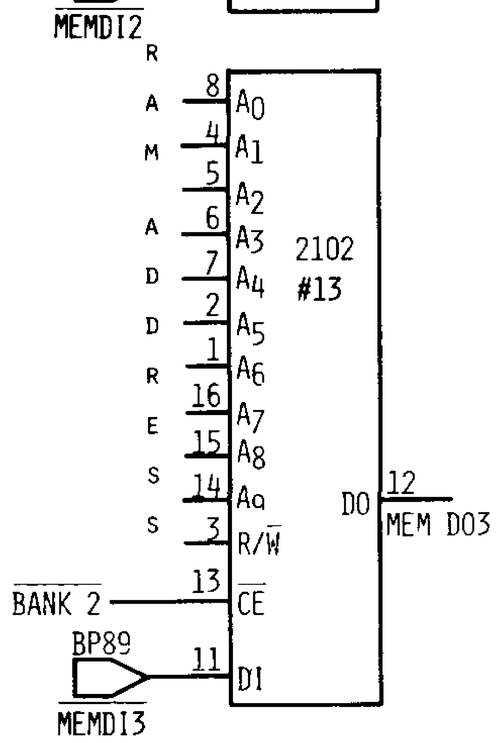

BANK 3
BP39
MEMDI5
2102
#3
MEM DO5

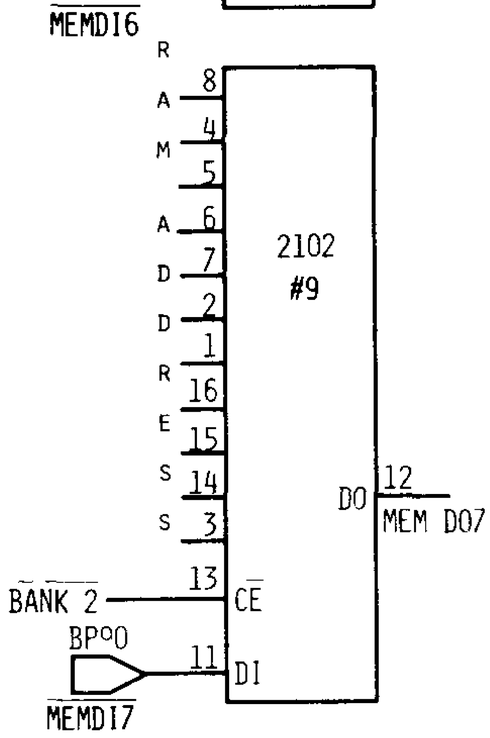

BANK 2
BP88
MEMDI2
2102
#14
MEM DO2

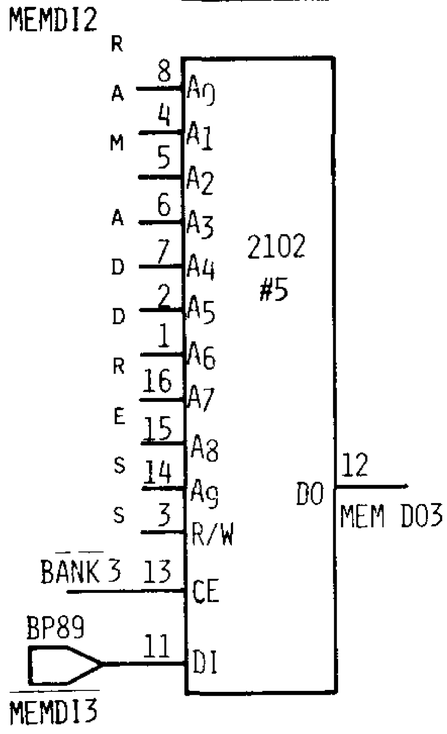

BANK 2
BP40
MEMDI6
2102
#10
MEM DO6


BANK 3
BP88
MEMDI2
2102
#6
MEM DO2


BANK 3
BP40
MEMDI6
2102
#2
MEM DO6


BANK 2
BP89
MEMDI3
2102
#13
MEM DO3


BANK 2
BP90
MEMDI7
2102
#9
MEM DO7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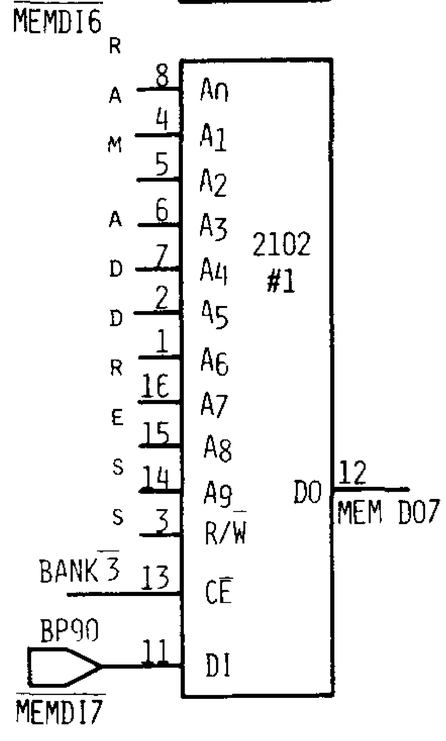
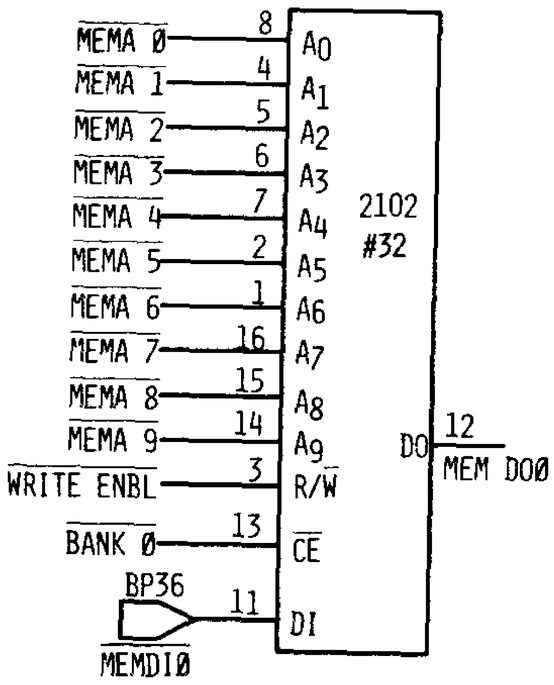
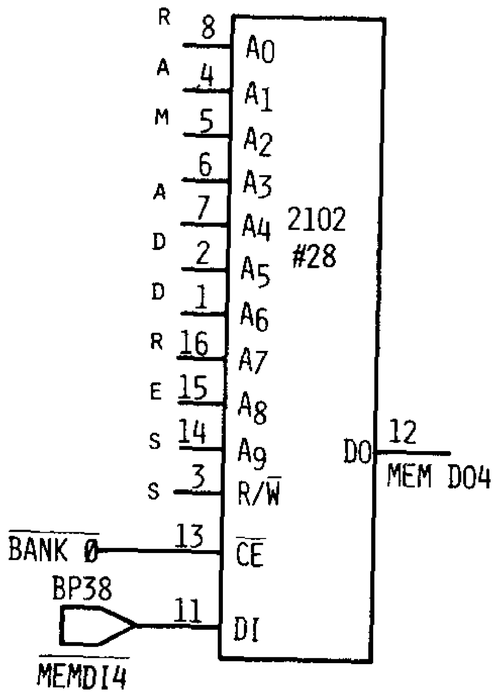
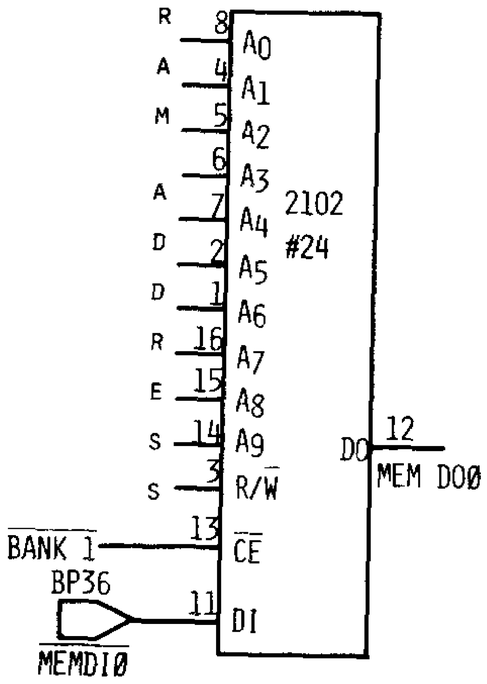
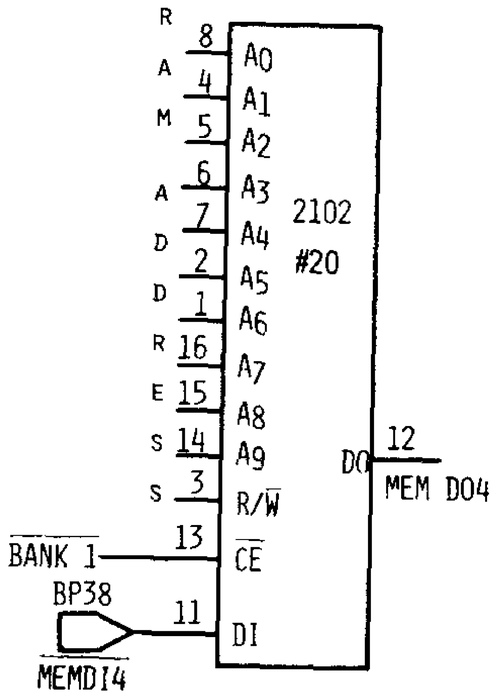
BP89
MEMDI3
2102
#5
MEM DO3

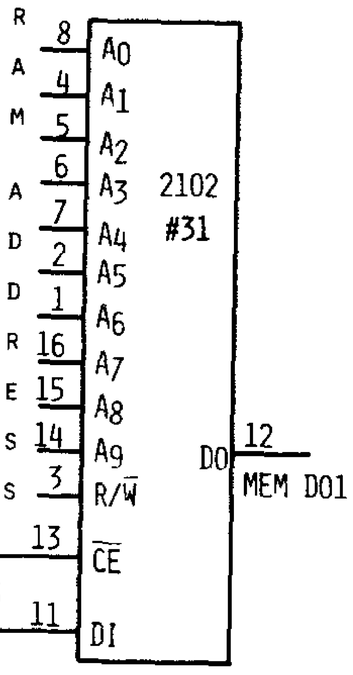

BANK 3
BP90
MEMDI7
2102
#1
MEM DO7

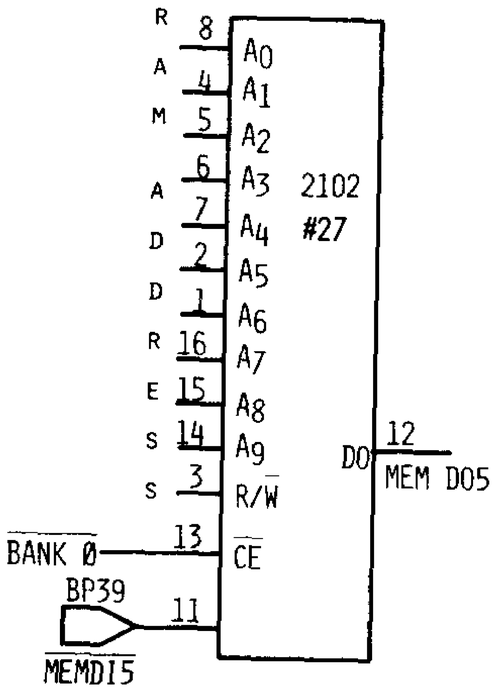

MEMA 0
MEMA 1
MEMA 2
MEMA 3
MEMA 4
MEMA 5
MEMA 6
MEMA 7
MEMA 8
MEMA 9
WRITE ENBL
BANK 0
BP36
MEMDI0
2102
#32
MEM DO0

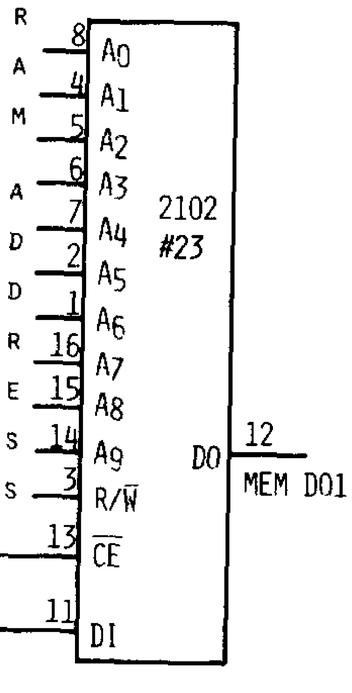

BANK 0
BP38
MEMDI4
2102
#28
MEM DO4

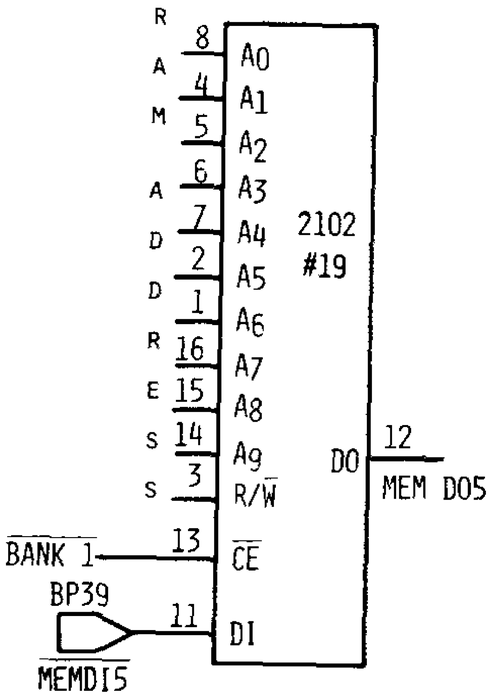

BANK 1
BP36
MEMDI0
2102
#24
MEM DO0

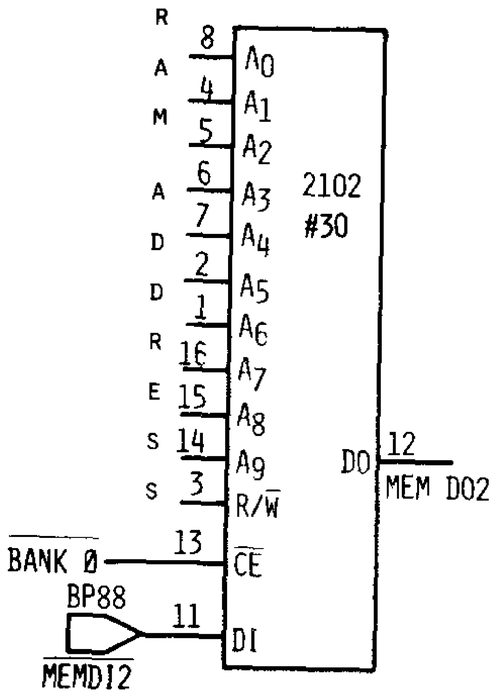

BANK 1
BP38
MEMDI4
2102
#20
MEM DO4

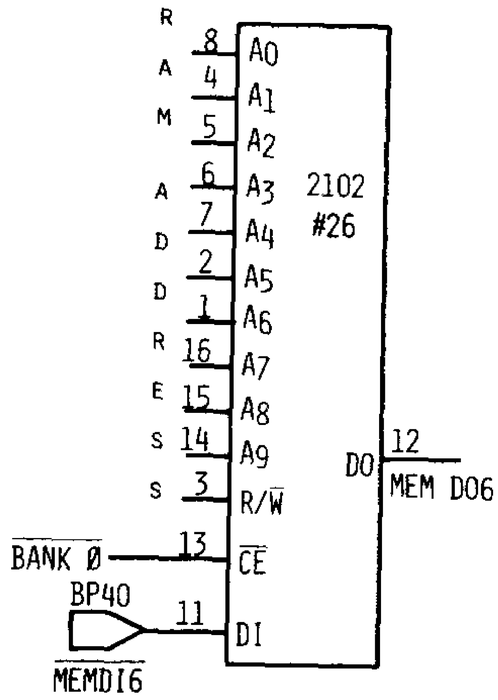

BANK 0
BP 35
MEMDI1
2102
#31
MEM DO1

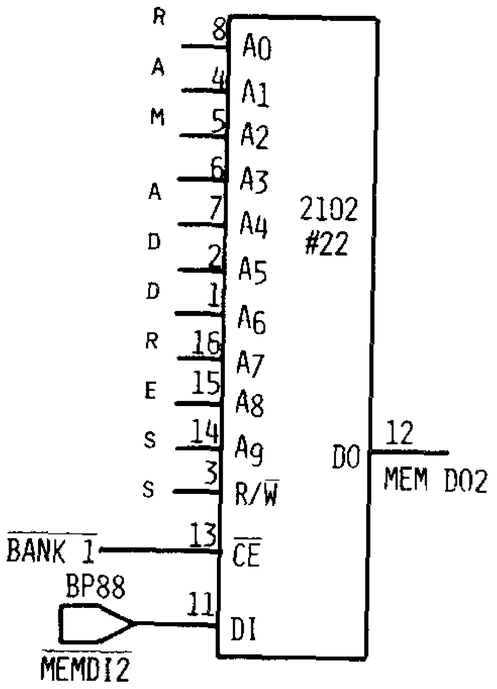

BANK 0
BP39
MEMDI5
2102
#27
MEM DO5

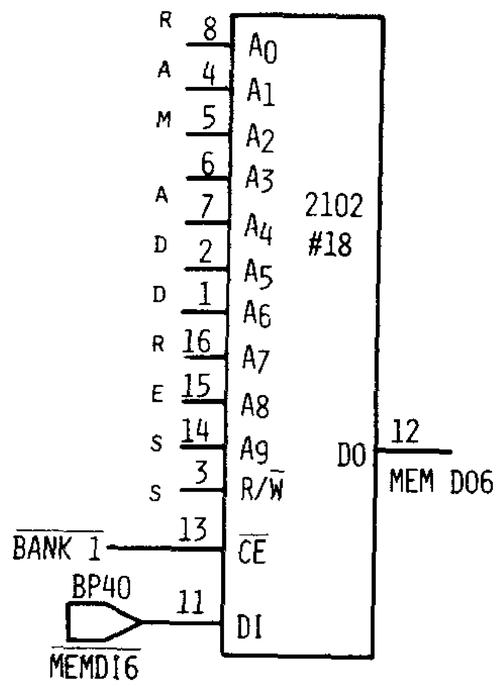

BANK 1
BP35
MEMDI1
2102
#23
MEM DO1

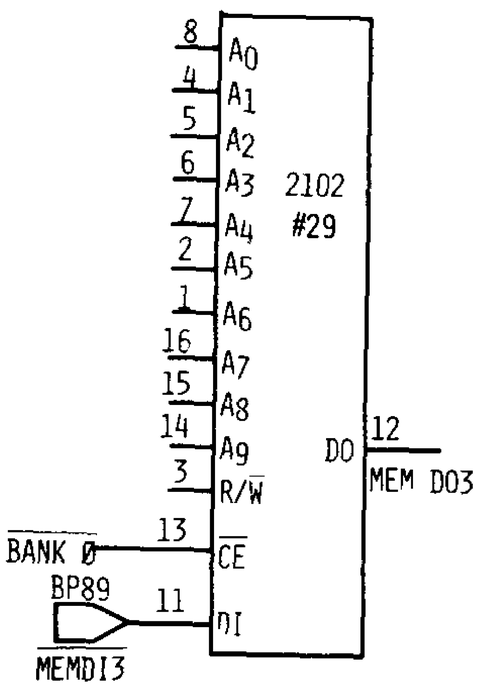

BANK 1
BP39
MEMDI5
2102
#19
MEM DO5

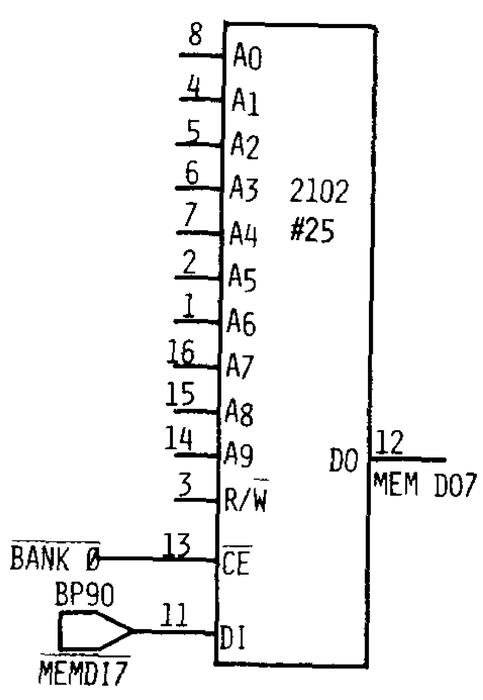

BANK 0
BP88
MEMDI2
2102
#30
MEM DO2

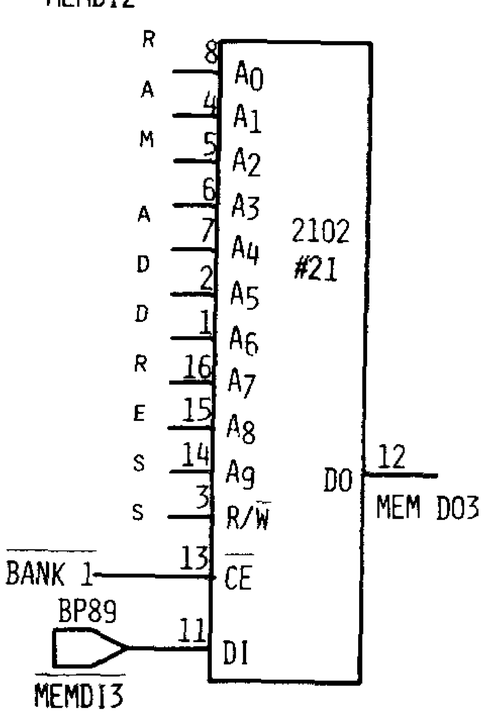

BANK 0
BP40
MEMDI6
2102
#26
MEM DO6

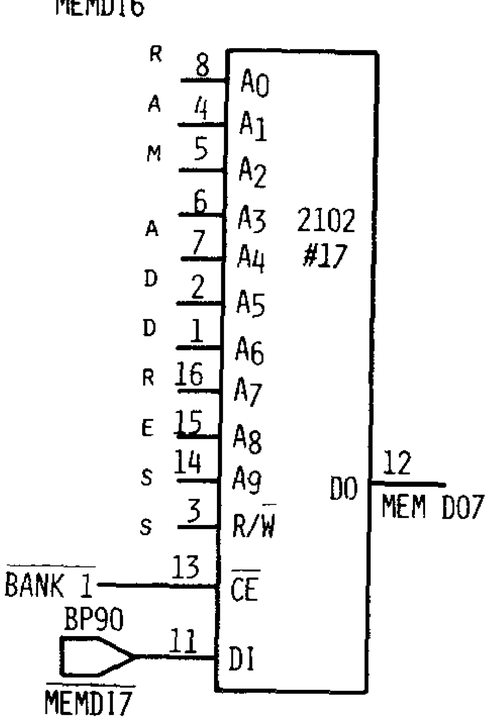

BANK 1
BP88
MEMDI2
2102
#22
MEM DO2

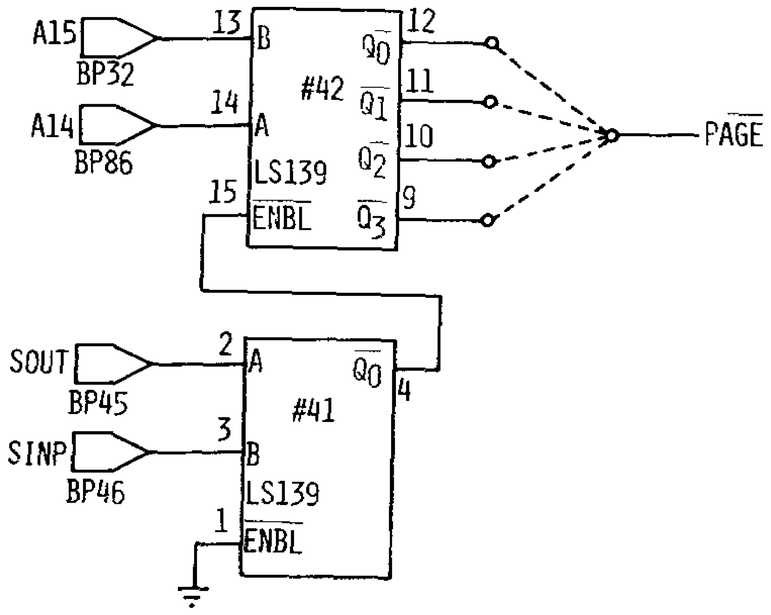

BANK 1
BP40
MEMDI6
2102
#18
MEM DO6

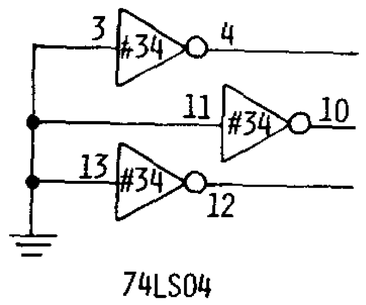

BANK 0
BP89
MEMDI3
2102
#29
MEM DO3

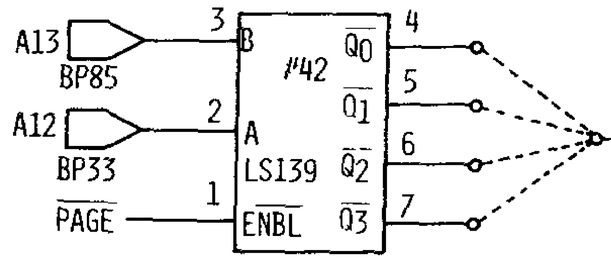

BANK 0
BP90
MEMDI7
2102
#25
MEM DO7

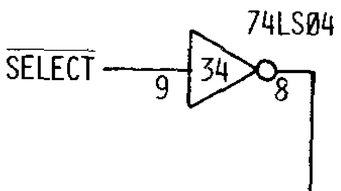

BANK 1
BP89
MEMDI3
2102
#21
MEM DO3

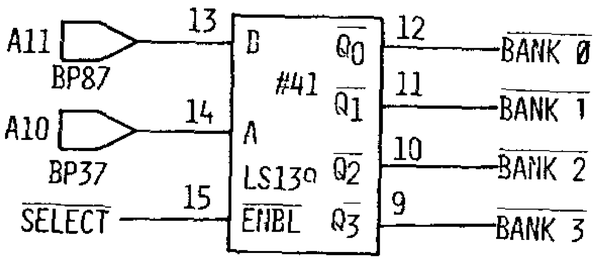

BANK 1
BP90
MEMDI7
2102
#17
MEM DO7

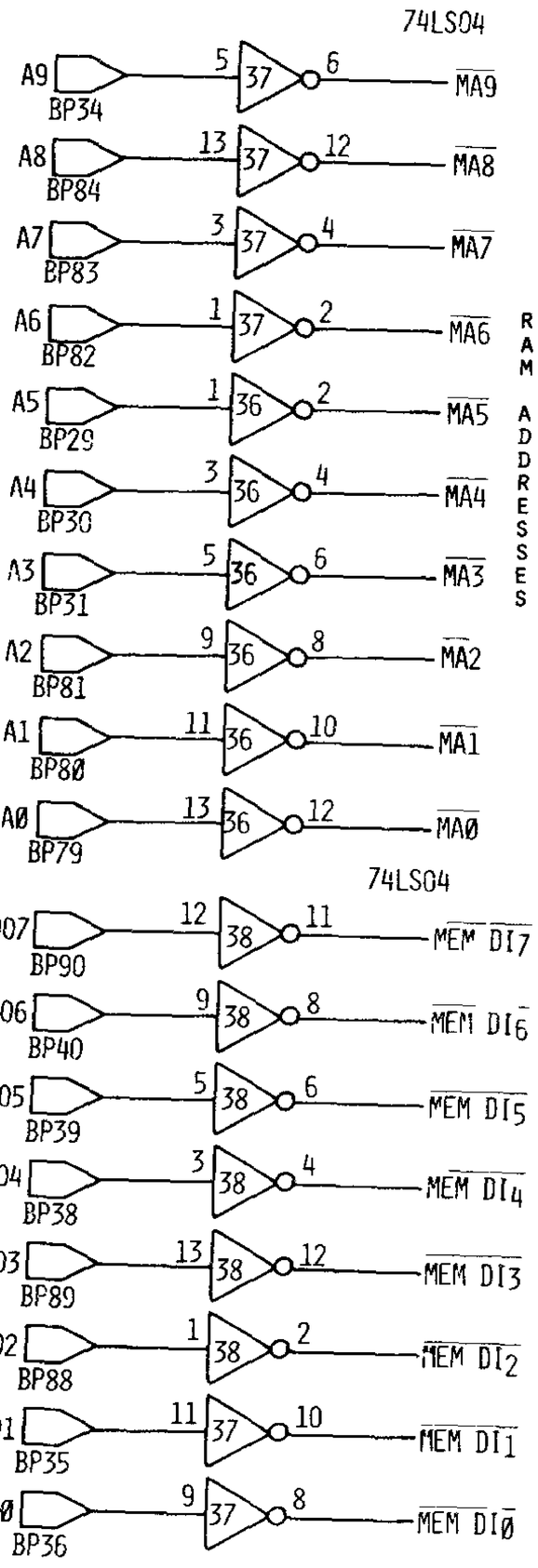


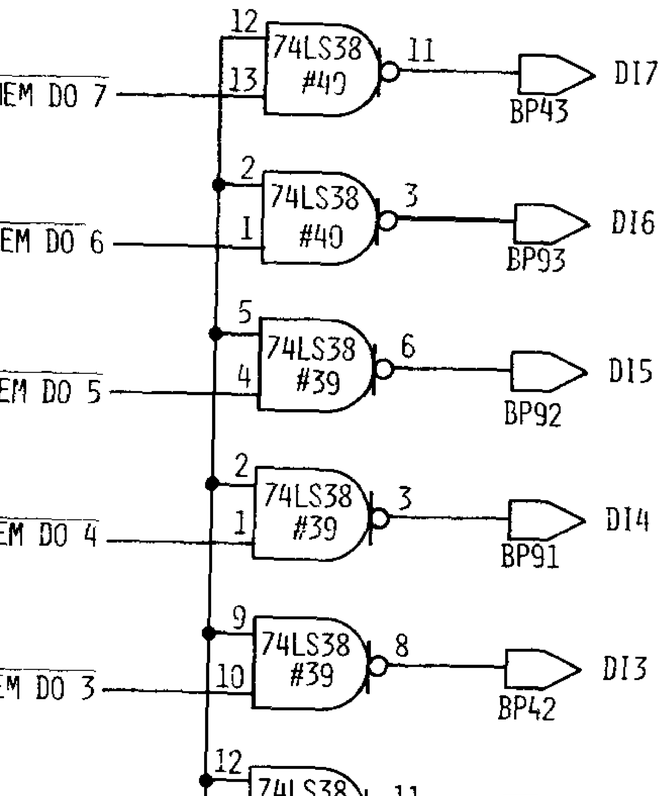


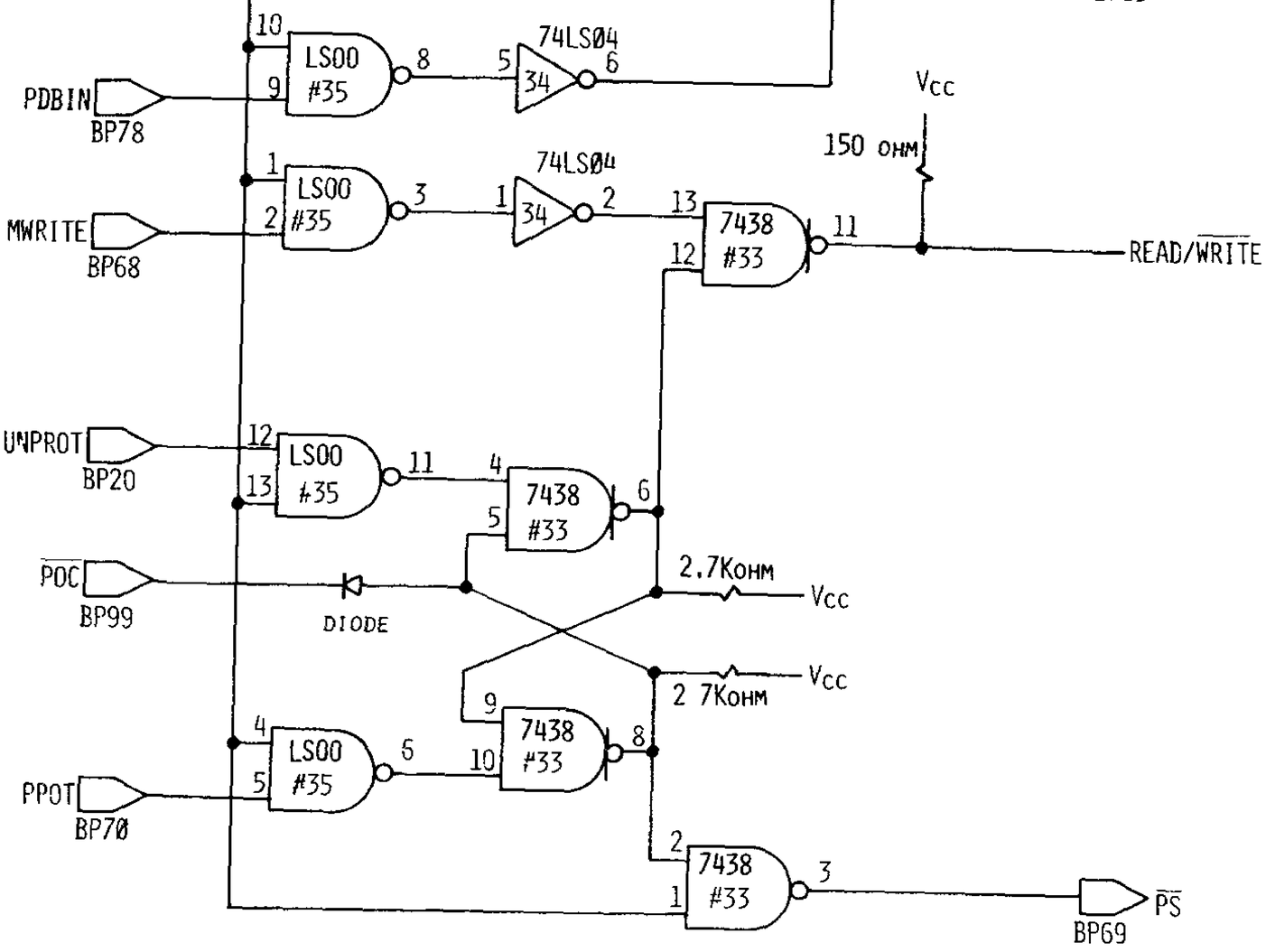




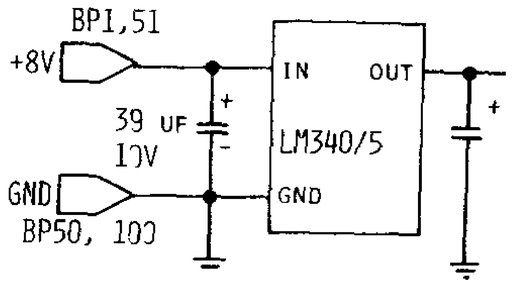








GODBOUT

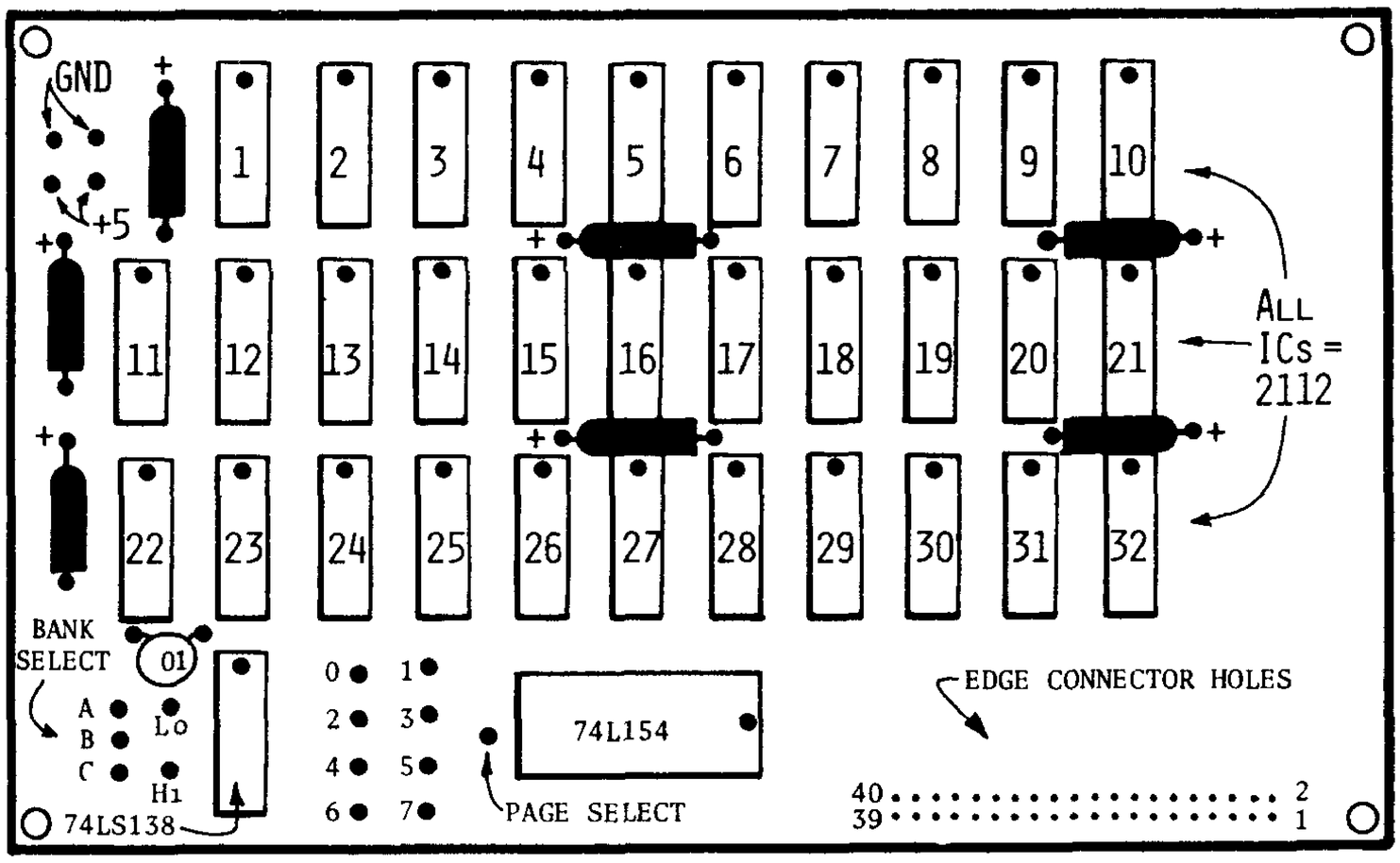


3 PLACES

MORROW'S Micro-STUFF
BOX 6194
ALBANY, CA 94706

IN COOPERATION WITH...

GODBOUT
BILL GODBOUT ELECTRONICS
BOX 2355, OAKLAND AIRPORT, CA 94614



4K BY 8 MEMORY BOARD---VIEWED FROM COMPONENT SIDE.

CAVE grafix

ASSEMBLY INSTRUCTIONS

First, check off your parts against the parts list. (1) double-sided printed circuit board, (7) 39 uF tantalum capacitors (please note the positive end is rounded, the negative end is flat), (1) 01 disc ceramic capacitor, (32) 2112 static RAM ICs, (1) 74LS138 (this IC may be numbered differently, but don't get confused. It's the only 16 pin IC with your kit that is not a 2112), and (1) 74L154 (the IC in a 24 pin package).

ASSEMBLY HINTS· Use a fine tip soldering iron, rated at about 25 watts Use ONLY rosin core solder, using any other type of solder (such as acid core or silver solder) invalidates the warantee. Solder every pin of every socket.

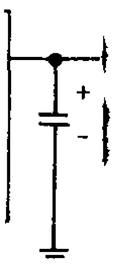
ORDER OF ASSEMBLY· 1) Solder in the 7 tantalum capacitors. OBSERVE POLARITY, as indicated on the board and the component layout diagram. Failure to do so will make any power supply most unhappy. 2) Solder in all IC sockets. 3) Solder in the 01 disc ceramic capacitor. 4) Check your work carefully, observing whether there are any solder bridges, cold joints, or other potential problems. If you're satisfied with your work, plug in all ICs (using MOS handling techniques on the 2112 ICs), now you're ready to set the BANK and PAGE select.

BANK SELECT PROCEDURE This memory board may be configured in the upper or lower 32 kbytes of memory via BANK SELECT. To select the lower 32K, jumper hole LO to hole B, and jumper hole HI to hole C. To select the upper 32K, jumper hole LO to hole A, and jumper hole HI to hole B.

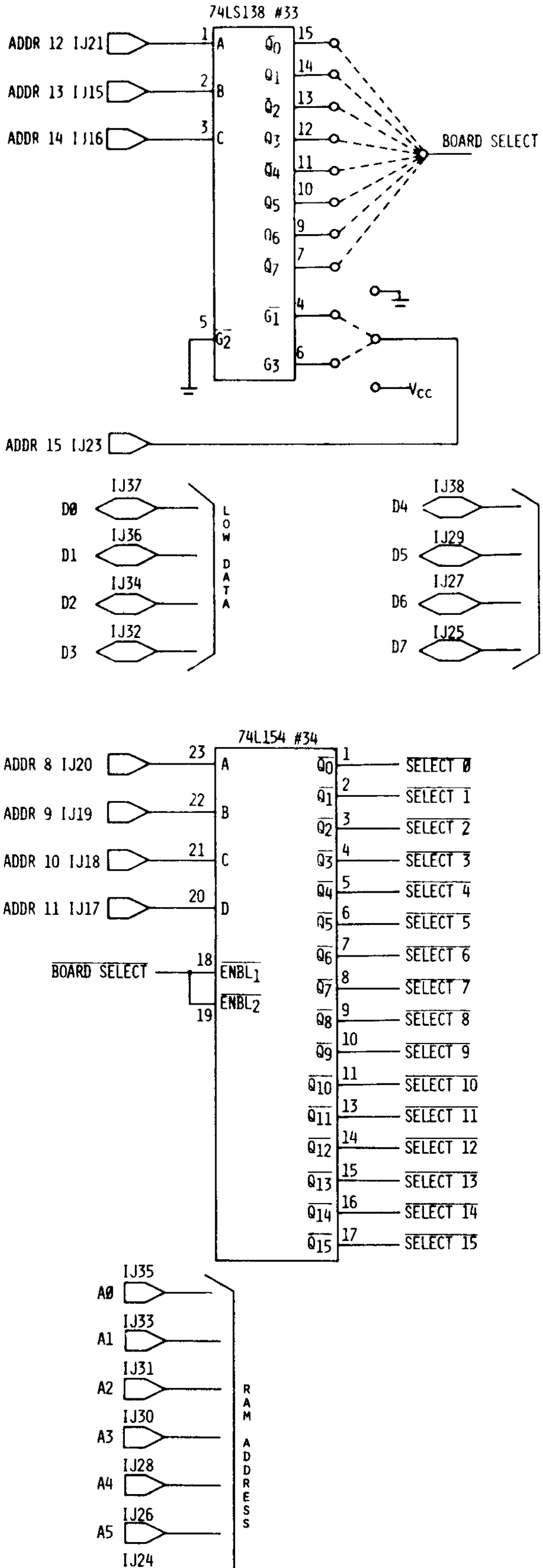
PAGE SELECT PROCEDURE This memory board can occupy any one of eight 4 kbyte blocks within the 32k of memory specified under BANK SELECT Jumpering from the hole labelled PAGE SELECT to hole 0 selects the lowest 4K block, jumpering to hole 1 selects the second lowest 4K block; and so on.. until jumpering to hole 7 selects the highest 4K block.

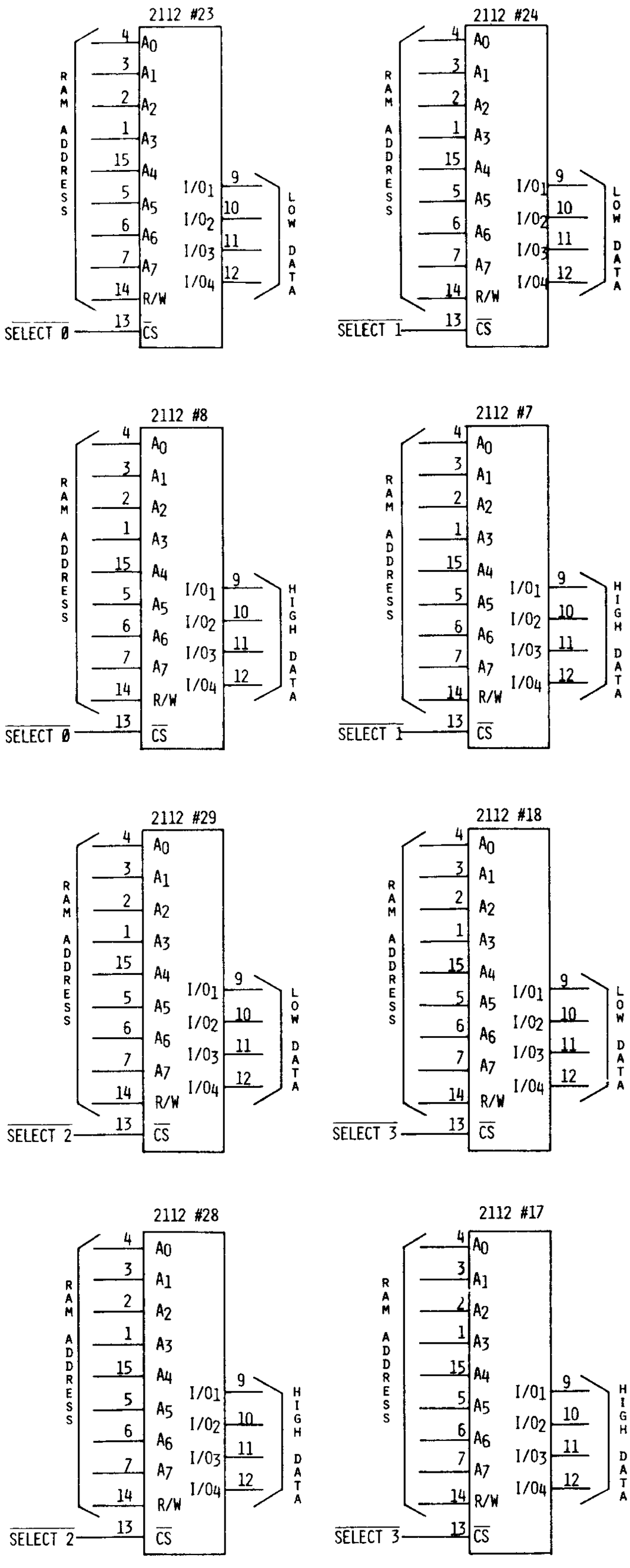
EDGE CONNECTOR HOLES The NAKED RAM's connections to the outside world are all numbered (see logic print overleaf). These numbers correspond to holes in the EDGE CONNECTOR HOLES area. You may either use a commerically available header-connector combination, or hard wire the holes into your system yourself. The numbering scheme of the holes is as follows as shown in the component layout diagram, hole 1 is in the bottom right-hand corner. The row counts upward, in odd integer increments (1 .3 .5 7 9 .11. 13 .15 etc) until hole 39, which is in the extreme bottom left-hand corner Similarly, hole 2 is in the upper right hand corner, the holes in the upper row count upward, in even integer increments (2..4..6..8..etc) until hole 40, which is in the extreme top left.

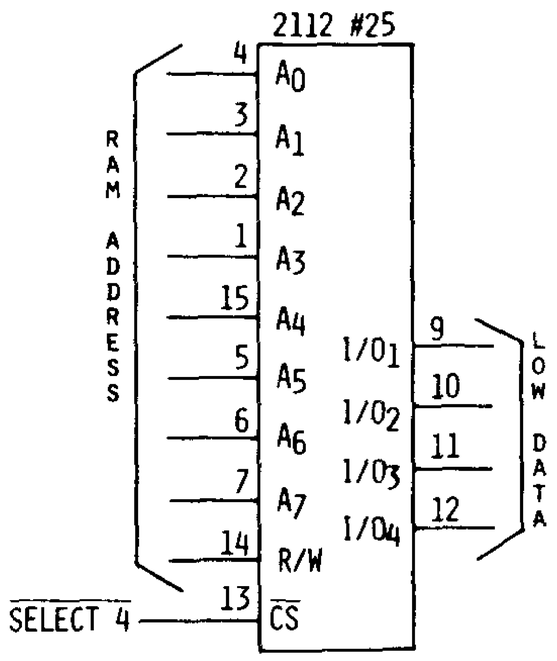
Should you wish to use a commercially available header/connector combination (which we recommend), here are the details The part that solders into the board is called the header. This plugs into a socket connector (which some companies call a transition connector). The socket connector connects to other socket connectors via a length of multiconductor flat cable Following is a partial list of suppliers for these products, and any special notes·
AP PRODUCTS (Box 110, 72 Corwin Drive, Painesville, OH 44077) They make a 40 pin header, part # 922585-40. They also sell a socket connector/multiconductor cable/socket connector combination as one molded unit, part #922521-40-X, where X is the length of the cable in inches
ELECTRONIC PRODUCTS DIVISION, 3M COMPANY (3M center, St Paul, Minnesota 55101) makes a header, part #3432-1002. You will also need two socket connectors, #3417-0000, as well as a length of cable, #3365/40 The two socket connectors press fit tightly onto the cable.
ANSLEY ELECTRONICS CORPORATION (3208 Humboldt St , Los Angeles, CA 90031) makes the same type of products The header is part #609-4002M, the transition connector is #609-4000M, and their cable number is #171-40

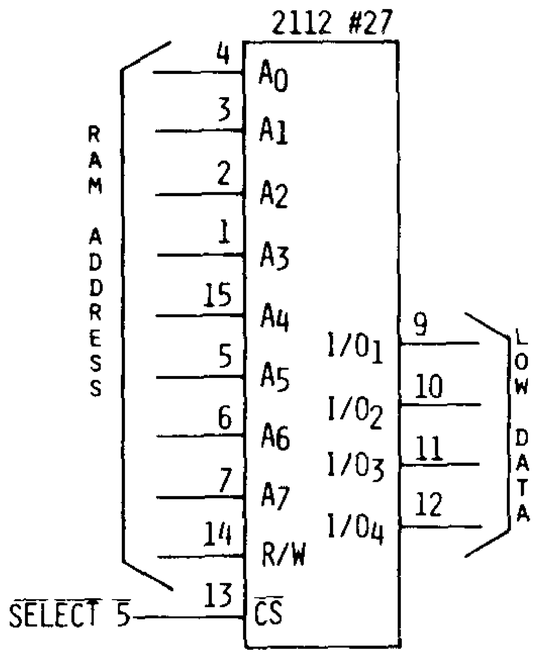


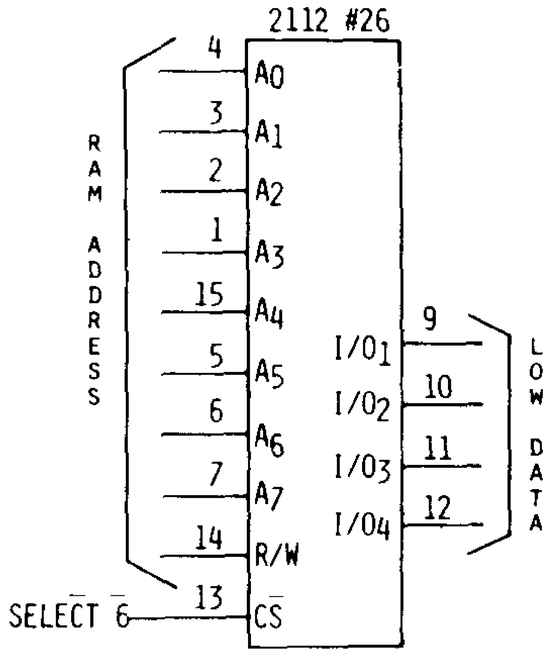
WE HOPE YOU ENJOY USING AND ASSEMBLING YOUR "NAKED RAM" KIT. WE ARE INTERESTED IN ANY COMMENTS OR CRITICISMS YOU MAY HAVE ON OUR PRODUCTS AND ENJOY GETTING FEEDBACK FROM USERS

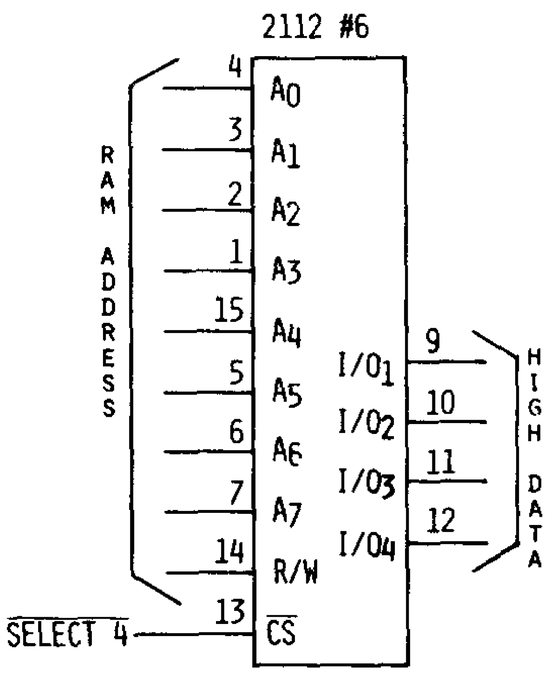

74LS138 #33
ADDR 12 IJ21
ADDR 13 IJ15
ADDR 14 IJ16
ADDR 15 IJ23
BOARD SELECT
Vcc
IJ37
D0
IJ36
D1
IJ34
D2
IJ32
D3
LOW DATA
IJ38
D4
IJ29
D5
IJ27
D6
IJ25
D7
HIGH DATA
74L154 #34
ADDR 8 IJ20
ADDR 9 IJ19
ADDR 10 IJ18
ADDR 11 IJ17
BOARD SELECT
SELECT 0
SELECT 1
SELECT 2
SELECT 3
SELECT 4
SELECT 5
SELECT 6
SELECT 7
SELECT 8
SELECT 9
SELECT 10
SELECT 11
SELECT 12
SELECT 13
SELECT 14
SELECT 15
IJ35
A0
IJ33
A1
IJ31
A2
IJ30
A3
IJ28
A4
IJ26
A5
IJ24
A6
IJ22
A7
IJ40
WRITE*
RAM ADDRESS

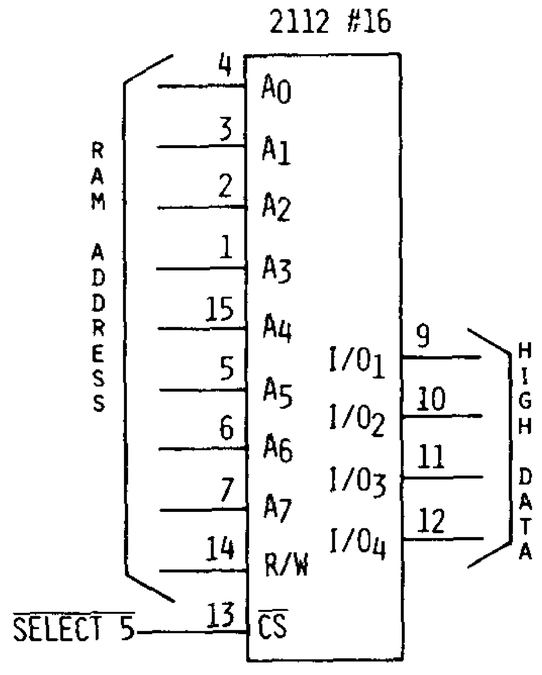

2112 #23
2112 #24
2112 #8
2112 #7
2112 #29
2112 #18
2112 #28
2112 #17
RAM ADDRESS
LOW DATA
HIGH DATA
SELECT 0
SELECT 1
SELECT 2
SELECT 3

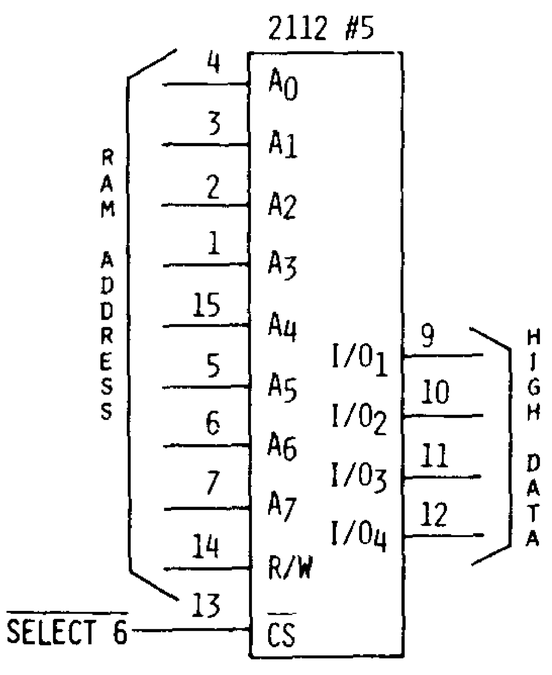

2112 #25
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 4
I/O1 9
I/O2 10
I/O3 11
I/O4 12
LOW DATA

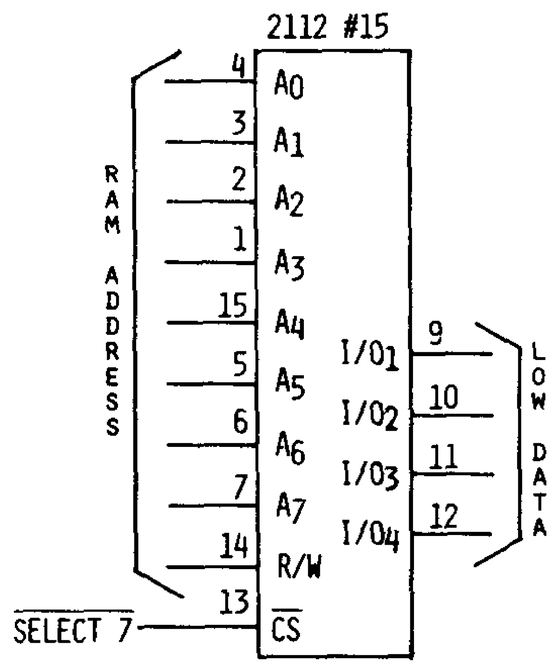

2112 #27
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 5
I/O1 9
I/O2 10
I/O3 11
I/O4 12
LOW DATA

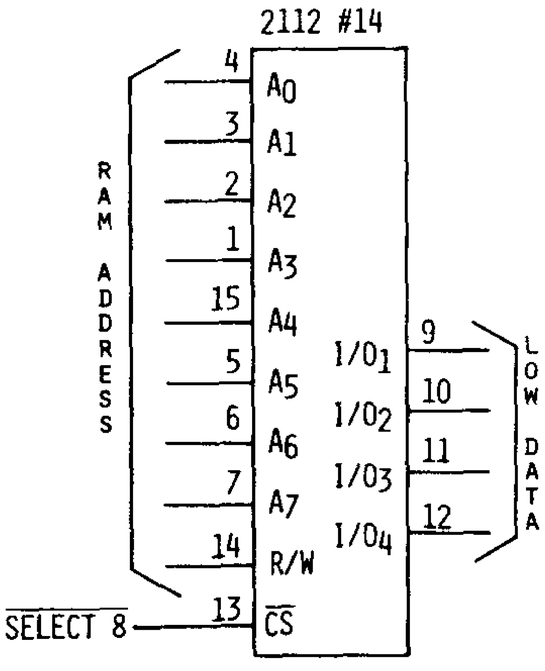

2112 #26
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 6
I/O1 9
I/O2 10
I/O3 11
I/O4 12
LOW DATA

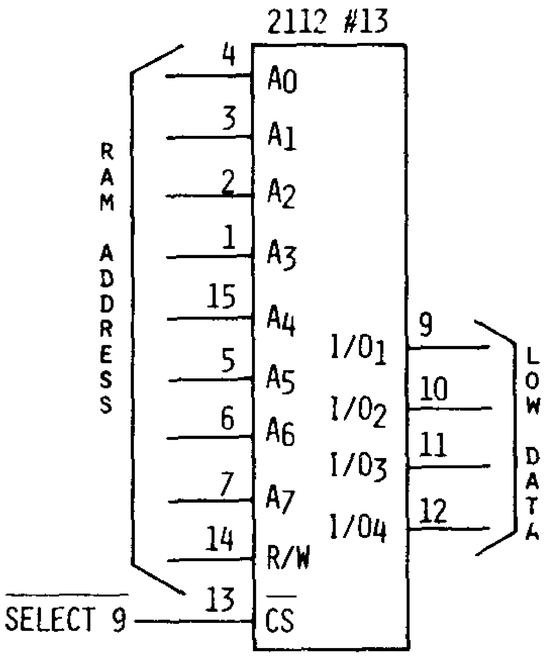

2112 #6
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 4
I/O1 9
I/O2 10
I/O3 11
I/O4 12
HIGH DATA

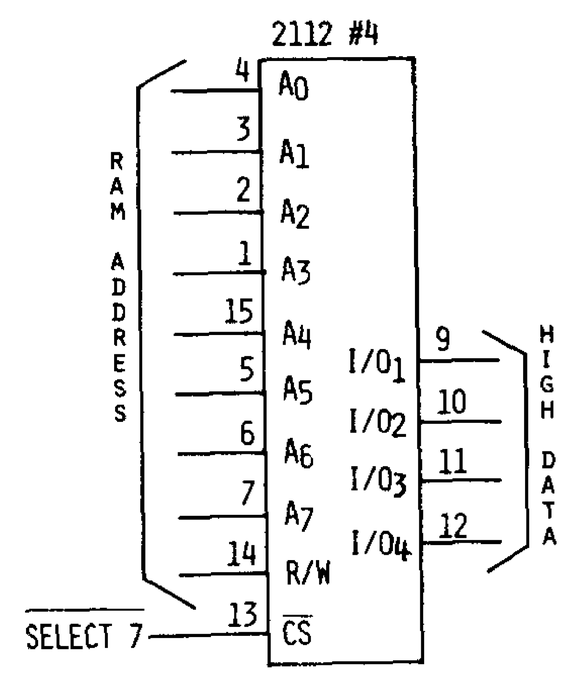

2112 #16
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 5
I/O1 9
I/O2 10
I/O3 11
I/O4 12
HIGH DATA

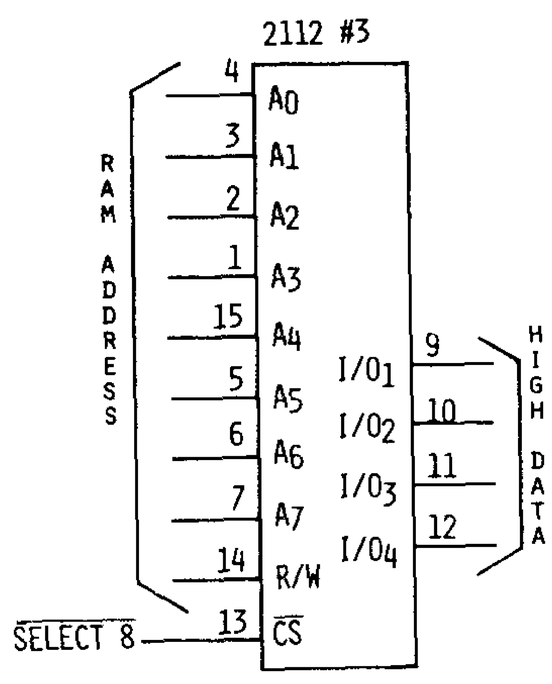

2112 #5
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 6
I/O1 9
I/O2 10
I/O3 11
I/O4 12
HIGH DATA

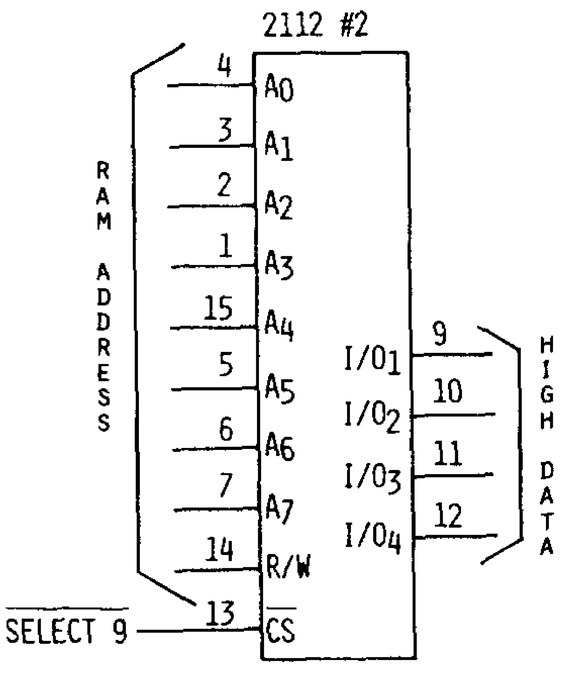

2112 #15
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 7
I/O1 9
I/O2 10
I/O3 11
I/O4 12
LOW DATA

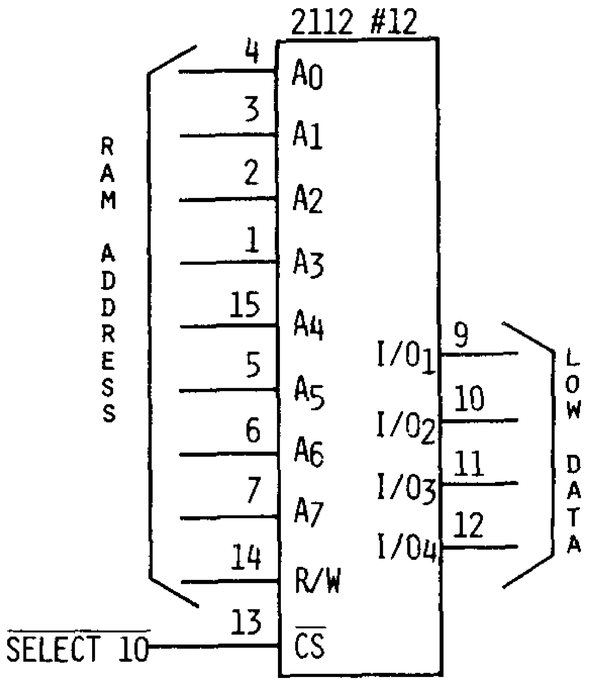

2112 #14
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 8
I/O1 9
I/O2 10
I/O3 11
I/O4 12
LOW DATA

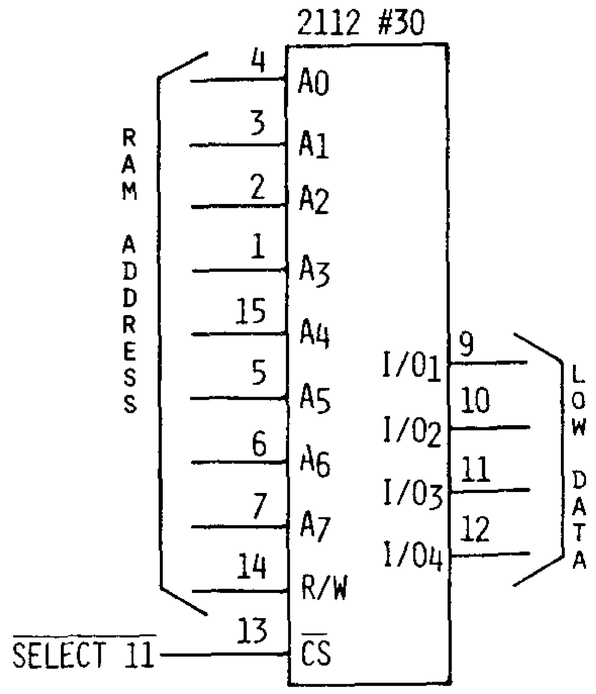

2112 #13
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 9
I/O1 9
I/O2 10
I/O3 11
I/O4 12
LOW DATA

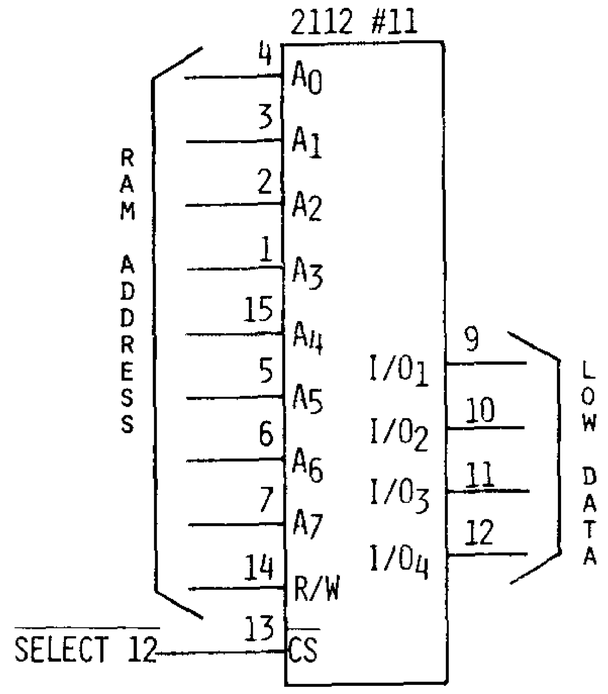

2112 #4
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 7
I/O1 9
I/O2 10
I/O3 11
I/O4 12
HIGH DATA

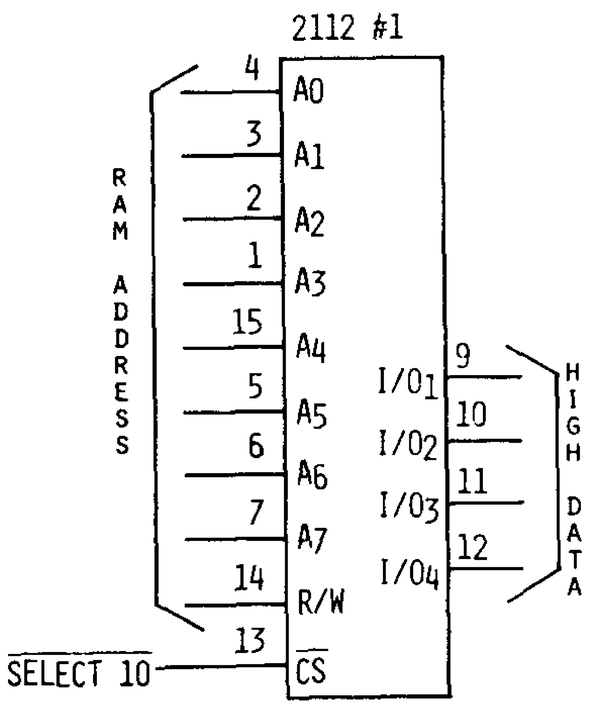

2112 #3
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 8
I/O1 9
I/O2 10
I/O3 11
I/O4 12
HIGH DATA

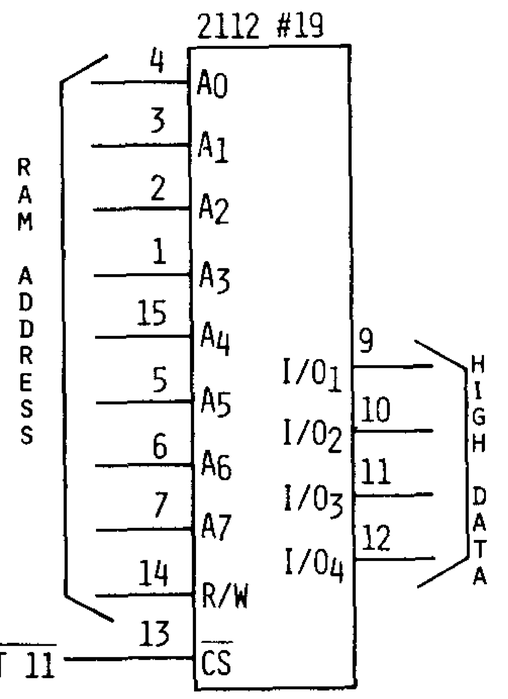

2112 #2
RAM ADDRESS
4 A0
3 A1
2 A2
1 A3
15 A4
5 A5
6 A6
7 A7
14 R/W
13 CS
SELECT 9
I/O1 9
I/O2 10
I/O3 11
I/O4 12
HIGH DATA

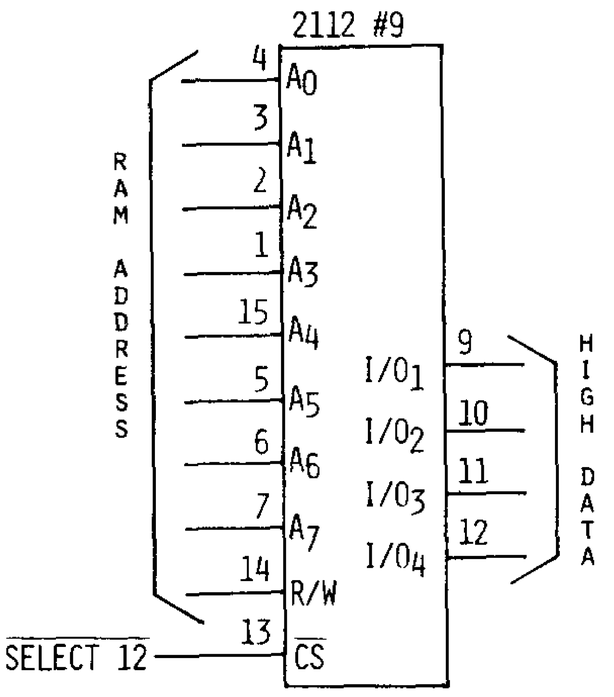

2112 #12
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
LOW DATA
SELECT 10

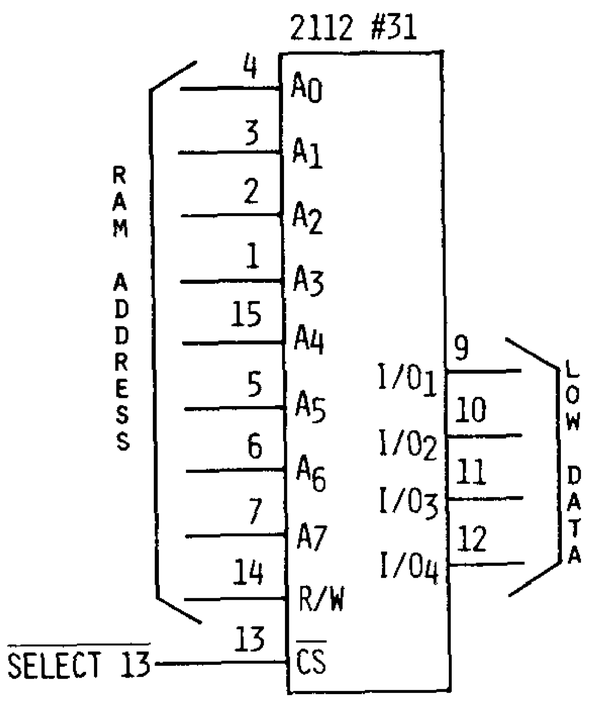

2112 #30
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
LOW DATA
SELECT 11

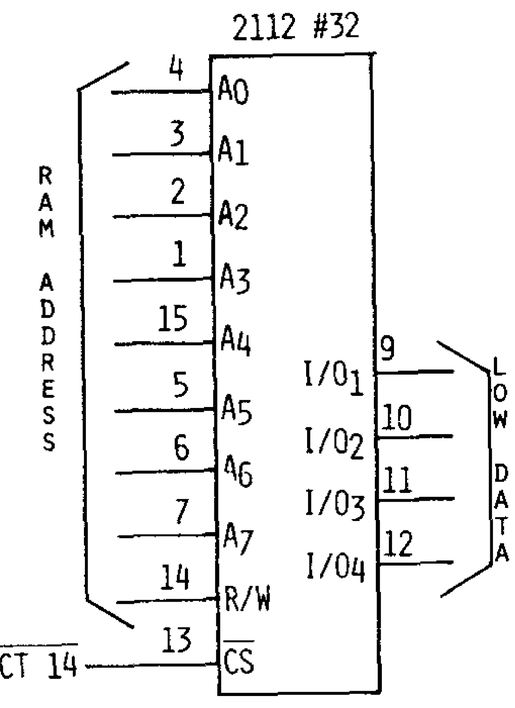

2112 #11
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
LOW DATA
SELECT 12

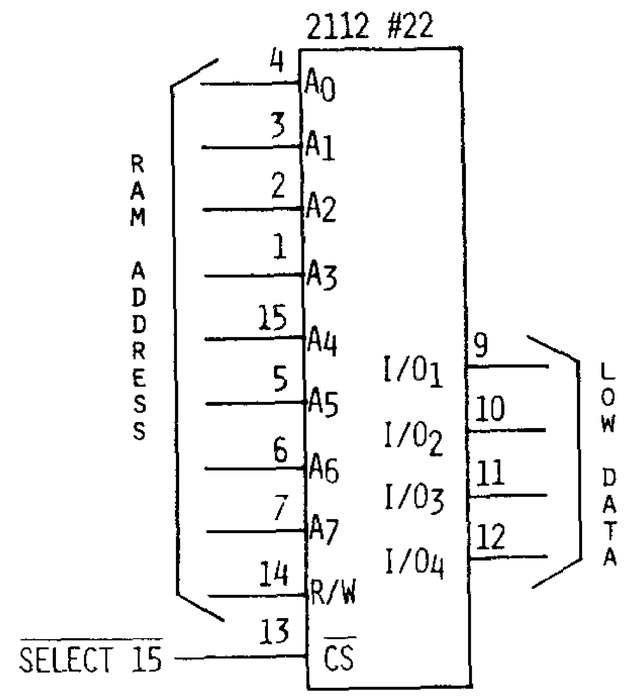

2112 #1
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
HIGH DATA
SELECT 10


2112 #19
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
HIGH DATA
SELECT 11


2112 #9
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
HIGH DATA
SELECT 12


2112 #31
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
LOW DATA
SELECT 13


2112 #32
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
LOW DATA
SELECT 14


2112 #22
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
LOW DATA
SELECT 15

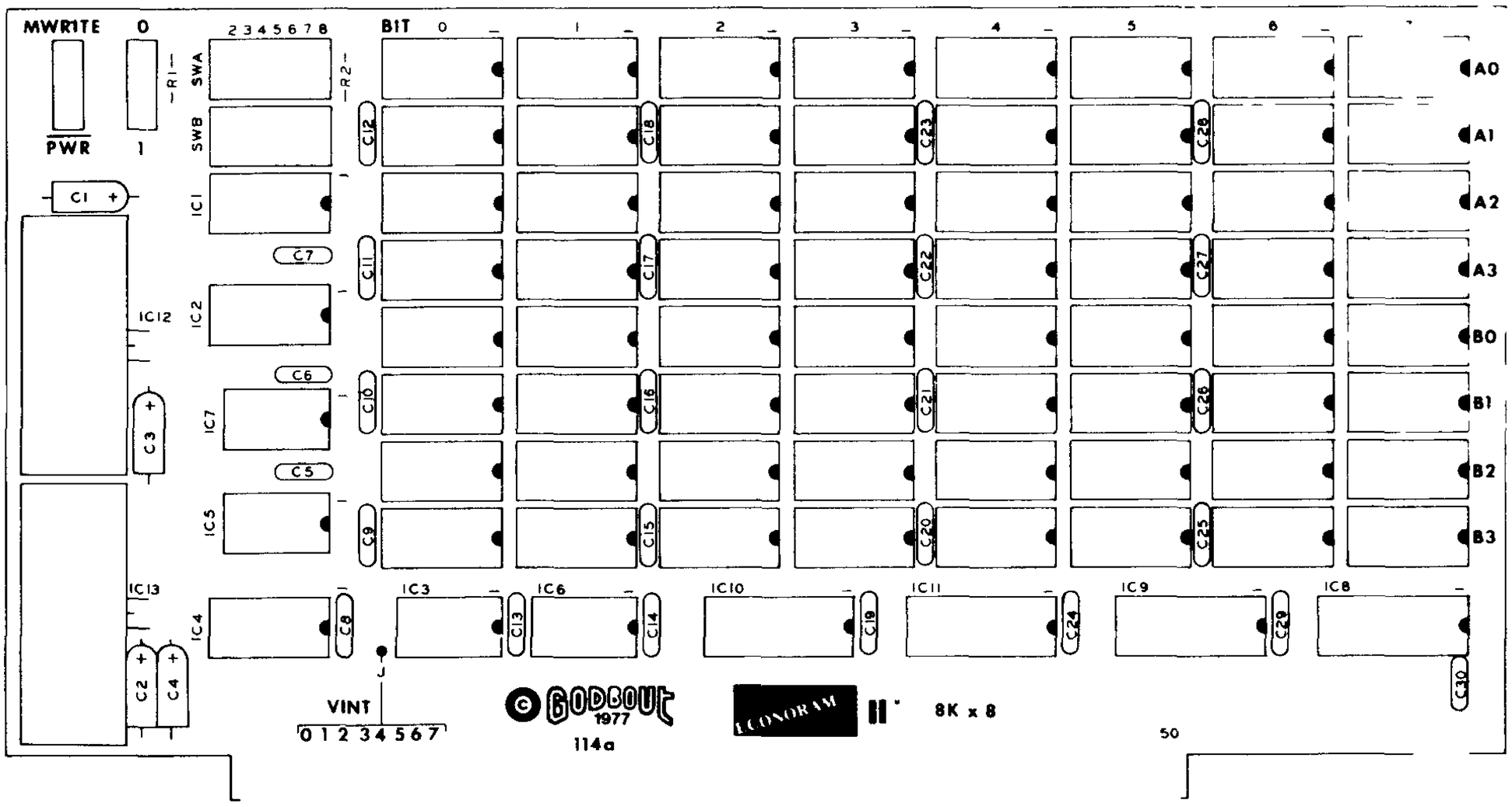
2112 #20
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
HIGH DATA
SELECT 13

2112 #21
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
HIGH DATA
SELECT 14

2112 #10
RAM ADDRESS
A0
A1
A2
A3
A4
A5
A6
A7
R/W
CS
I/O1
I/O2
I/O3
I/O4
HIGH DATA
SELECT 15

8k/4k ECONORAM II™ DATA SHEET

PROJECT 114A



ORDER OF ASSEMBLY Read these instructions carefully take your time and don t rush This board accomodates 8K worth of memory, if you have ordered the 4K version it may be expanded to a full 8K at a later date by adding more parts

PRELIMINARIES Check off the parts in your kit against the parts list to familiarize yourself with the various components Note that the rounded ends of the 39 uF tantalum capacitors are the (+) ends

SOLDERING Use a fine tip soldering iron rated at about 25 Watts Use only rosin core solder using any other type of solder invalidates the warranty Solder every pin of every socket This board uses a solder mask to reduce the chances of bridges and solder shorts be sparing with your solder and heat both the lead and pad while soldering

(1) Mount resistors R1 and R2 then solder and remove excess lead lengths
(2) Mount the sockets for support ICs (IC1 IC11) and solder them To prevent the sockets from falling out as you turn the board over to solder put a piece of cardboard over the top of the sockets and turn the board over while holding the cardboard against the sockets to keep them in place
(3) Mount and solder the 64 remaining 16 pin sockets (NOTE In the 4K version only 32 sockets will be left Mount and solder them in rows AØ A1 A2 and A3 leaving rows BØ B1 B2 and B3 unpopulated)
(4) Mount and solder C1 C4 observe polarity (NOTE In the 4K version omit C2 and C4)
(5) Mount and solder all other capacitors in place (NOTE In the 4K version do not solder capacitors into locations C9, C10, C15 C16, C20 C21 C25 and C26)
(6) Check for solder shorts before proceeding by attaching an ohmmeter across C3+C4 A reading of 0 ohms indicates a problem check your work over if this is the case
(7) Mount the regulators (IC12 & IC13) on to the board by pushing their leads into the designated holes on the board then bend them over on top of the heat sinks as shown in figure 1 Although not required adding some silicone heat sink compound between the regulator and heat sink improves the efficiency of the heat sink Bolt the regulator/heat sink combinations into place using the hardware provided (NOTE *In the 4K version IC13* along with associated hardware/heat sink is not required) Finally solder the regulator leads
(8) To check the card and regulators plug this board into your system Measure the voltages across C3+C4 (NOTE C4 not included on 4K board) with an ohmmeter If you obtain readings other than 5V +5% recheck your work
(9) Orient the board with the component side facing you and the edge connector pointing down Solder the two slide switches into place in the upper left hand corner of the board
(10) Solder the two DIP switches into place making sure that the numbers on the DIP switches correspond with the numbers screened on the board (NOTE In the 4K version DIP switch B is not used)
(11) Carefully check your solder connections for bridges cold joints or other potential causes of difficulty Once satisfied with your work plug in the various ICs as shown on the component layout diagram This completes assembly of your unit

SETTING THE DIP SWITCHES The ICs contained in rows AØ A3 form a 4K block of memory designated Block A The ICs contained in rows BØ B3 form another 4K block of memory designated Block B Either block may be configured anywhere in the 64K range directly addressable by your computer via setting the appropriate DIP switch switch A corresponds to block A switch B corresponds to block B On both switches the four right hand toggles (5 8) choose one of 4 16K blocks the left hand toggle switches (1 4) choose a 4K block within the chosen 16K block Table 1 shows which toggles must be ON in order to select the desired block of memory Note two points of interest unlike some other memory boards blocks A & B need not be configured next to each other Additionally having all switches in the OFF position makes it impossible to either read from or write into the memory This can be useful if you want to have two blocks of memory occupying the same space and need to disable one or the other as the need arises

SETTING THE SLIDE SWITCHES Orient the board with the component side facing you and the edge connector pointing down *The right hand slide switch should normally be in the UP position* (0 wait states) For machines using the Z 80 processor driven by a 4 MHz clock 1 wait state is required In this instance slide the switch into the DOWN position

The left hand switch is the write strobe select switch For most conventional systems employing a front panel this switch should be in the UP position which selects MWRITE as the write strobe If you have a system with no front panel (and therefore no MWRITE signal) the switch should be in the DOWN position which selects $\overline{PWR}$ as the write strobe

VECTOR INTERRUPT OPTION This board has provisions to provide your system with a vectored interrupt (by strobing one of the vector interrupt lines) when an attempt is made to write into any protected memory The vector interrupt is generated if $\overline{PS}$ goes low while the write strobe signal is present It should be noted that this option is not uniquely associated with the board on which it is implemented and will also generate the vectored interrupt if $\overline{PS}$ is produced by any other board in the system during a write attempt

Your system must be configured so that it can latch this interrupt signal during the write attempt which requires appropriate hardware and software *Unless your system is specifically designed to accomodate this option do not attempt implementation* standard S 100 buss systems do not require implementation of this feature for proper functioning

Vector interrupts Ø 7 correspond to like numbered holes on the circuit board To select the desired vector interrupt simply add a jumper from hole J to the hole associated with the appropriate vector interrupt

OTHER NOTES Tri state outputs are employed so that this memory may also be used with bi directional busses as well as the S 100 buss Also all parts are warranted for 1 year from date of purchase against defects in manufa turing Should any part be defective send it back to us for a free replacement We also maintain a repair service for malfunctioning boards Describe the problem as accurately and completely as possible and return the board to us c/o Repairs Department We strongly recommend insuring the board when you send it back to us

Your comments and feedback enable us to constantly upgrade both our products and out service all letters are welcome and all comments carefully read We hope you enjoy using your ECONORAM IItm

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PARTS LIST ELECTRONIC ITEMS

R1	R2	2 7K resistor (red/violet/red)
C1	C3	39 uF @ 10V tantalum capacitor
C2	C4*	39 uF @ 10V tantalum capacitor
C5	C30**	0 05 uF green disc ceramic capacitor
IC1	IC2	74LS139 dual 2 to 4 line decoder/demult
IC3		74LS125 quad tri state non inverting buffer
IC4		74LS109 dual JK flip flop w/ preset & clear
IC5		74LS00 quad 2 input NAND gate
IC6		74LS74 dual D pos edge triggered flip flop
IC7		74LS32 quad 2 input OR gate
IC8	IC10	81LS95 octal tri state non inverting buffer
IC11		81LS96 octal tri state inverting buffer
IC12		LM340/5T (7805) 5V regulator (TO 220 pack)
IC13*		LM340/5T (7805) 5V regulator (TO 220 pack)
IC14	IC45	2102 L1 1K static low power RAM (450 ns)
IC46	IC77*	2102 L1 1K static low power RAM (450 ns)

*not included in 4K board
**C9 10 15 16 20 21 25, 26 not included in 4K board

PARTS LIST MECHANICAL ITEMS

(2)	Slide switches SPDT
(2)*	DIP switches 8 position
(2)*	Heat sinks #THS 6070
(1)	PC board #114A
(4)	Socket IC 14 pin low profile
(67)**	Socket IC 16 pin low profile
(4)	Socket IC 20 pin low profile
(2)*	Screws 6 32 x 5/16
(2)*	Hex nuts 6 32 X 1/4
(2)*	Lockwashers #6

*(1) included in 4K board
**(35) included in 4K board

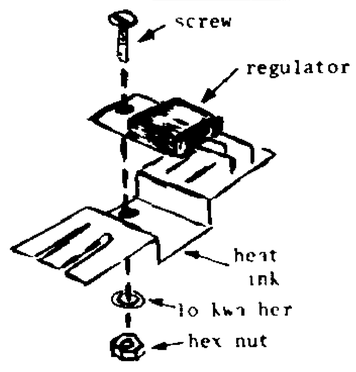

Fig 1 Screw goes through regulator heat sink mounting hole and board and is secured with hex nut and lock washer

TABLE #1

1st 4K	1 + 5
2nd 4K	2 + 5
3rd 4K	3 + 5
4th 4K	4 + 5
5th 4K	1 + 6
6th 4K	+ 6
7th 4K	+ 7
8th 4K	1 + 7
9th 4K	1 +
10th 4K	+
11th 4K	+
12th 4K	4 + 7
13th 4K	1 + 8
14th 4K	+ 8
15th 4K	2 + 8
16th 4K	1 + 8

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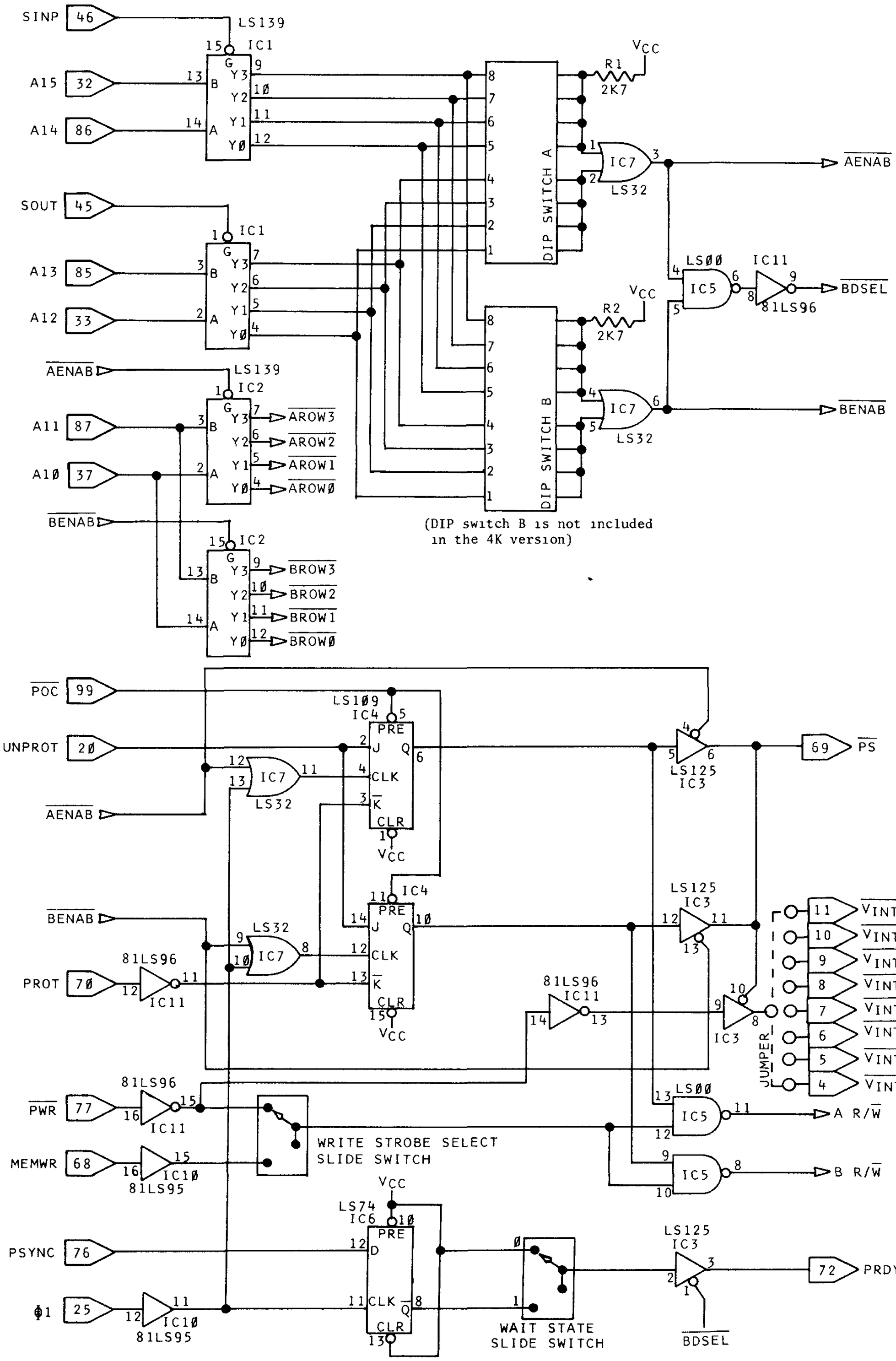
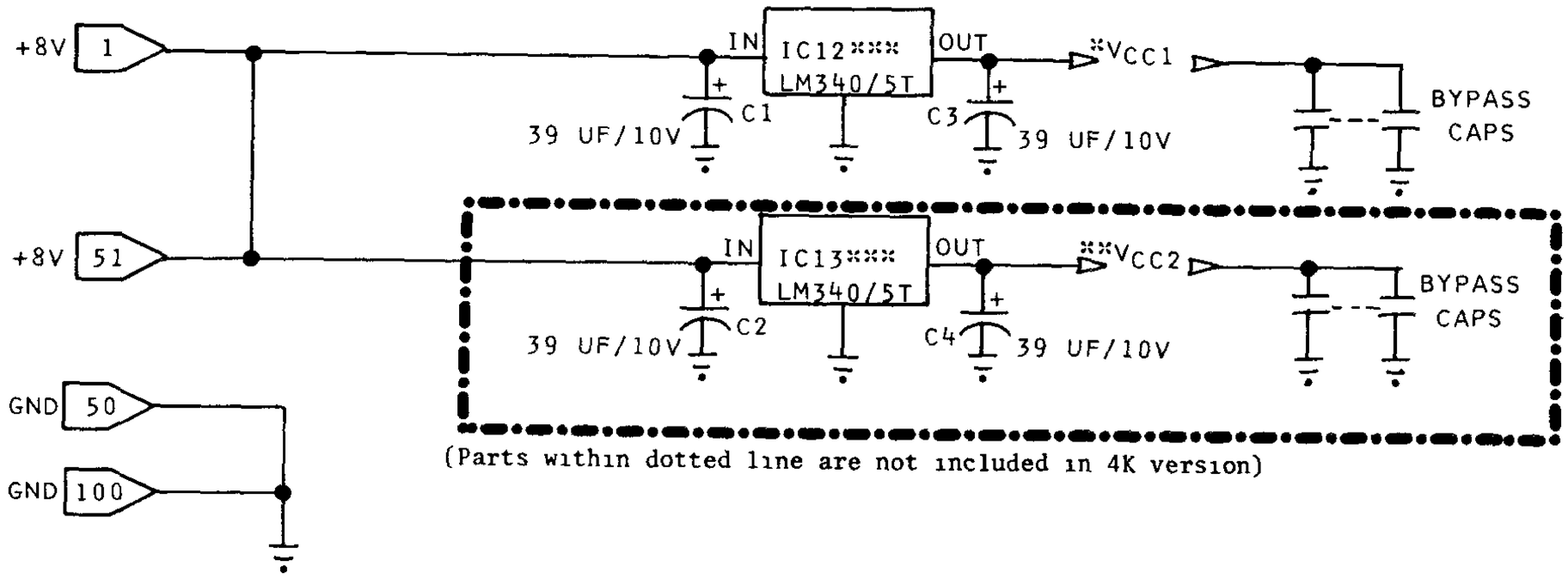
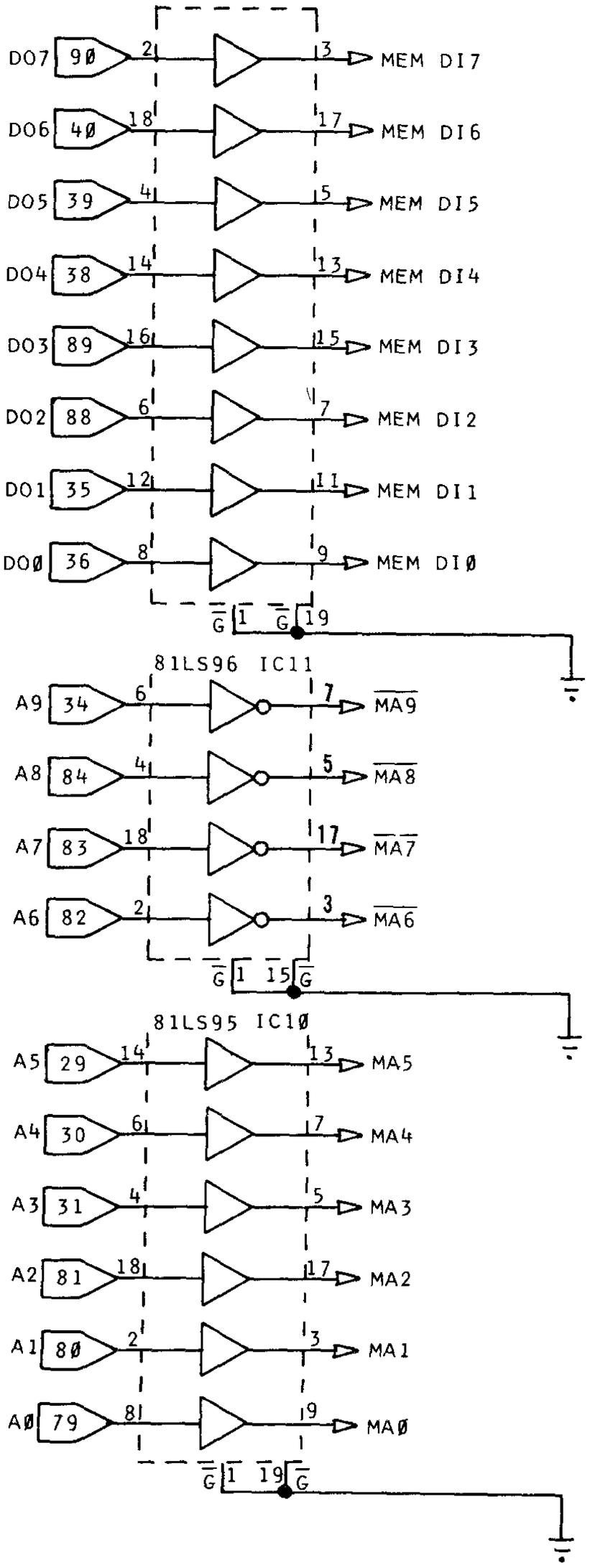
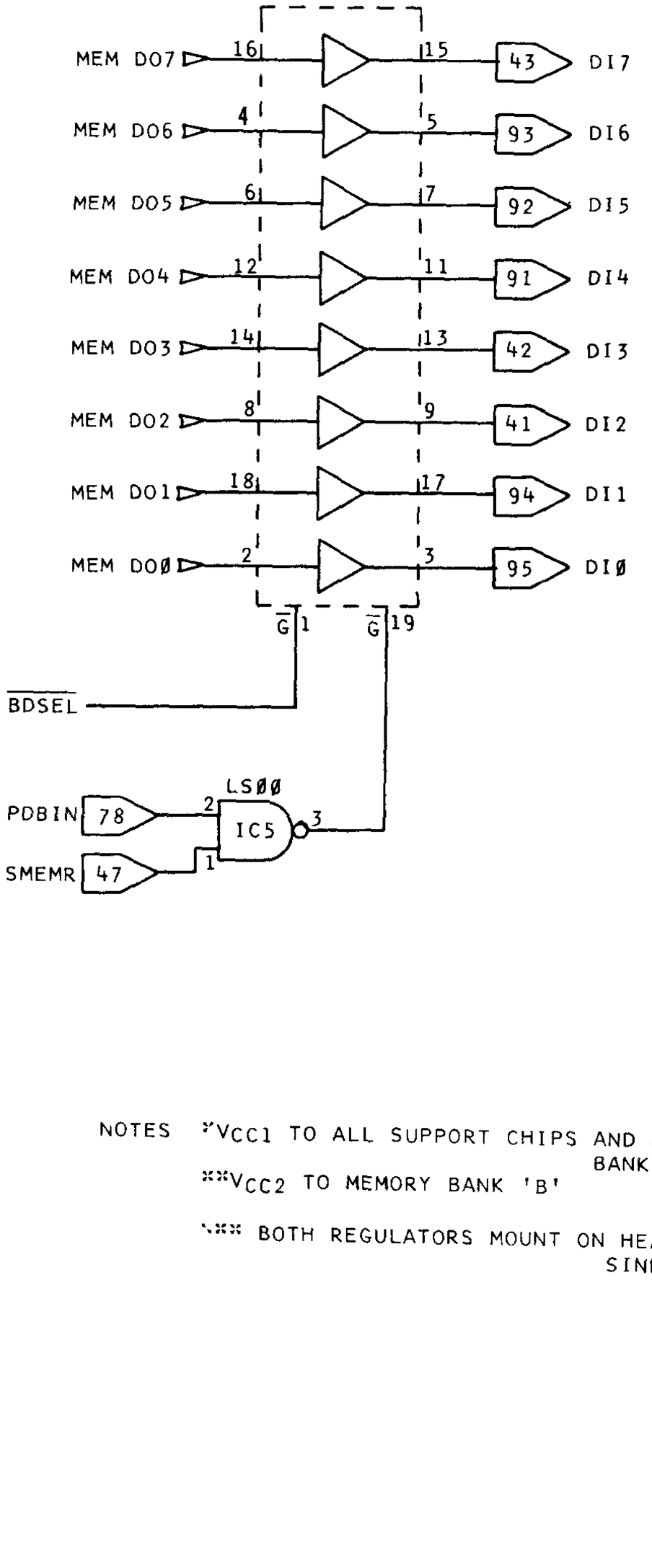
BOX 2355 OAKLAND AIRPORT CA 94614


SINP 46
LS139
15 G
IC1
A15 32
13 B
A14 86
14 A
Y3 9
Y2 10
Y1 11
Y0 12
SOUT 45
1 G
IC1
A13 85
3 B
A12 33
2 A
Y3 7
Y2 6
Y1 5
Y0 4
AENAB
LS139
1 G
IC2
A11 87
3 B
A10 37
2 A
Y3 7 AROW3
Y2 6 AROW2
Y1 5 AROW1
Y0 4 AROW0
BENAB
15 G
IC2
13 B
14 A
Y3 9 BROW3
Y2 10 BROW2
Y1 11 BROW1
Y0 12 BROW0
DIP SWITCH A
DIP SWITCH B
VCC
R1
2K7
R2
2K7
IC7
LS32
AENAB
BENAB
LS00
IC5
IC11
81LS96
BDSEL
(DIP switch B is not included in the 4K version)
POC 99
UNPROT 20
AENAB
LS109
IC4
5 PRE
2 J
Q 6
12
13
IC7
LS32
11
4 CLK
3 K
CLR
1 VCC
IC4
11 PRE
14 J
Q 10
12 CLK
13 K
CLR
15 VCC
LS125
IC3
4
5
6
69 PS
BENAB
9
10
LS32
IC7
8
81LS96
PROT 70
12
11
IC11
81LS96
IC11
14
13
LS125
IC3
12
11
13
10
9
8
IC3
JUMPER
11 VINT7
10 VINT6
9 VINT5
8 VINT4
7 VINT3
6 VINT2
5 VINT1
4 VINT0
81LS96
PWR 77
16
15
IC11
WRITE STROBE SELECT
SLIDE SWITCH
MEMWR 68
16
15
IC10
81LS95
LS00
IC5
13
12
11
A R/W
9
10
8
B R/W
VCC
LS74
IC6
10 PRE
12 D
11 CLK
Q 8
CLR
13
PSYNC 76
Φ1 25
12
11
IC10
81LS95
0
1
WAIT STATE
SLIDE SWITCH
LS125
IC3
2
1
3
72 PRDY
BDSEL



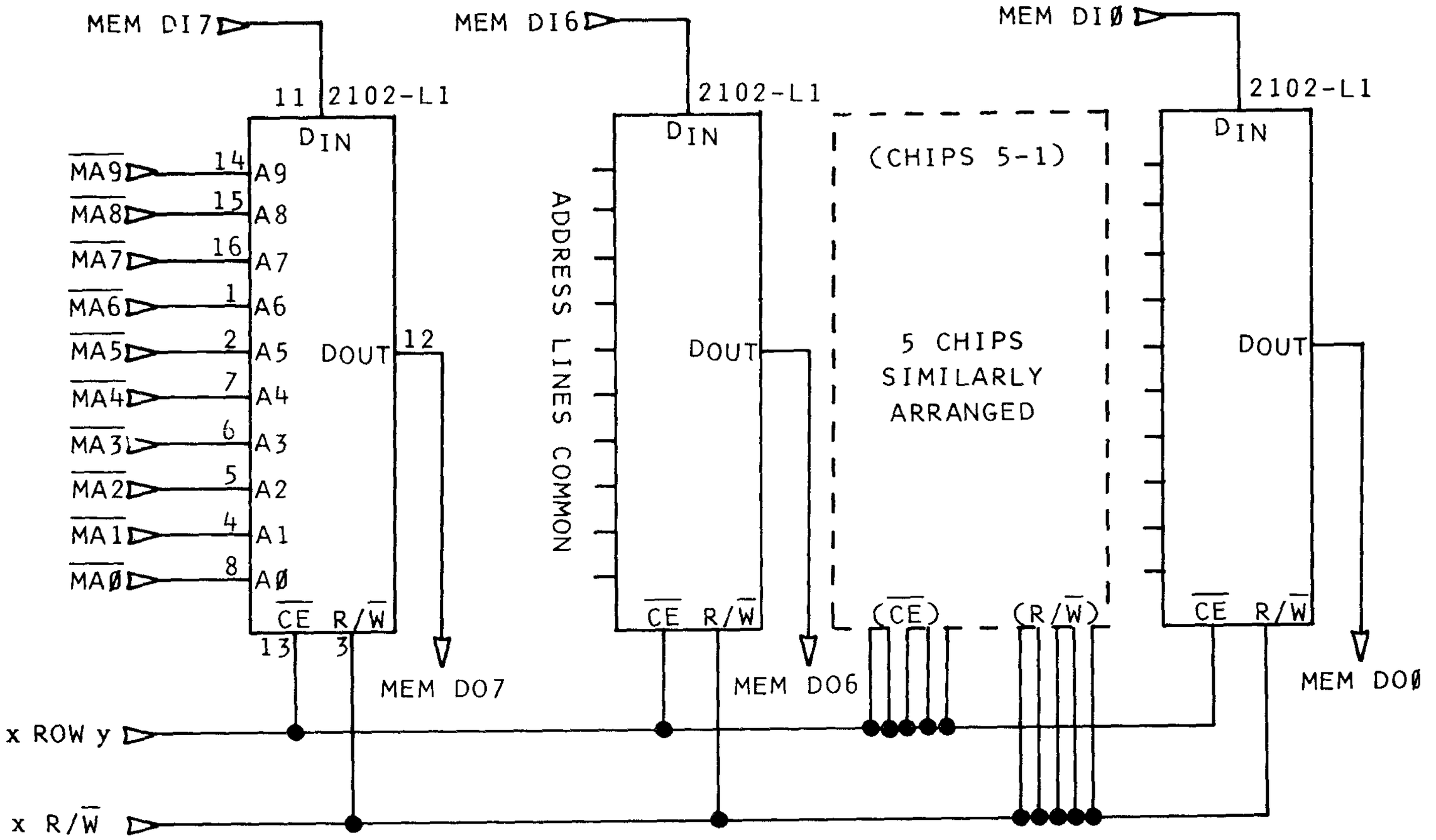


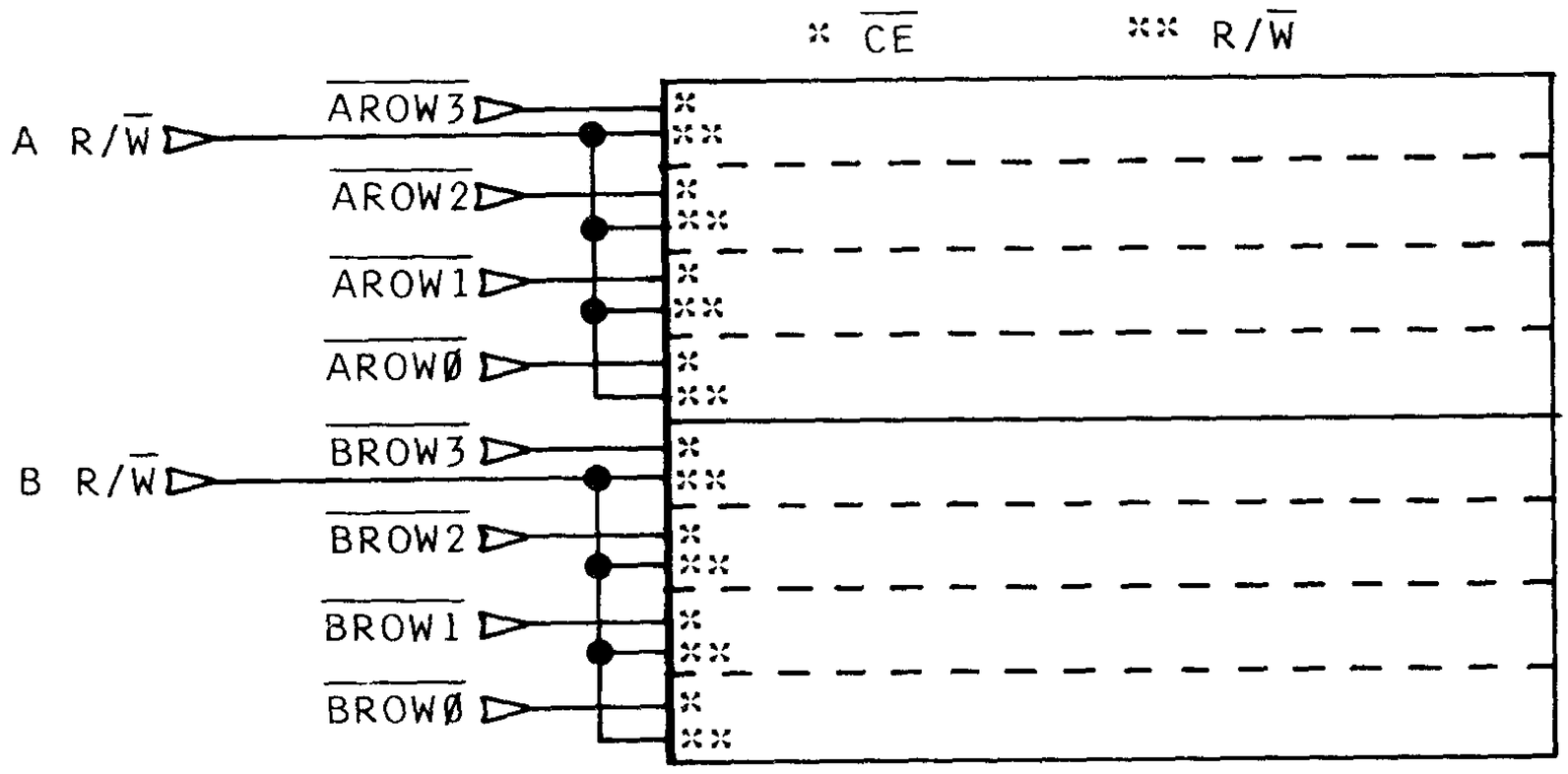


NOTES *VCC1 TO ALL SUPPORT CHIPS AND MEMORY BANK 'A'

**VCC2 TO MEMORY BANK 'B'

*** BOTH REGULATORS MOUNT ON HEAT SINKS

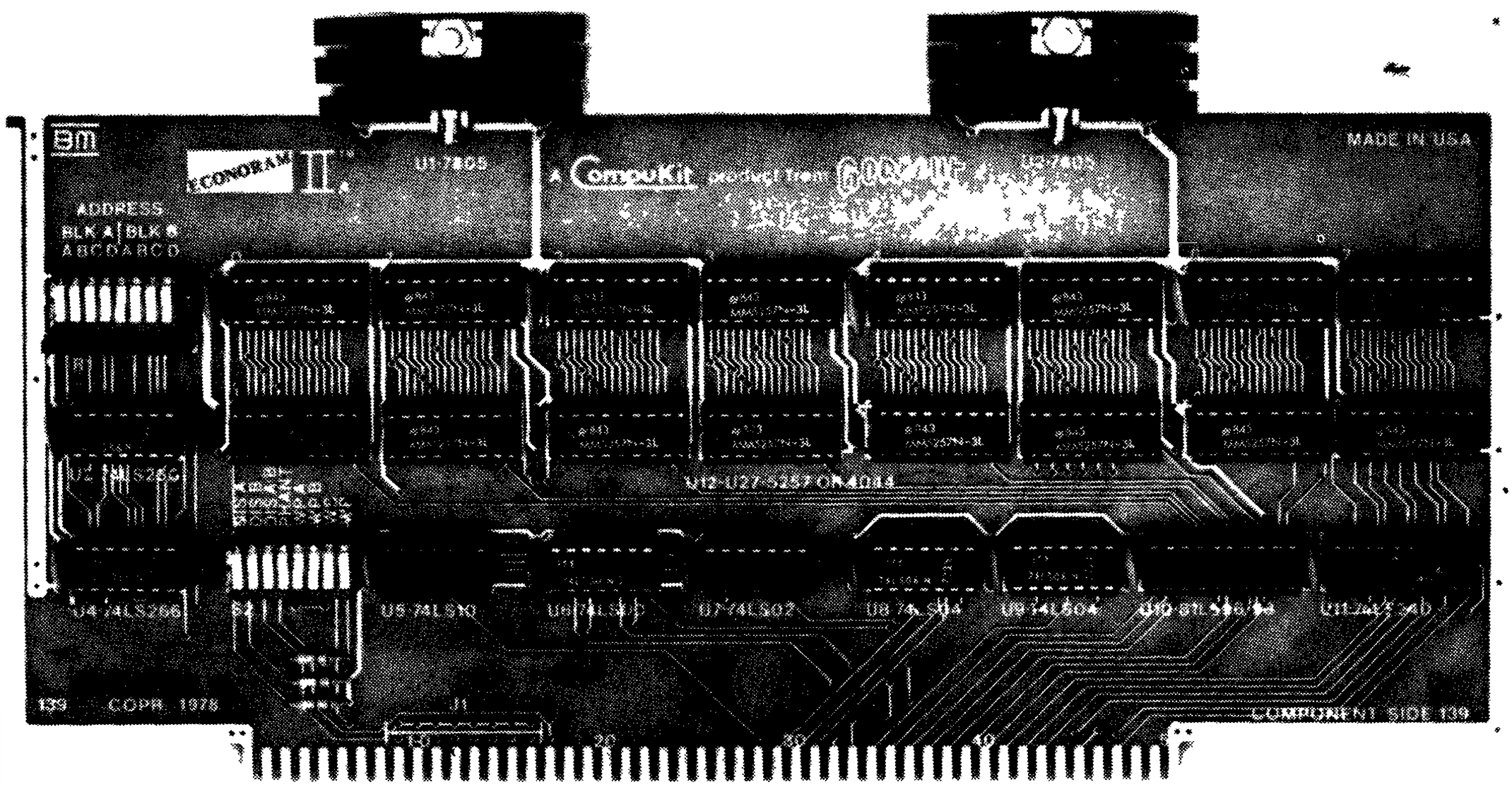




GODBOUT

THANK YOU FOR CHOOSING THIS MEMORY BOARD. MUCH TIME AND EFFORT HAVE GONE INTO MAKING THIS UNIT NOT JUST ANOTHER MEMORY BOARD, BUT ONE WITH A FULL RANGE OF OPTIONS...LIKE THE VECTOR INTERRUPT PROVISION, THE TRI-STATE OUTPUTS, ABILITY TO CONFIGURE AS TWO SEPARATE BLOCKS, AND SO ON. STATIC RAMS AND CONSERVATIVE ENGINEERING CONTRIBUTE TO A BOARD THAT WILL NOT JUST WORK, BUT WORK FOR A LONG TIME IN YOUR SYSTEM. IF WE CAN BE OF ANY HELP TO YOU IN APPLYING THIS BOARD; LET US KNOW.

ECONORAM IIa™
USER'S MANUAL



8K x 8 static memory • S-100
4/5 MHz

139 mac

CompuPro™ from GODBOUT

7/79

ABOUT ECONORAM IIA

Congratulations on your decision to purchase the ECONORAM IIA, an 8K x 8 memory board designed specifically for electrical and mechanical compatibility with the proposed IEEE S-100 buss standard The S-100 buss currently is one of the most popular in the industry and by far the most prolific We believe that this board, with the rest of the S-100 portion of the CompuPro family, is one of the best boards available for that Buss

Features, such as two independent 4K blocks, easy switch assignment of blocks to desired memory address locations, switch selectable BLOCK DISABLE, and WRITE PROTECT, follow the design of the original ECONORAM II

.....

As amateur radio operators have contributed greatly to communication technology, so has the computer hobbyist provided the microcomputer industry with many significant developments In recognition of this fact, we also make this professional quality board available in "UNKIT" form for those who enjoy the challenge of assembling and testing a fine computer board

.....

When you plug in and start using your board, you will discover as thousands of satisfied ECONORAM owners have discovered, the pleasure of using a fine memory board that just works and works and works

As the first company to nationally offer memory kits to computer hobbyists, we thank you for choosing a CompuPro product welcome to the club

TECHNICAL OVERVIEW

This board incorporates proven static memory technology using industrial design techniques and generous safety factors to insure extremely reliable operation.

Of the two currently popular approaches to memory design - static and dynamic - static memories are the overwhelming choice in applications where speed, simplicity, ease of use, and reliability must be considered.

In order to retain data, dynamic memory must be continually refreshed This board, due to its static design, will retain data as long as power is applied This is of particular interest to those who will be using this board in systems where DMA operations are involved, as the static memory requires no refresh and therefore there is never a conflict between the DMA device and the CPU attempting to refresh memory

The individual memory chips used on this board are grouped together to form two 4K blocks of memory Each of these 4K blocks is individually addressable on any 4K boundary The starting addresses of each block may be set by DIP switches on the board

Additional features include WRITE PROTECT for each 4K block, a DISABLE feature for each 4K block, plus a switch to provide for totally disabling the entire board PHANTOM is provided on this board and is DIP switch selectable Provision is also made for operating this board in systems that do not generate the MWRITE signal It can be operated using $\overline{PWR}$ alone or $\overline{PWR}$ in conjunction with the MWRITE signal

The ECONORAM IIA also includes provision for incorporating this board in systems using memory management without modification to the board

Extra heavy duty power supply traces, generous bypassing of supply lines, sockets for all integrated circuits, careful layout, and a double-sided, solder-masked printed circuit board with complete component and switch legends make this a versatile memory board which will give exceptionally long and trouble-free service

Parts List

☐ (1) ECONORAM IIA circuit board

INTEGRATED CIRCUITS (Note The following parts may have letter suffixes and prefixes along with the key numbers given below)

☐ (16) MM5257-3L or TMS40L44 4K memories (U12-U27)
☐ (1) 74LS00 quad 2-input NAND (U6)
☐ (1) 74LS02 quad 2-input NOR (U7)
☐ (2) 74LS04 hex inverters (U8, U9)
☐ (1) 74LS10 triple 3-input NAND (U5)
☐ (1) 74LS240 TRI-STATE* buffer (U11)
☐ (2) 74LS266 quad exclusive NOR o c (U3, U4)
☐ (2) 7805 5 volt regulators (U1, U2)
☐ (1) 81LS96/98 octal buffer (U10?)

OTHER ELECTRICAL COMPONENTS

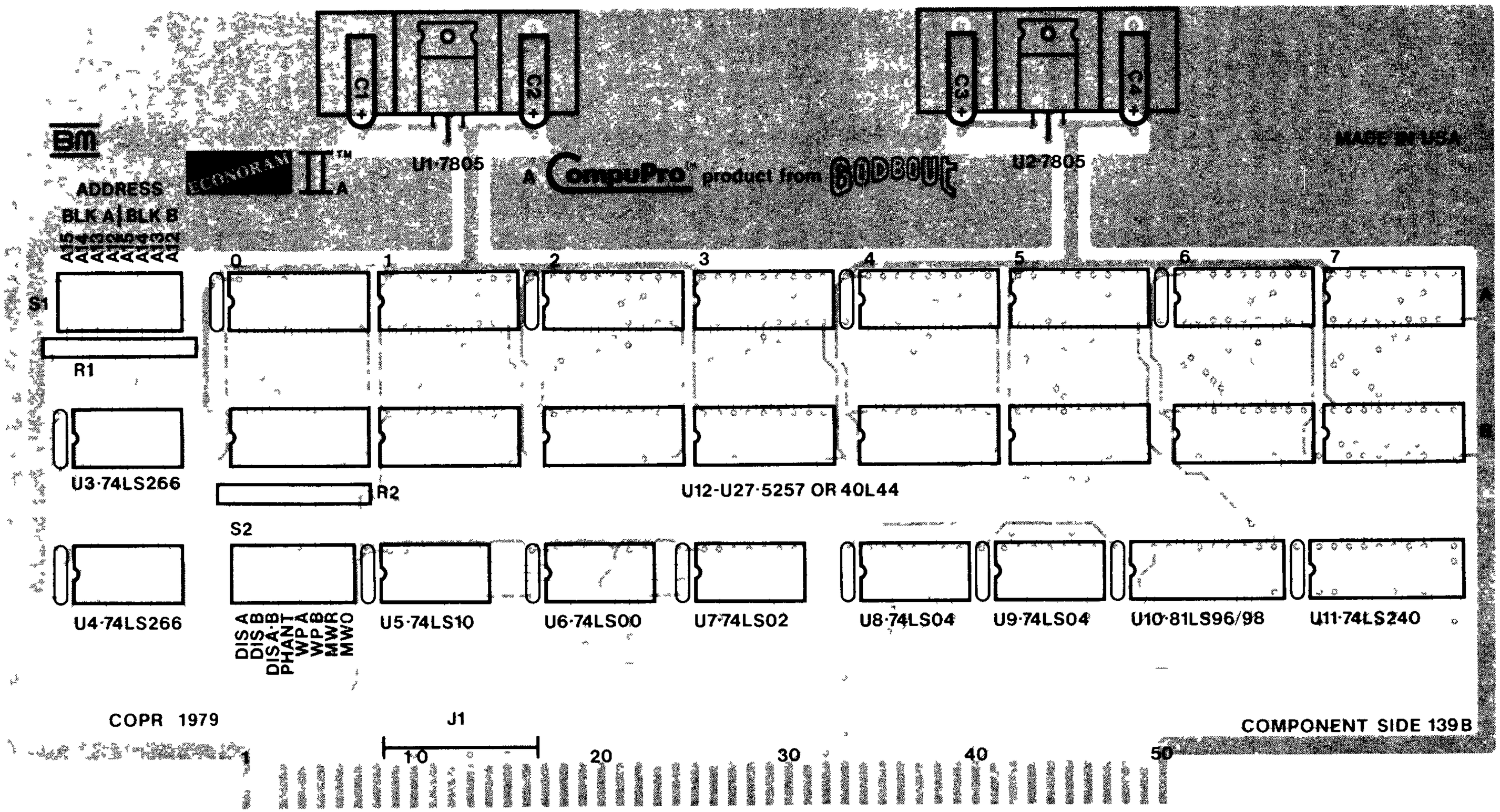
☐ (2) S I P resistor packs (R1, R2)**
☐ (13) ceramic bypass capacitors**
☐ (4) 38 uF tantalum capacitors

MECHANICAL COMPONENTS

☐ (25) DIP sockets**
☐ (2) 8-pole DIP switches (S1, S2)**
☐ (2) heat sinks for regulatory ICs
☐ (2) 6-32 bolts
☐ (2) 6-32 lock washers
☐ (2) 6-32 nuts
☐ (1) user manual

* TRI-STATE is a trademark of National Semiconductor Corp

** Supplied soldered to board in "Unkit" version



Component Layout

UP

MEMORY ADDRESS ASSIGNMENT

This board is configured as two 4K blocks Each 4K block may be assigned to any area of memory beginning on a 4K boundary (0K, 4K, 8K, 56K, etc) The only limitation is that the assigned locations should not overlap each other or any other RAM in your system

NOTE S1 is located in the upper-left portion of the board It has eight individual switch sections number 1 through 8 In the table below, a "0" = switch OFF, and "1" = switch ON

STARTING ADDRESS			SWITCH POSITION
			BLOCK A, B
hex		(split octal)	4K
			A S1- 1234
			B S1-.5678
0K	0000	(000/000)	0000
4K	1000	(020/000)	0001
8K	2000	(040/000)	0010
12K	3000	(060/000)	0011
16K	4000	(100/000)	0100
20K	5000	(120/000)	0101
24K	6000	(140/000)	0110
28K	7000	(160/000)	0111
32K	8000	(200/000)	1000
36K	9000	(220/000)	1001
40K	A000	(240/000)	1010
44K	B000	(260/000)	1011
48K	C000	(300/000)	1100
52K	D000	(320/000)	1101
56K	E000	(340/000)	1110
60K	F000	(360/000)	1111

NOTE If the desired starting address is represented as a binary number, the switch setting represents the 4 most significant bits of that address Once you become familiar with the addresses of the various boundaries, you will find it easy to re-assign various boundaries, you will find it easy to re-assign memory blocks without referring to the above table

BLOCK DISABLE SWITCHES

Switch 2, positions 1, 2, and 3, provide DISABLE functions. S2-1, when turned to the ON position, disables the A block, or one 4K block of the board, rendering it transparent, that is, totally invisible to the buss You can neither write in it nor read from it so that the board would appear to the buss as merely a 4K block of memory

S2-2 provides a similar function for block B

S2-3 is a master disable switch which will render the entire board transparent, that is, both blocks A and B

WRITE PROTECT/ENABLE SWITCHES

Switch 2, positions 5 and 6, provides a WRITE PROTECT feature, that is, in normal operations, both of these switches are ON and they ENABLE the WRITE signal to blocks A and B of the board

In certain operations, you may want to use a portion of this RAM as if it were READ ONLY MEMORY (ROM), that is, memory that you can READ from, but not WRITE into, once you've stored in it S2-5, when it's turned to the OFF position, disables the MEMORY WRITE for block A S2-6 in the OFF position will disable MEMORY WRITE for block B

Whenever you want to write into these blocks, the respective switches should be in the ON position

WRITE STROBE SELECT SWITCHES

S2-7 and -8 select the use or non-use of the S-100 buss signal MWRITE (pin 68). This signal is normally produced by a front panel and is not available in some front panel-less machines Other CPU boards do implement this signal If MWRITE is present in your machine, turn Switch 2-7 ON and S2-8 OFF

If the MWRITE signal is not used in your system, turn S2-7 OFF and S2-8 ON

PLEASE NOTE When S2-8 is in the ON position, and S2-7 is in the ON position, buss line 68 will be grounded.

PHANTOM LINE

In response to increasing number of users who have requested inclusion of PHANTOM line, this board includes the PHANTOM feature PHANTOM is an active low signal The feature may be enabled on this board by placing S2-4 in the ON position

CAUTION

Some manufacturers use the PHANTOM line (buss pin 67) for a REFRESH signal This will conflict with the PHANTOM feature and cause board with PHANTOM on, to fail If your system has this conflict, it must be resolved by either eliminating the REFRESH signal on the CPU board, or by turning the PHANTOM feature (S2-4) OFF

If you want the PHANTOM feature, the conflicting REFRESH signal may be eliminated, if it's not used elsewhere in the system, by cutting the trace connected to buss pin 67 on your CPU board Be sure of your system configuration before cutting any traces

MEMORY TESTING

If the memory board seems to be working properly, the Memory Testing Routine (figure 1) can be used to give the board a more thorough workout It is rather slow, but will do the job well It can be entered via editor/assembler or front panel switches

The routine is set up to test 8K from 4000 hex up to 6000 hex This may be changed by entering a different starting address at "STRT" (3001 - 3002) and/or a different end address at "END" (3004 - high order byte only)

If the memory passes the test it starts over again You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart

If the memory fails the test, critical information is stored and the routine enters a software "HALT", that is a "jump to here" at "SHLT" Front panel lights, if any, will show this state The user may then use the front panel or dump routines to display the following stored failure info

3069* "FDE" = D, E pair D is the fill character and E is the test character
306B* "FHL" = H, L pair . the failure address
306D* "FOUT" = the data expected at this address
306E* "FIN" = the data read from, the address
* address from *Memory Testing Routine Listing*

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine

The difference between "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem

This test will find most of the harder to distinguish errors

MEMORY TESTING ROUTINE

```
3000 21 00 40           0010 STRT LXI  H,4000H
3003 3E A0              0020 END  MVI  A,0A0H
3005 32 6E 30           0030      STA  FIN
3008 3E 10              0040      MVI  A,10H
300A 84                 0050      ADD  H
300B 4F                 0060      MOV  C,A
300C 16 00              0070      MVI  D,0
300E 1E FF              0080      MVI  E,0FFH
3010 22 65 30           0090 DONE SHLD STAD
3013 AF                 0100      XRA  A
3014 47                 0110      MOV  B,A
3015 7B                 0120 SCND MOV  A,E
3016 5A                 0130      MOV  E,D
3017 57                 0140      MOV  D,A
3018 79                 0150      MOV  A,C
3019 2A 65 30           0160      LHLD STAD
301C 72                 0170 FILL MOV  M,D
301D 23                 0180      INX  H
301E BC                 0190      CMP  H
301F C2 1C 30           0200      JNZ  FILL
3022 2A 65 30           0210      LHLD STAD
3025 73                 0220 NEXT MOV  M,E
3026 7B                 0230      MOV  A,E
3027 BE                 0240      CMP  M
3028 C2 6F 30           0250      JNZ  FAIL'
302B 79                 0260      MOV  A,C
302C 23                 0270      INX  H
302D 94                 0280      SUB  H
302E C2 4D 30           0290      JNZ  NDON
3031 B8                 0300      CMP  B
3032 44                 0310      MOV  B,H
3033 CA 15 30           0320      JZ   SCND
3036 3A 66 30           0325      LDA  STAD+1
3039 00                 0330 MARK NOP
303A 00                 0331      NOP
303B 00                 0332      NOP
303C 3A 6E 30           0340      LDA  FIN
303F B9                 0350      CMP  C
3040 CA 00 30           0360      JZ   STRT
3043 79                 0370      MOV  A,C
3044 67                 0380      MOV  H,A
3045 2E 00              0390      MVI  L,0
3047 C6 10              0400      ADI  10H
3049 4F                 0410      MOV  C,A
304A C3 10 30           0420      JMP   DONE
304D 22 67 30           0430 NDON SHLD NXAD
3050 7A                 0440 LOPB MOV  A,D
3051 BE                 0450 LOPA CMP  M
3052 C2 6F 30           0460      JNZ  FAIL
3055 2C                 0470      INR  L
3056 C2 51 30           0480      JNZ  LOPA
3059 79                 0490      MOV  A,C
305A 24                 0500      INR  H
305B BC                 0510      CMP  H
305C C2 50 30           0520      JNZ  LOPB
305F 2A 67 30           0530      LHLD NXAD
3062 C3 25 30           0540      JMP  NEXT
3065                    0550 STAD DS   2
3067                    0560 NXAD DS   2
3069                    0570 FDE  DS   2
306B                    0580 FHL  DS   2
306D                    0590 FOUT DS   1
306E                    0600 FIN  DS   1
306F 22 6B 30           0610 FAIL SHLD FHL
3072 32 6D 30           0620      STA  FOUT
3075 7E                 0630      MOV  A,M
3076 32 6E 30           0640      STA  FIN
3079 EB                 0650      XCHG
307A 22 69 30           0660      SHLD FDE
307D C3 7D 30           0670 SHLT JMP SHLT
3080                    0680 *
```

CIRCUIT DESCRIPTION

The heart of ECONORAM IIA is the MM5257N-3L-/TMS40L44-25 static memory IC (RAM), which can store 4096 single bits of information, thus, each is a 4K x 1 memory IC Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts

These ICs are arranged in rows that are 8 ICs wide This way, each row can store 4K x 8 bits of information Paralleling 4 of these rows together produces a total memory storage of 16K x 8 bits (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array)

Now that we have this storage, there are still other aspects we must consider First, we need to address a specific location in memory, and, we need to be able to *write* data into the memory, or *read* data from the memory

The schematics on pages 8 and 9 show the address circuitry along with the other Econoram IIA circuitry Each memory IC requires 12 address bits (A0-A11) to access any one of the 4096 bits available in the IC These address bits are generated by the CPU and are buffered by a number of inverters After buffering, a particular address is presented to all IC address selection pins However, we additionally need to select which particular row of ICs is to react to the given address This requires 4 more address bits (A12-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array)

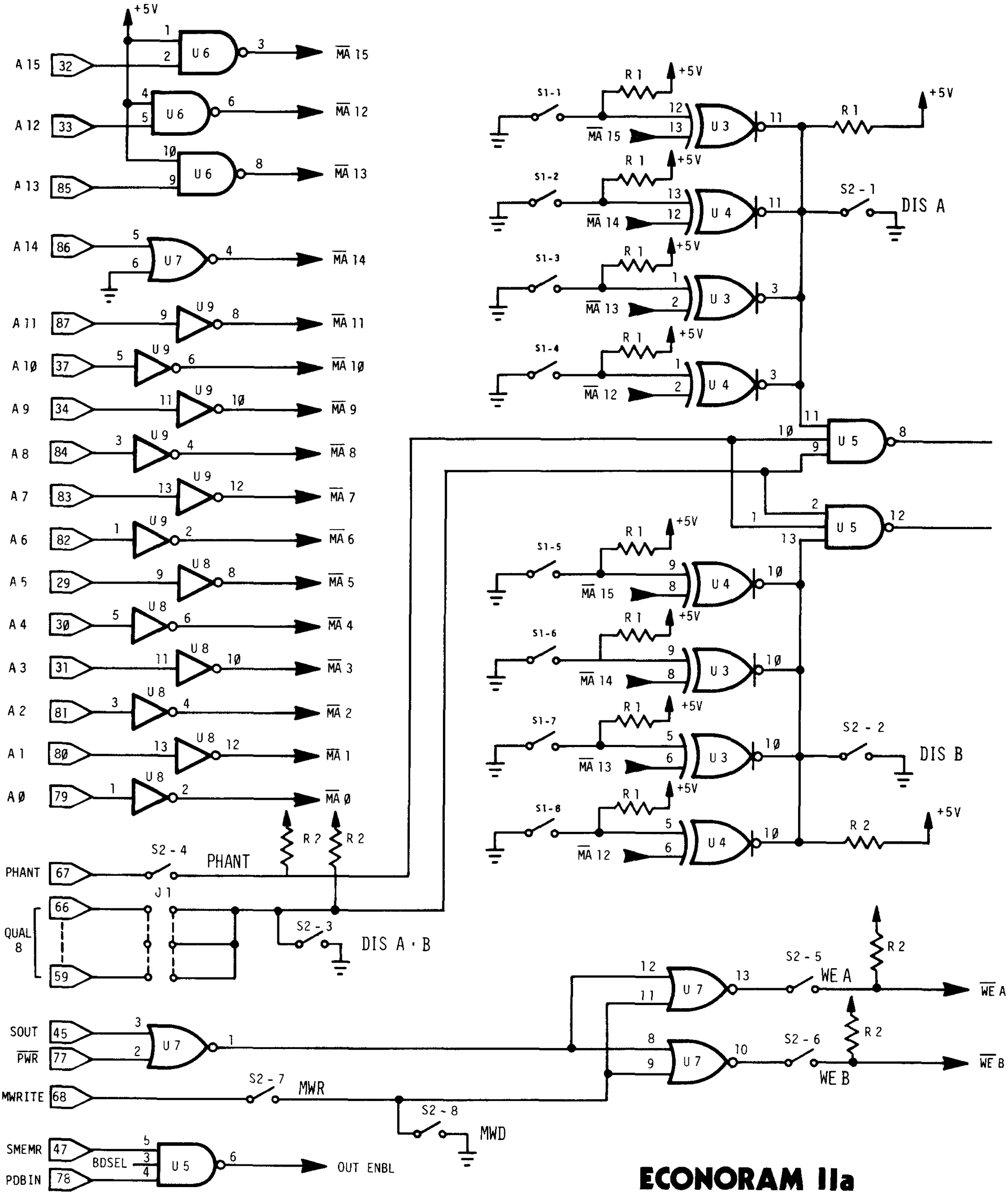
When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss) Data to be read on to the data buss from memory passes through 8 TRI-STATE® inverting buss drivers, when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines If these transients work their way into the logic circuitry, problems can appear To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC

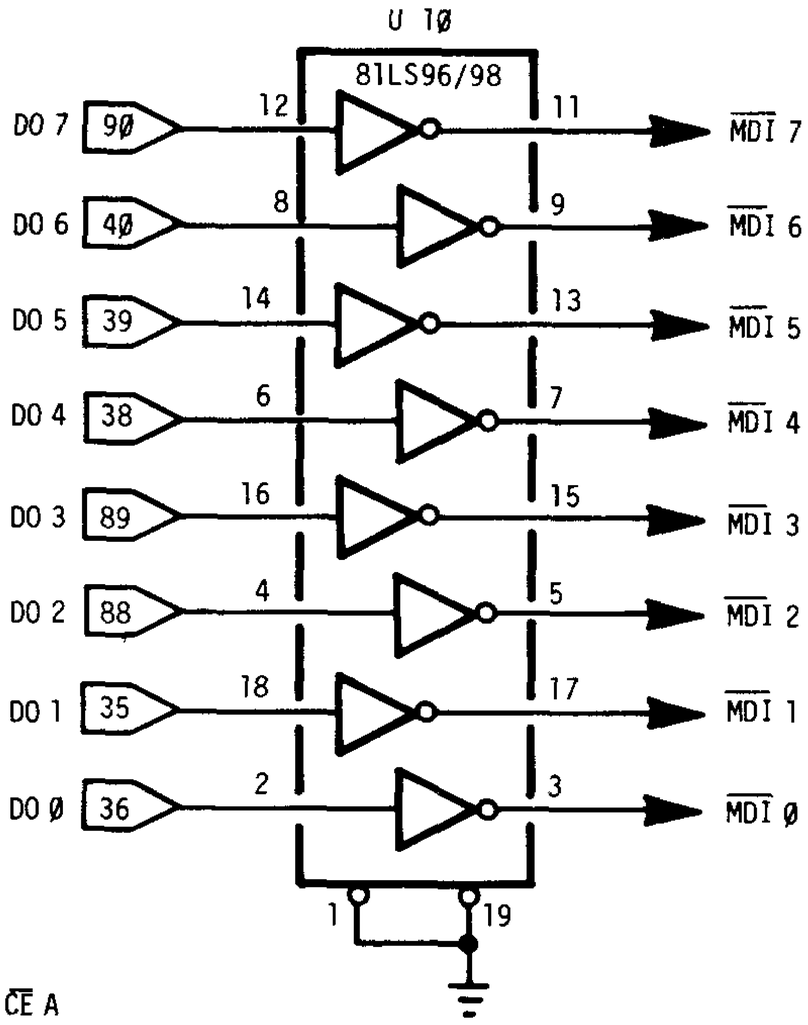
This board is guaranteed to operate at 4 MHz* over the full temperature range (0-70°C ambient) and to draw less than 1000 mA (1 amp)

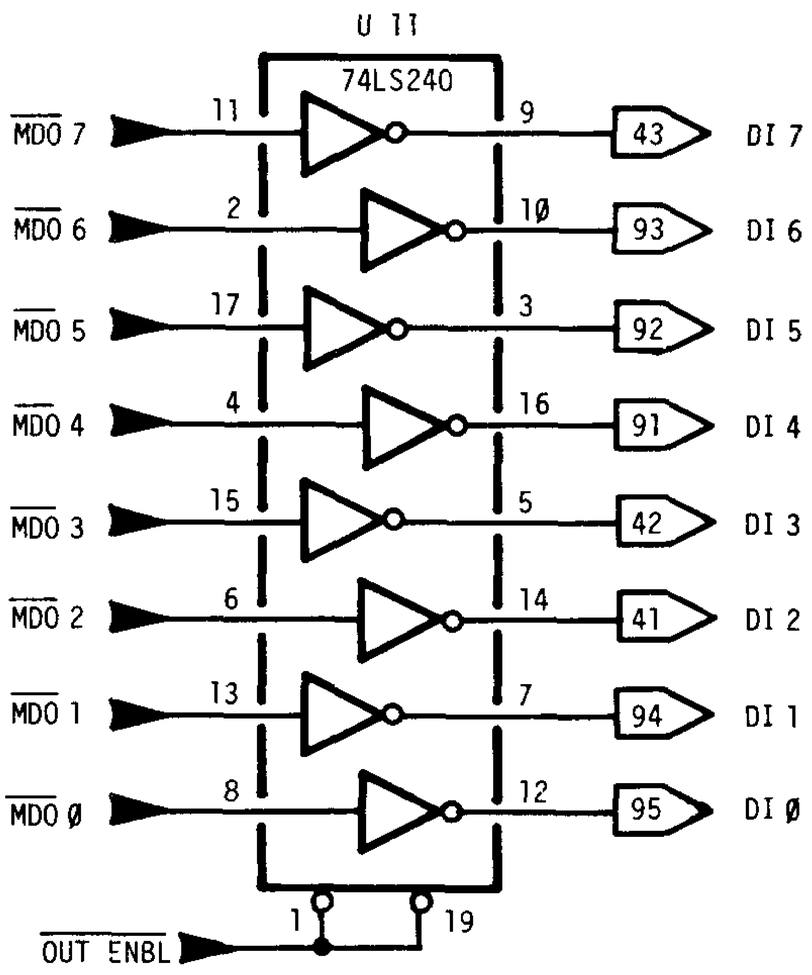
It is interesting to note that static RAM technology has progressed to the point that this high performance static RAM board is comparable in cost and power consumption to dynamic memory boards

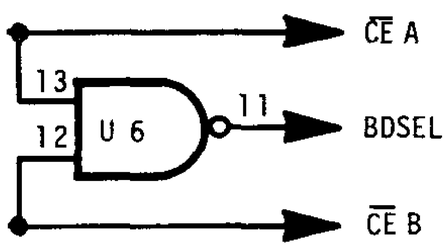
* 5 MHz with 8085 CPU

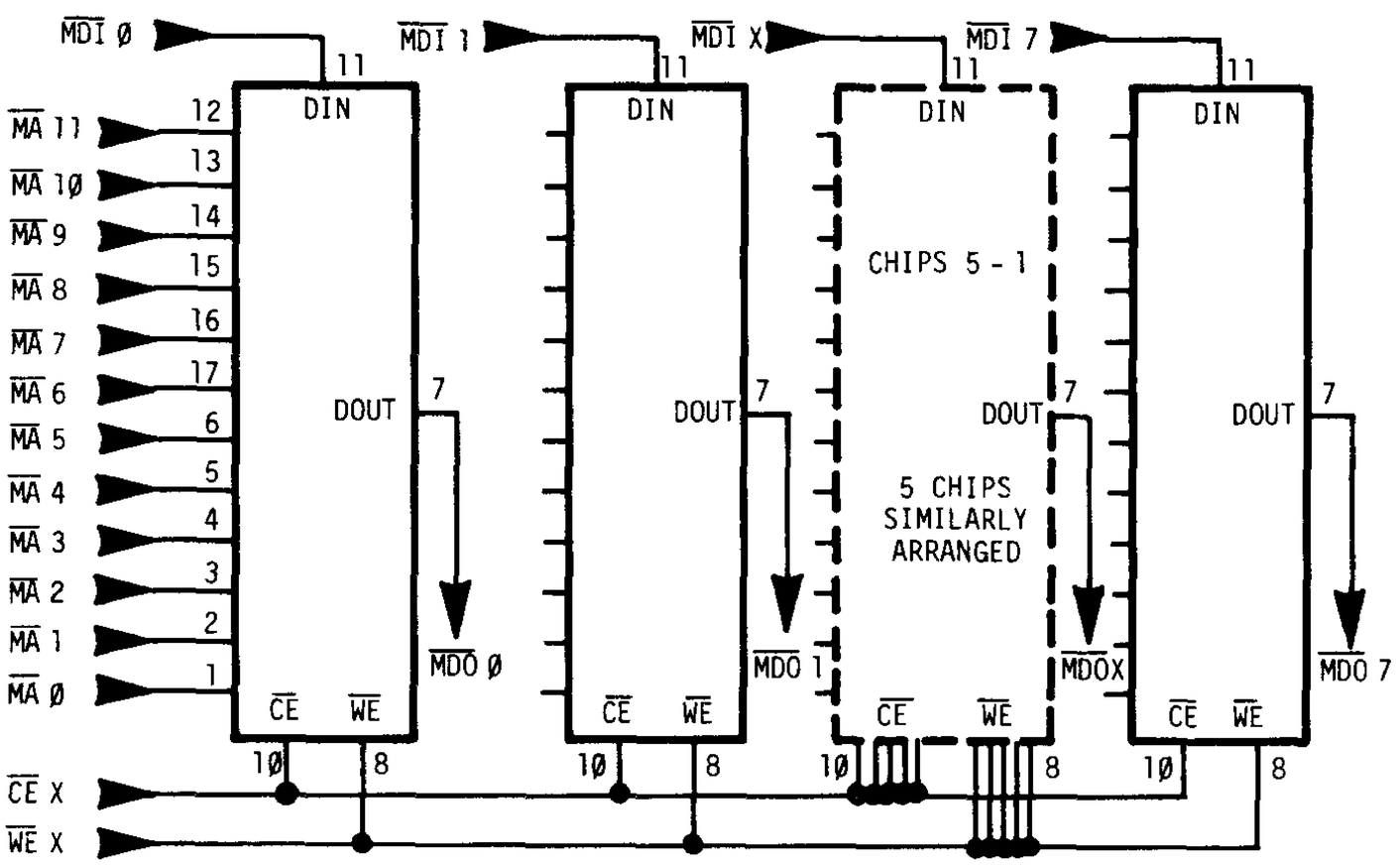


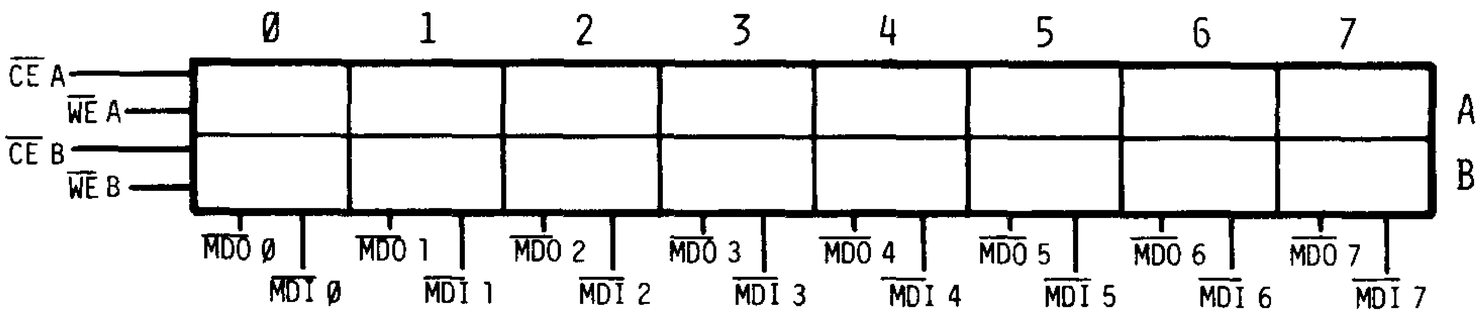
ECONORAM IIa


U 10
81LS96/98
DO 7
90
DO 6
40
DO 5
39
DO 4
38
DO 3
89
DO 2
88
DO 1
35
DO Ø
36
MDI 7
MDI 6
MDI 5
MDI 4
MDI 3
MDI 2
MDI 1
MDI Ø


U 11
74LS240
MDO 7
MDO 6
MDO 5
MDO 4
MDO 3
MDO 2
MDO 1
MDO Ø
OUT ENBL
43
93
92
91
42
41
94
95
DI 7
DI 6
DI 5
DI 4
DI 3
DI 2
DI 1
DI Ø


U 6
CE A
BDSEL
CE B


MDI Ø
MDI 1
MDI X
MDI 7
DIN
DOUT
MA 11
MA 10
MA 9
MA 8
MA 7
MA 6
MA 5
MA 4
MA 3
MA 2
MA 1
MA Ø
CE
WE
MDO Ø
MDO 1
MDOX
MDO 7
CHIPS 5 - 1
5 CHIPS
SIMILARLY
ARRANGED
CE X
WE X


0
1
2
3
4
5
6
7
CE A
WE A
CE B
WE B
A
B
MDO Ø
MDO 1
MDO 2
MDO 3
MDO 4
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MDO 7
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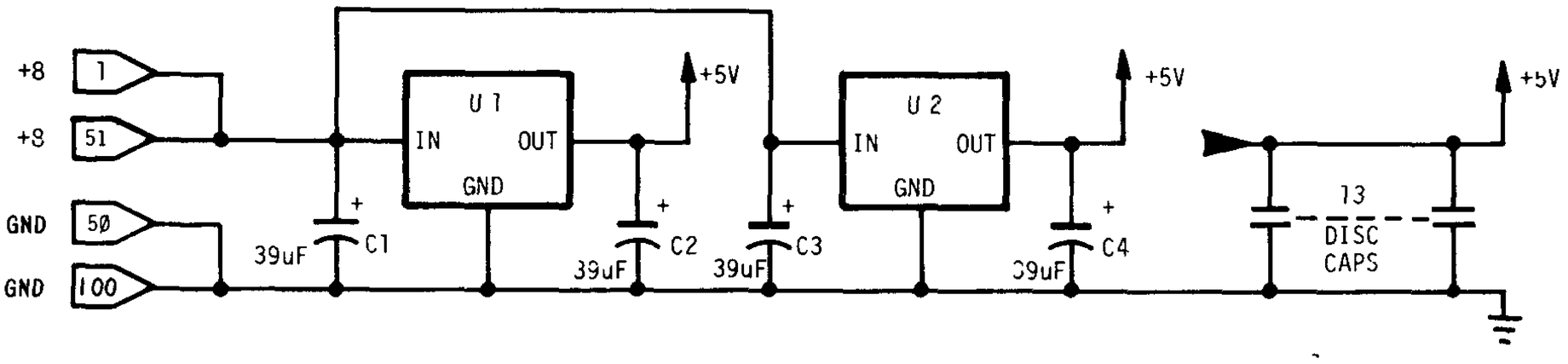
MDI 4
MDI 5
MDI 6
MDI 7


+8
+8
GND
GND
1
51
50
100
U 1
U 2
IN
OUT
GND
+5V
39uF
C1
C2
C3
C4
13
DISC
CAPS

reverse order returns control of the bus to the Host Processor. A bus limited to one temporary master needs only control transfer logic.

The IEEE 696/S100 bus provides for a permanent master/Host Processor and up to 16 temporary masters on the same bus. The S100 DMA priority and bus arbitration protocol prevents contention between two or more temporary masters. DMA0* through DMA3* are the four lines which carry the priority information which controls the arbitration process. All temporary masters requesting a bus grant continuously sample the four DMA priority lines in parallel. Dot OR-ing active low priority outputs on the bus permits each requestor to simultaneously sample the bus and assert its priority. When disagreement occurs at any position the temporary master with lower priority disables all its less significant output bits. Temporary masters may assert their priorities and HOLD* request only when HOLD* and pHLDA are not asserted on the bus. Bus control is always given to the first requestor without regard to priority. The arbitration protocol comes into play only when more than one temporary master requests bus control. Arbitration logic on all temporary masters must be fast enough to insure completion of arbitration and bus settling time within the shortest period that can occur between assertion of Hold* and the response pHLDA.

7. VECTORED INTERRUPTS

8 Lines VI0 through VI7

IEEE 696 provides an eight level vectored interrupt system. Interrupts provide the the means for a bus slave or peripheral device to obtain the services of a bus master in such a fashion that the master can return to the task which was in progress when service was requested. An interrupt controller slave may be included on the permanent bus master or on a separate bus slave. INT*, the general interrupt line, is used for communication between the interrupt controller and any master. Interrupt controllers vary all the way from single chips to entire front end processors.

Regardless of type, only one interrupt controller may exist on the bus. If additional controllers are required they must be either daisy chained or operate in a polled mode. A sINTA cycle acknowledges receipt of an interrupt request, INT*, however, a vectored interrupt may occur and be serviced by an interrupt controller without the assertion of INT*. Interrupt controllers need not assert INT*.

8. UTILITIES 25 lines

The system utilities are ordered essentially as they appear in IEEE 696, however, some headings are relocated in the interest of clarity.

A. System clock, phi, provides control timing for all bus cycles. It is always generated by the host processor. In cases where there are more than one MPU on the host processor the clock may be transferred when MPU's are transferred. This transfer must be synchronous and glitch free.

B. Clock is an asynchronous 2 MHz +/- 0.5 percent signal. It is intended for use by timers, baud rate generators, etc.

C. Reset Functions 3 Lines

1. RESET* resets all bus masters.

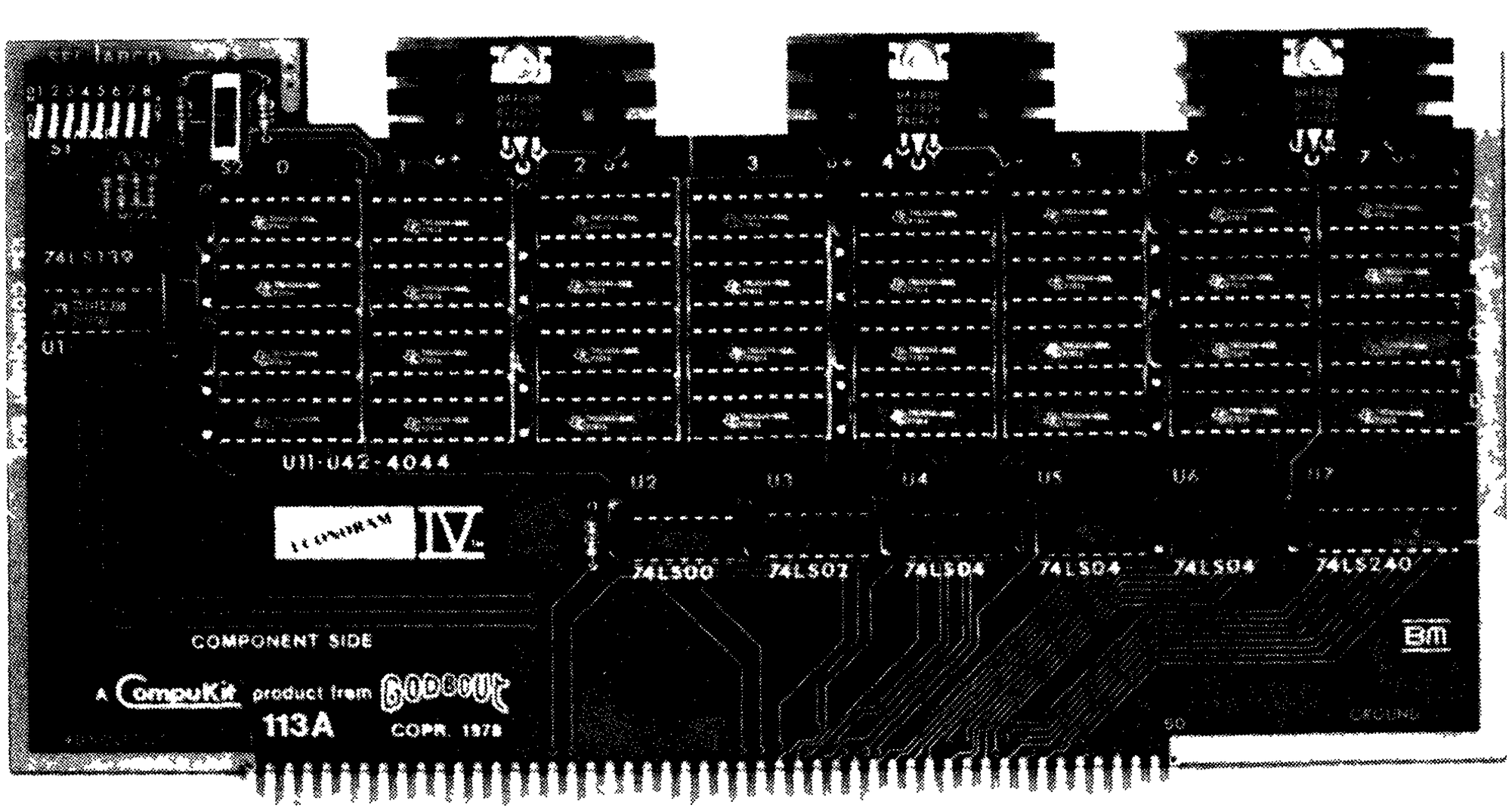
2. SLAVE CLR*, SLAVE CLeaR, resets all bus slaves.

3. POC*, power on clear, is asserted only during power up and forces assertion of both RESET* and SLAVE CLR*. Reset and slave clr are open collector lines.

D. MWRT, Memory WRiTe strobe, is the signal which provides the timing for memory write operations. MWRT must be generated at only on point in a system. The host processor is the preferred location for this generator. MWRT = pWR . -sOUT. Care must be exercised in generating MWRT so that the strobe has minimum delay from PWR*.

CONTINUED ON PAGE 42

ECONORAM IV™
USER'S MANUAL



16K x 8 static memory • S-100
using TMS40L44/MM5257 • 4MHz

113 mac

A CompuKit™ product from GODBOUT

Rev 3/79

ABOUT ECONORAM IV

Congratulations on your decision to purchase ECONORAM IV, a 16K x 8 memory board designed specifically for electrical and mechanical compatibility with the S-100 buss standard The S-100 buss currently is one of the most popular in the industry and by far the most prolific, we believe this board, with the rest of the S-100 portion of the ECONORAM family, is one of the best memory boards available for that buss

We recommend that the parts in this kit be checked against the parts list for completeness and that these instructions be read through carefully before starting Completion of the assembly should take from one to four hours, depending on previous assembly experience, and upon completion, you will discover -- as thousands of satisfied ECONORAM owners have discovered -- the pleasure of using a fine memory board that just works, and works, and works

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing ECONORAM IV welcome to the club

TECHNICAL OVERVIEW

This board incorporates proven static memory technology There are currently two popular types of memory being used in products such as this static and dynamic Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered there is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement

The individual memory ICs used on this board are grouped together to form a single 16K x 8 block of memory, addressable on any 16K boundary using the on-board dip switch (no jumpers required) Additional features include write protect switches for each 4K sector of the 16K block, a write strobe selection switch which allows use of memory in systems with or without a front panel (MWRITE strobe), allowance for use with or without the PHANTOM line, thorough capacitor bypassing of supply lines to suppress transients, plus on-board regulation and heat-sinking for reliably cool operation All this and sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend

Parts List

Upon receipt of your kit, check your parts against the list below

- ☐ (1) Econoram IV circuit board

INTEGRATED CIRCUITS (note the following parts may have letter suffixes and prefixes along with the key numbers given below)

- ☐ (32) TMS4044 or MM5257N-3L memories (U11 - U42)
- ☐ (1) 74LS00 nand gate (U2)
- ☐ (1) 74LS02 nor gate (U3)
- ☐ (3) 74LS04 hex inverters (U4 - U6)
- ☐ (1) 74LS240 TRI-STATE® inverters (U7)
- ☐ (1) 74LS139 dual 1 of 4 decoder (U1)
- ☐ (3) 7805 positive 5V regulators (U8 - U10)

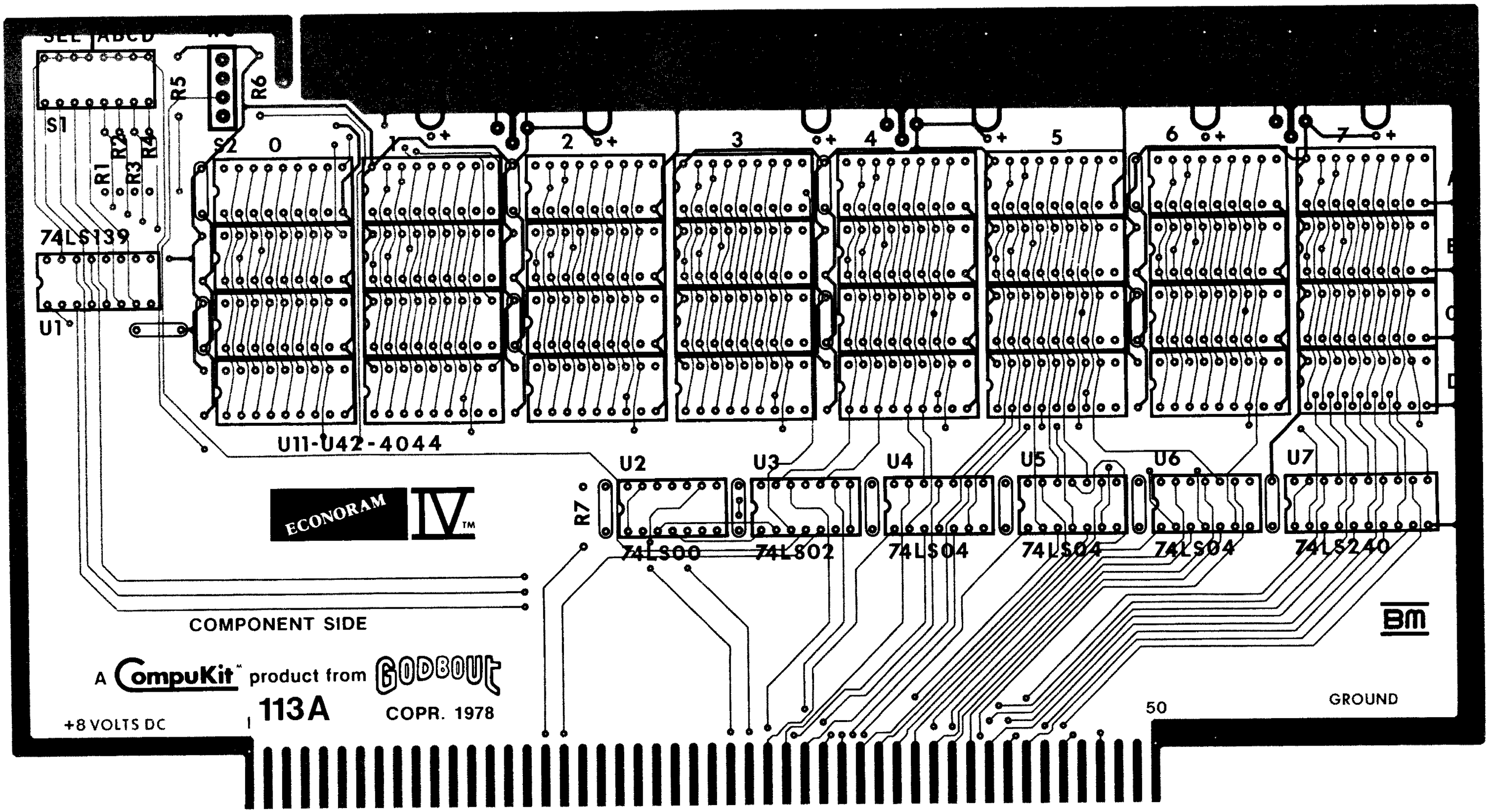
OTHER ELECTRONIC COMPONENTS

- ☐ (7) 2 7K ohm resistors (red-violet-red, R1 - R7)
- ☐ (6) 39uF tantalum capacitors (C1 - C6)
- ☐ (14) ceramic disk bypass capacitors*

MECHANICAL COMPONENTS

- ☐ (39) low profile sockets*
- ☐ (1) slide switch (S2)
- ☐ (1) 8 pole dip switch (S1)
- ☐ (3) heat sinks for regulator ICs
- ☐ (3) 6-32 bolts
- ☐ (3) 6-32 lockwashers
- ☐ (3) 6-32 nuts
- ☐ (1) instruction booklet

*supplied already soldered to board



Component Layout

UP

MEMORY ADDRESS ASSIGNMENT

This board is addressable as a single 16K block on any 16K boundary DIP switch positions 1-4 select which 16K area of memory the board will be associated with as follows

1 - 0000 - 3FFF (hex)
2 - 4000 - 7FFF (hex)
3 - 8000 - BFFF (hex)
4 - C000 - FFFF (hex)

Only one of these four switches may be up (on) at a time, however, all four may be down which will deselect the board (content of the memory may neither be changed nor read) and the board is transparent to the system allowing other boards to be addressed to that area as long as it is disabled

MEMORY PROTECT SWITCHES

DIP switch positions 5-8 are write enable switches Inversely they may be used for manual write protection of the memory Each enable protects 1/4 of the 16K block of memory (4K) as follows

5 - 1st 4K of 16K block
6 - 2nd 4K of 16K block
7 - 3rd 4K of 16K block
8 - 4th 4K of 16K block

Any combination of these four switches may be up/on with up write enabling the particular 4K area and down write protecting that area

WRITE STROBE SELECT SWITCH

This switch selects use or non-use of the S-100 buss signal MWRITE (pin 68) This signal is normally produced by a front panel and would not be available in front panel-less machines, however, some CPU boards now implement this signal If MWRITE is present in your machine, place the slide switch in the center position If not present, this switch should be in the up position

PHANTOM LINE

In response to increasing numbers of users who have requested inclusion of "Phantom" line, Buss pin 67 which is often used for implementing power on jump features This board is designed for use with active or inactive phantom lines Boards which are revision "A" or earlier have this line solidly connected Revision "B" and later boards require a jumper to implement this feature

CAUTION

Some manufacturers use the PHANTOM line (buss pin 67) for a refresh signal This will conflict with the PHANTOM feature, and cause boards with PHANTOM to fail If your system has this conflict it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards

On revision "A" or earlier boards the Phantom feature may be disabled by cutting the trace where it leaves buss pin 67 On revision "B" and later boards the PHANTOM feature is disabled if the jumper is NOT CONNECTED on the trace to buss pin 67 (see figure 11)

If you want the PHANTOM feature, the conflicting refresh signal may be eliminated (IF NOT USED ELSEWHERE IN THE SYSTEM) by cutting the trace connected to buss pin 67 on the CPU board BE SURE OF YOUR SYSTEM CONFIGURATION BEFORE CUTTING ANY TRACES

MEMORY TESTING

If the memory board seems to be working properly, the Memory Testing Routine (figure 13) can be used to give the board a more thorough workout It is rather slow, but will do the job well It can be entered via editor/assembler or front panel switches

The routine is set up to test 16K from 4000 hex up to 8000 hex This may be changed by entering a different starting address at "STRT" (3001 - 3002) and/or a different end address at "END' (3004 - high order byte only)

If the memory passes the test it starts over again You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart

If the memory fails the test, critical information is stored and the routine enters a software "HALT", that is a "jump to here' at "SHLT" Front panel lights, if any, will show this state The user may then use the front panel or dump routines to display the following stored failure info

3069*	"FDE'	=	D, E pair D is the fill character and E is the test character
306B*	"FHL'	=	H, L pair the failure address
306D*	"FOUT"	=	the data expected at this address
306E*	"FIN"	=	the data read from, the address

* address from *Memory Testing Routine Listing*

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine

The difference between "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem

This test will find most of the harder to distinguish errors

MEMORY TESTING ROUTINE

```
3000 21 00 40          0010 STRT LXI  H,4000H
3003 3E 80             0020 END  MVI  A,80H
3005 32 6E 30          0030      STA  FIN
3008 3E 10             0040      MVI  A,10H
300A 84                0050      ADD  H
300B 4F                0060      MOV  C,A
300C 16 00             0070      MVI  D,0
300E 1E FF             0080      MVI  E,0FFH
3010 22 65 30          0090 DONE SHLD STAD
3013 AF                0100      XRA  A
3014 47                0110      MOV  B,A
3015 7B                0120 SCND MOV  A,E
3016 5A                0130      MOV  E,D
3017 57                0140      MOV  D,A
3018 79                0150      MOV  A,C
3019 2A 65 30          0160      LHLD STAD
301C 72                0170 FILL MOV  M,D
301D 23                0180      INX  H
301E BC                0190      CMP  H
301F C2 1C 30          0200      JNZ  FILL
3022 2A 65 30          0210      LHLD STAD
3025 73                0220 NEXT MOV  M,E
3026 7B                0230      MOV  A,E
3027 BE                0240      CMP  M
3028 C2 6F 30          0250      JNZ  FAIL
302B 79                0260      MOV  A,C
302C 23                0270      INX  H
302D 94                0280      SUB  H
302E C2 4D 30          0290      JNZ  NDON
3031 B8                0300      CMP  B
3032 44                0310      MOV  B,H
3033 CA 15 30          0320      JZ   SCND
3036 3A 66 30          0325      LDA  STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA  FIN
303F B9                0350      CMP  C
3040 CA 00 30          0360      JZ   STRT
3043 79                0370      MOV  A,C
3044 67                0380      MOV  H,A
3045 2E 00             0390      MVI  L,0
3047 C6 10             0400      ADI  10H
3049 4F                0410      MOV  C,A
304A C3 10 30          0420      JMP   DONE
304D 22 67 30          0430 NDON SHLD NXAD
3050 7A                0440 LOPB MOV  A,D
3051 BE                0450 LOPA CMP  M
3052 C2 6F 30          0460      JNZ  FAIL
3055 2C                0470      INR  L
3056 C2 51 30          0480      JNZ  LOPA
3059 79                0490      MOV  A,C
305A 24                0500      INR  H
305B BC                0510      CMP  H
305C C2 50 30          0520      JNZ  LOPB
305F 2A 67 30          0530      LHLD NXAD
3062 C3 25 30          0540      JMP  NEXT
3065                   0550 STAD DS   2
3067                   0560 NXAD DS   2
3069                   0570 FDE  DS   2
306B                   0580 FHL  DS   2
306D                   0590 FOUT DS   1
306E                   0600 FIN  DS   1
306F 22 6B 30          0610 FAIL SHLD FHL
3072 32 6D 30          0620      STA  FOUT
3075 7E                0630      MOV  A,M
3076 32 6E 30          0640      STA  FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD FDE
307D C3 7D 30          0670 SHLT JMP SHLT
3080                   0680 *
```

CIRCUIT DESCRIPTON

The heart of Econoram IV is the TMS4044/MM5257 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts.

These ICs are arranged in rows that are 8 ICs wide This way, each row can store 4K x 8 bits of information. Paralleling 4 of these rows together produces a total memory storage of 16K x 8 bits (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array)

Now that we have this storage, there are still other aspects we must consider First, we need to address a specific location in memory, and, we need to be able to *write* data into the memory, or *read* data from the memory

The schematics on pages 8 and 9 show the address circuitry along with the other Econoram IV circuitry Each memory IC requires 12 address bits (A0-A11) to access any one of the 4096 bits available in the IC These address bits are generated by the CPU and are buffered by a number of inverters After buffering, a particular address is presented to all IC address selection pins However, we additionally need to select which particular row of ICs is to react to the given address This requires 4 more address bits (A12-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array)

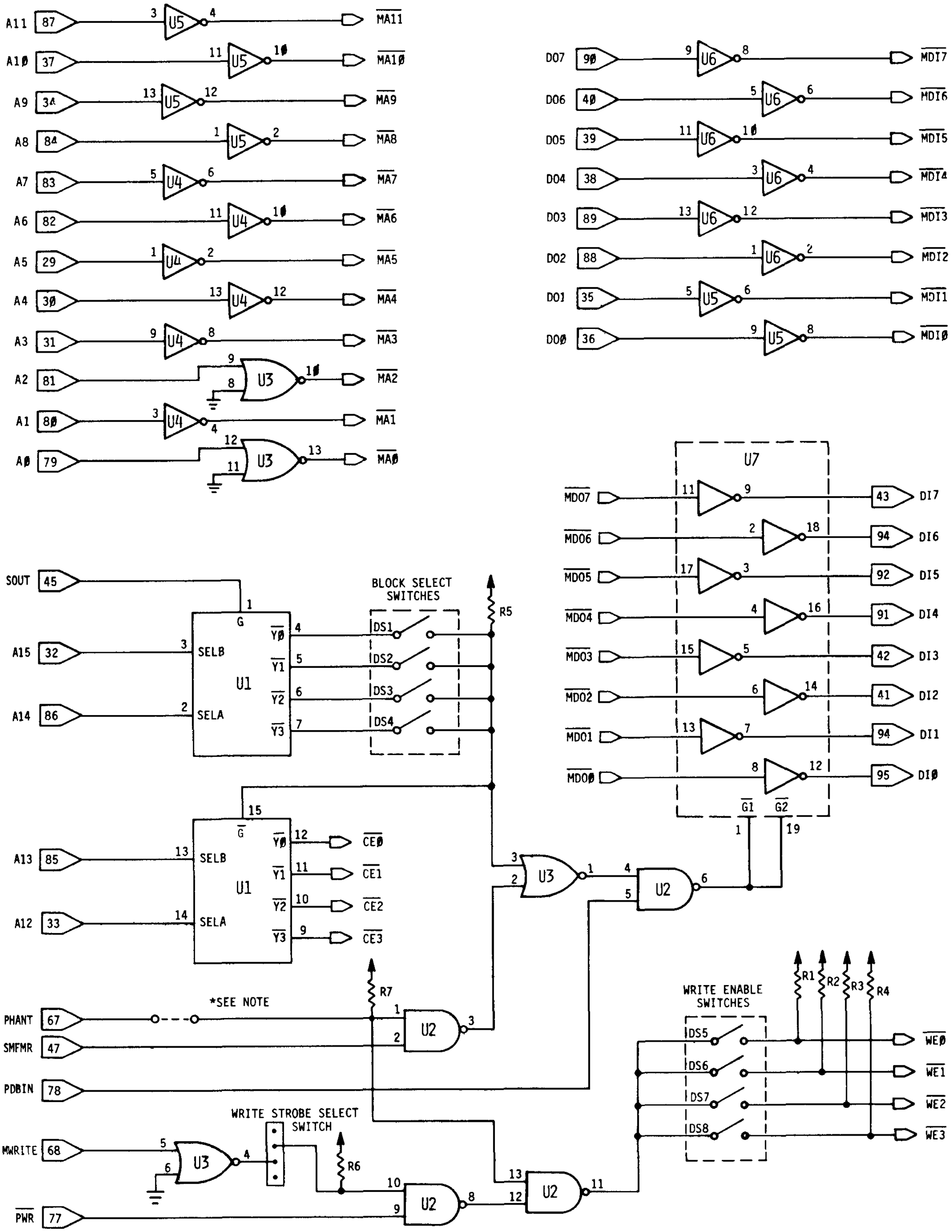
When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss) Data to be read on to the data buss from memory passes through 8 TRI-STATE® inverting buss drivers, when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines If these transients work their way into the logic circuitry, problems can appear To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC

This board is guaranteed to operate at 4MHz over the full temperature range (0° - 70° C ambient) and to draw less than 2000 mA (2 amps) Our typical measured currents were less than 1600 mA at cold start-up, rapidly decreasing to around 1200-1400 mA, depending on the surrounding temperature We have heard similar reports from the people already using these boards

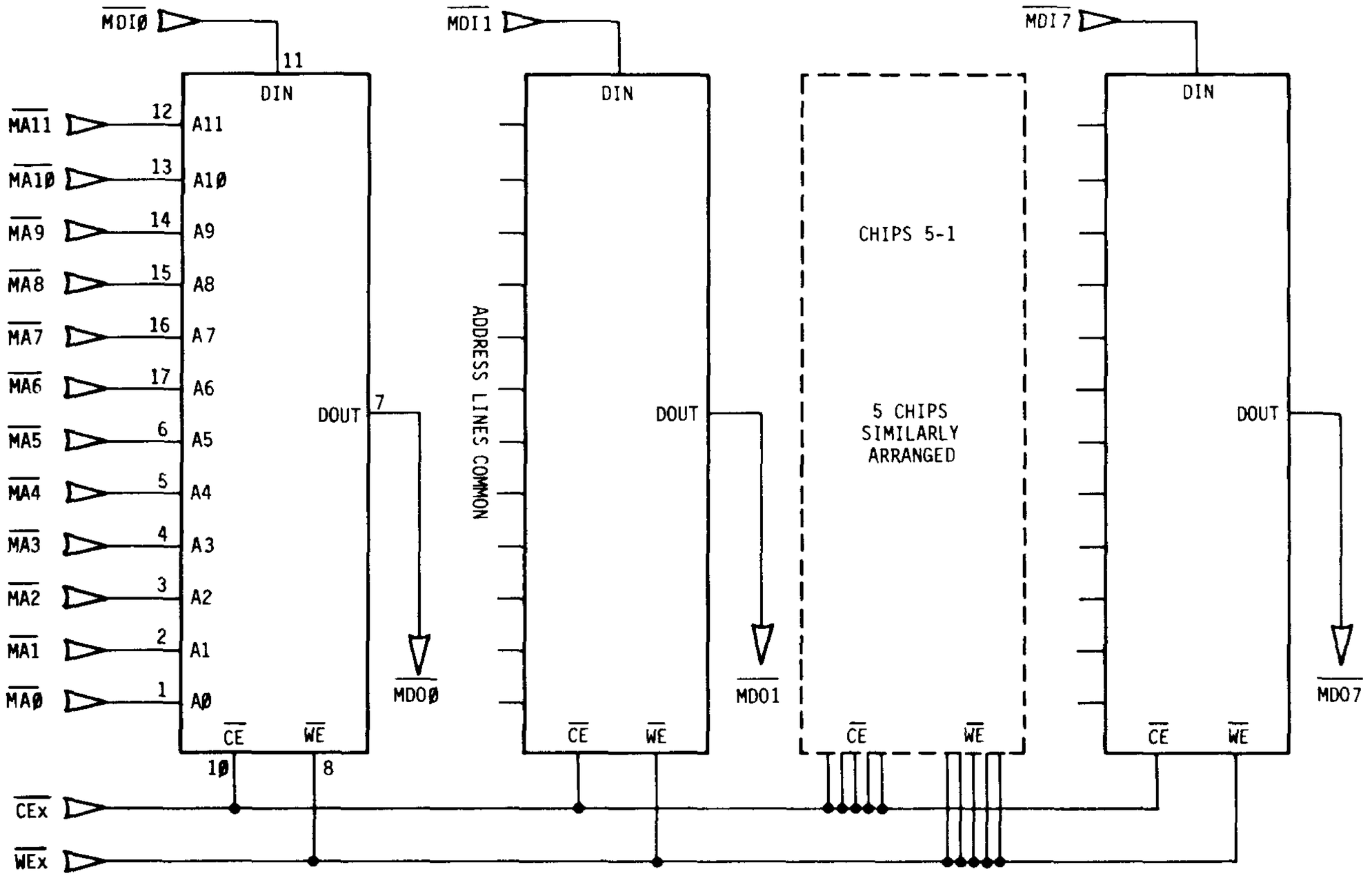
It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards

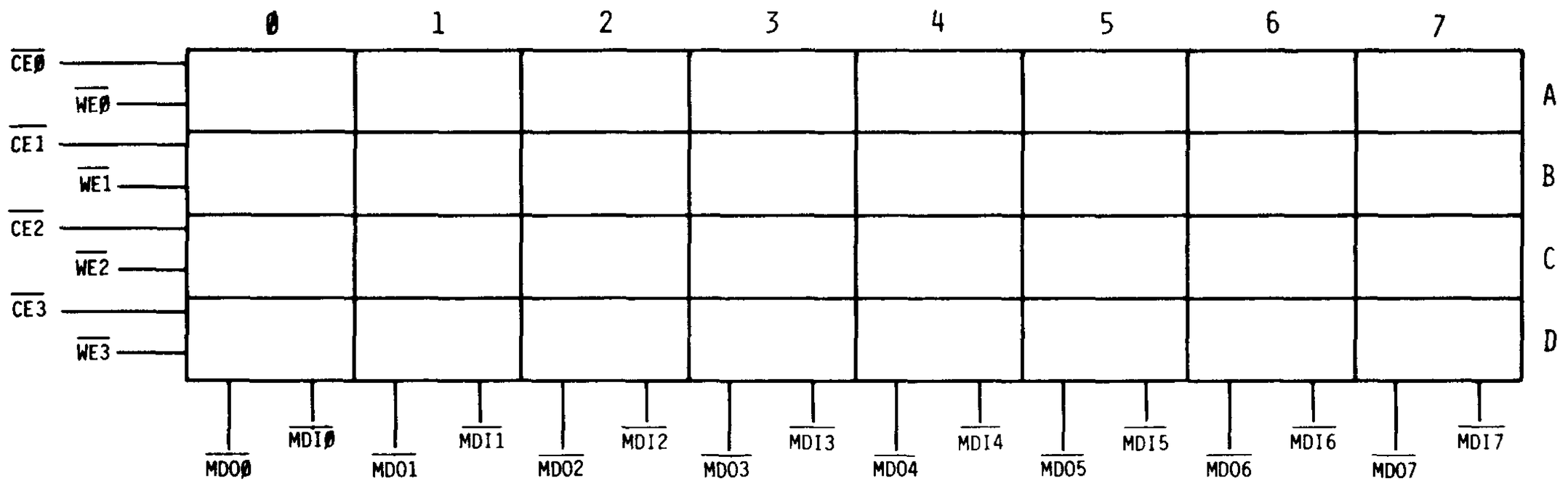
SCHEMATIC - ECONORAM IV

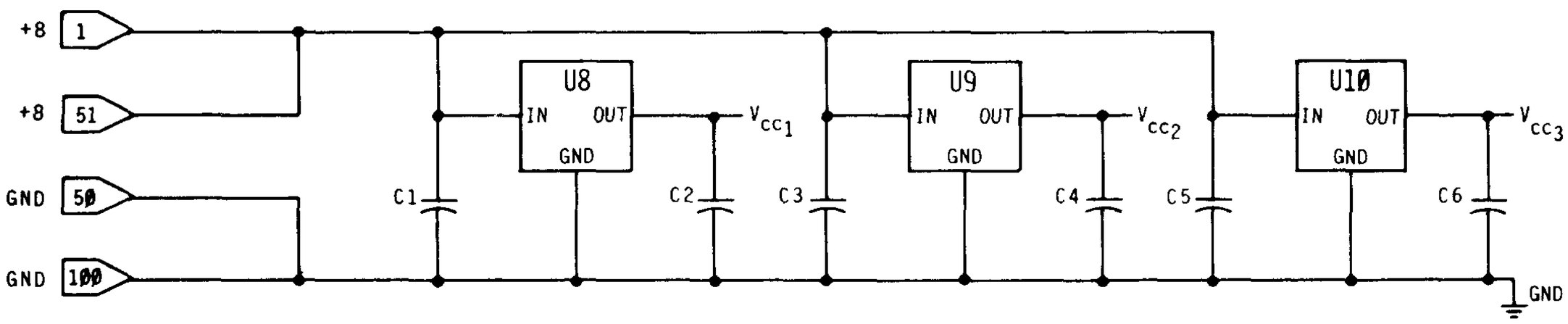


NOTE On revision 'A' boards this trace is solid, on revision "B' and later boards require a jumper to implement

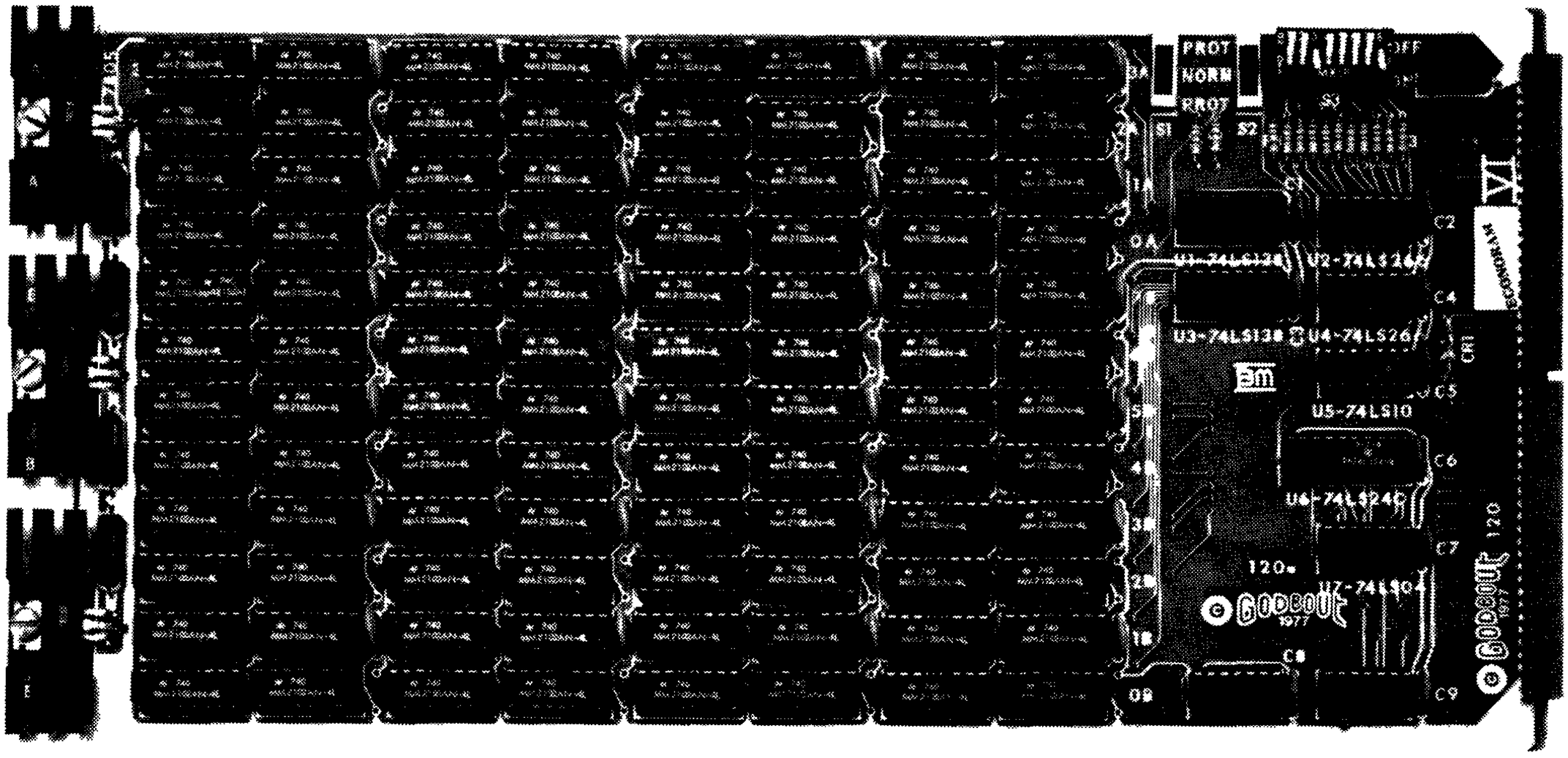
SCHEMATIC - ECONORAM IV







ECONORAM VI™
USER'S MANUAL



12K x 8 static memory for the H8

GODBOUT

BILL GODBOUT ELECTRONICS
BOX 2355, OAKLAND AIRPORT, CA 94614

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ABOUT ECONORAM VI

Congratulations on your decision to purchase ECONORAM VI, a 12K×8 memory board designed specifically for electrical and mechanical compatibility with the Heath Company H8 microcomputer. Heath has come up with a fine, user-oriented machine, we've come up with the perfect memory to complement that machine.

All IC sockets and disc bypass capacitors are pre-soldered into place on the board, so the tedious work in putting a kit such as this together has already been done. Completion of the remaining assembly steps should take only an hour or two at most, and upon completion, you will discover — as thousands of satisfied ECONORAM owners have discovered — the pleasure of using a fine memory board that just works, and works, and works

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing ECONORAM VI . . welcome to the club.

TECHNICAL OVERVIEW

This board incorporates proven static memor technology. There are currently two popular types o memory being used in products such as this: static an dynamic. Static memories are the overwhelming choice i applications where speed, complexity, ease of use, an reliability must all be considered . . there is no refres slowdown, the CPU is freed from the drudgery of caretak ing the memory, and techniques such as direct memor access (DMA) are far easier to implement

The individual memory ICs used on this board ar grouped together to form two larger blocks of memory one 4K×8 and one 8K×8 The 4K block may be addresse on any 4K boundary, and the 8K block on any 8K boundary by setting the starting locations with the on-board di switch (no jumpers required). Additional features include write protect switches for both blocks to prevent acciden tal alteration or erasure of memory contents, a boar disable switch (the board retains stored memory dat while in the disable mode), 38 bypass capacitors to sup press transients on the supply lines, plus on-board regula tion and heat sinking for cool operation All of this goes o a double-sided, solder-masked printed circuit board wit all sockets and disc capacitors pre-soldered into positio for maximum ease of assembly.

PARTS LIST

Upon receipt of your kit, check your parts against the list below.

- ☐ (1) Econoram VI circuit board.

INTEGRATED CIRCUITS (note The following parts may have letter suffixes and prefixes along with the key numbers given below)

- ☐ (96) 2102 memories (U13-U208 on schematic and board legend)
- ☐ (3) 74LS04 hex inverters (U7-U9)
- ☐ (3) 7805 (may be marked 340-5) positive 5V regulators (U10-U12)
- ☐ (2) 74LS138 1 of 8 line decoders (U1, U3)
- ☐ (2) 74LS266 exclusive NOR gates (U2, U4)
- ☐ (1) 74LS10 NAND gates (U5)
- ☐ (1) 74LS240 tri-state inverters (U6)

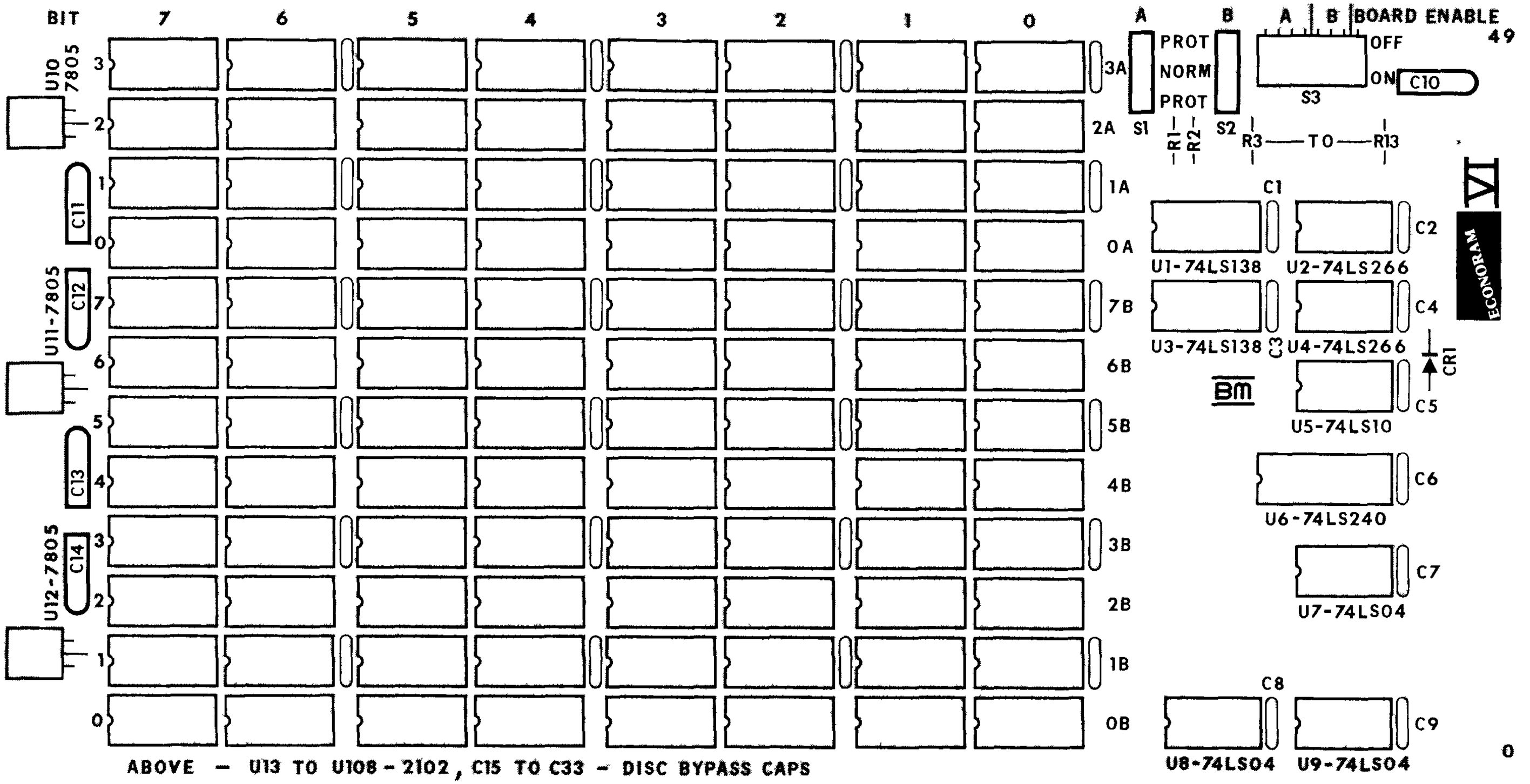
OTHER ELECTRONIC COMPONENTS

- ☐ (13) 2 7K ohm resistors (red/violet/red, R1-R13)
- ☐ (5) 39 uF tantalum capacitors (C10-14)
- ☐ (1) glass diode (CR1)
- ☐ (33) ceramic bypass capacitors* (C1-C9 and C15-C38)

MECHANICAL COMPONENTS

- ☐ (105) low profile sockets*
- ☐ (2) slide switches
- ☐ (1) 8 pole dip switch
- ☐ (3) heat sinks for regulator ICs
- ☐ (2) 25 pin right angle female connectors
- ☐ (5) 6-32 bolts
- ☐ (3) 6-32 lockwashers
- ☐ (3) 6-32 nuts
- ☐ (1) bracket to mount board in H8 card cage
- ☐ (1) instruction booklet

*supplied already soldered to board



Component Layout

MEMORY ADDRESS ASSIGNMENT

Microcomputers are designed to have the capability of accessing large amounts of memory (up to 64K in most cases) For convenience, we usually break the full 64K down to a smaller number of blocks, you may think of this 64K as breaking down into two 32K blocks, four 16K blocks, eight 8K blocks, sixteen 4K blocks, and so on. Whichever way you look at it, each block has specific *starting address*, which is the address at which the block begins In the case of 8K blocks, for example, the first block would begin at octal address 000 000, the next at 040 000, the next at 100 000, and so on through all 8 blocks. In the case of 4K blocks, the first block would begin at 000 000, the next at 020 000, the next at 040 000, and so on.

With Econoram VI, the two blocks of memory (one 4K and one 8K) may be assigned independent or non-consecutive locations if desired, the only requirement is that they not overlap

Proper manipulation of the dip switch levers accomplishes memory assignment Switches 1-4 set the starting address location of the 4K block, switches 5-7 set the starting address of the 8K block Switch 8 does not apply to memory assignment and will be discussed later

The following tables show the octal starting address of the 4K block relative to the setting of switches 1-4, and the octal starting address of the 8K block relative to the setting of switches 5-7 When setting these switches, the board should be oriented as shown in the component layout so that the dip switch is in the upper right hand corner

BOARD ENABLE SWITCH

Switch #8 of the dip switch is a board enable switch. In the down position, the board is enabled and in the up position, the board is disabled When disabled, the board is transparent or invisible as far as the machine is concerned (just as if it were unplugged) You may neither write into, nor read from, a disabled memory board However, data stored in memory prior to disabling is retained

On application of this feature involves having different programming languages stored in different boards Suppose you need to run some programs in BASIC, and then wish to switch over to some other language, and then get back to BASIC again You may load both languages into boards occupying the same area of memory, when using BASIC, merely disable the board containing the other language, and when you wish to switch, disable the BASIC board Note that if 2 boards share the same address space, only 1 may be enabled at any time

MEMORY PROTECT SWITCHES

S1 and S2 are the memory protect switches for this board With both switches in the middle position, board operation is normal and you may either write into or read from both blocks of memory With S1 in either the up or down position, the 4K block (block A) is in the protect mode With S2 in either the up or down position, the 8K block (block B) is in the protect mode While in protect mode, data may be read from the protected block of memory, but any attempt to write into protected memory is inhibited

MEMORY ASSIGNMENT TABLE

1 = switch up; 0 = switch down

4K block:	SWITCH NUMBER	OCTAL STARTING ADDRESS (what you see on front panel readouts)
	1 2 3 4	
	0 0 0 0	000 000
	0 0 0 1	020 000
	0 0 1 0	040 000
	0 0 1 1	060 000
	0 1 0 0	100 000
	0 1 0 1	120 000
	0 1 1 0	140 000
	0 1 1 1	160 000
	1 0 0 0	200 000
	1 0 0 1	220 000
	1 0 1 0	240 000
	1 0 1 1	260 000
	1 1 0 0	300 000
	1 1 0 1	320 000
	1 1 1 0	340 000
	1 1 1 1	360 000

8K block:	SWITCH NUMBER	OCTAL STARTING ADDRESS (what you see on front panel readouts)
	5 6 7	
	0 0 0	000 000
	0 0 1	040 000
	0 1 0	100 000
	0 1 1	140 000
	1 0 0	200 000
	1 0 1	240 000
	1 1 0	300 000
	1 1 1	340 000

Remember, the two blocks may not overlap.

MEMORY TESTING

ECONORAM VI is functionally and electrically equivalent to Heath Company memory boards All diagnostic routines specified by Heath in the H8 owner's manual are applicable to testing out this memory, in case the board fails this test, follow the procedures given below to uncover the cause of failure

Upon failing, the test routine leaves the failing data in the B register and the address of the failure in the H,L pair If the failure is immediate (data of 00 or 01) re-check the address selection switches of the block you are testing Also, be sure the board disable switch (dip switch #8) is down, and the two write protect slide switches are in the center position

Failure may be caused by a variety of reasons, but two of the most common are a defective IC or an improperly inserted IC (typically, a bent pin or incorrect orientation) To locate which IC is causing the problem, first find the row, and then the bit, that corresponds to the suspected IC

To find the row, read the H,L pair to find the address of the failure Subtract the starting address of the block being tested The remainder gives the row address as follows

000 000 - 003 377	Row 0
004 000 - 007 377	Row 1
010 000 - 013 377	Row 2
014 000 - 017 377	Row 3
020 000 023 377	Row 4
024 000 - 027 377	Row 5
030 000 - 033 377	Row 6
034 000 - 037 377	Row 7

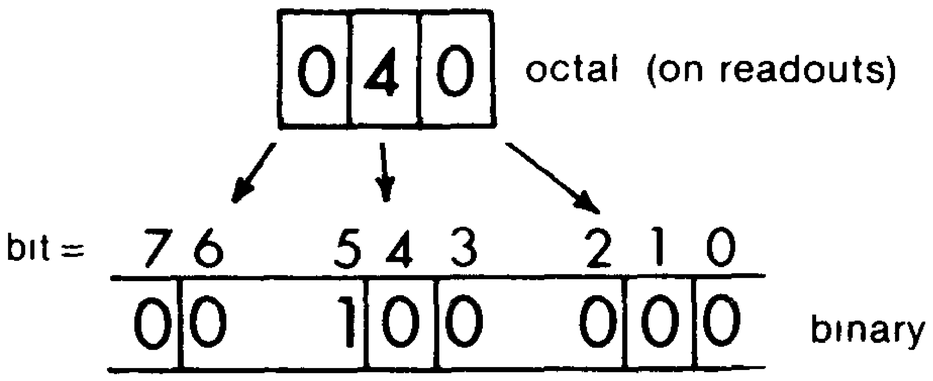
Example Failure 356 250
-Block start 340 000
016 250

This address corresponds to row 3, either row A3 if in the A (4K) block, or row B3 if in the B (8K) block

Proper manipulation of the dip switch levers accomplishes memory assignment. Switches 1-4 set the starting address location of the 4K block, switches 5-7 set the starting address of the 8K block Switch 8 does not apply to memory assignment and will be discussed later

The following tables show the octal starting address of the 4K block relative to the setting of switches 1-4, and the octal starting address of the 8K block relative to the setting of switches 5-7 When setting these switches, the board should be oriented as shown in the component layout so that the dip switch is in the upper right hand corner

To find the bit number, first note that each column of 2102s on the board corresponds to a bit in the 8 bit byte Then, read the failing data for the B register Convert to an 8 bit binary byte as shown in the following example



From this, we see bit 5 is indicated as suspect

Now we know both the row number and bit number of the IC in question To find this IC among the matrix of 2102s on the board, simply locate the row numbers and bit numbers legended on the board (note that the bit numbers read from right to left) Locate and remove the IC, if any of the leads are bent over, carefully re straighten them and replace the chip Otherwise, exchange the suspected IC with another from whichever block is not being tested at the time Retest the failing block to verify that the failure was associated with the IC just replaced

If the board still doesn't work, once again check over your work If problems persist, the kit may be returned for service in accordance with our warranty instructions

CIRCUIT DESCRIPTION

The heart of Econoram VI is the time proven 2102 static memory IC, which can store 1,024 single bits of information (thus, the 2102 is a "1K × 1" memory IC) Unlike standard 2102s, the 2102s included with your kit are specifically designated by the manufacturer as low power, high speed parts

These ICs are arranged in rows that are 8 ICs wide This way, each row can store 1K × 8 bits of information Paralleling 12 of these rows together produces a total memory storage of 12K × 8 bits (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory board)

Now that we have this storage, there are still other aspects we must consider First, we need to address a specific location in memory; and, we need to be able to *write* data into the memory, or *read* data from the memory

Figures 11 and 12 show the address circuitry along with the other Econoram VI circuitry Each memory IC requires 10 address bits (A0-A9) to access any one of the 1,024 bits available in the IC These address bits are generated from the computer and are buffered by a number of inverters After buffering, a particular address is presented to all IC address selection pins However, we additionally need to select which particular row of ICs is to react to the given address This requires 6 more address bits (A10-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array)

The H8 microcomputer uses an 8 bit bidirectional buss When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the 2102s (buffering prevents loading of the data buss) Data to be read on to the data buss from memory passes through 8 tri-state inverters, when data is *not* being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines If these transients work their way into the logic circuitry, problems can appear To prevent such occurrances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC

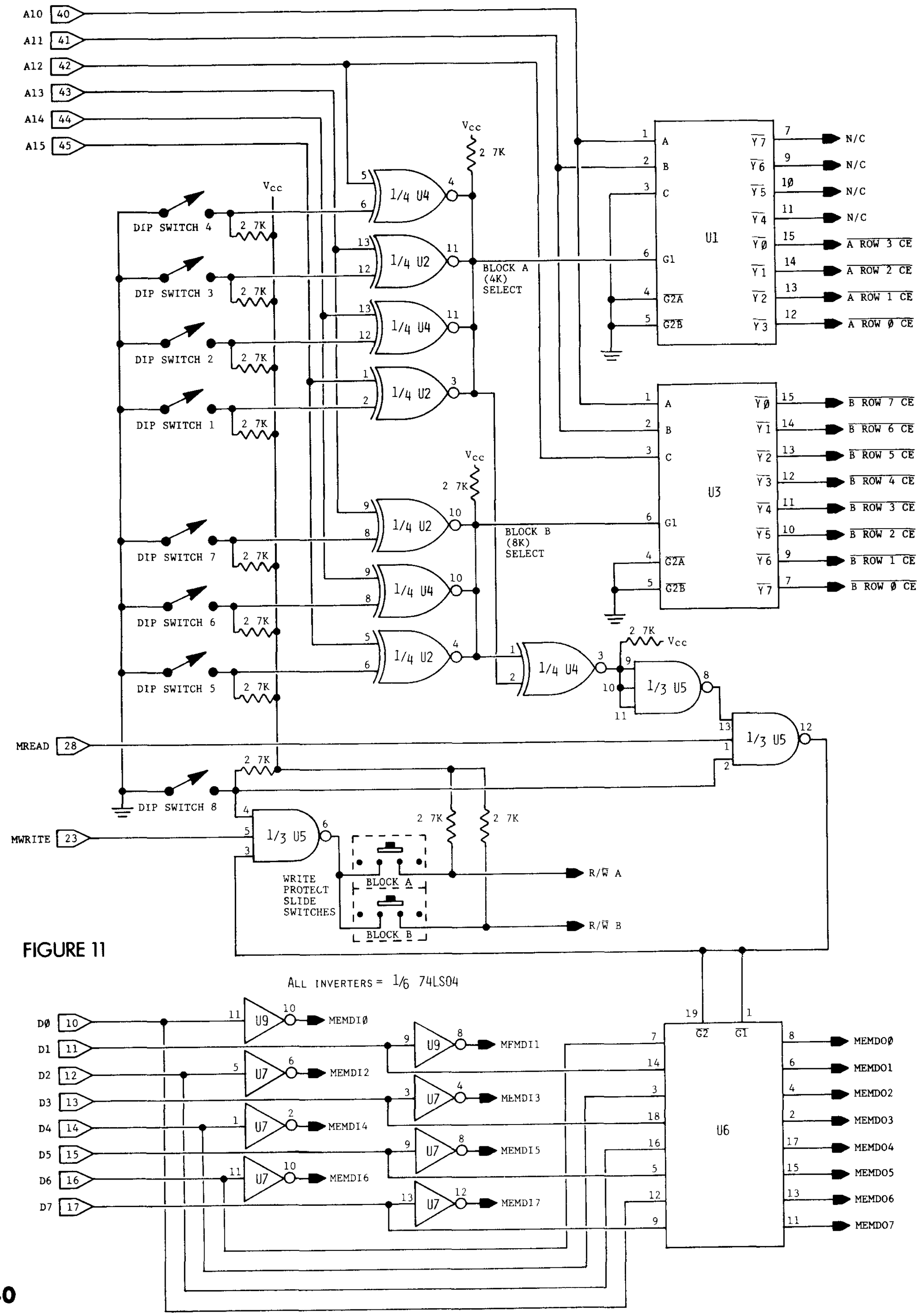
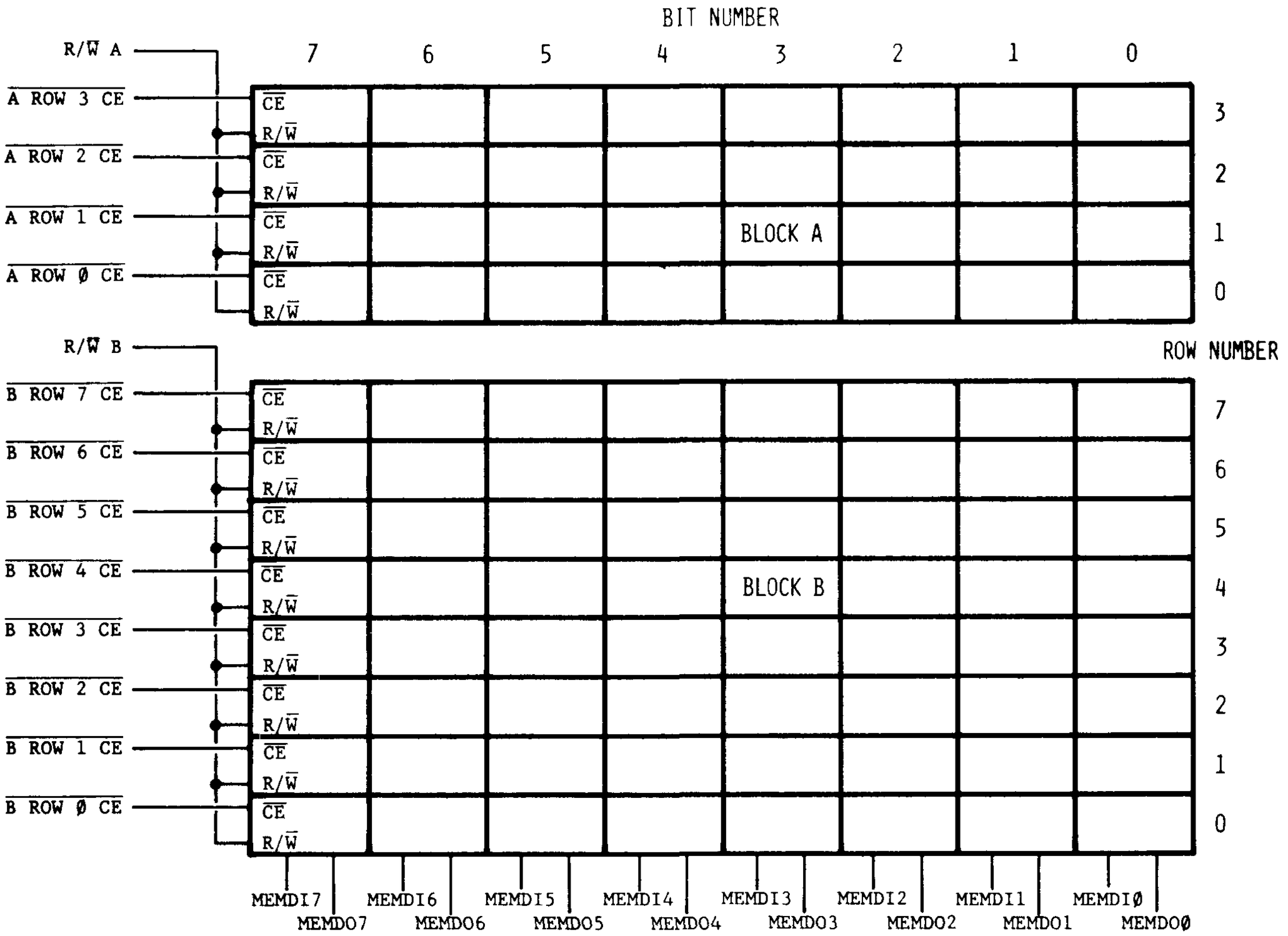
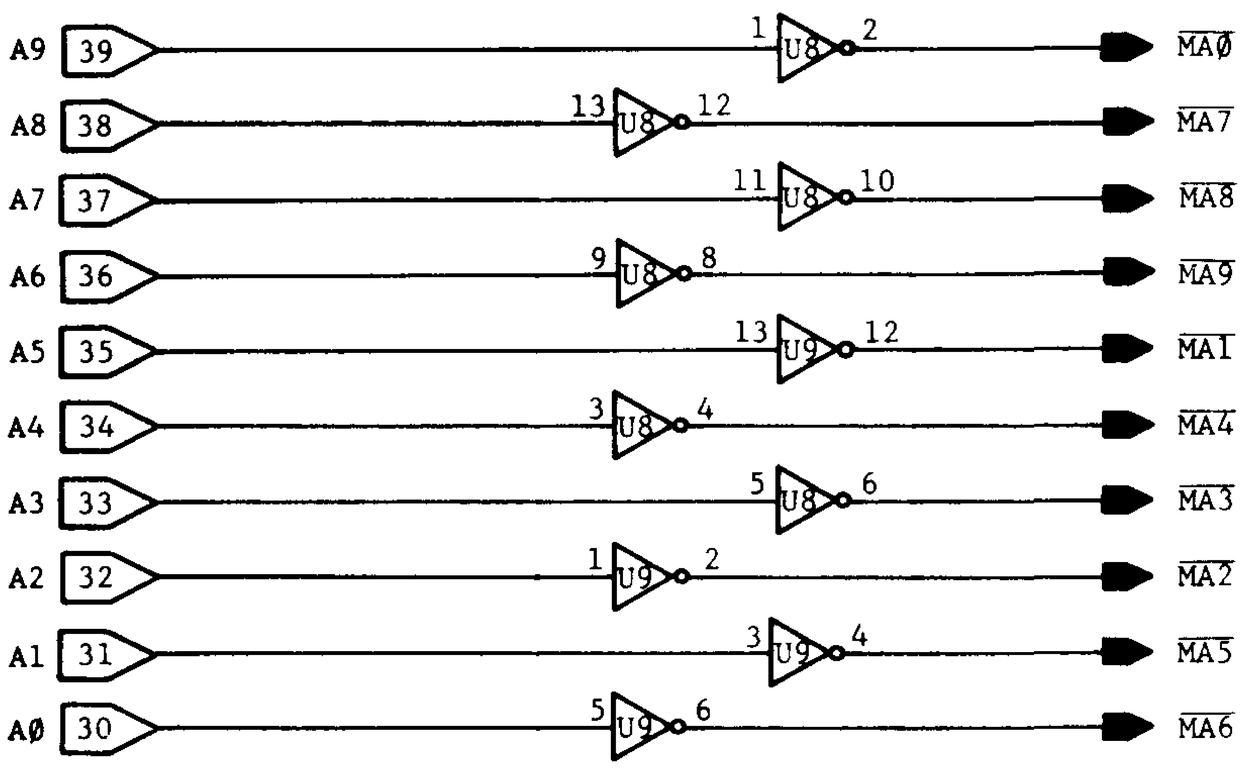

A10 40
A11 41
A12 42
A13 43
A14 44
A15 45
Vcc
2 7K
DIP SWITCH 4
DIP SWITCH 3
DIP SWITCH 2
DIP SWITCH 1
DIP SWITCH 7
DIP SWITCH 6
DIP SWITCH 5
DIP SWITCH 8
1/4 U4
1/4 U2
BLOCK A (4K) SELECT
BLOCK B (8K) SELECT
U1
U3
G1
G2A
G2B
N/C
A ROW 3 CE
A ROW 2 CE
A ROW 1 CE
A ROW Ø CE
B ROW 7 CE
B ROW 6 CE
B ROW 5 CE
B ROW 4 CE
B ROW 3 CE
B ROW 2 CE
B ROW 1 CE
B ROW Ø CE
1/3 U5
MREAD 28
MWRITE 23
WRITE PROTECT SLIDE SWITCHES
BLOCK A
BLOCK B
R/W A
R/W B
ALL INVERTERS = 1/6 74LS04
U9
U7
U6
D0 10
D1 11
D2 12
D3 13
D4 14
D5 15
D6 16
D7 17
MEMDI0
MFMDI1
MEMDI2
MEMDI3
MEMDI4
MEMDI5
MEMDI6
MEMDI7
MEMDO0
MEMDO1
MEMDO2
MEMDO3
MEMDO4
MEMDO5
MEMDO6
MEMDO7

FIGURE 11



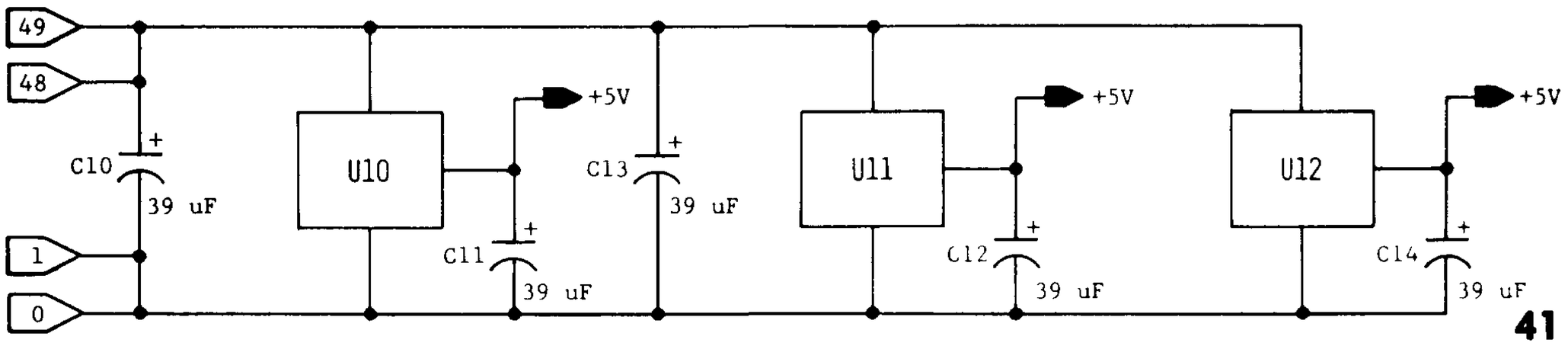


BLOCK A = 4K BLOCK

BLOCK B = 8K BLOCK

ALL INVERTERS = 1/6 74LS04

FIGURE 12



E. PHANTOM* is an open collector line used to overlay slaves at the same address location. Phantom must inhibit both read and write operations in disabled slaves.

F. ERROR* is an open collector general error line which may be asserted when an error of any type occurs in the current bus cycle.

G. PWRFAIL*, PoWeR FAILure, indicates impending power failure. POC* clears PWRFAIL*. PWRFAIL* should be generated in the system power supply to insure that there is sufficient stored energy available for the system to go into cocoon mode. Cocoon mode means that operation is terminated in such a fashion that operation can be resumed upon restoration of power. This implies that no damage occur to stored data and system hardware. A proper power fail sequence insures that machine state is stored, disk heads unloaded, etc.

H. POWER 6 Lines plus 3 Lines?
Plus 3 lines? These three lines were formerly protect (bus pin 70) unprotect (bus pin 20) and sense switch disable (bus pin 53). These lines are now defined as ground in IEEE 696. The stated purpose for this redefinition was to provide low impedance grounds on both sides of both the board and edge connector. In actual practice, the impedance of these lines is likely to be higher than desirable because of their locations within the physical bus structure. Additionally, the assignment of pin 53 has been changed twice since the proposed specification was published in July of 1979. In the author's experience, inclusion of a ground on pin 53 produced numerous reports of various front panels and CPU's failing to operate with pin 53 grounded. This writer recommends that designers avoid using line 53 in new products. If this recommendation is followed, this lines will be available for reassignment for future bus expansion.

1. Ground 2 Lines (Ground is both signal and DC common for the bus).

2. +8 Volts 2 Lines (7 < +8 < 25 Vav < 11 V +8 is the primary supply for +5 regulators on the bus).

3. +16 Volts 1 Line (14.5 < +16 < 35 Vav < 21.5 V +16 is the primary supply for +12 regulators on the bus).

4. -16 Volt 1 Line (-14.5 > -16 > -35 Vav > -21.5 V -16 is the primary supply for -12 regulators on the bus).

Inspection of the instantaneous and average voltage limits established by IEEE 696 shows that three terminal regulators may be used with an unregulated capacitor input power supply. Very small minimum cost system configurations may lend themselves to this approach. Thermal and power efficiency considerations become quite important with larger systems. Let us consider the case of a system requiring 25 Amps of +8 supply. If the power supply delivers the 11 volt maximum average, our system is consuming 275 Watts to deliver 125 Watts of Vcc power to system logic. The remaining 150 Watts are dissipated as heat from our voltage regulators. If the power supply delivers 7.3 volts to the bus, our system is consuming 182.5 Watts to deliver 125 Watts of Vcc power to system logic. The remaining 57.5 Watts are dissipated as heat from our voltage regulators. The above examples do not include any losses occurring within our power supply. Reducing power dissipation within the system lowers the operating temperature of the system components with a corollary increase in their life expectancy. Additionally, power consumption is reduced not only for the system itself but also in the amount of power expended to provide air conditioning for the space in which the system operates. These are extremely important considerations in these times of decreasing energy availability and increasing energy costs. As with all good things, there is a cost. The power supply used in the second example provides a pre-regulated + 8 volts. The cost of using monolythic switching regulators to provide 7.3 volts +/- 0.250 volts is minimal when compared with the resultant savings in cooling requirements and power consumption of the system. Further efficiency may be

CONTINUED ON PAGE 78

THESE INSTRUCTIONS APPLY ONLY TO REVISION 122D OR EARLIER

We recommend that you check the parts in this kit against the parts list for completeness and that you completely read these instructions carefully before starting.

ASSEMBLY INSTRUCTIONS

Proper operation of your kit depends on good soldering techniques, along with correct identification and handling of the various parts used during construction.

SOLDERING TECHNIQUES. The Econoram board is "solder-masked" These boards are similar to standard PC boards, but are screened with a solder-resistant coating. Soldering a solder-masked board requires a bit of care. All soldering is performed on the solder side of the board. Keep component leads straight up, clip off after soldering. When soldering, bring the iron tip in at an angle, against the pad and component lead. Feed in a tiny bit of solder at the lead base where it touches the pad, (Figure 1). This makes a good joint with no excess solder. NOTE: Use of any type of solder other than rosin core invalidates the warranty. Do not use any type of solder paste or corrosive flux under any conditions.

IDENTIFICATION OF PARTS. Many ICs are used in this kit, each must be oriented correctly for proper operation. Most ICs have a dot near one corner that indicates pin 1; sometimes this dot appears in conjunction with a deeply cup notch, or a notch within a shallow circle. The 6 tantalum capacitors must be correctly oriented. (The (+) end is the rounded end).

HANDLING OF PARTS. All integrated circuits may be damaged by static electric discharges. To prevent this, leave the ICs in their protective foil until needed. Avoid wearing clothing that is prone to generate a static electricity while constructing, (sweaters, acrylic fabrics, etc). Another caution concerns the mounting of resistors and diodes. Use needle-nose pliers to grasp the lead close to the body of the resistor or diode and then gently bend the lead downward.

CONSTRUCTION

Keeping the preceding information in mind, follow the steps below in the order given.

1. Bend leads, mount and solder the resistors in place.
2. Bend leads, mount and solder the tantalum capacitors in place, be careful to correctly orient the capacitors. The (+)end is rounded.
3. Mount the slide switches in position. (NOTE: Orientation of switch is not important).
4. Mount the three regulators and the regulator heat sinks into place. If desired, a small dab of heat sink compound may be added between the regulator cases and heat sinks to improve thermal transfer.
5. Before proceeding, check your work by testing the board for any shorts between supply lines and ground. (See Figure 2), use a Voltmeter to test for shorts at test points indicated on the regulator. Do this test for each regulator.
6. Plug in all ICs, follow the component legend. A common problem with boards returned for repair is improper insertion of ICs. Make sure the ICs are correctly oriented. Sometimes one of the IC's leads will bend under the part instead of going into the socket. We recommend, that you insert each IC halfway, and verify visually that all pins are indeed going into the socket. Then, push the IC in the rest of the way.
7. Check your work carefully for errors in construction, improperly inserted ICs, or the tantalum capacitors in reversed.

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PARTS LIST Upon receipt of your kit, check parts received against the list below.

(1) Econoram VII circuit board

INTEGRATED CIRCUITS. (Note: The following parts may have letter suffixes and prefixes along with the key numbers given below).
(48) MM5257 or TMS 4044 memories (U14 - U61)
(1) 74LS00 nand gate (U5)
(1) 74LS10 3-input nand gate (U7)
(1) 74LS02 nor gate (U6)
(5) 74LS04 hex inverters (U8 - U12)
(1) 74LS240 TRI-STATE® inverters (U13)
(4) 74LS266 ex-nor open collector (U1 - U4)
(3) 7805 positive 5 volt regulators (U62 - U64)

OTHER ELECTRONIC COMPONENTS
(2) S.I.P. resistor packs (R1 - R2)*
(11) 2.7K ¼ watt resistors (red-violet-red)(R3 - R12)
(6) 39uF tantalum capacitors (C1 - C6)
(25) ceramic disc bypass capacitors*

MECHANICAL COMPONENTS
(61) low profile sockets*
(2) dip switch (S1 - S2)*
(5) slide switch (S3 - S7)
(3) TO-220 heat sinks
(3) 6-32 bolts
(3) 6-32 lockwashers
(3) 6-32 hex nuts
(1) instruction set

* Supplied already soldered to board.

TRI-STATE® TRADEMARK OF NATIONAL SEMICONDUCTOR CORP.

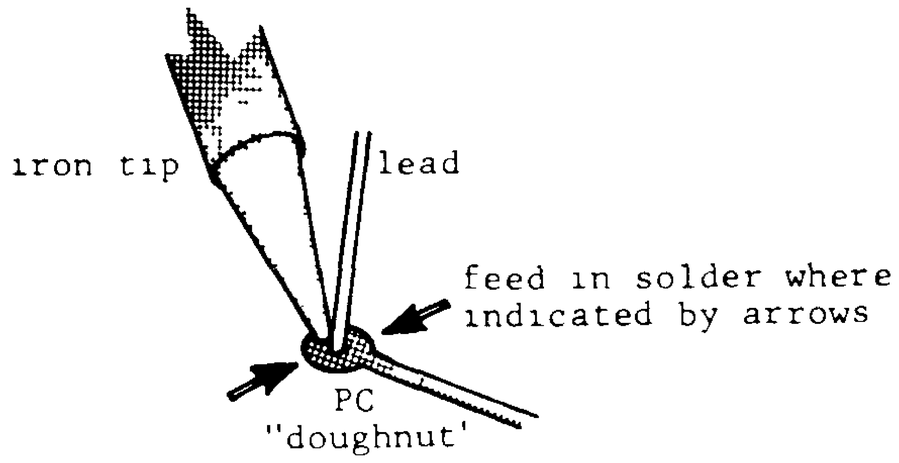

FIGURE 1

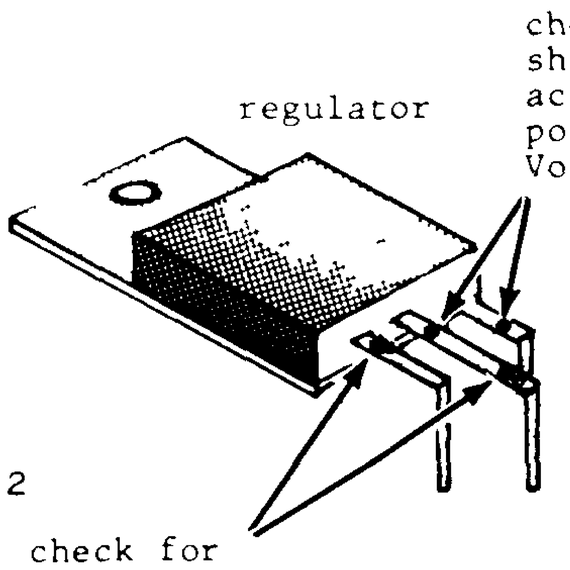

FIGURE 2

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MEMORY ADDRESS CONFIGURATION

This board is configured as two 12K "areas" each having one 4K block addressable on 4K boundaries and one 8K block independently addressable on 8K boundaries. One dip switch is used to select each 12K area (switch S1 : block A - 4K and block B - 8K, switch S2 : block C - 4K and block D - 8K) as follows:

4K		8K	
SWITCH POSITION	STARTING ADDRESS	SWITCH POSITION	STARTING ADDRESS
1234		567	
ØØØØ	ØØØØ	ØØØ	ØØØØ
ØØØ1	1ØØØ	ØØ1	2ØØØ
ØØ1Ø	2ØØØ	Ø1Ø	4ØØØ
ØØ11	3ØØØ	Ø11	6ØØØ
Ø1ØØ	4ØØØ	1ØØ	8ØØØ
Ø1Ø1	5ØØØ	1Ø1	AØØØ
Ø11Ø	6ØØØ	11Ø	CØØØ
Ø111	7ØØØ	111	EØØØ
1ØØØ	8ØØØ		
1ØØ1	9ØØØ		
1Ø1Ø	AØØØ		
1Ø11	BØØØ		
11ØØ	CØØØ		
11Ø1	DØØØ		
111Ø	EØØØ		
1111	FØØØ		

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In addition, position 8 on each switch enables (UP) or disables (DOWN) the associated 12K area.

Slide switch S3 selects use/non-use of MWRITE strobe. For use in machines with front panels or means of generating MWRITE, S3 should be in the extreme UP position. Otherwise, S3 should be in the CENTER position.

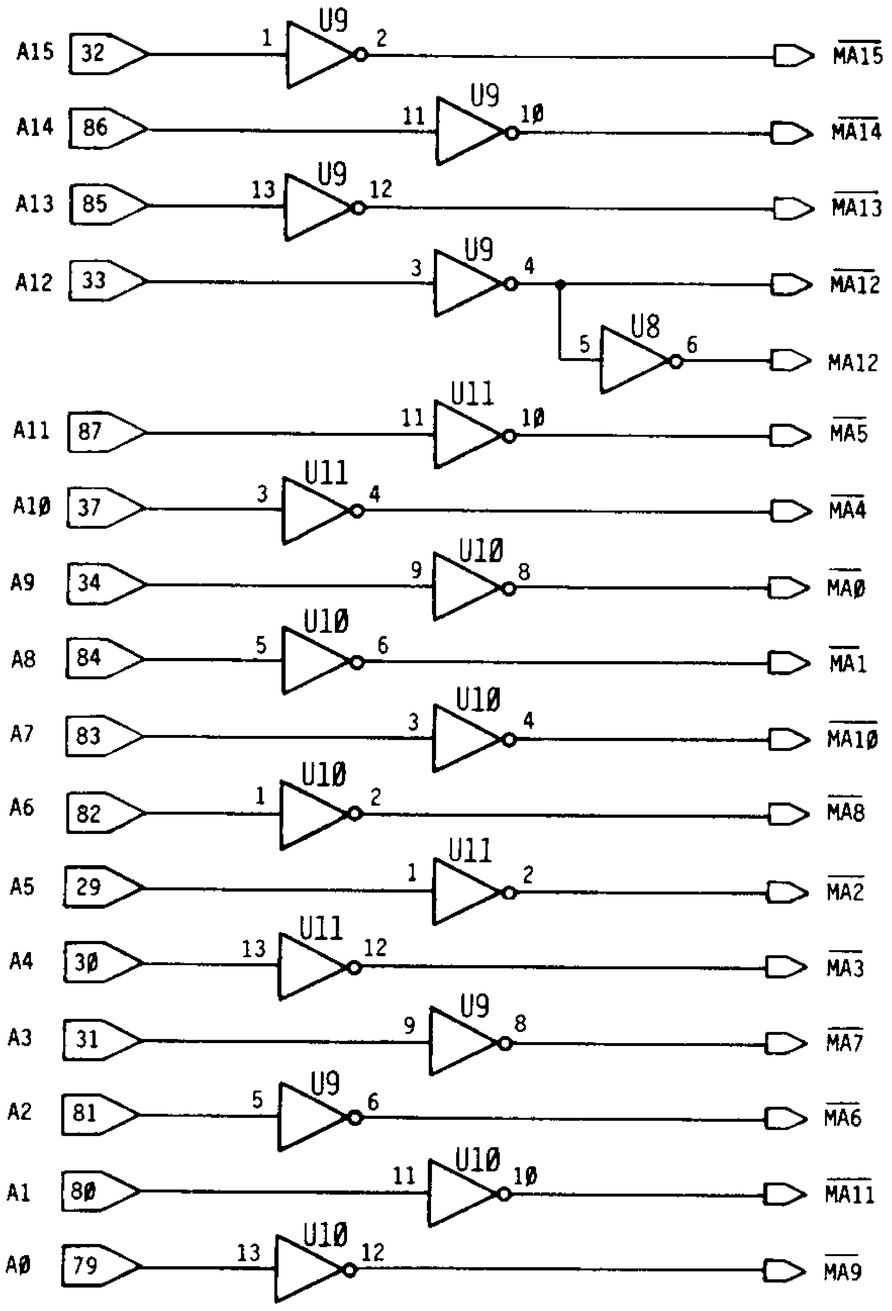
Slide switches S4 - S8 manually write enable the four blocks A - D respectively. For write enable place the desired switch in the CENTER position. To write protect a block place the appropriate switch in the extreme UP position.

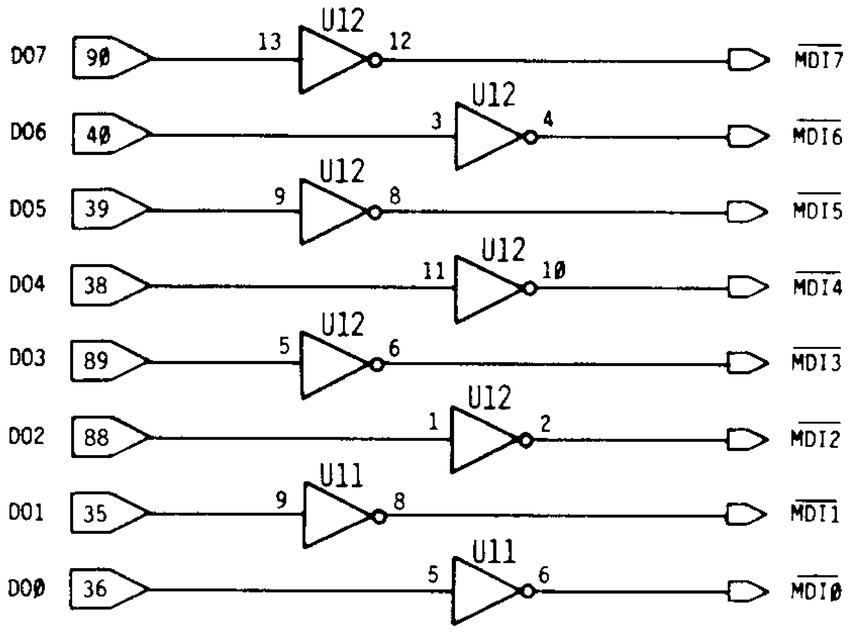
LIMITED WARRANTY INFORMATION

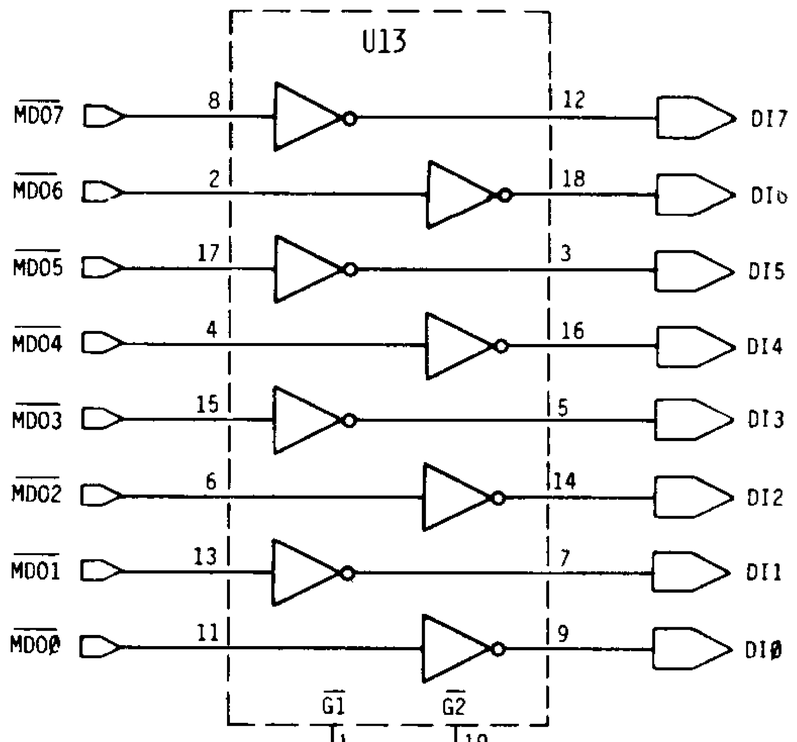
GODBOUT ELECTRONICS WILL REPAIR OR REPLACE, AT OUR OPTION, ANY PARTS FOUND TO BE DEFECTIVE IN EITHER MATERIALS OR WORKMANSHIP FOR A PERIOD OF 1 YEAR FROM DATE OF INVOICE.

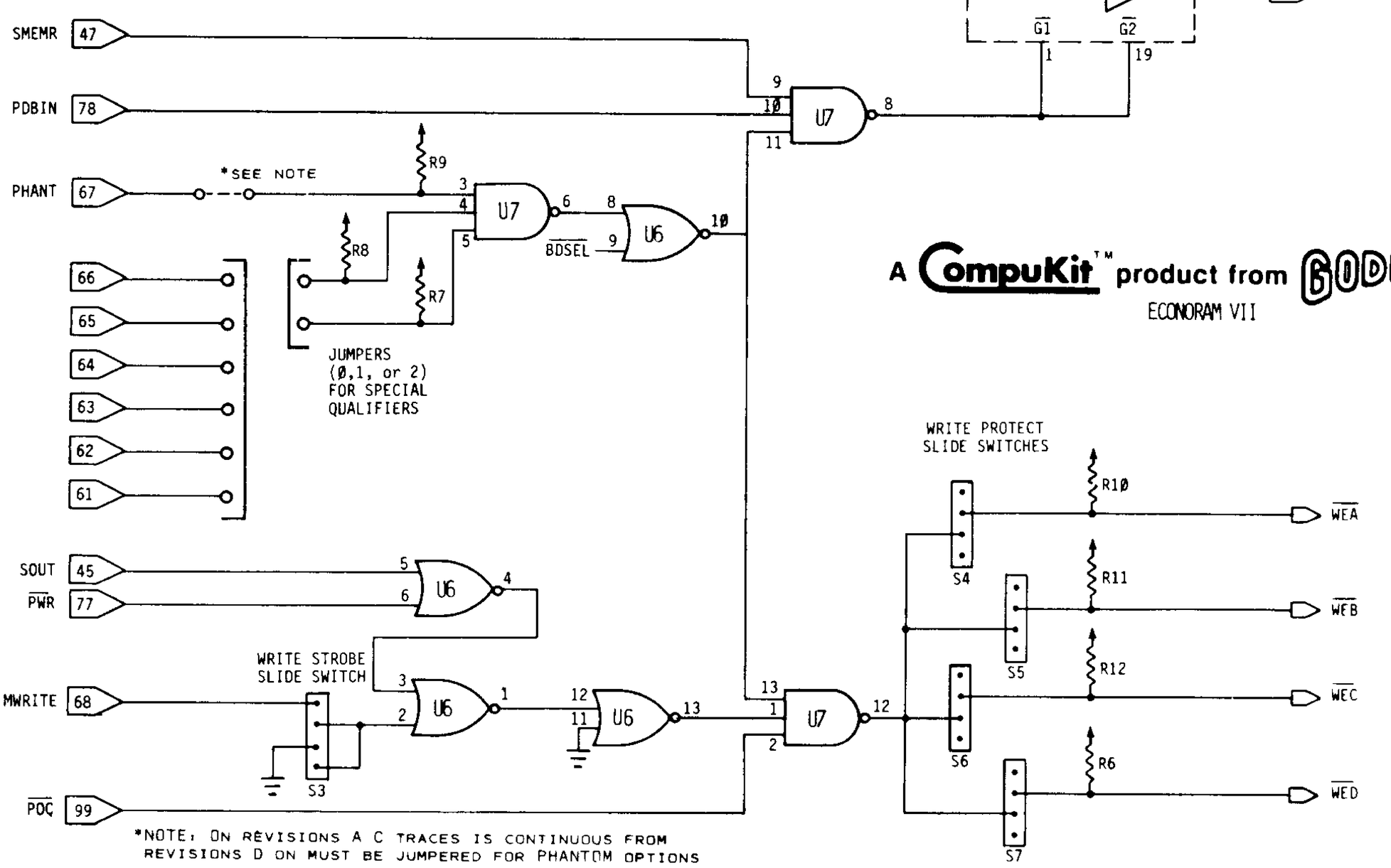
WE ARE NOT RESPONSIBLE FOR DAMAGE CAUSED BY USE OF SOLDER INTENDED FOR PURPOSES OTHER THAN ELECTRONIC EQUIPMENT CONSTRUCTION, MISUSE OR ABUSE, UNAUTHORIZED MODIFICATION, USE OF OUR PRODUCTS IN APPLICATIONS OTHER THAN THOSE INTENDED BY GODBOUT ELECTRONICS, THEFT, FIRE, OR ACCIDENTS.

RETURN TO PURCHASER OF A FULLY FUNCTIONING UNIT MEETING ALL ADVERTISED SPECIFICATIONS IN EFFECT AS OF DATE OF PURCHASE IS CONSIDERED TO BE COMPLETE FULFILLMENT OF ALL WARRANTY OBLIGATIONS ASSUMED BY GODBOUT ELECTRONICS AND DOES NOT COVER OTHER EQUIPMENT USED IN CONJUNCTION WITH SAID PRODUCTS. WE ARE NOT RESPONSIBLE FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES.









*NOTE: ON REVISIONS A C TRACES IS CONTINUOUS FROM REVISIONS D ON MUST BE JUMPERED FOR PHANTOM OPTIONS

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ECONORAM VII

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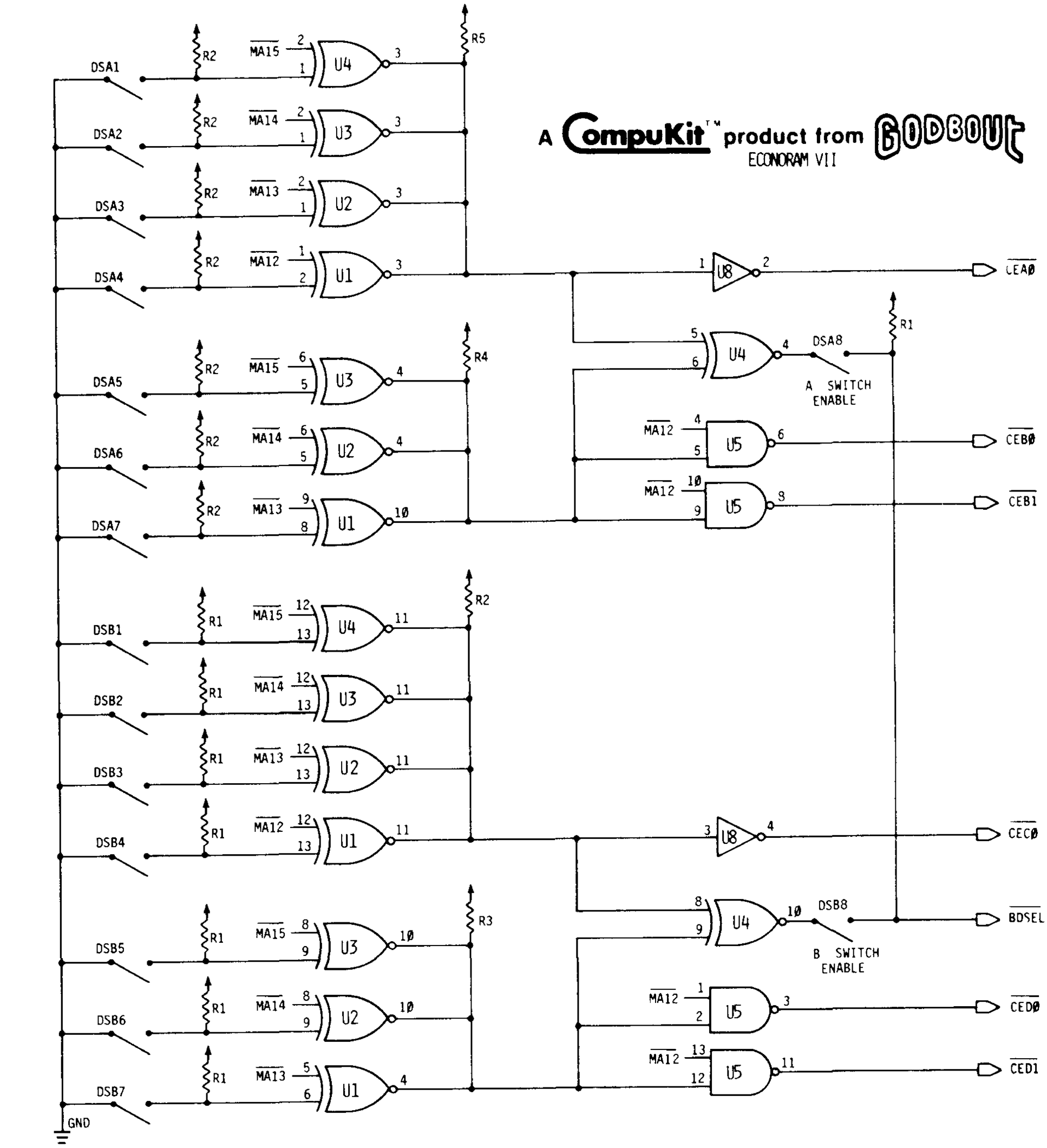
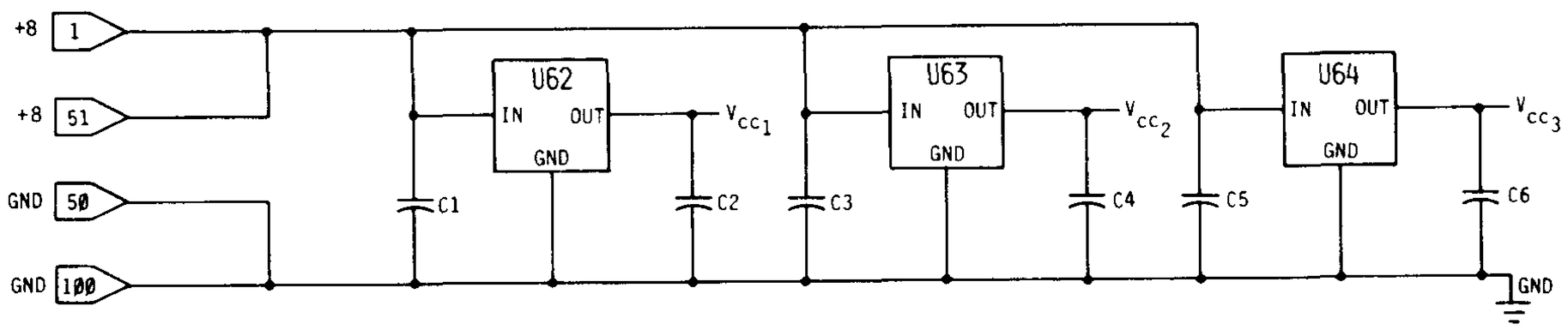
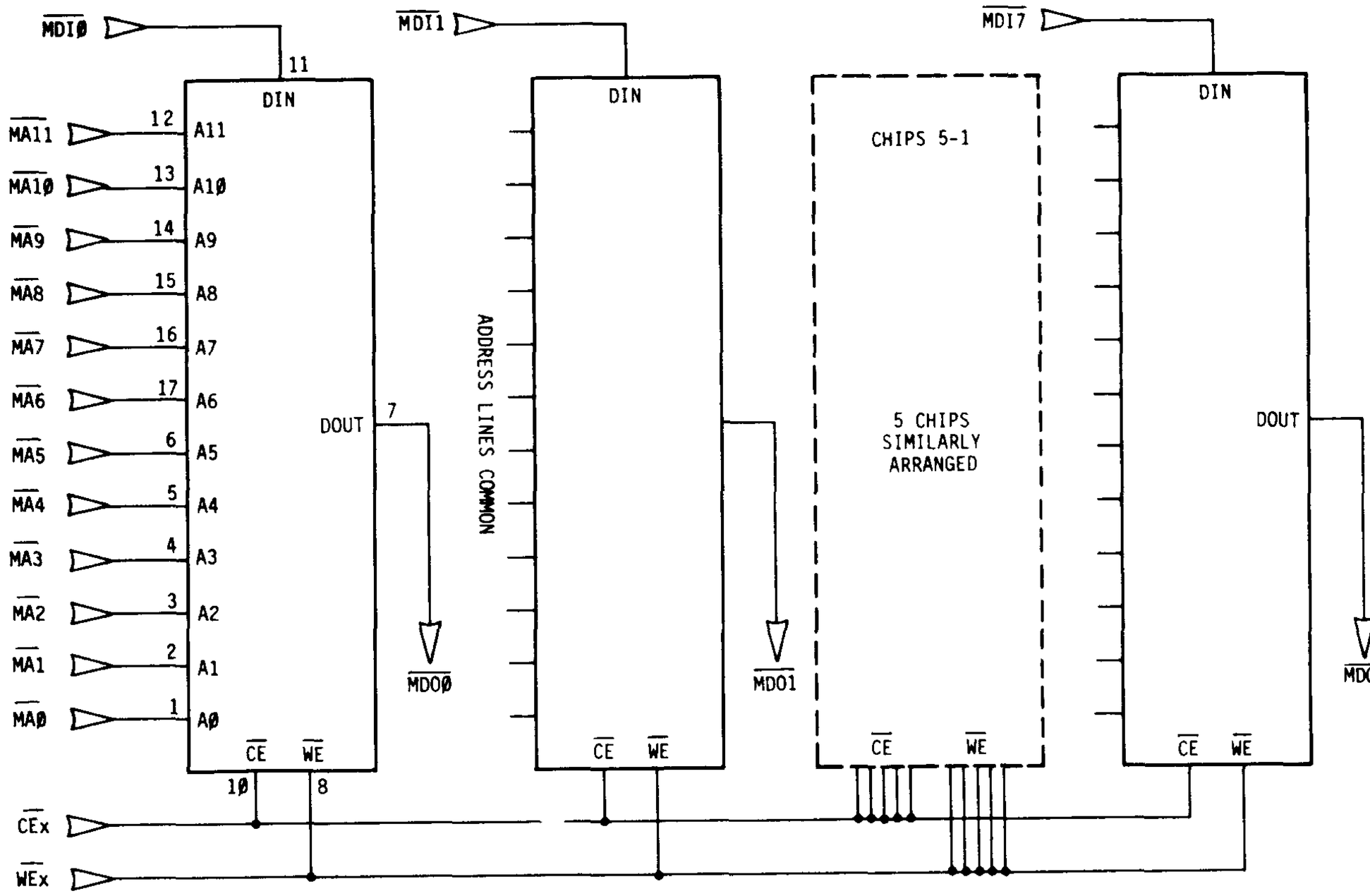
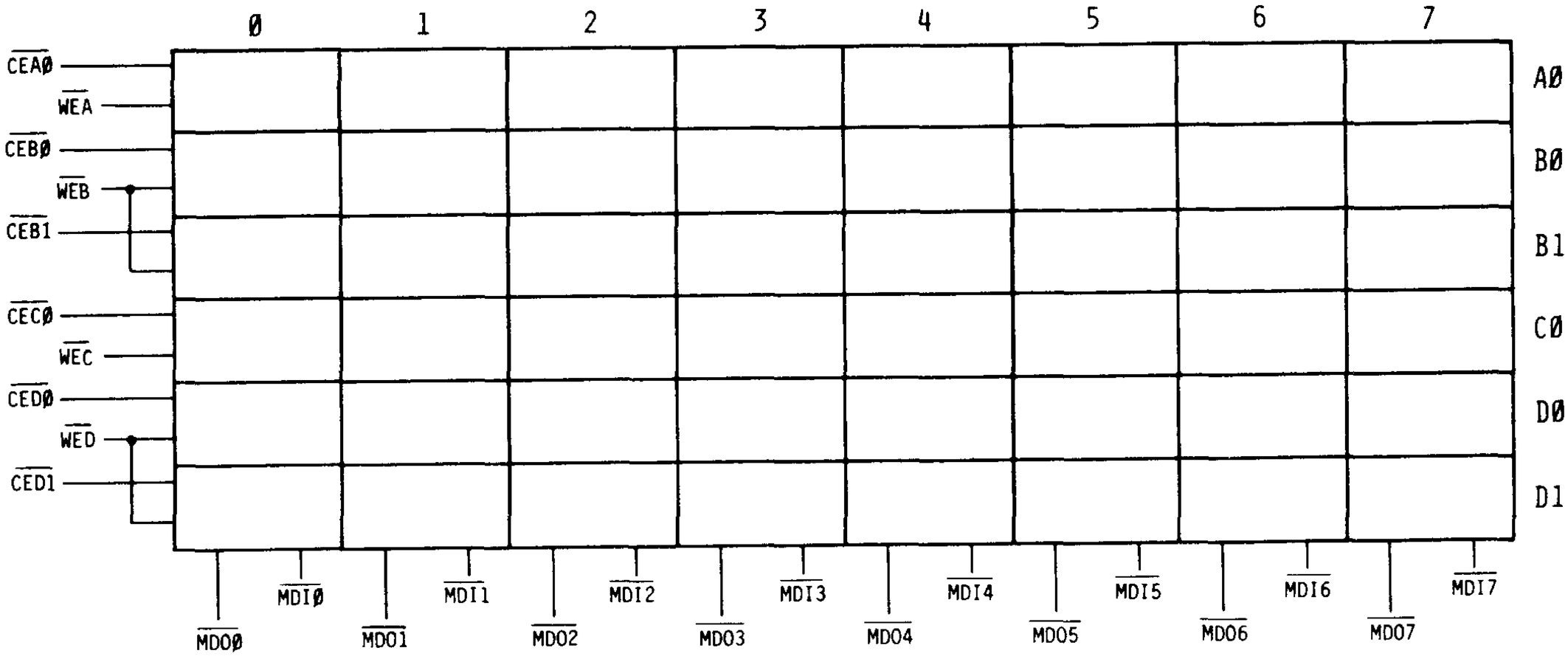
ECONORAM VII









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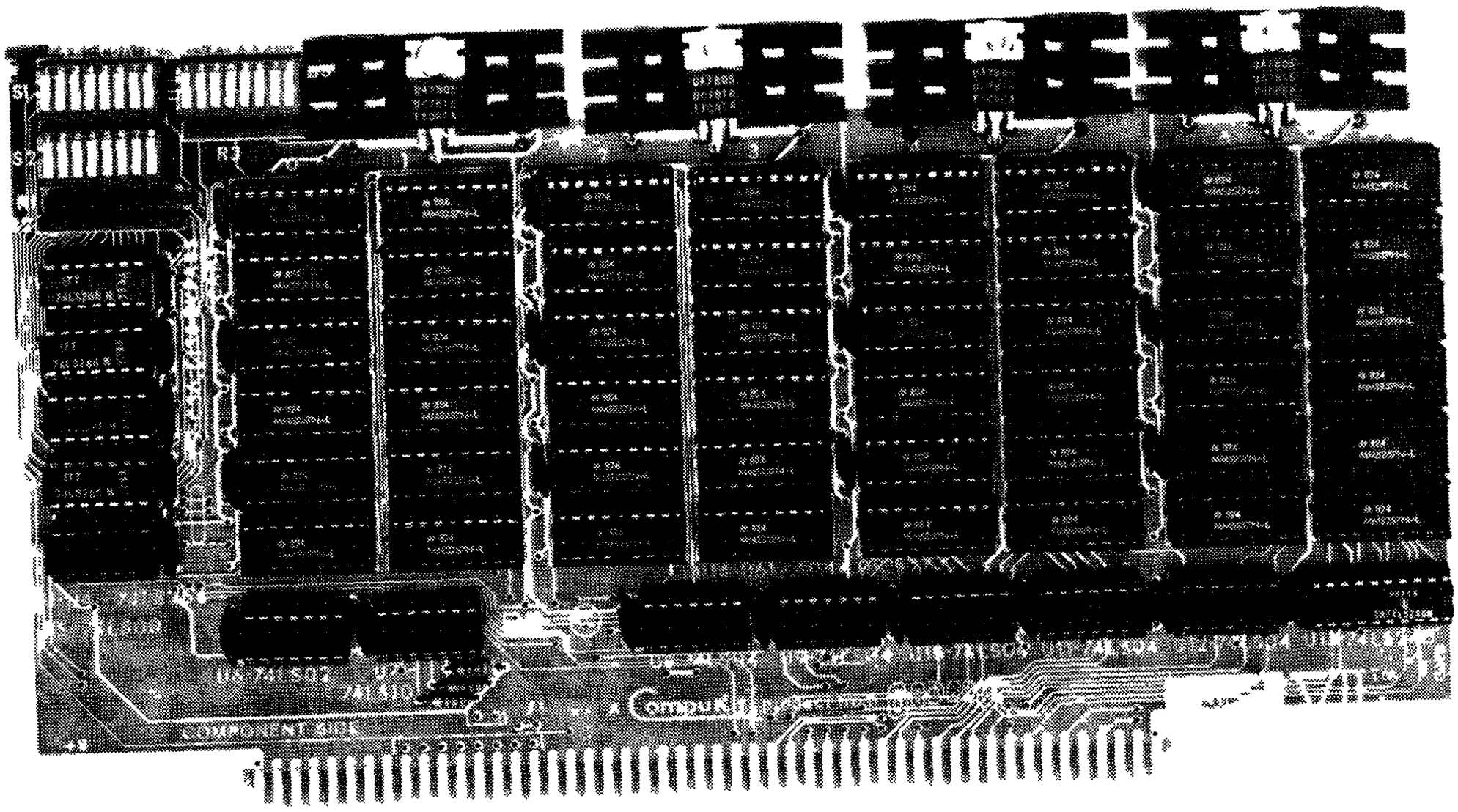
ECONORAM VII

ECONORAM VII T.M. A
USER'S MANUAL



24K x 8 static memory · S-100
using MM5257/TMS40L44 · 4MHz

122 mac

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Rev 3/79

ABOUT ECONORAM VII

Congratulations on your decision to purchase ECONORAM VII, a 24K x 8 memory board designed specifically for electrical and mechanical compatibility with the S-100 buss standard The S-100 buss currently is one of the most popular in the industry and by far the most prolific we believe this board, with the rest of the S-100 portion of the ECONORAM family, is one of the best memory boards available for that buss

We recommend that the parts in this kit be checked against the parts list for completeness and that these instructions be read through carefully before starting Completion of the assembly should take from one to four hours, depending on previous assembly experience, and upon completion, you will discover -- as thousands of satisfied ECONORAM owners have discovered -- the pleasure of using a fine memory board that just works, and works and works

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing ECONORAM VII welcome to the club

TECHNICAL OVERVIEW

This board incorporates proven static memory technology There are currently two popular types of memory being used in products such as this static and dynamic Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered There is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement

The individual memory ICs used on this board are grouped together to form four larger blocks of memory, two 4K X 8 and two 8K X 8 The 4K blocks may be addressed on any 4K boundary, and the 8K blocks on any 8K boundary by setting the starting locations with the on-board dip switch (no jumpers required) Additional features include write protect switches for each of the four blocks, a write strobe selection switch which allows use of memory in systems with or without a front panel (MWRITE strobe), allowance for use with or without the PHANTOM line, thorough capacitor bypassing of supply lines to suppress transients plus on-board regulation and heat-sinking for reliably cool operation All this and sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend

Parts List

Upon receipt of your kit, check your parts against the list below

☐ (1) Econoram VIIA circuit board

INTEGRATED CIRCUITS (note the following parts may have letter suffixes and prefixes along with the key numbers given below)

☐ (48) MM5257N-3L or TMS 40L44 (U14 - U61)
☐ (1) 74LS00 nand gate (U5)
☐ (1) 74LS10 3-input nand gate (U7)
☐ (1) 74LS02 nor gate (U6)
☐ (5) 74LS04 hex inverters (U8 - U12)
☐ (1) 74LS240 TRI-STATE® inverters (U13)
☐ (4) 74LS266 ex-nor o c (U1 - U4)
☐ (4) 7805 positive 5V regulators (U62 - U65)

OTHER ELECTRONIC COMPONENTS

☐ (3) S I P resistor packs (R1 - R3)*
☐ (3) 2 7K 1/4 watt resistors (red-violet-red, R4 - R6)
☐ (8) 39uF tantalum capacitors (C1 - C8)
☐ (25) ceramic disk bypass capacitors*

MECHANICAL COMPONENTS

☐ (61) low profile sockets*
☐ (3) dipswitch (S1 - S3)*
☐ (4) TO-220 heat sinks
☐ (4) 6-32 bolts
☐ (4) 6-32 lockwashers
☐ (4) 6-32 hex nuts
☐ (1) instruction booklet

*supplied already soldered to board

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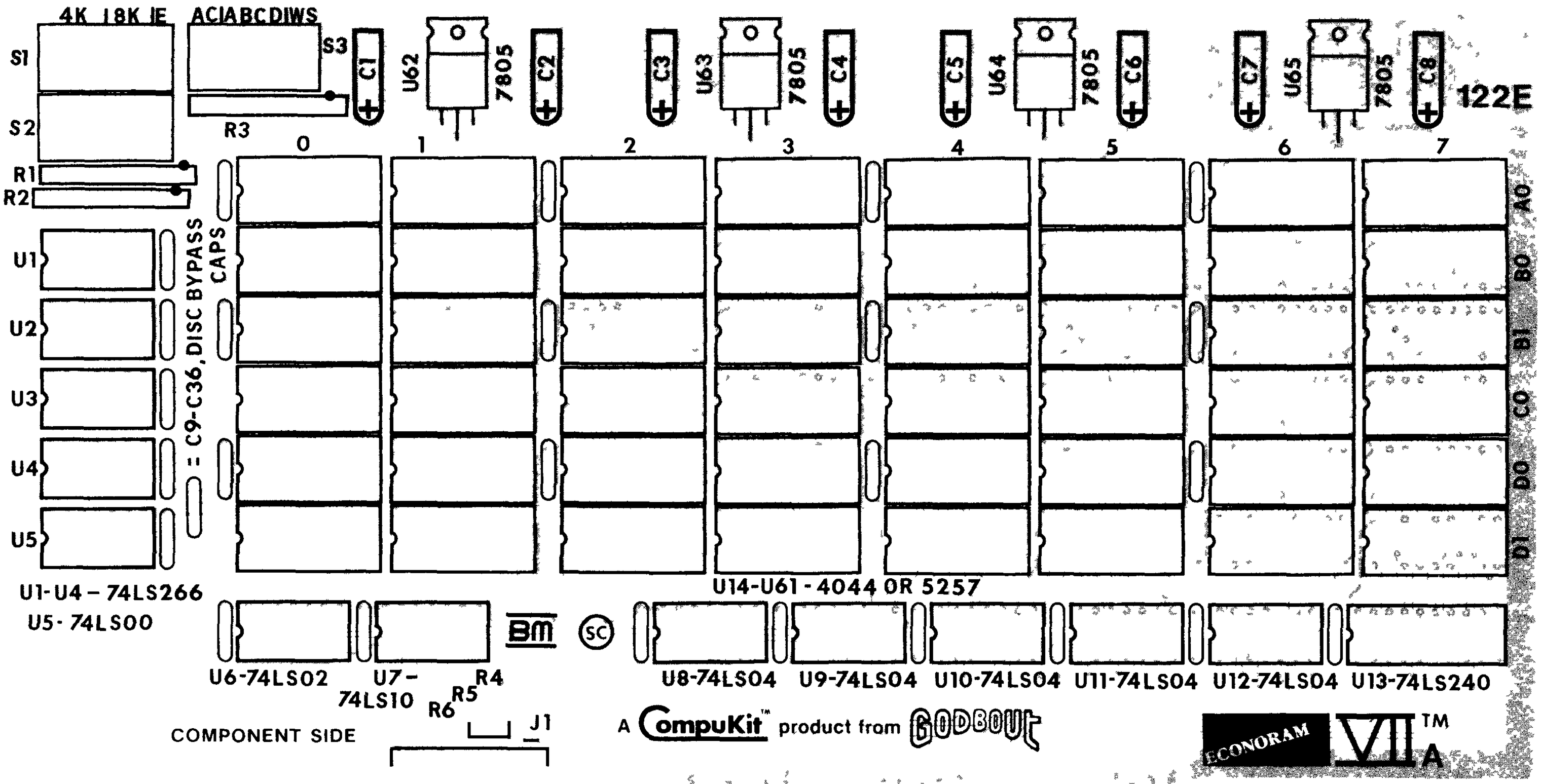

Component Layout

UP

MEMORY ADDRESS CONFIGURATION

This board is configured as two 4K blocks addressable on 4K boundaries and two 8K blocks independently addressable on 8K boundaries Switches S1 and S2 each select one 4K and one 8K block (switch S1 block A - 4K and block B - 8K, switch S2 block C - 4K and block D - 8K) as follows

4K SWITCH POSITION 1 2 3 4	4K STARTING ADDRESS	8K SWITCH POSITION 5 6 7	8K STARTING ADDRESS
Ø Ø Ø Ø	ØØØØ	Ø Ø Ø	ØØØØ
Ø Ø Ø 1	1ØØØ	Ø Ø 1	2ØØØ
Ø Ø 1 Ø	2ØØØ	Ø 1 Ø	4ØØØ
Ø Ø 1 1	3ØØØ	Ø 1 1	6ØØØ
Ø 1 Ø Ø	4ØØØ	1 Ø Ø	8ØØØ
Ø 1 Ø 1	5ØØØ	1 Ø 1	AØØØ
Ø 1 1 Ø	6ØØØ	1 1 Ø	CØØØ
Ø 1 1 1	7ØØØ	1 1 1	EØØØ
1 Ø Ø Ø	8ØØØ		
1 Ø Ø 1	9ØØØ		
1 Ø 1 Ø	AØØØ		
1 Ø 1 1	BØØØ		
1 1 Ø Ø	CØØØ		
1 1 Ø 1	DØØØ		
1 1 1 Ø	EØØØ		
1 1 1 1	FØØØ		

Ø = OFF

1 = ON

In addition, position 8 on each switch enables (OFF) or disables (ON) the associated 8K block Positions 1 and 2 of switch S3 disable/enable the 4K blocks A and C respectively

MEMORY PROTECT SWITCHES

Switch S3 positions 3-6 are write enable switches Conversely they may be used for manual write protection of the memory Each position 3, 4, 5 and 6 is associated wih one memory block A B, C and D respectively Any combination of these four swtiches may be ON write enabling or OFF write protecting the particular block

WRITE STROBE SELECT SWITCHES

Switch S3 positions 7 and 8 select write strobe S3-8 ON causes $\overline{\text{PWR}}$ to qualify the memory for write commands S3-7 ON causes MWRITE to qualify the memory for write commands In normal operations with systems which have front panels ie , Altair, Imsai etc , or others which generate MWRITE with or without front panels use MWRITE All others use $\overline{\text{PWR}}$ Positions 7 and 8 both ON at the same time will ground MWRITE on the buss This condition must be avoided if MWRITE is present

MEMORY TESTING

If the memory board seems to be working properly the Memory Testing Routine (page 11) can be used to give the board a more thorough workout It is rather slow but will do the job well It can be entered via editor/assembler or front panel switches

The routine is set up to test 24K from 4000 hex up to AØØØ hex This may be changed by entering a different starting address at STRT (3001 - 3002) and/or a different end address at END (3004 - high order byte only)

If the memory passes the test it starts over again You may on the other hand, insert a jump instruction at "MARK to some user routine or if desired the user may enter an output instruction or, can do a notification routine at "MARK to show successful completion and restart

If the memory fails the test, critical information is stored and the routine enters a software "HALT ', that is a "jump to here at "SHLT Front panel lights, if any, will show this state The user may then use the front panel or dump routines to display the following stored failure info

3069*	"FDE	=	D E pair D is the fill character and E is the test character
306B*	"FHL	=	H, L pair the failure address
306D*	FOUT	=	the data expected at this address
306E*	"FIN	=	the data read from the address

* address from *Memory Testing Routine Listing*

The user may replace the "jump at "SHLT with a jump to a display or notification routine

The difference between "FOUT" and "FIN ' should indicate which bit is failing, indicating which chip or area is causing the problem

This test will find most of the harder to distinguish errors

PHANTOM LINE

In response to increasing numbers of users who have requested inclusion of PHANTOM LINE , buss pin 67 which is often used for implementing power on jump features This board is designed for use with active or inactive PHANTOM lines

CAUTION

Some manufacturers use PHANTOM line (buss pin 67) for a refresh signal This will conflict with the PHANTOM feature, and cause boards with PHANTOM to fail If your system has this conflict it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards

The PHANTOM feature may be disabled by cutting the trace on the back of the PC board between pads for J1 It may be reactivated at any time simply by installing a jumper at J1 (see Figure 11)

If you want the PHANTOM feature the conficting refresh signal may be eliminated (IF NOT USED ELSEWHERE IN THE SYSTEM) by cutting the trace connected to buss pin 67 on the CPU board *BE SURE OF YOUR SYSTEM CONFIGURATION BEFORE CUTTING ANY TRACES*

ME

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MEMORY TESTING ROUTINE

```
3000 21 00 40          0010 STRT LXI  H,4000H
3003 3E A0             0020 END  MVI  A,0A0H
3005 32 6E 30          0030      STA  FIN
3008 3E 10             0040      MVI  A,10H
300A 84                0050      ADD  H
300B 4F                0060      MOV  C,A
300C 16 00             0070      MVI  D,0
300E 1E FF             0080      MVI  E,0FFH
3010 22 65 30          0090 DONE SHLD STAD
3013 AF                0100      XRA  A
3014 47                0110      MOV  B,A
3015 7B                0120 SCND MOV  A,E
3016 5A                0130      MOV  E,D
3017 57                0140      MOV  D,A
3018 79                0150      MOV  A,C
3019 2A 65 30          0160      LHLD STAD
301C 72                0170 FILL MOV  M,D
301D 23                0180      INX  H
301E BC                0190      CMP  H
301F C2 1C 30          0200      JNZ  FILL
3022 2A 65 30          0210      LHLD STAD
3025 73                0220 NEXT MOV  M,E
3026 7B                0230      MOV  A,E
3027 BE                0240      CMP  M
3028 C2 6F 30          0250      JNZ  FAIL
302B 79                0260      MOV  A,C
302C 23                0270      INX  H
302D 94                0280      SUB  H
302E C2 4D 30          0290      JNZ  NDON
3031 B8                0300      CMP  B
3032 44                0310      MOV  B,H
3033 CA 15 30          0320      JZ   SCND
3036 3A 66 30          0325      LDA  STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA  FIN
303F B9                0350      CMP  C
3040 CA 00 30          0360      JZ   STRT
3043 79                0370      MOV  A,C
3044 67                0380      MOV  H,A
3045 2E 00             0390      MVI  L,0
3047 C6 10             0400      ADI  10H
3049 4F                0410      MOV  C,A
304A C3 10 30          0420      JMP   DONE
304D 22 67 30          0430 NDON SHLD NXAD
3050 7A                0440 LOPB MOV  A,D
3051 BE                0450 LOPA CMP  M
3052 C2 6F 30          0460      JNZ  FAIL
3055 2C                0470      INR  L
3056 C2 51 30          0480      JNZ  LOPA
3059 79                0490      MOV  A,C
305A 24                0500      INR  H
305B BC                0510      CMP  H
305C C2 50 30          0520      JNZ  LOPB
305F 2A 67 30          0530      LHLD NXAD
3062 C3 25 30          0540      JMP  NEXT
3065                   0550 STAD DS   2
3067                   0560 NXAD DS   2
3069                   0570 FDE  DS   2
306B                   0580 FHL  DS   2
306D                   0590 FOUT DS   1
306E                   0600 FIN  DS   1
306F 22 6B 30          0610 FAIL SHLD FHL
3072 32 6D 30          0620      STA  FOUT
3075 7E                0630      MOV  A,M
3076 32 6E 30          0640      STA  FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD FDE
307D C3 7D 30          0670 SHLT JMP SHLT
3080                   0680 *
```

CIRCUIT DESCRIPTION

The heart of Econoram VII is the MM5257/TMS4044 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC) Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts

These ICs are arranged in rows that are 8 ICs wide This way, each row can store 4K x 8 bits of information Paralleling 6 of these rows together produces a total memory storage of 24K x 8 bits (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array)

Now that we have this storage, there are still other aspects we must consider First, we need to address a specific location in memory, and, we need to be able to *write* data into the memory, or *read* data from the memory

The schematics on pages 8 and 9 show the address circuitry along with the other Econoram VII circuitry Each memory IC requires 12 address bits (A0-A11) to access any one of the 4096 bits available in the IC These address bits are generated by the CPU and are buffered by a number of inverters After buffering, a particular address is presented to all IC address selection pins However, we additionally need to select which particular row of ICs is to react to the given address This requires 4 more address bits (A12-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array)

When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss) Data to be read on to the data buss from memory passes through 8 TRI-STATE® inverting buss drivers, when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or ' disconnected ' state

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines If these transients work their way into the logic circuitry, problems can appear To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC

This board is guaranteed to operate at 4MHz over the full temperature range (0° - 70° C ambient) and to draw less than 2500 mA (2 5 amps) Our typical measured currents were less than 1210 mA at cold start-up, rapidly decreasing to around 1600-1900 mA, depending on the surrounding temperature We have heard similar reports from the people already using these boards

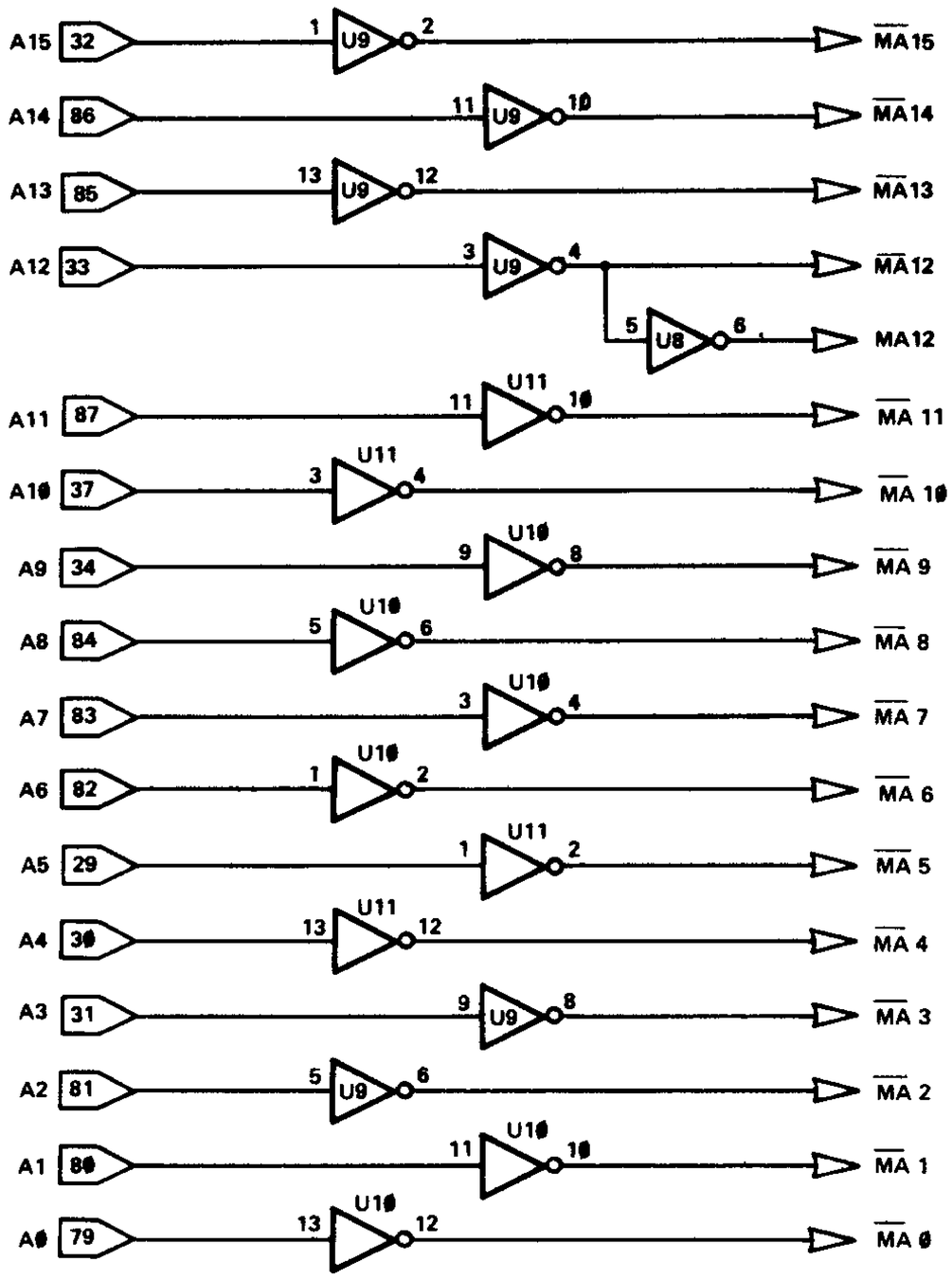
It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards

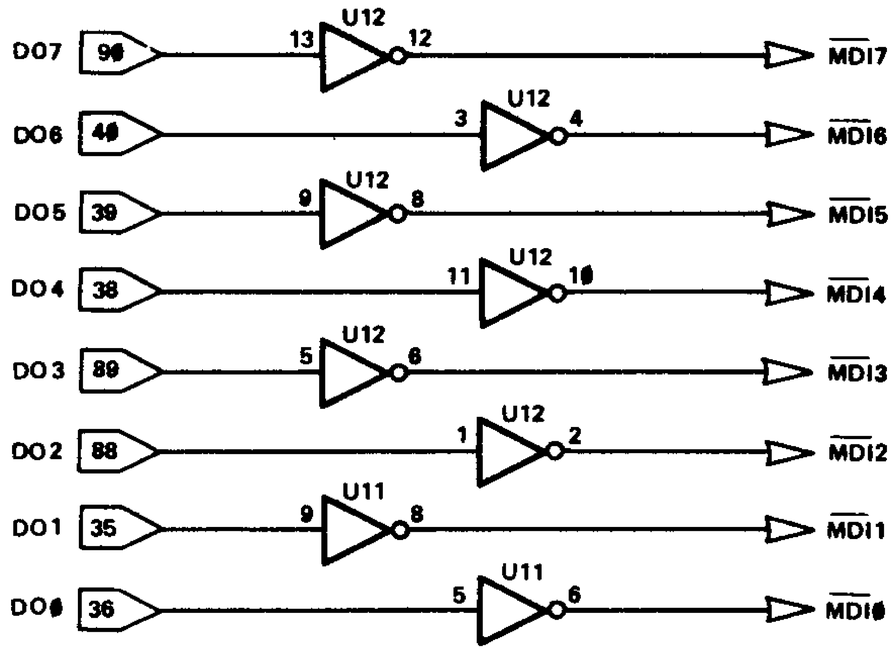
THANK YOU

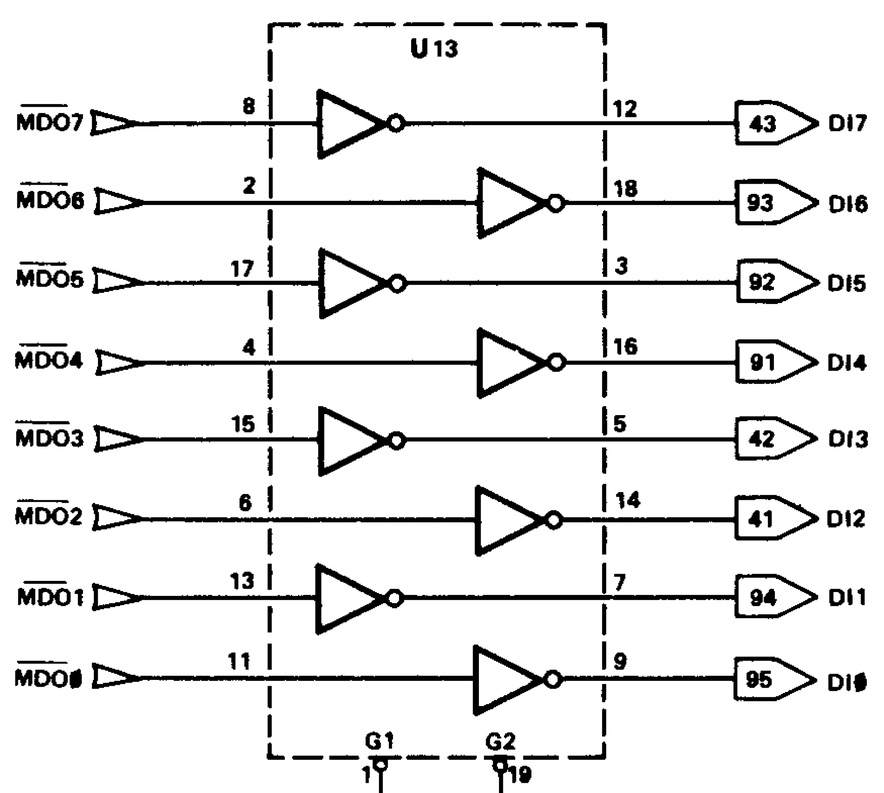
This board is the result of much time, work and experience on the part of a number of people

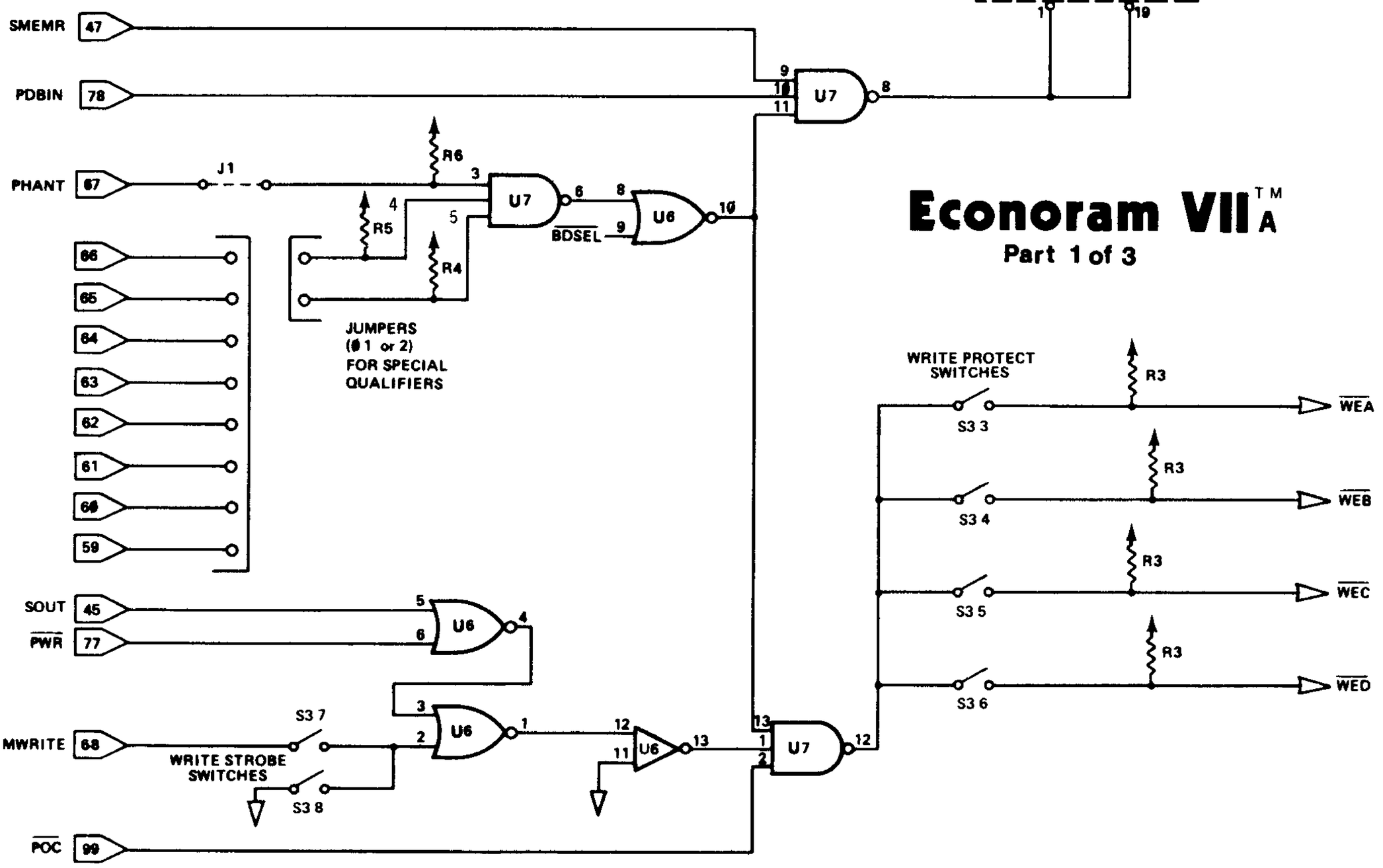
We strive for a board that doesn't just work the first time, but continues to give reliable operation for a long time If we can be of any help to you in applying this board, or if you have any questions, please let us know As always, we solicit your comments, letters, and new product suggestions

HAPPY COMPUTING!









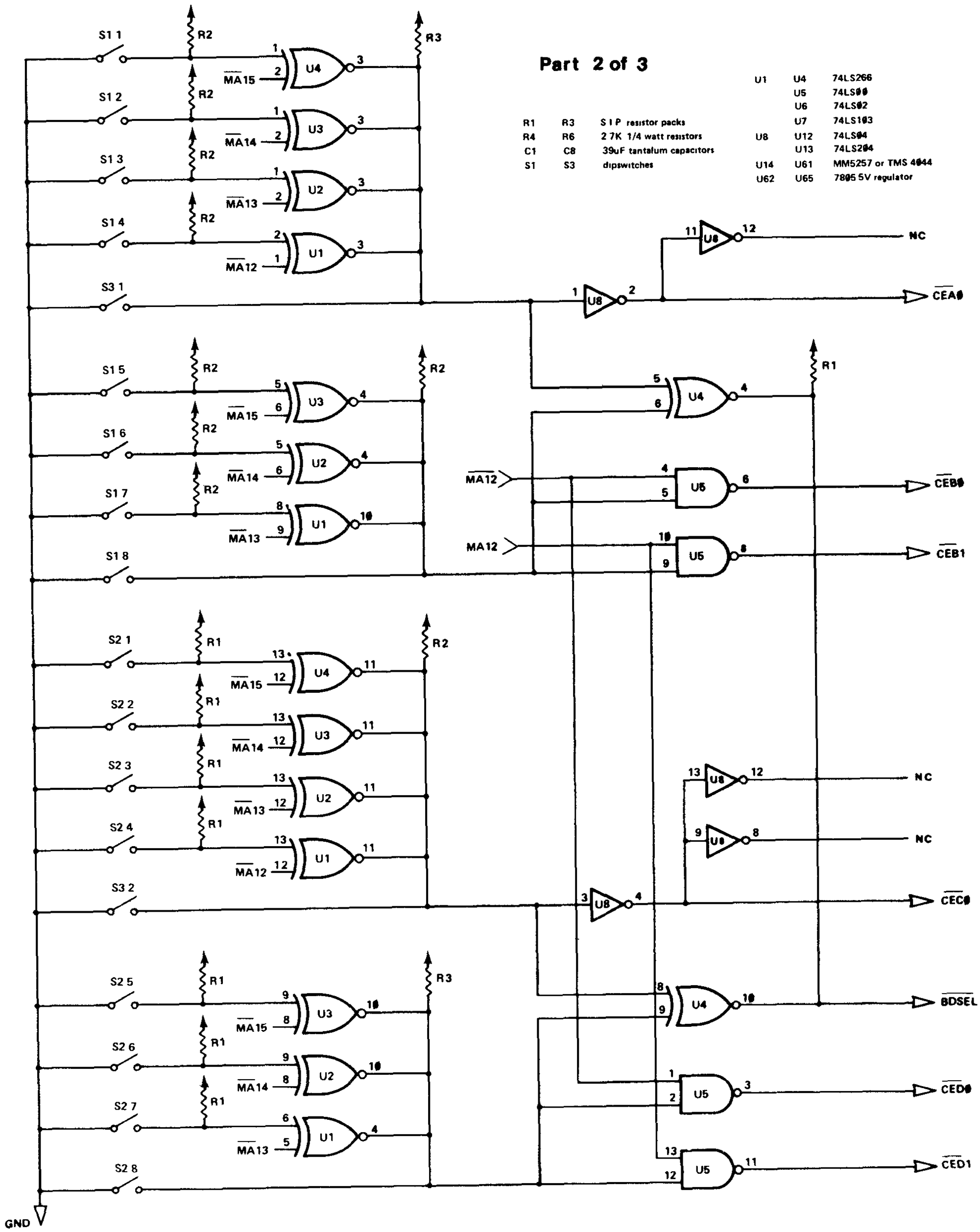
Econoram VII A™

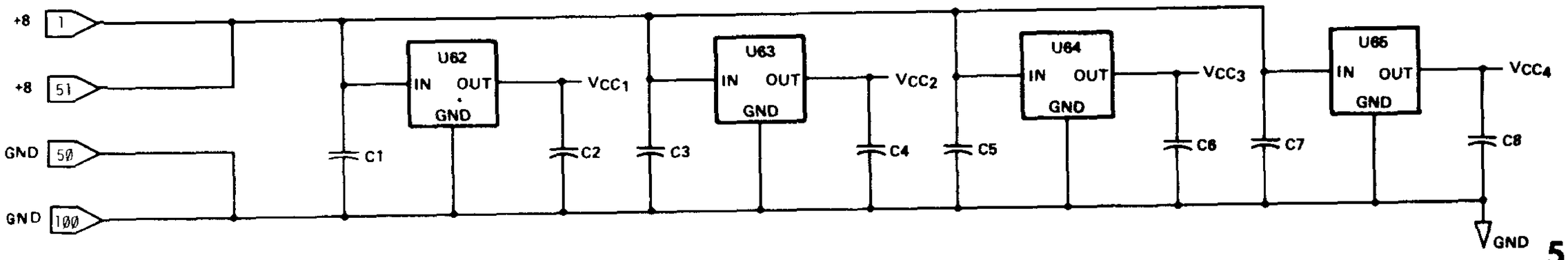
Part 1 of 3

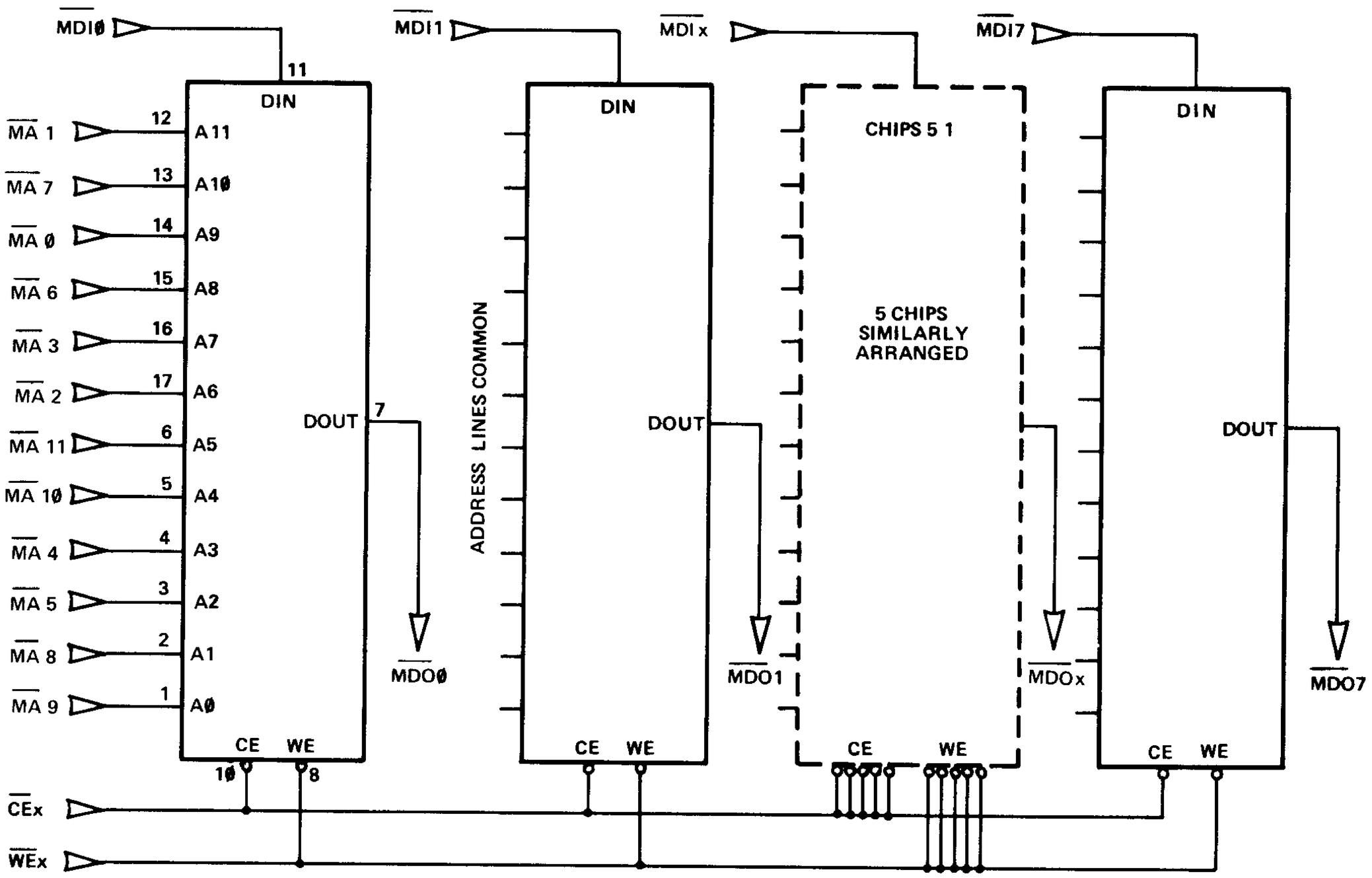
Part 2 of 3

R1	R3	S I P resistor packs
R4	R6	2 7K 1/4 watt resistors
C1	C8	39uF tantalum capacitors
S1	S3	dipswitches

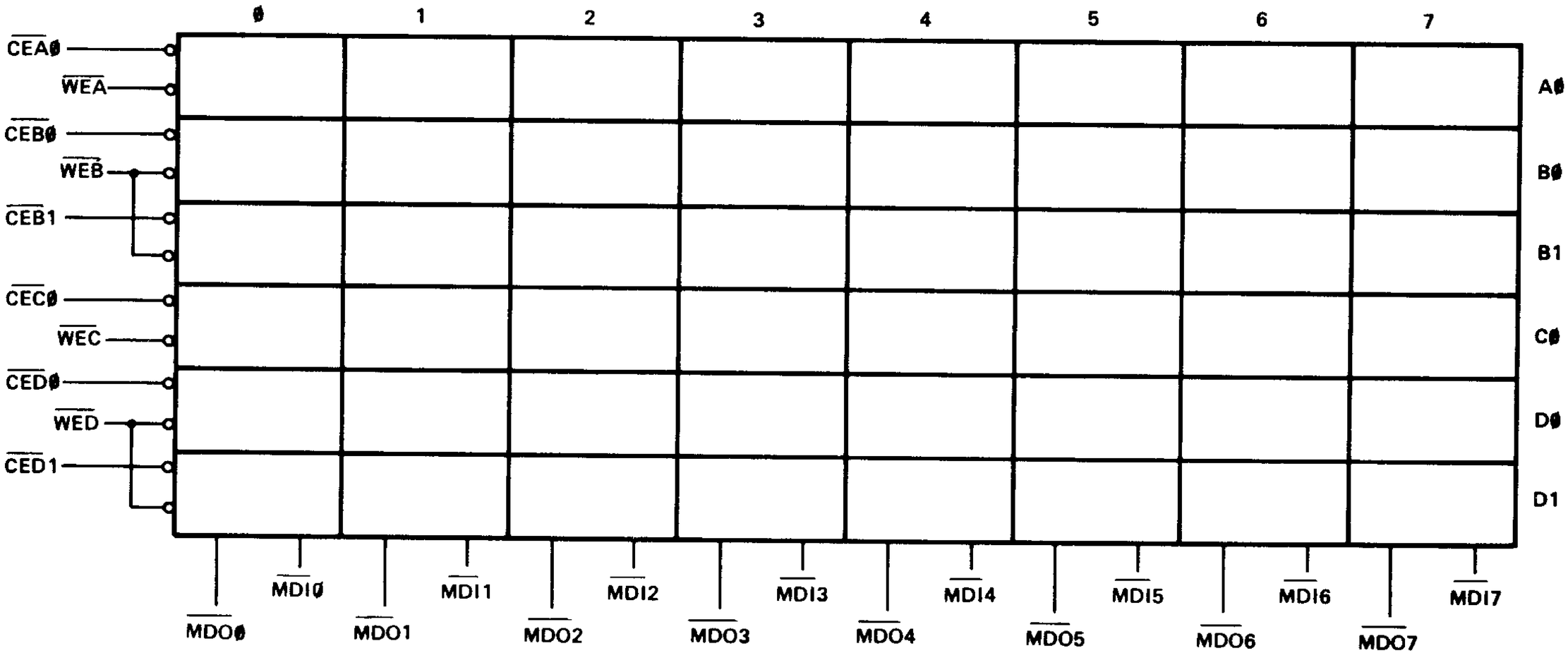
U1	U4	74LS266
	U5	74LS00
	U6	74LS02
	U7	74LS103
U8	U12	74LS04
	U13	74LS204
U14	U61	MM5257 or TMS 4044
U62	U65	7805 5V regulator



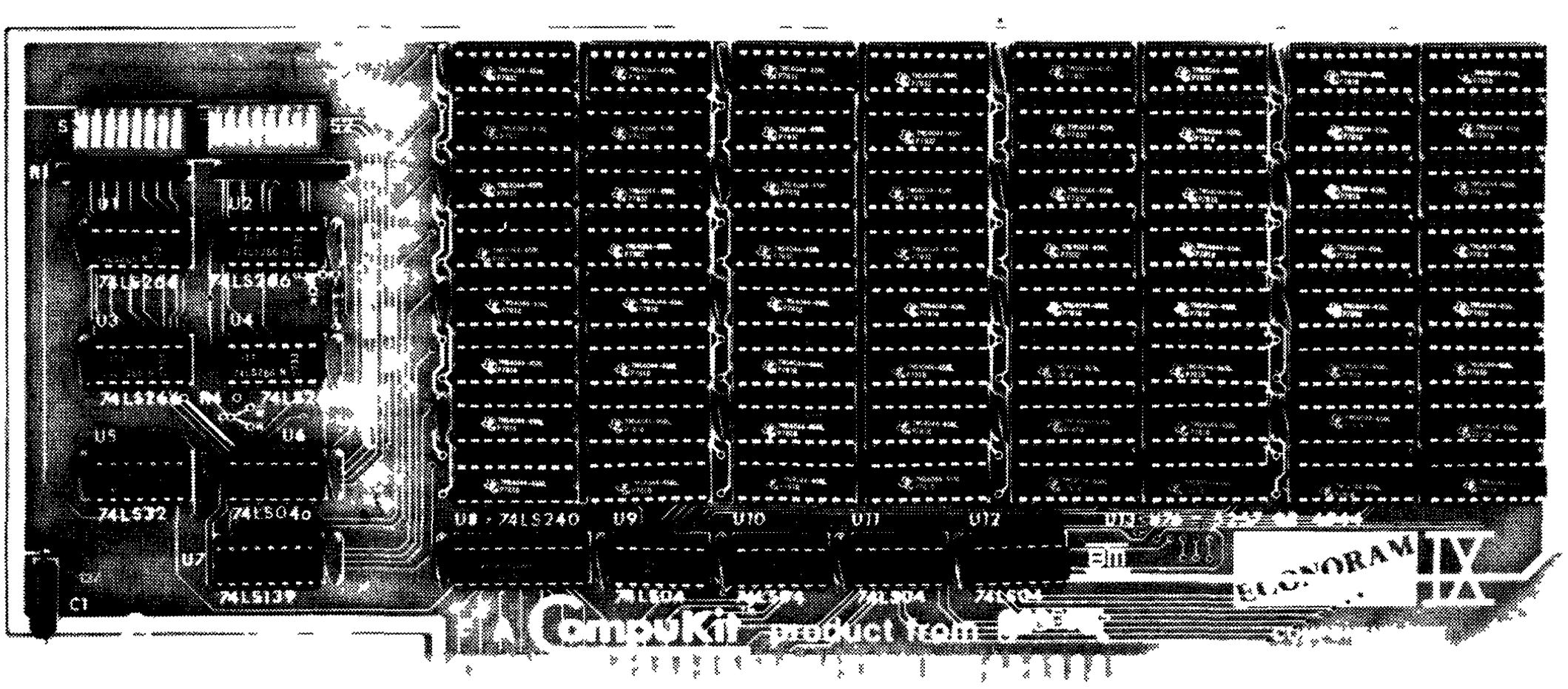




BIT POSITION



ECONORAM IX™
USER'S MANUAL



32K x 8 static memory
Digital Group Buss
using MM5257/TMS40L44 · 4 MHz

A CompuKit™ product from GODBOUT

ABOUT ECONORAM IX

Congratulations on your choice of the ECONORAM IX, a 32K x 8 memory board designed specifically for electrical and mechanical compatibility with the Digital Group buss

All IC sockets, bypass capacitors, and other components, are soldered on the board in order to eliminate the most tedious and error-prone aspects of the assembly of this type of kit Assembly should take only an hour or so We encourage you to take the time to familiarize yourself with the features and the circuit design of the board prior to assembly Several of the features - such as independent block organization, easy switch assignment of blocks to the desired memory address location, switch selectable block disable and write protect - have been unavailable to Digital Group System owners until now

Upon completion of the board you will discover - as thousands of satisfied ECONORAM owners have discovered - the pleasure of using a fine memory board that just works, and works, and works

As the first company to nationally offer memory kits to computer hobbyists, we thank you for choosing ECONORAM IX welcome to the club

TECHNICAL OVERVIEW

This board incorporates proven static memory technology using industrial design techniques and generous safety factors to avoid marginal operation

Of the two currently popular approaches to memory design - static and dynamic - static memories are the overwhelming choice in applications where speed, simplicity, ease of use and reliability must be considered

In order to retain data, dynamic memory must be continually refreshed This board, due to its static design, will retain data as long as power is applied This is of particular interest to Digital Group owners, since the Digital Group system makes use of the unique ability of the Z-80 CPU to take care of dynamic memory refresh rather than using refresh circuitry on each individual memory board Unfortunately, while this is a valid and economical approach, it precludes the use of the normal system RESET or the use of the WAIT line since the CPU cannot continue to refresh the memory while RESET is held or CPU WAIT is used For instance, in order to use the Digital Group disk controller with dynamic memory, both the controller board and the CPU board must be modified, an extra input port bit is required, and special software is necessary The Econoram IX is not subject to the above problems because of its static design

The individual memory chips used on this board are grouped together to form four blocks of memory two 4K blocks, one 8K block and one 16K block Each block may be assigned to any of its respective boundaries (i e., either 4K block to any 4K boundary, the 8K block to any 8K boundary and the 16K block to any of the four 16K boundaries) by setting the starting address with the on-board DIP switches (no jumpers required) Additional features include a write-protect switch for the 16K block and disable switches for both the 8K and 16K blocks Also included are jumper pads for adapting the board to non-standard polarities of the WRITE strobe and the ROM strobe (the signal which disables the board when the bootstrap EROM is being accessed) No jumpers are required for standard Digital Group systems, since traces have been provided to connect the pads for the standard signal polarities

Extra heavy power supply traces, generous bypassing of power supply lines, sockets for all integrated circuits, careful layout and a double-sided, solder-masked printed circuit board with complete component and switch legends make this a versatile memory board which will give exceptionally long and trouble-free service

Parts List

Upon receipt of your kit, check your parts against the list below

☐ (1) Econoram IX circuit board

INTEGRATED CIRCUITS (note the following parts may have letter suffixes and prefixes along with the key numbers given below)

☐ (64) MM5257 or TMS40L44 memories (U13-U76)
☐ (5) 74LS04 hex inverter (U6-U12)
☐ (1) 74LS32 quad 2-input OR gate (U5)
☐ (1) 74LS139 decoder / demultiplexer (U7)
☐ (1) 74LS240 TRI-STATE® buffer (U8)
☐ (4) 74LS266 ex-NOR o c (U1-U4)

OTHER ELECTRONIC COMPONENTS

☐ (2) S I P resistor packs (R1, R2)*
☐ (2) 2K7 ohm ¼ watt resistors (red-violet-red R3, R4)*
☐ (1) 39 μF tantalum capacitor (C1)*
☐ (28) ceramic capacitors*

MECHANICAL COMPONENTS

☐ (76) low profile sockets*
☐ (2) 8 pole dipswitches (S1, S2)*
☐ (1) user manual

*supplied already soldered to board

MEMORY ADDRESS ASSIGNMENT

This board is configured as two 4K blocks, one 8K block and one 16K block Each 4K block may be assigned to any area of memory beginning on a 4K boundary (0K, 4K, 8K, 56K, etc) The 8K block may be assigned to any 8K boundary (0K, 8K, 32K, 40K, etc) and the 16K block on any 16K boundard (0K, 16K, 32K or 48K) The only other limitation is that the assigned locations should not overlap each other or any other RAM in your system

NOTE In the following table, S1 is the first dipswitch and S2 if the second dipswitch Each dipswitch has eight individual switch sections numbered 1 through 8 "0" = switch off and "1" = switch on S2-4, -7 and -8 are not used for address selection and are explained in the next section

STARTING ADDRESS		SWITCH POSITION		
		BLOCK A, B	C	D
hex	(split octal)	4K	8K	16K
		A S1- 1234	S2- 123	S2- 56
		B S1- 5678		
0K 0000	(000/000)	0000	000	00
4K 1000	(020/000)	0001		
8K 2000	(040/000)	0010	001	
12K 3000	(060/000)	0011		
16K 4000	(100/000)	0100	010	01
20K 5000	(120/000)	0101		
24K 6000	(140/000)	0110	011	
28K 7000	(160/000)	0111		
32K 8000	(200/000)	1000	100	10
36K 9000	(220/000)	1001		
40K A000	(240/000)	1010	101	
44K B000	(260/000)	1011		
48K C000	(300/000)	1100	110	11
52K D000	(320/000)	1101		
56K E000	(340/000)	1110	111	
60K F000	(360/000)	1111		

NOTE If the desired starting address is represented as a binary number, the switch setting represents the 2, 3, or 4 most significant bits of that address Once you become familiar with the addresses of the various boundaries, you will find it easy to re-assign various boundaries, you will find it easy to re-assign memory blocks without referring to the above table

BLOCK DISABLE SWITCHES

Switch S2-4 and S2-7 are disable switches for the 8K ("C") block and the 16K ("D") block respectively These switches should be OFF for normal operation If either switch is moved to the ON position, the corresponding block is effectively removed from memory (although as long as power is maintained, data previously stored in the block is not disturbed and may be re-accessed by returning the switch to the OFF position) This feature is primarily designed to allow the use of a partially populated board (any block without a full complement of memory ICs must be disabled to prevent conflicts if other RAM in the system is assigned an address which overlaps that of the incomplete block) However, the disable switch can also be used as an aid in trouble-shooting and as a *pseudo write-protect* to protect a section of code while de-bugging another program

WRITE ENABLE SWITCH

Switch S2-8 is the WRITE ENABLE switch for the 16K ("D") block of memory This switch should be ON for normal operation However, if the switch is placed in the OFF position after data has been written into this block, the block will be WRITE PROTECTED and the data can be read but not changed This is a very powerful tool for program development and debugging, since the data in the write protected block cannot be destroyed by a wayward program You must remember, however, that data buffers which must be changed by the program must reside outside the protected area

MEMORY TESTING

An excellent memory testing routine is distributed by the Digital Group which will test both the data integrity and the speed of the memory If this is unavailable to you, we have included a test route (page 10) which gives the board a somewhat slow but thorough workout It can be entered in machine code through the programming options in your operating system or in source code through an assembler (to use the Digital Group Assembler the mnemonics must be changed from INTEL 8080 mnemonics to Zilog Z-80 mnemonics)

The routine is initially set up to test a 32K segment of memory starting at 4000 hex and ending at BFFF hex The starting address may be changed by entering the desired start address at 3001 and 3002 hex (low byte first) The ending address may be changed by entering the high byte of the address following the last tested byte at 3004 hex (if the test is to end at E7FF hex, enter E8 at 3004)

If the memory passes the test, it starts over again Three bytes have been left open at "MARK" (3039 hex) to enable you to insert a call to a routine to display the test address if desired

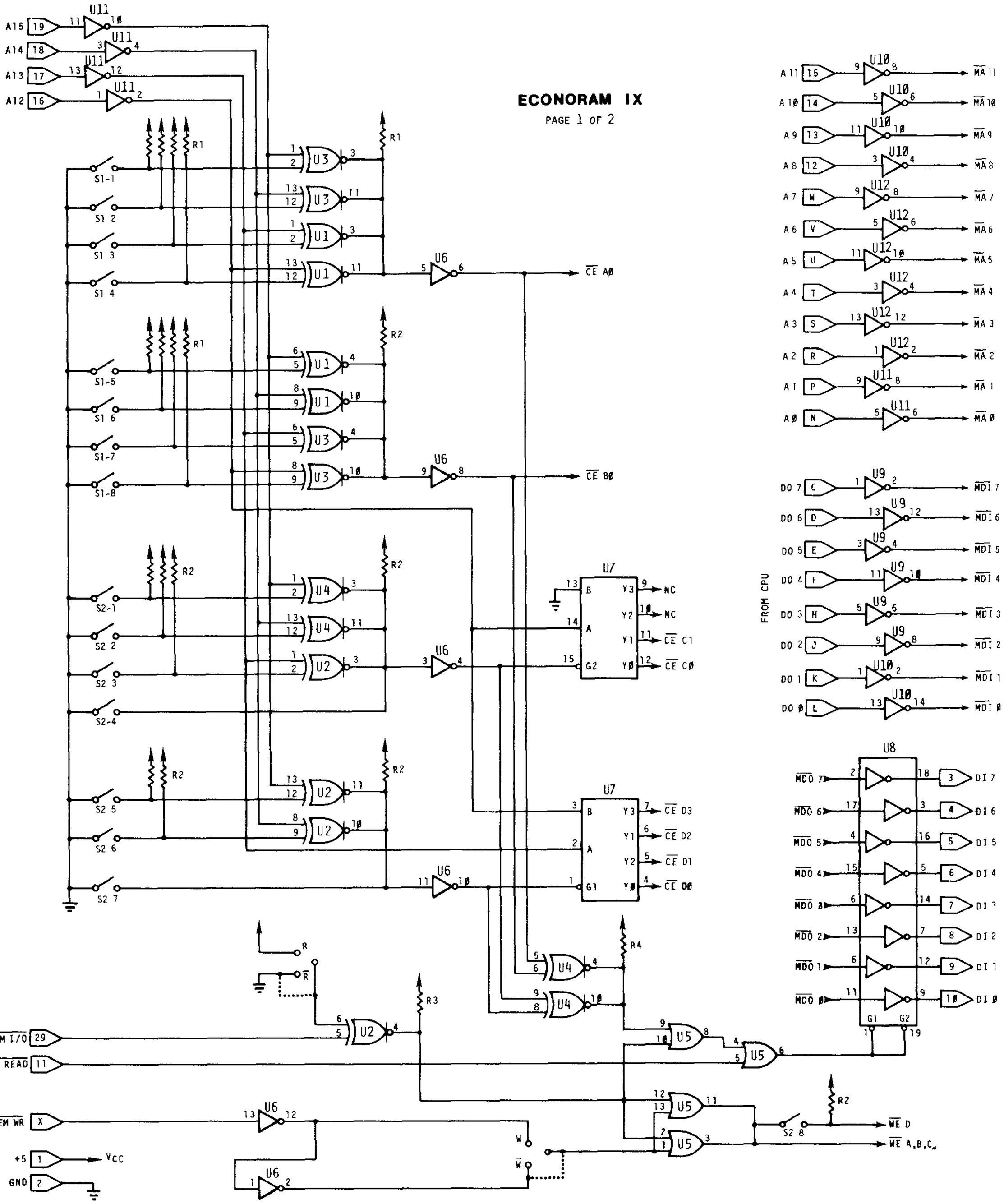
If any portion of memory fails the test, critical information is stored and the routine enters an endless loop at "SHLT" (307D hex) This "jump to itself" may be replaced by a "jump to a routine" which notifies you of the failure, or the loop may be terminated by a RESET to your monitor, from which you can examine the following locations where the information regarding the failure is stored·

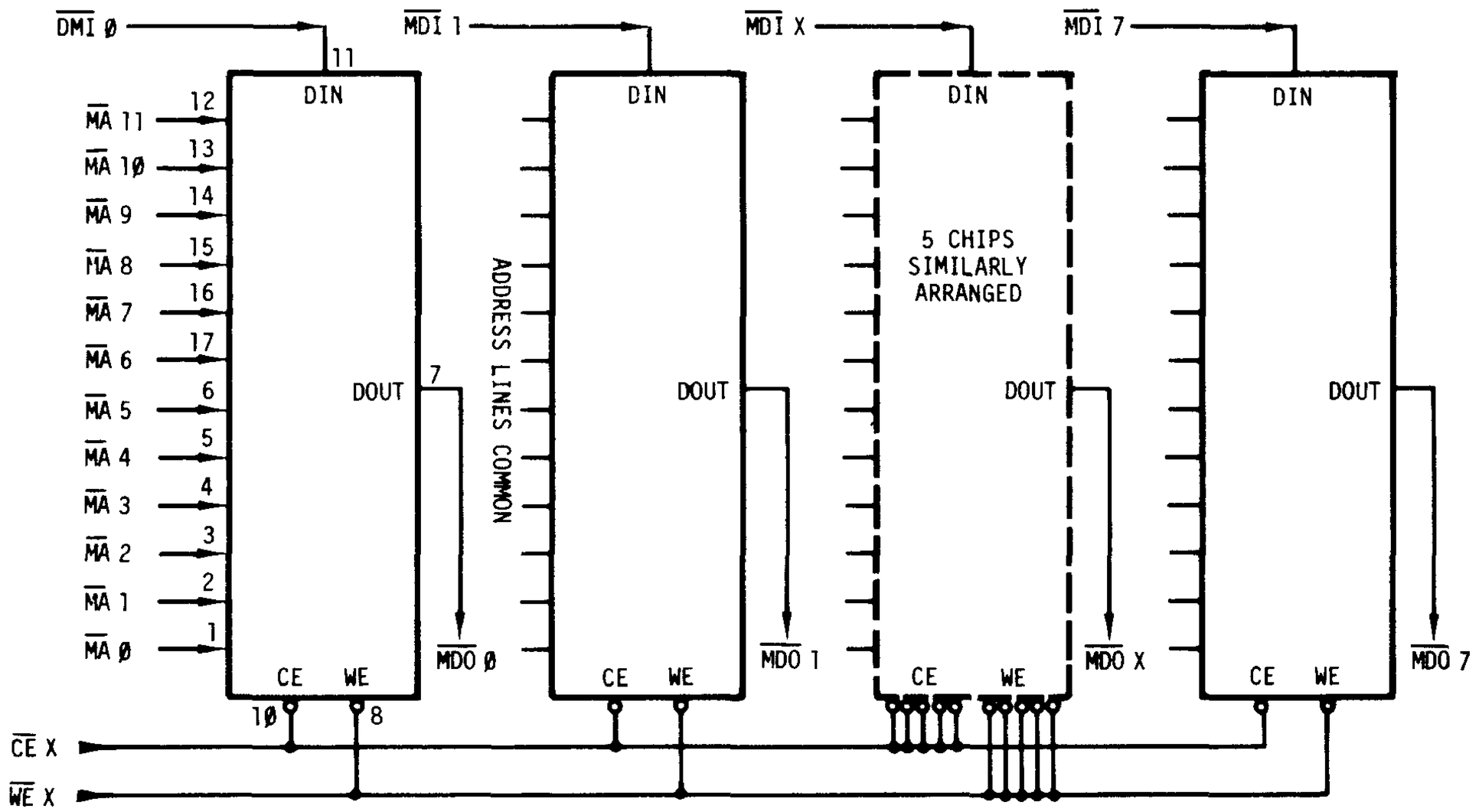
3069	"FDE"	test character
306A	"FDE"+1	fill character
306B	"FHL"	failure address (low-high)
306D	"FOUT"	data expected at this address
306E	"FIN"	data read from this address

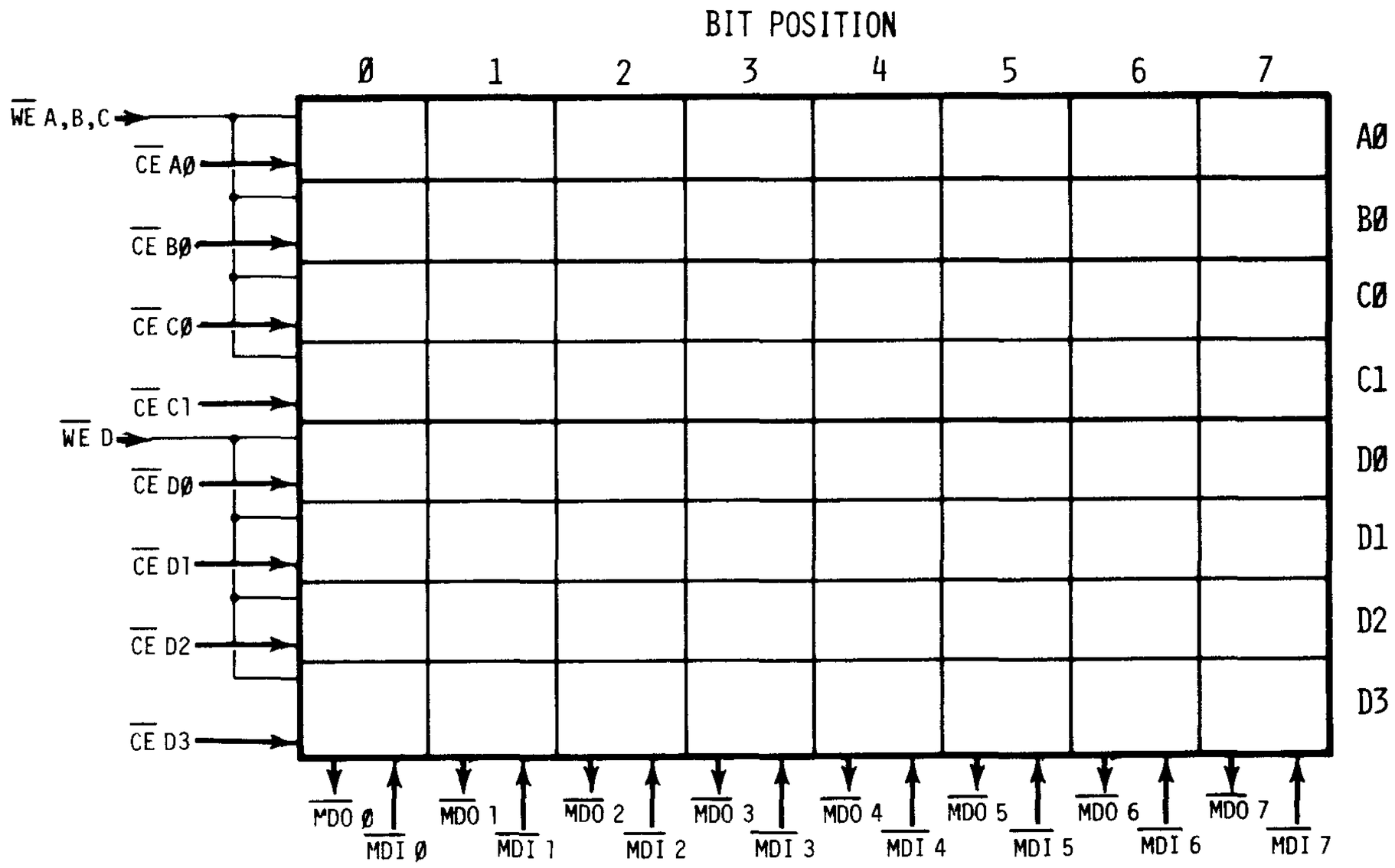
The difference between "FOUT" and "FIN" should indicate which bit is failing, and together with "FHL" should point to the bad memory IC If several bits are different, the problem could be an address decoding problem caused by the failure of one of the support chips

ECONORAM IX

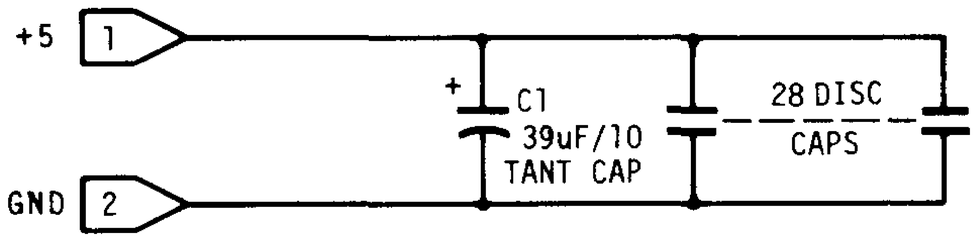
PAGE 1 OF 2







ARRAY CONSISTS OF 64 (1 x 4096) STATIC RAMS



MEMORY TESTING ROUTINE

```
3000 21 00 40          0010 STRT LXI   H,4000H
3003 3E A0             0020 END  MVI   A,0A0H
3005 32 6E 30          0030      STA   FIN
3008 3E 10             0040      MVI   A,10H
300A 84                0050      ADD   H
300B 4F                0060      MOV   C,A
300C 16 00             0070      MVI   D,0
300E 1E FF             0080      MVI   E,0FFH
3010 22 65 30          0090 DONE SHLD  STAD
3013 AF                0100      XRA   A
3014 47                0110      MOV   B,A
3015 7B                0120 SCND MOV   A,E
3016 5A                0130      MOV   E,D
3017 57                0140      MOV   D,A
3018 79                0150      MOV   A,C
3019 2A 65 30          0160      LHLD  STAD
301C 72                0170 FILL MOV   M,D
301D 23                0180      INX   H
301E BC                0190      CMP   H
301F C2 1C 30          0200      JNZ   FILL
3022 2A 65 30          0210      LHLD  STAD
3025 73                0220 NEXT MOV   M,E
3026 7B                0230      MOV   A,E
3027 BE                0240      CMP   M
3028 C2 6F 30          0250      JNZ   FAIL
302B 79                0260      MOV   A,C
302C 23                0270      INX   H
302D 94                0280      SUB   H
302E C2 4D 30          0290      JNZ   NDON
3031 B8                0300      CMP   B
3032 44                0310      MOV   B,H
3033 CA 15 30          0320      JZ    SCND
3036 3A 66 30          0325      LDA   STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA   FIN
303F B9                0350      CMP   C
3040 CA 00 30          0360      JZ    STRT
3043 79                0370      MOV   A,C
3044 67                0380      MOV   H,A
3045 2E 00             0390      MVI   L,0
3047 C6 10             0400      ADI   10H
3049 4F                0410      MOV   C,A
304A C3 10 30          0420      JMP    DONE
304D 22 67 30          0430 NDON SHLD  NXAD
3050 7A                0440 LOPB MOV   A,D
3051 BE                0450 LOPA CMP   M
3052 C2 6F 30          0460      JNZ   FAIL
3055 2C                0470      INR   L
3056 C2 51 30          0480      JNZ   LOPA
3059 79                0490      MOV   A,C
305A 24                0500      INR   H
305B BC                0510      CMP   H
305C C2 50 30          0520      JNZ   LOPB
305F 2A 67 30          0530      LHLD  NXAD
3062 C3 25 30          0540      JMP   NEXT
3065                   0550 STAD DS    2
3067                   0560 NXAD DS    2
3069                   0570 FDE  DS    2
306B                   0580 FHL  DS    2
306D                   0590 FOUT DS    1
306E                   0600 FIN  DS    1
306F 22 6B 30          0610 FAIL SHLD  FHL
3072 32 6D 30          0620      STA   FOUT
3075 7E                0630      MOV   A,M
3076 32 6E 30          0640      STA   FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD  FDE
307D C3 7D 30          0670 SHLT JMP SHLT
3080                   0680 *
```

SUGGESTED ADDITIONS TO DIGITAL GROUP Z-80 CPU BOARD *

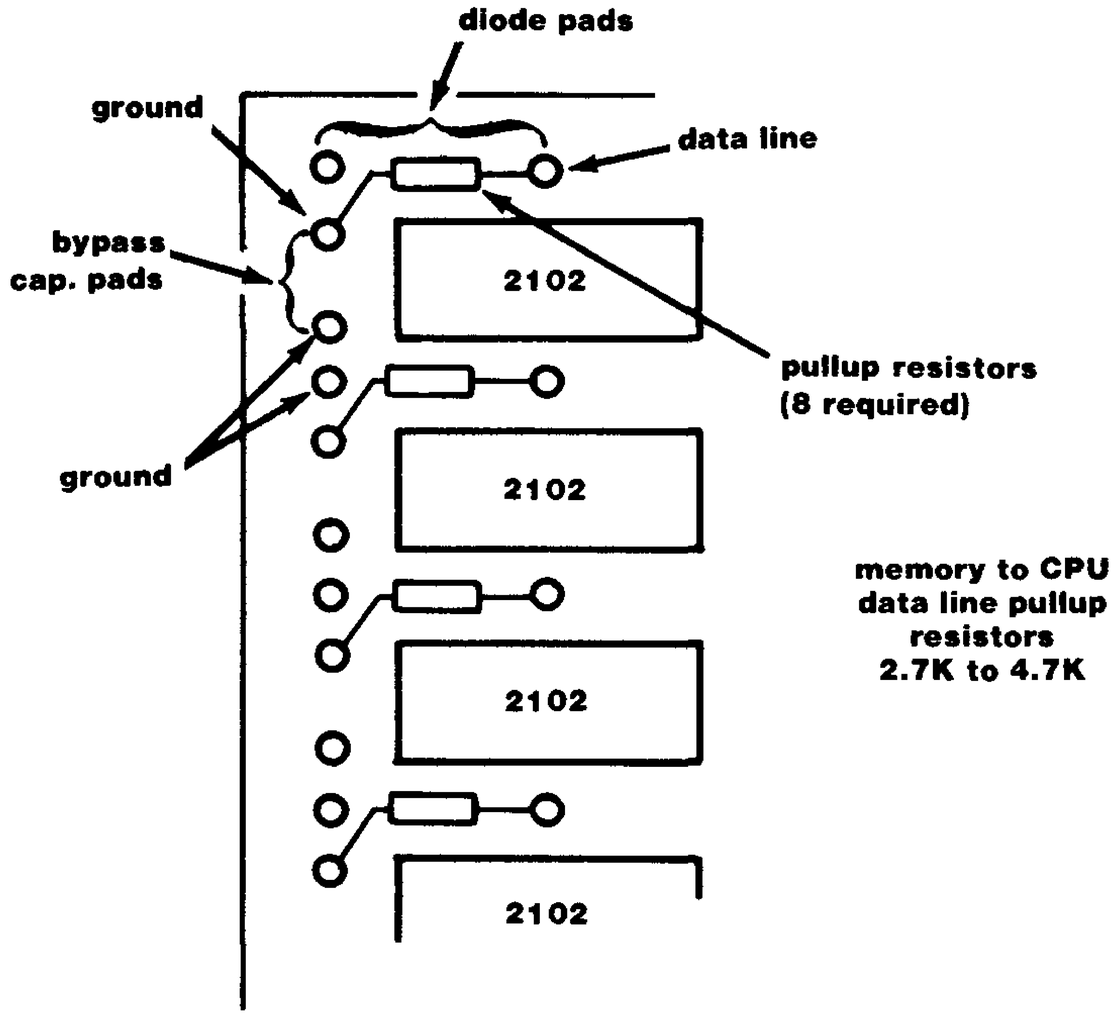
The following comments and fixes have been reported to us by digital group users

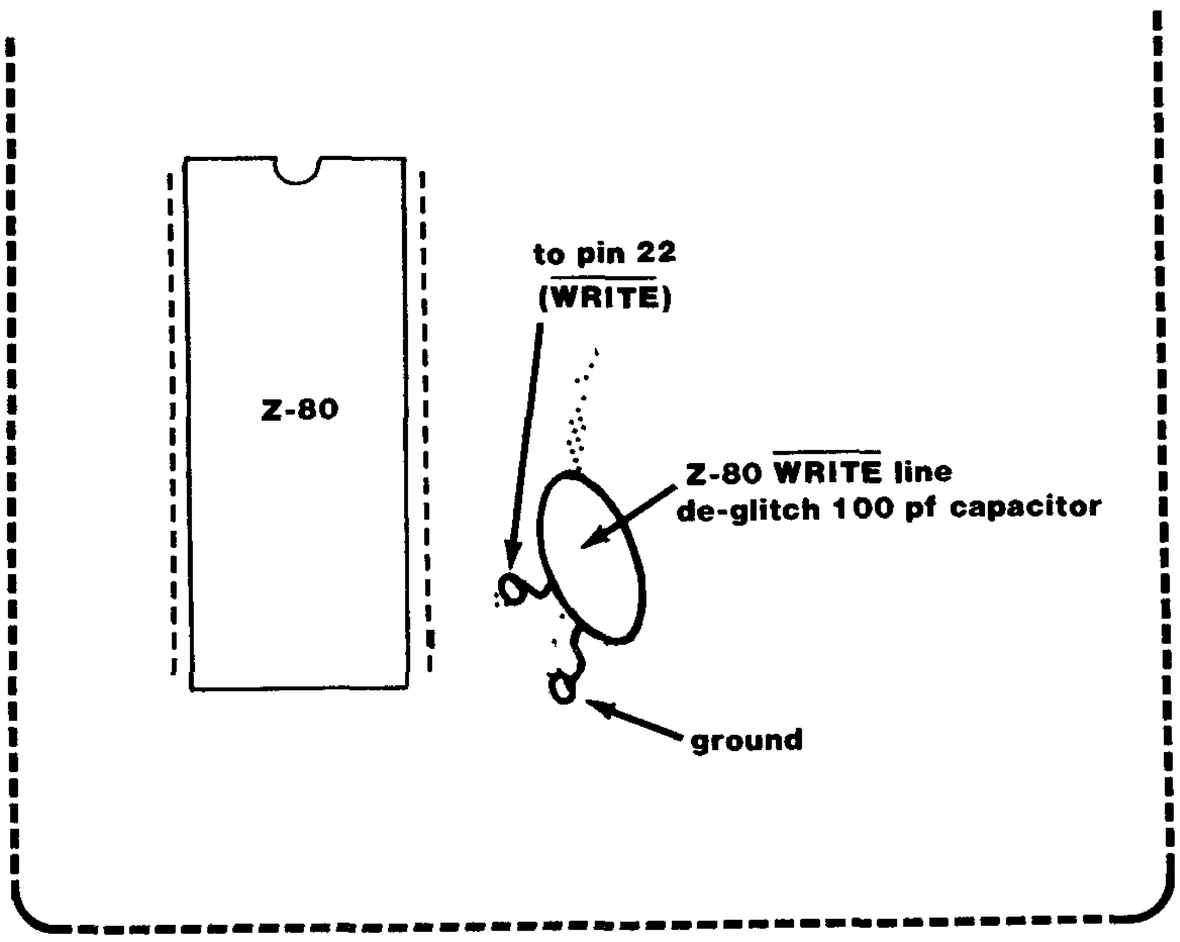
The data lines from memory to the CPU are not terminated on the Digital Group Z-80 CPU board, and because of this the CPU will occasionally get a data byte other than "FF" when accessing a non-existent memogxkmtqkuwxvs with programs (such as the Digital Group Memory Test Routines) which use this to find memory limits These lines should be pulled up to +5 through 2 7K resistors (3 9K and 4 7K resistors have been used with satisfactory results) A convenient location to install these pullup resistors is on the *left-hand* side of the CPU board Above each 2102 location in the first column of IC's two unused plated-through holes are provided (for undershoot clamping diodes) The right-hand hole is connected to its respective data line Also, on the left side of each of these 2102's are two unused plated-through holes for bypass capacitors The pullup resistors may be connected from the top hole (+5) of each of these pairs to the right-hand diode pad (data line) above each 2102

There is an occational glitch on the "WRITE" line of some Z-80's which, if not corrected, can be a problem With memory (such as this board) fast enough to respond to it, the glitch can write garbage into whichever location happens to be on the address buss at the time The problem can be easily corrected by the addition of a 100 pF capacitor between pin 22 of the Z-80 and ground on the CPU board Two plated-through holes connected to these lines are conveniently located near the lower right corner of the Z-80 and may be used to install the capacitor

Although the above problems may not be noticeable on your system, we feel that the addition of the recommended fixes will add an extra measure of reliability to it and perhaps help you to avoid those inexplicable program crashes

* These mods will help any system but are mandatory for successful 4MHz operation





CIRCUIT DESCRIPTION

The heart of ECONORAM IX is the MM5257-3L or TMS40L44-25 memory IC (RAM), which can store 4096 bits ("4K" bits) of information (thus, each is a "4K x 1 ' memory IC) These are *not* standard MM5257/TMS40L44's, the memory ICs included in this kit are specifically tested and designated by the manufacturer as *low power, high speed* parts

These ICs are arranged in rows that are 8 ICs wide - each IC contributing one bit of an 8-bit byte Thus each row can store 4K x 8 bits (4K bytes) By connecting 8 of these rows together in parallel, a total of 32K bytes of memory storage is produced (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array and the row number corresponding to the 4K segment within a given block is indicated along the right hand edge of the array)

Now that we have this storage, there are other aspects to consider in order to be able to make use of it First, addressing a specific location in memory, and second, writing data into the memory or reading data from it

The logic diagram on pages 8 and 9 show the address decoding, read/write control, memory array, input buffering and output buss driver circuits for the Econoram IX Each row of memory ICs requires 12 address bits (A0-A11) to select one unique location of the 4096 available locations These bits are brought onto the board through inverting buffers (so as to present only one low-power TTL load to the buss) and distributed to the 12 address select pins on each of the memory ICs The remaining 4 address bits are also buffered/decoded, and if they represent a valid address for the board (as determined by the settings of the address select switches), used to enable the appropriate row of memory ICs

When a row of ICs is thus enabled, it presents the data byte stored at the addressed location to the output buss driver This IC is normally in a high-impedance state (essentially disconnected) When a valid address has been received and a MEMORY READ strobe is received from the CPU, the output driver places the selected data onto the data buss to the CPU

Data to be written into a memory location is buffered and presented to the data in pins of each column of memory ICs However, when a memory write strobe is received from the CPU, the data is loaded into the addressed location of the enabled row of ICs only

When the output of a logic IC changes state, it draws a very short high-current 'spike' from the power lines If unchecked, the electrical noise created by these transient spikes might couple into the logic lines and cause erratic operation of the board To absorb these transients, bypass capacitors are liberally placed across the power distribution lines throughout the memory array and at every support IC

This board is guaranteed to operate at 4 0 MHz over the full temperature range 0° to 70° C and to draw less than 3500 mA (3 5 amps) The typical measured current draw is less than 3000 mA at cold start-up, rapidly decreasing to around 2400 to 2800mA as the board warms up

It is interesting to note that static RAM technology has progressed to the point at which this high performance static RAM board is comparable in cost and power consumption to dynamic memory boards

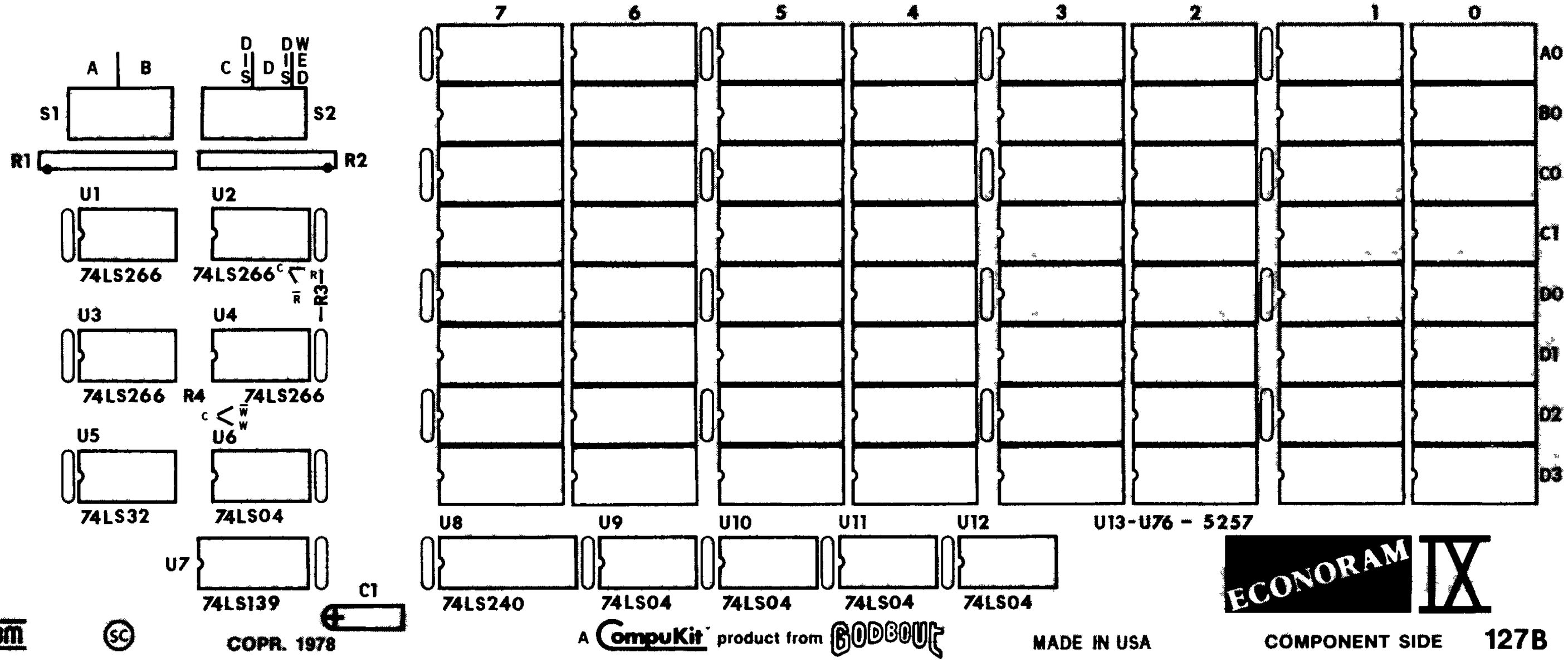
THANK YOU

This board is the result of much time, work and experience on the part of a number of people In addition to thanking you for choosing this board, we'd like to thank the Phantom* and many others for their help with this project

We strive for a board that doesn't just work the first time, but continues to give reliable operation for a long time If we can be of any help to you in applying this board, or if you have any questions, please let us know As always, we solicit your comments, letters and new product suggestions

HAPPY COMPUTING!

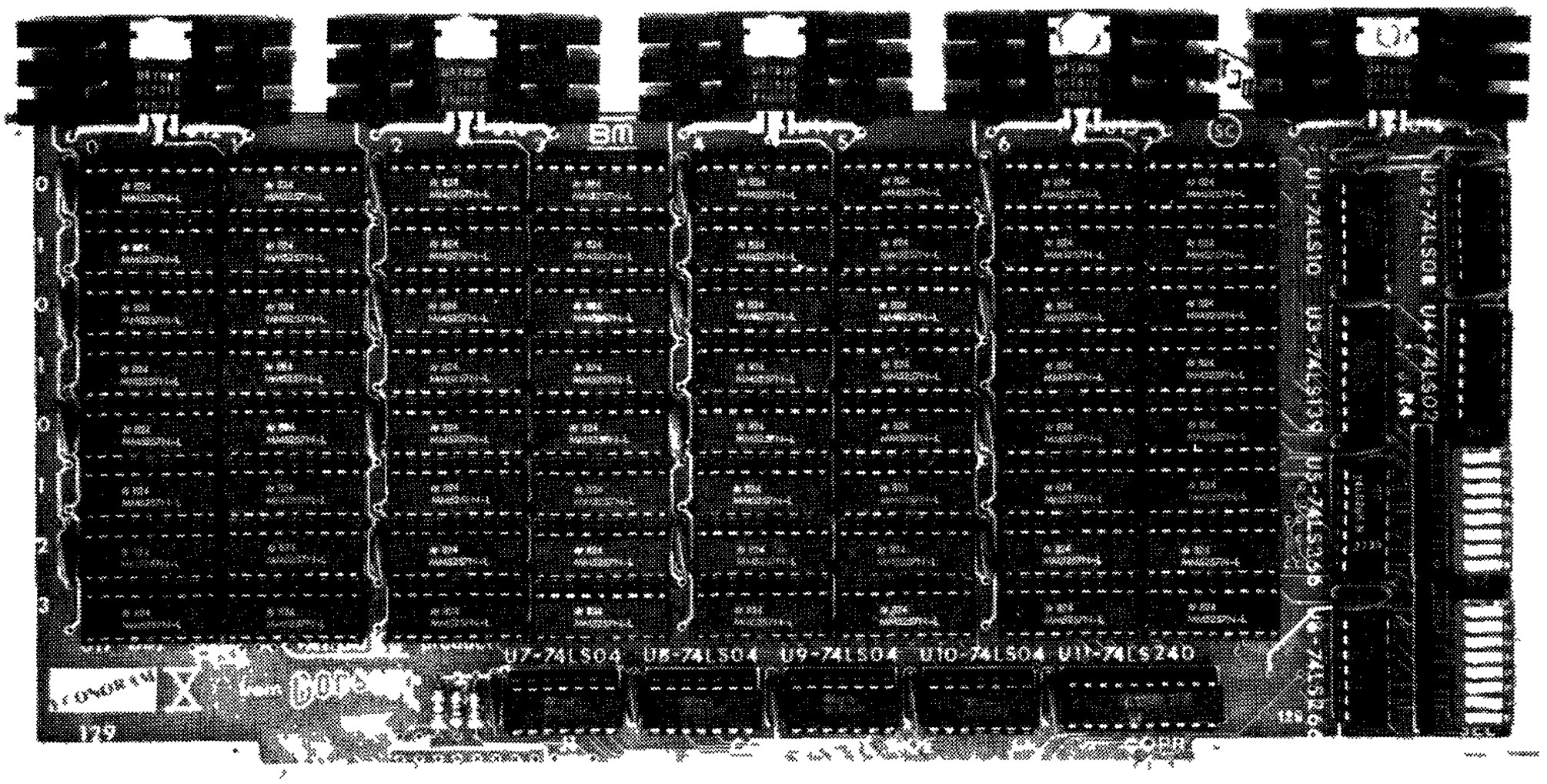
**Editor s Note* 'THE PHANTOM' is Doug Bell, who provided the impetous for producing this kit and then wrote these instructions using a word processor/text editor on his Digital Group System which included prototypes of this memory and a disk system of his own design



Component Layout

UP

ECONORAM X™
USER'S MANUAL



32K x 8 static memory • S-100
using MM5257/TMS40L44 • 4MHz

129 A CompuKit™ product from GODBOUT

mac 1/79

ABOUT ECONORAM X

Congratulations on your decision to purchase ECONORAM X, a 32K x 8 memory board designed specifically for electrical and mechanical compatibility with the proposed IEEE S-100 buss standard The S-100 buss currently is one of the most popular in the industry and by far the most prolific we believe this board with the rest of the S-100 portions of the ECONORAM family to be the best memory boards available for that buss

We recommend that the parts in this kit be checked against the parts list for completeness and that these instructions be read through carefully before starting All IC sockets and disc bypass capacitors are soldered into place on the board so the tedious work in putting the kit together has already been done Completion of the assembly should take from one to four hours depending on previous assembly experience and upon completion, you will discover -- as thousands of satisfied ECONORAM owners have discovered -- the pleasure of using a fine memory board that just works, and works

As the first company to nationally offer memory kits to computer hobbyists and professionals, we again thank you for choosing ECONORAM X welcome to the club

TECHNICAL OVERVIEW

This board incorporates proven static memory technology There are currently two popular types of memory being used in products such as this static and dynamic Static memories are the overwhelming choice in applications where speed, complexity, ease of use and reliability must all be considered there is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement

The individual memory ICs used on this board are grouped together to form three blocks of memory, two 8K x 8, one 16K x 8 The 8K blocks are addressable on any 8K boundary, the 16K block on any 16K boundary by setting the starting locations with the onboard dip switch (no jumpers required) Additional features include a write protect switch for each block, a write strobe selection switch which allows use of memory in systems with or without a front panel (MWRITE strobe), allowance for use with or without the PHANTOM line, "2 of 8 extra qualifiers, disable switches for each block, thorough capacitor bypassing of supply lines to suppress transients plus on-board regulation and heat-sinking for reliably cool operation All this and sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend

Parts List

Upon receipt of your kit, check your parts against the list below

- ☐ (1) Econoram X circuit board

INTEGRATED CIRCUITS (note the following parts may have letter suffixes and previxes along with the key numbers given below)

- ☐ (64) MM5257N-3L or TMS 40L44 (U17-U80)
- ☐ (1) 74LS02 quad nor gate (U4)
- ☐ (4) 74LS04 hex inverter (U7-U10)
- ☐ (1) 74LS08 quad and gate (U2)
- ☐ (1) 74LS10 triple nand gate (U1)
- ☐ (1) 74LS139 dual decoder (U3)
- ☐ (1) 74LS240 octal buffer (U11)
- ☐ (2) 74LS266 quad ex-nor (U5, 6)
- ☐ (5) 7805 or 340T5 5U regulators (U12-U16)

OTHER ELECTRONIC COMPONENTS

- ☐ (2) SIP resistor packs (R4, R5)*
- ☐ (3) 2K7 ± 20% ¼ watt resistors (R1-R3)*
- ☐ (10) 39 uF tantalum capacitors (C1-C10)
- ☐ (27) Ceramic disk bypass capacitors*

MECHANICAL COMPONENTS

- ☐ (75) Low profile IC sockets*
- ☐ (2) Dipswitch, 8 position (S1-S2)*
- ☐ (5) TO220 heat sinks
- ☐ (5) 6 - 32 machine screws
- ☐ (5) 6 - 32 lockwashers
- ☐ (5) 6 - 32 x ¼ hex nuts
- ☐ (1) Econoram X user manual

*supplied already soldered to board

MEMORY ADDRESS ASSIGNMENT

This board is addressable as three separate blocks, identified as A, B and C Blocks A and B are 8K, Block C 16K addressed as shown below (See Figure 10)

	SWITCH POSITION	BLOCK HEX STARTING ADDRESS	SWITCH DISABLE
BLOCK A	S2 123		S1 - 5
BLOCK B	S2 456		S1 - 6
	000	0000	
	001	2000	
	010	4000	
	011	6000	ON = "1"
	100	8000	OFF = "0"
	101	A000	
	110	C000	
	111	E000	
BLOCK C	S2 78		S1 - 7
	00	0000	
	10	4000	
	01	8000	
	11	C000	

Also each block may be disabled by putting the associated switch (shown above) in the on position A disabled block is transparent to the system and the contents may be neither changed nor read

ENABLE/PROTECT SWITCHES

Dip switch 1 positions 1 - 4 are write enable (WE) switches They may be used for manual write protection of each 8K area of the board as follows

SWITCH POSITION	PROTECT
S1 - 1	A
S1 - 2	B
S1 - 3	C0-C1 (CL)
S1 - 4	C2-C3 (CH)

Any combination of these four switches may be on/off with ON write enabling the particular 8K area and OFF write protecting that area

WRITE STROBE SELECT SWITCH

This switch selects use or non-use of the S-100 buss signal MWRITE (pin 68) This signal is normally produced by a front panel and would not be available in front panel-less machines, however, some CPU boards now implement this signal If MWRITE is present on your machine, place S1 position 8 (WS) OFF If not present, ON NOTE switch ON grounds MWRITE on the buss This condition should be avoided if MWRITE is present

PHANTOM LINE

In response to increasing numbers of users who have requested inclusion of "PHANTOM line buss pin 67 which is often used for implementing power on jump features This board is designed for use with active or inactive PHANTOM lines

CAUTION

Some manufacturers use the PHANTOM line (buss pin 67) for a refresh signal This will conflict with the PHANTOM feature and cause boards with PHANTOM to fail If your system has this conflict it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards

The PHANTOM feature may be activated at any time simply by installing a jumper at J1

If you want the PHANTOM feature the conflicting refresh signal may be eliminated (IF NOT USED ELSEWHERE IN THE SYSTEM) by cutting the trace connected to buss pin 67 on the CPU board *BE SURE OF YOUR SYSTEM CONFIGURATION BEFORE CUTTING ANY TRACES*

MEMORY TESTING

If the memory board seems to be working properly, the Memory Testing Routine can be used to give the board a more thorough workout It is rather slow, but will do the job well It can be entered via editor/assembler or front panel switches

The routine is set up to test 32K from 4000 hex up to C000 hex This may be changed by entering a different starting address at "STRT (3001 - 3002) and/or a different end address at "END (3004 - high order byte only)

If the memory passes the test, it starts over again You may, on the other hand, insert a jump instruction at "MARK ' to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart

If the memory fails the test, critical information is stored and the routine enters a software "HALT' , that is a "jump to here at "SHLT" Front panel lights, if any, will show this state The user may then use the front panel or dump routines to display the following stored failured info

3069+	"FDE'	= D, E pair D is the fill character and E is the test character
306B*	"FHL	= H, L pair the failure address
306D*	"FOUT	= the data expected at this address
306E*	"FIN '	= the data read from the address

*address from Memory Testing Routine Listing

The user may replace the "jump" at "SHLT' with a jump to a display or notification routine

The difference between "FOUT' and "FIN should indicate which bit is failing indicating which chip or area is causing the problem

This test will find most of the harder to distinguish errors

MEMORY TESTING ROUTINE

```
3000 21 00 40
3003 3E A0
3005 32 6E 30
3008 3E 10
300A 84
300B 4F
300C 16 00
300E 1E FF
3010 22 65 30
3013 AF
3014 47
3015 7B
3016 5A
3017 57
3018 79
3019 2A 65 30
301C 72
301D 23
301E BC
301F C2 1C 30
3022 2A 65 30
3025 73
3026 7B
3027 BE
3028 C2 6F 30
302B 79
302C 23
302D 94
302E C2 4D 30
3031 B8
3032 44
3033 CA 15 30
3036 3A 66 30
3039 00
303A 00
303B 00
303C 3A 6E 30
303F B9
3040 CA 00 30
3043 79
3044 67
3045 2E 00
3047 C6 10
3049 4F
304A C3 10 30
304D 22 67 30
3050 7A
3051 BE
3052 C2 6F 30
3055 2C
3056 C2 51 30
3059 79
305A 24
305B BC
305C C2 50 30
305F 2A 67 30
3062 C3 25 30
3065
3067
3069
306B
306D
306E
306F 22 6B 30
3072 32 6D 30
3075 7E
3076 32 6E 30
3079 EB
307A 22 69 30
307D C3 7D 30
3080
```

```
0010 STRT LXI  H,40C0H
0020 END  MVI  A,0A0H
0030      STA  FIN
0040      MVI  A,10H
0050      ADD  H
0060      MOV  C,A
0070      MVI  D,0
0080      MVI  E,0FFH
0090 DONE SHLD STAD
0100      XRA  A
0110      MOV  B,A
0120 SCND MOV  A,E
0130      MOV  E,D
0140      MOV  D,A
0150      MOV  A,C
0160      LHLD STAD
0170 FILL MOV  M,D
0180      INX  H
0190      CMP  H
0200      JNZ  FILL
0210      LHLD STAD
0220 NEXT MOV  M,E
0230      MOV  A,E
0240      CMP  M
0250      JNZ  FAIL
0260      MOV  A,C
0270      INX  H
0280      SUB  H
0290      JNZ  NDON
0300      CMP  B
0310      MOV  B,H
0320      JZ   SCND
0325      LDA  STAD+1
0330 MARK NOP
0331      NOP
0332      NOP
0340      LDA  FIN
0350      CMP  C
0360      JZ   STRT
0370      MOV  A,C
0380      MOV  H,A
0390      MVI  L,0
0400      ADI  10H
0410      MOV  C,A
0420      JMP   DONE
0430 NDON SHLD NXAD
0440 LOPB MOV  A,D
0450 LOPA CMP  M
0460      JNZ  FAIL
0470      INR  L
0480      JNZ  LOPA
0490      MOV  A,C
0500      INR  H
0510      CMP  H
0520      JNZ  LOPB
0530      LHLD NXAD
0540      JMP  NEXT
0550 STAD DS   2
0560 NXAD DS   2
0570 FDE  DS   2
0580 FHL  DS   2
0590 FOUT DS   1
0600 FIN  DS   1
0610 FAIL SHLD FHL
0620      STA  FOUT
0630      MOV  A,M
0640      STA  FIN
0650      XCHG
0660      SHLD FDE
0670 SHLT JMP SHLT
0680 *
```

CIRCUIT DESCRIPTON

The heart of ECONORAM X is the MM5257/TMS40L44 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC) Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts

These ICs are arranged in rows that are 8 ICs wide This way, each row can store 4K x 8 bits of information Paralleling 8 of these rows produces a total memory of 32K x 8 bits (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array)

Now that we have this storage, there are still other aspects we must consider First, we need to address a specific location in memory, and we need to be able to *write* data into the memory, or *read* data from the memory

The logic diagrams on pages 8 and 9 show the address circuitry along with the other ECONORAM X circuitry Each memory IC requires 12 address bits (A0-A11) to access any one of the 4096 bits available in the IC These address bits are generated by the CPU and are buffered by a number of inverters After buffering, a particular address is presented to all IC address selection pins However, we additionally need to select which particular row of ICs is to react to the given address This requires 4 more address bits (A12-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array)

When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss) Data to be read on the data buss from memory passes through 8 TRI-STATE® inverting buss drivers, when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected state

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines If these transients work their way into the logic circuitry, problems can appear To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC

This board is guaranteed to operate at 4 MHZ over the full temperature range (0-70 C ambient) and to draw less than 3500 mA (3 5 amps) Also, our typical measured currents were less than 3100 mA at cold start-up, rapidly decreasing to around 2900 mA or less depending upon the surrounding temperature We have heard similar reports from the people already using these boards

It is interesting to note that static RAM technology has progressed to the pont that this high-performance static RAM board is comparable in cost and power consumption to the dynamic memory boards

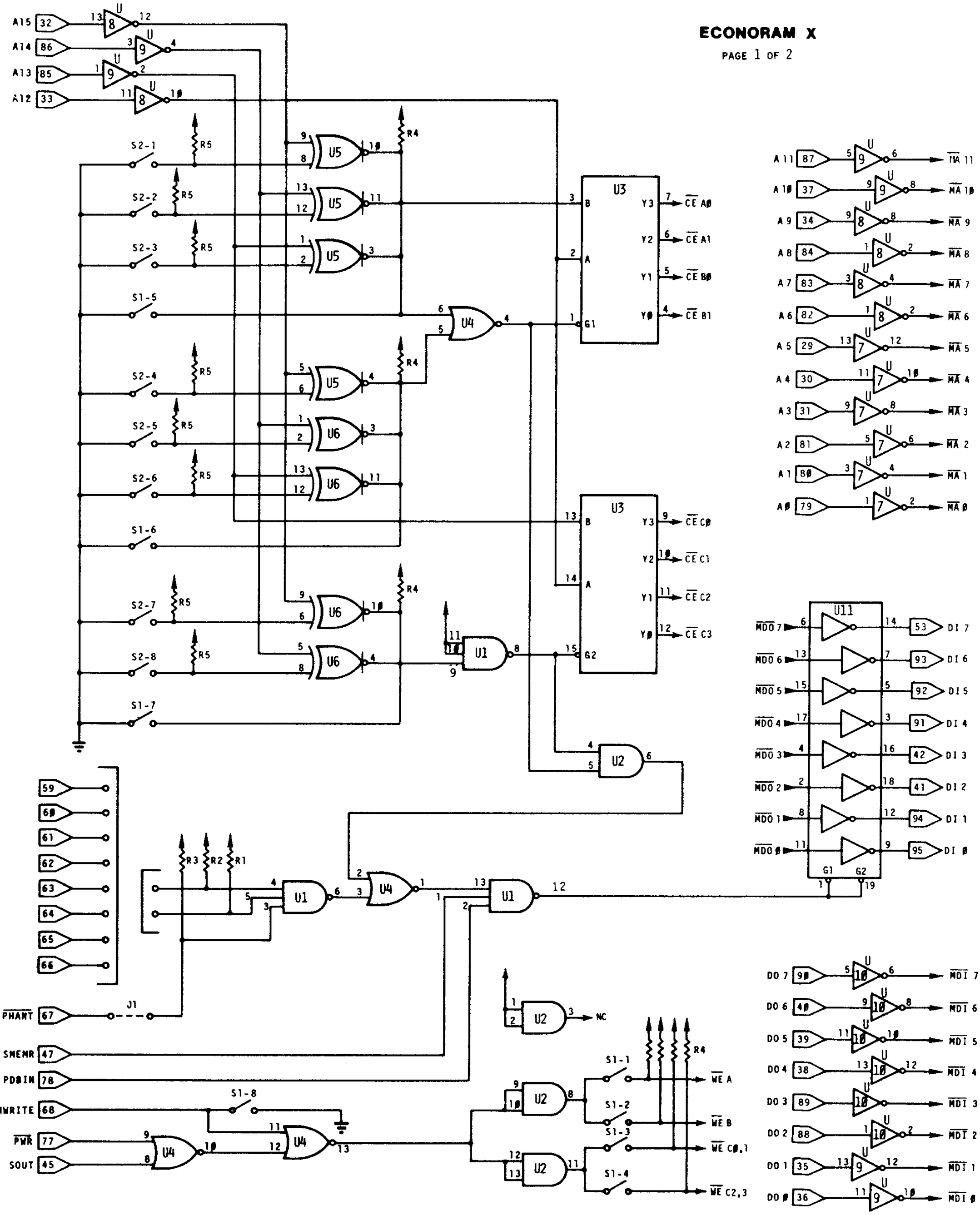
THANK YOU

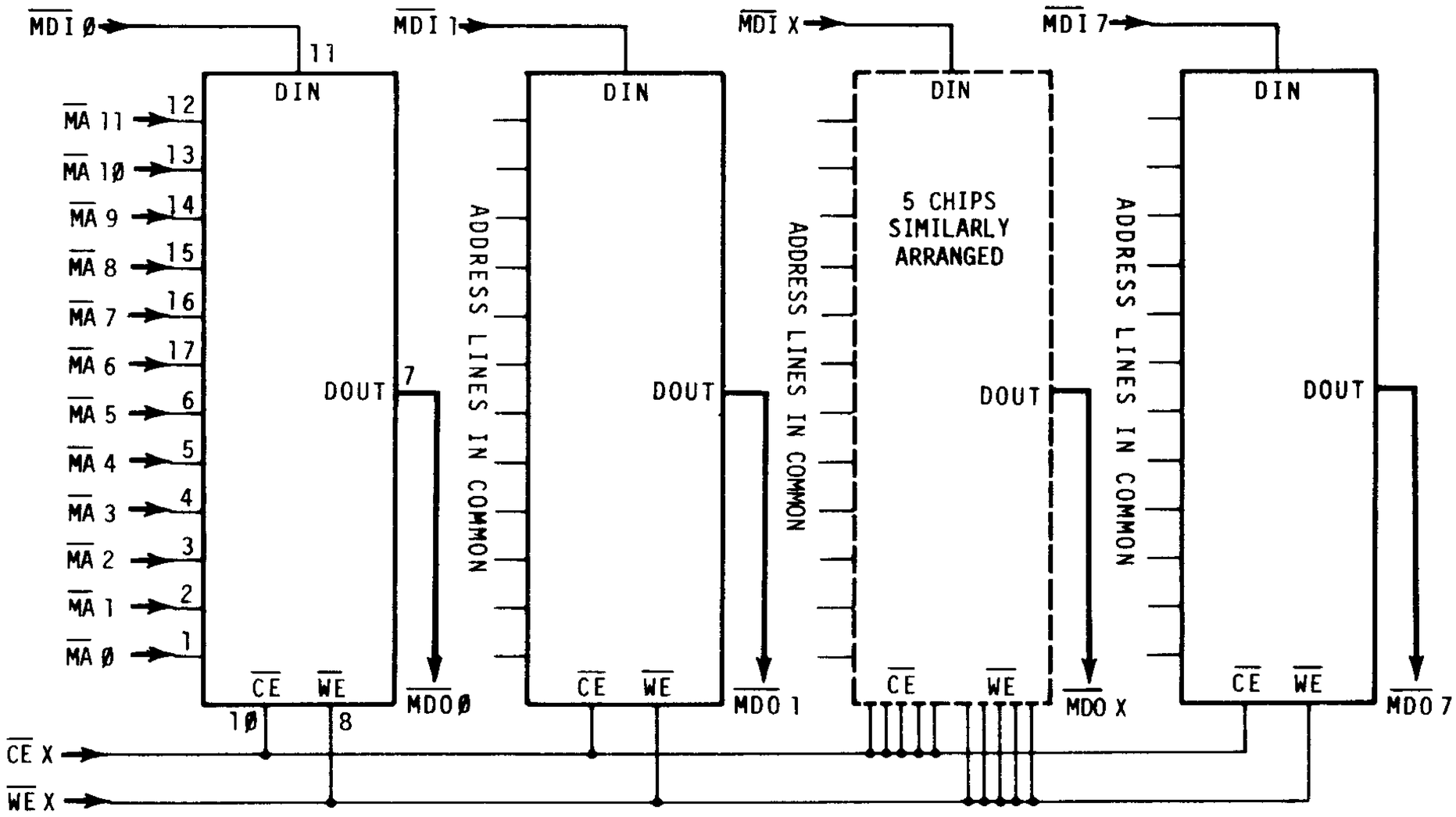
This board is the result of much time, work and experience on the part of a number of people

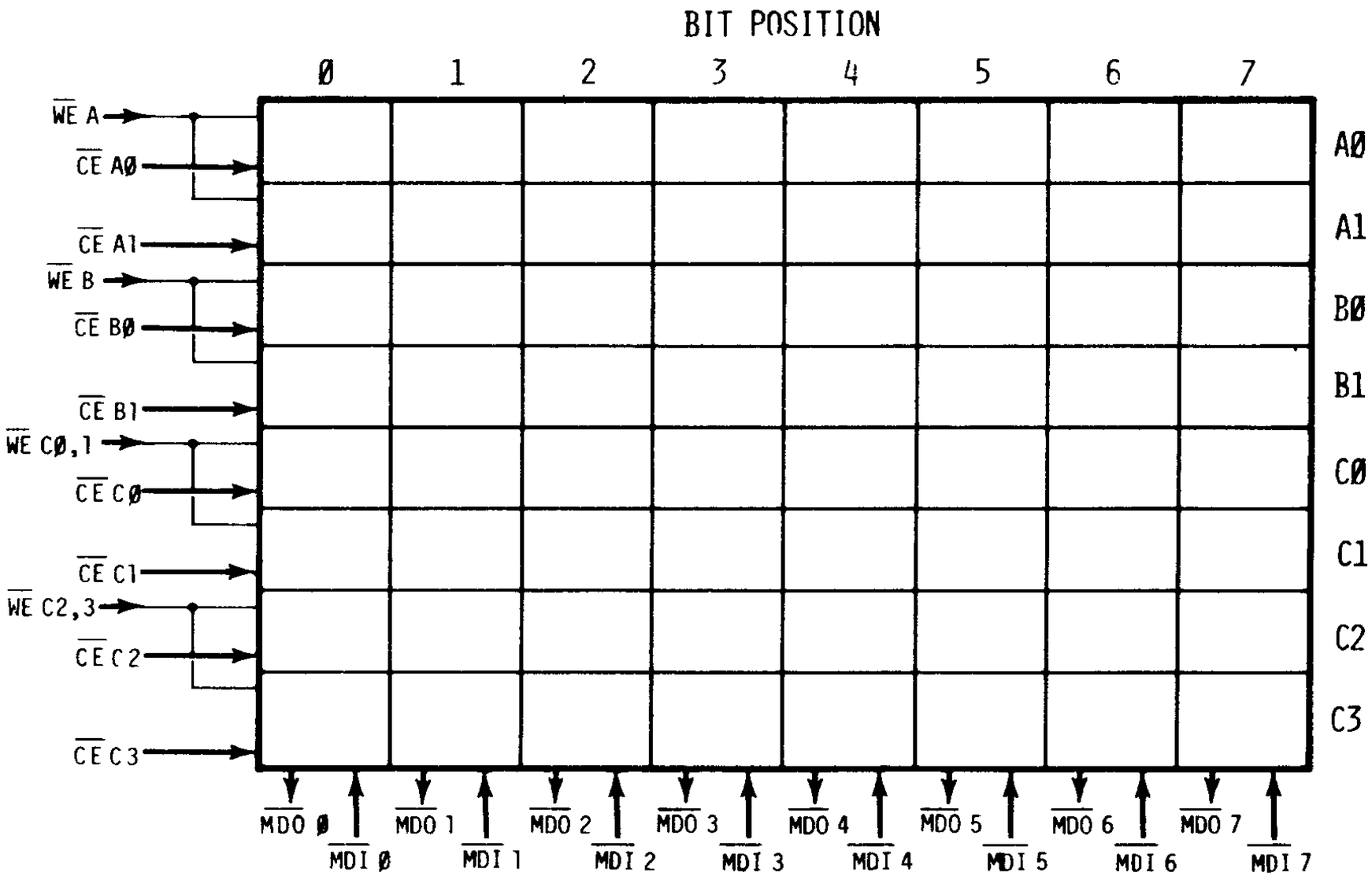
We strive for a board that doesn't just work the first time, but continues to give reliable operation for a long time If we can be of any help to you in applying this board, or if you have any questions, please let us know As always, we solicit your comments, letters and new product suggestions

HAPPY COMPUTING!

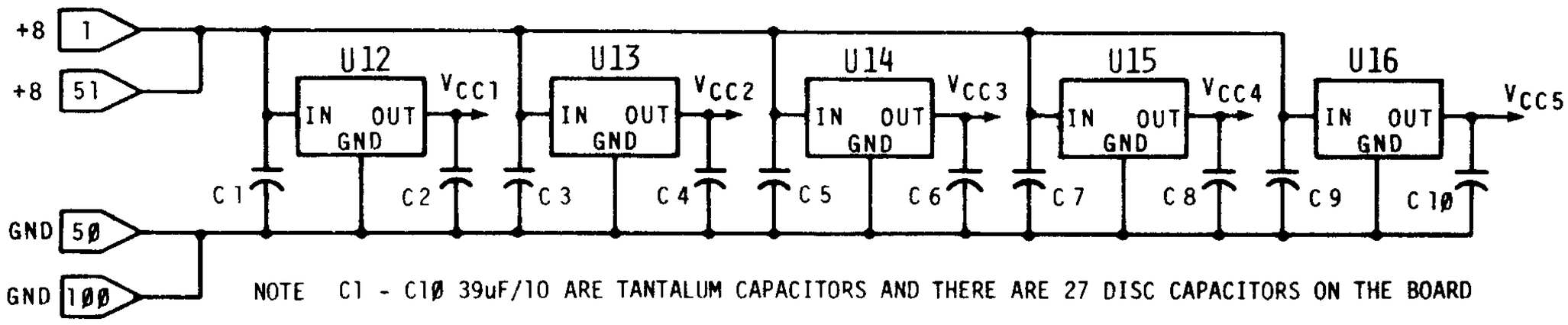
ECONORAM X


A15 32
A14 86
A13 85
A12 33
A11 87
A10 37
A9 34
A8 84
A7 83
A6 82
A5 29
A4 30
A3 31
A2 81
A1 80
A0 79
S2-1
S2-2
S2-3
S1-5
S2-4
S2-5
S2-6
S1-6
S2-7
S2-8
S1-7
R5
R4
R3
R2
R1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
CE A0
CE A1
CE B0
CE B1
CE C0
CE C1
CE C2
CE C3
MA 11
MA 10
MA 9
MA 8
MA 7
MA 6
MA 5
MA 4
MA 3
MA 2
MA 1
MA 0
MDO 7
MDO 6
MDO 5
MDO 4
MDO 3
MDO 2
MDO 1
MDO 0
DI 7
DI 6
DI 5
DI 4
DI 3
DI 2
DI 1
DI 0
59
60
61
62
63
64
65
66
PHANT 67
J1
SMEMR 47
PDBIN 78
MWRITE 68
PWR 77
SOUT 45
S1-8
NC
S1-1
S1-2
S1-3
S1-4
WE A
WE B
WE C0,1
WE C2,3
DO 7
DO 6
DO 5
DO 4
DO 3
DO 2
DO 1
DO 0
MDI 7
MDI 6
MDI 5
MDI 4
MDI 3
MDI 2
MDI 1
MDI 0

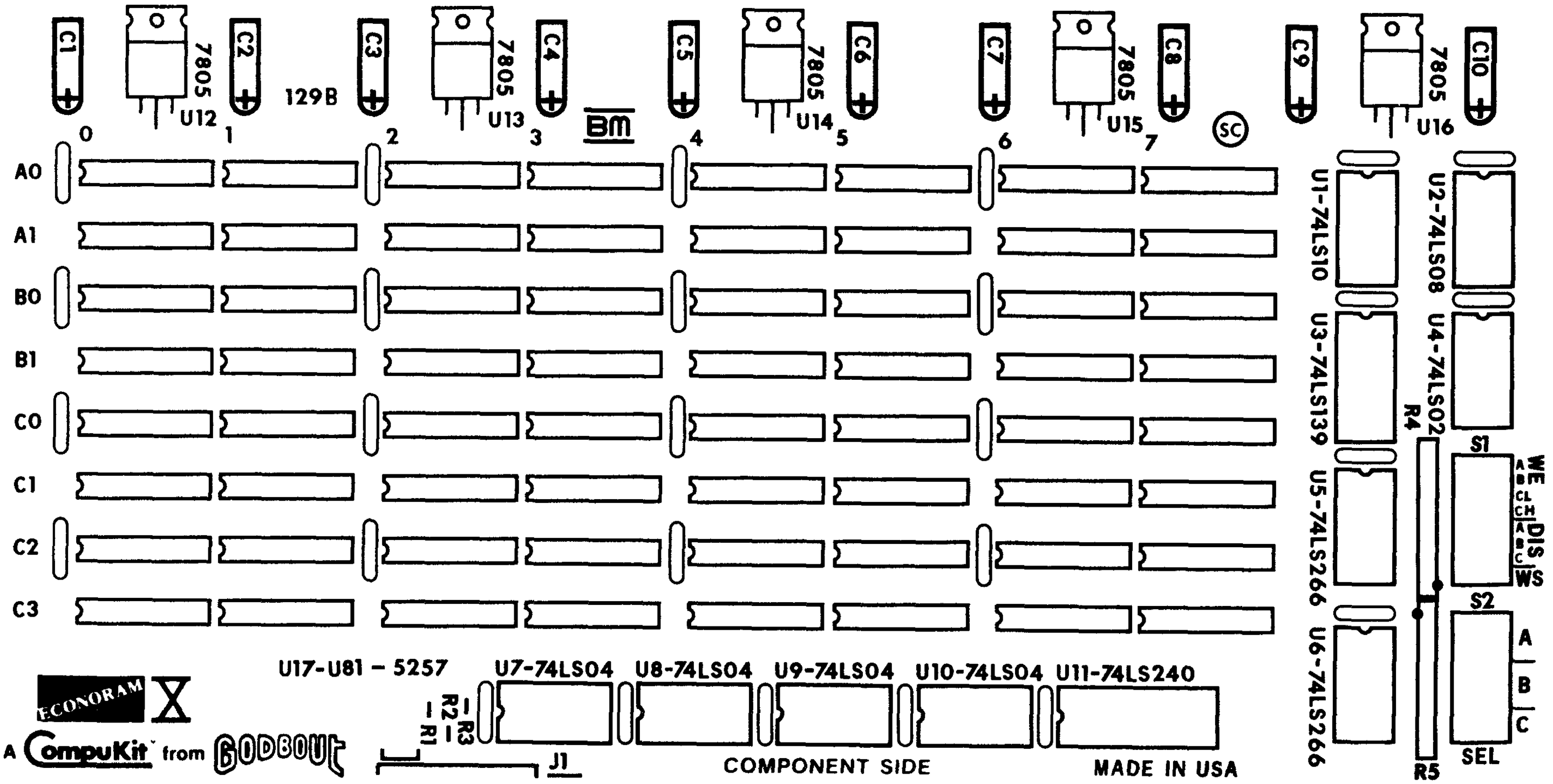




ARRAY CONSISTS OF 64 (1 x 4096) STATIC RAMS



NOTE C1 - C1Ø 39uF/10 ARE TANTALUM CAPACITORS AND THERE ARE 27 DISC CAPACITORS ON THE BOARD



Component Layout

up

ECONORAM Xa T.M.

ABOUT THE ECONORAM Xa

Congratulations on your purchase of the Econoram Xa, a 32 x 8 memory board designed specifically for electrical and mechanical compatability with the IEEE bus standard. The S 100 bus systems are professional level machines used in commercial, industrial, and scientific applications. Because of the bus oriented architecture, S 100 machines provide superior performance without the built in obsolescence of other systems. We believe that this board with the rest of the S-100 portion of the Compupro family is one of the best boards available for that bus.

We recommend that the parts in this kit be checked against the part list for completeness and that these instructions be read through carefully before starting. All IC sockets and disc bypass capacitors are soldered into place on the board, so the tedious work in putting the kit together has already been done. Completion of the assembly should take from one to four hours, depending on previous assembly experience, and upon completion, you will discover - as thousands of satisfied ECONORAM owners have discovered -- the pleasure of using a fine memory board that just works, and works.

As the first company to nationally offer memory kits to computer hobbyists and professionals, we again thank you for choosing ECONORAM Xa...welcome to the club.

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This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this· static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use and reliability must all be considered...there is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement.

The individual memory ICs used on this board are grouped together to form two 16K x 8 blocks of memory. Each of these 16K blocks can be started on any 4K boundary by setting the dipswitch (no jumpers required). Additional features include a write protect switch and an enable switch for each block, write strobe selection switches for use in systems with or without MWRITE strobe 24 bit extended addressing with disable switch for memory expansion beyond 64K, thorough capacitor bypassing of supply lines to suppress transients plus on-board regulation and heat-sinking for reliably cool operation. All this and sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend.

16K BLOCK ADDRESSING

Each 16K block on this board can be set to start on any 4K boundary in the currently addressed 64K page. The starting address of the board is set by adding the switch value indicated on the diagram below. If the starting address is 52K or greater, the remaining memory that would exist beyond 64K is wrapped around to 0K. For example, if a block is addressed to start at 56K, then there would be 8K from 56K to 64K and 8K from 0K to 8K.

SWITCH S3

BLOCK	BLOCK B				BLOCK A				
SWITCH POSITION	1	2	3	4	5	6	7	8	ON = VALUE
SWITCH VALUE	32K	16K	8K	4K	32K	16K	8K	4K	OFF = 0

SWITCH POSITION AND SETTING

BLOCK A	5	6	7	8	STARTING ADDRESS
BLOCK B	1	2	3	4	
	OFF	OFF	OFF	OFF	0K + 0K + 0K + 0K = 0K
	OFF	OFF	OFF	ON	0K + 0K + 0K + 4K = 4K
	OFF	OFF	ON	OFF	0K + 0K + 8K + 0K = 8K
	OFF	OFF	ON	ON	0K + 0K + 8K + 4K = 12K
	OFF	ON	OFF	OFF	0K + 16K+ 0K + 0K = 16K
	OFF	ON	OFF	ON	0K + 16K+ 0K + 4K = 20K
	OFF	ON	ON	OFF	0K + 16K+ 8K + 0K = 24K
	OFF	ON	ON	ON	0K + 16K+ 8K + 4K = 28K
	ON	OFF	OFF	OFF	32K+ 0K + 0K + 0K = 32K
	ON	OFF	OFF	ON	32K+ 0K + 0K + 4K = 36K
	ON	OFF	ON	OFF	32K+ 0K + 8K + 0K = 40K
	ON	OFF	ON	ON	32K+ 0K + 8K + 4K = 44K
	ON	ON	OFF	OFF	32K+ 16K+ 0K + 0K = 48K
	ON	ON	OFF	ON	32K+ 16K+ 0K + 4K = 52K
	ON	ON	ON	OFF	32K+ 16K+ 8K + 0K = 56K
	ON	ON	ON	ON	32K+ 16K+ 8K + 4K = 60K

EXTENDED ADDRESS SELECTION

The memory on this board may be placed in any of the 256-64K pages that can be addressed by this board. This is accomplished by setting the 64K page address on switch S1 as shown below, and turning XA* (S2-8) to the OFF position.

ADDRESS	A23	A22	A21	A20	A19	A18	A17	A16	ON = "0"
	1	2	3	4	5	6	7	8	OFF = "1"

NOTE: If using this board in a system that does not have EXTENDED ADDRESSING, the user should remove U12 (25LS2521), turn all positions of S1 to the OFF position, and turn S2-8 (XA*) to the ON position.

BLOCK ENABLE SWITCHES

Each 16K block on this board may be selectively disabled and removed from memory space at any time by turning the appropriate enable switch to the OFF position. For normal operation, the enable switches should be left in the ON position.

	SWITCH NAME	SWITCH POSITION	
BLOCK A	EA	S2-6	ON = ENABLED
BLOCK B	EB	S2-7	OFF = DISABLED

WRITE PROTECT SWITCHES

Each 16K block on this board may be selectively write protected at any time by turning the appropriate write enable switch to the OFF position. This allows the user to read from the RAM. but not to alter its contents. For normal operation, the write enable switches should be left in the ON position.

	SWITCH NAME	SWITCH POSITION	
BLOCK A	WA	S2-4	ON = WRITE ENABLED
BLOCK B	WB	S2-5	OFF = WRITE PROTECTED

MWRITE SELECTION SWITCHES

The MWRITE selection switches should be set as shown below to conform to your system's implementation of the MWRITE line (S-100 bus pin 68).

If your system has.....

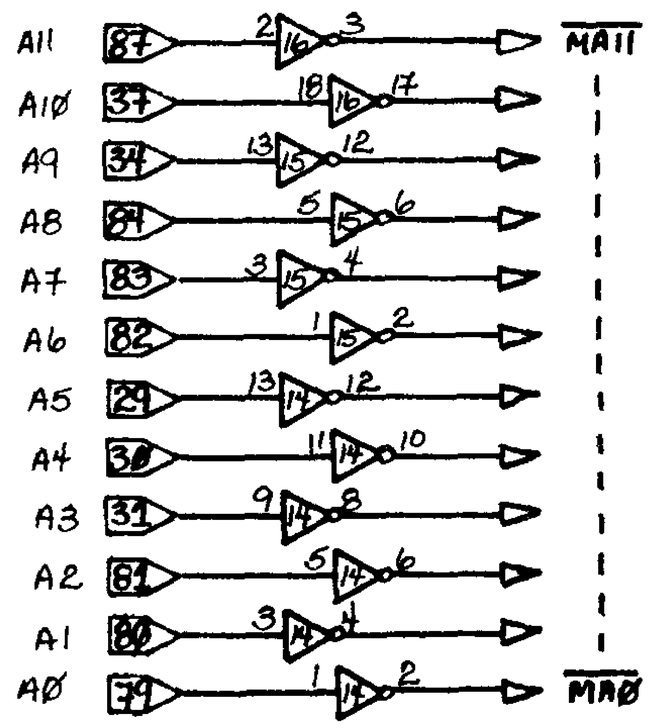
MWRITE IMPLEMENTED: Turn S2-2 (MW) to the ON position, and S2-3 (MG) to the OFF position.

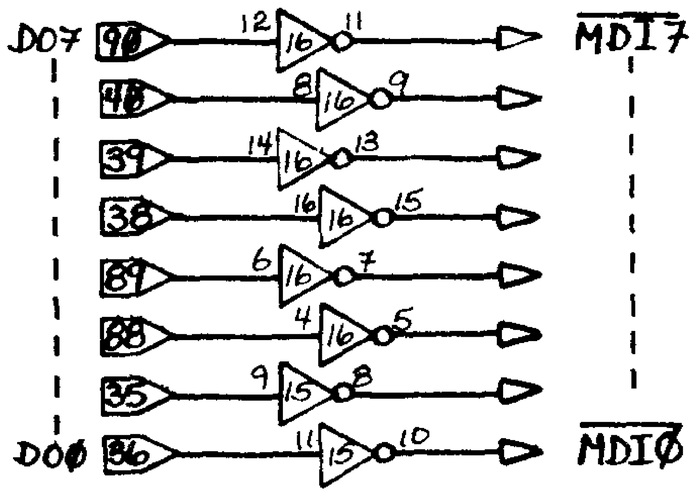
MWRITE NOT IMPLEMENTED: Turn S2-2 (MW) to the OFF position, and S2-3 (MG) to the ON position.

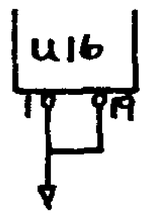
NOTE: If your system leaves MWRITE disconnected or floating, it might be a good idea to ground the line by turning both S2-2 and S2-3 (MW and MG) to the ON position. This should allow all boards using both MWRITE and PWR* to operate properly.

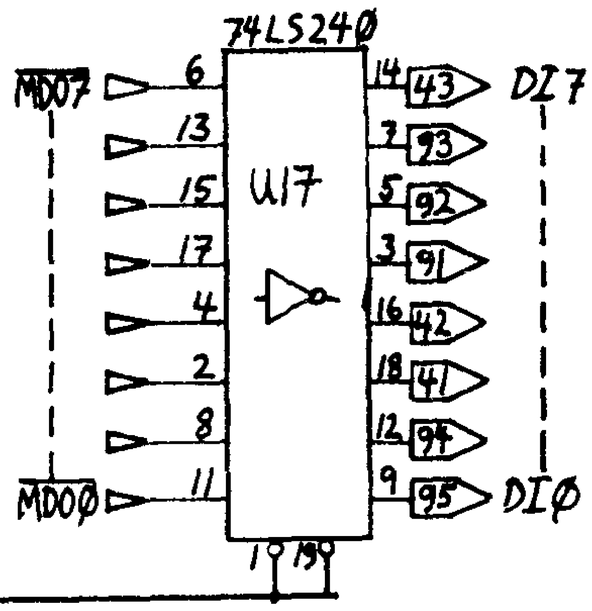
PHANTOM LINE

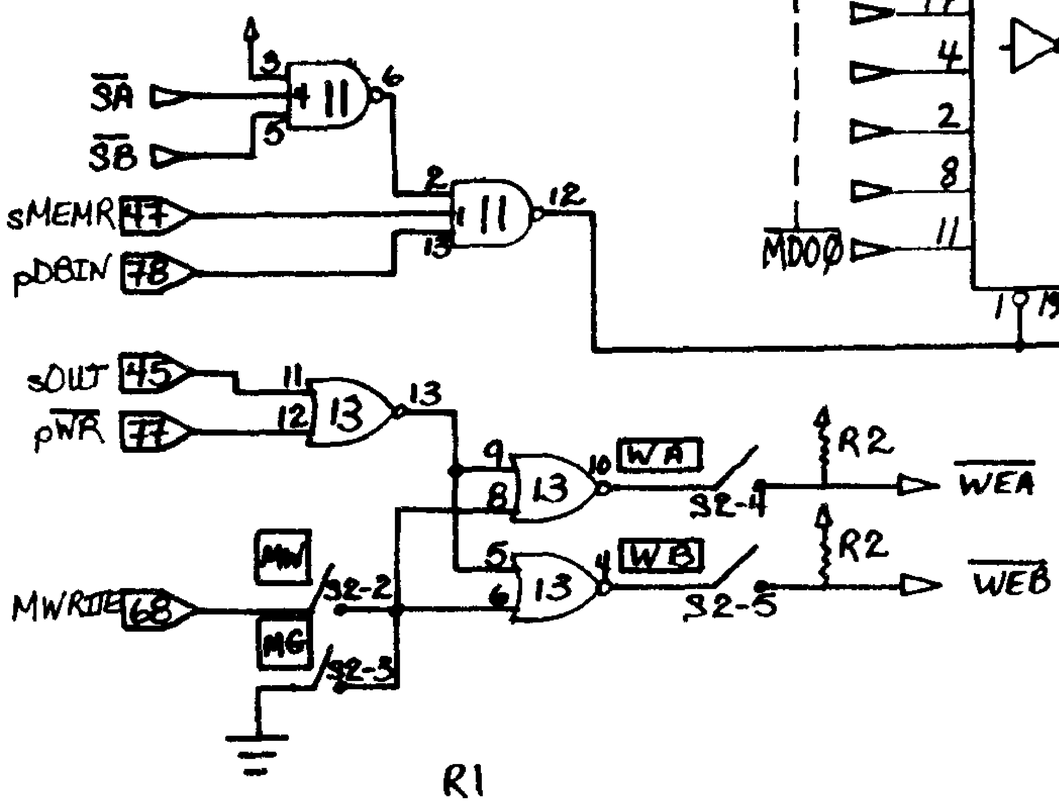
This board may be disabled by the PHANTOM* line (S-100 bus pin 67) if desired by placing S2-1 (PH) in the ON position. For normal operation unaffected by PHANTOM*, leave S2-1 (PH) in the OFF position.



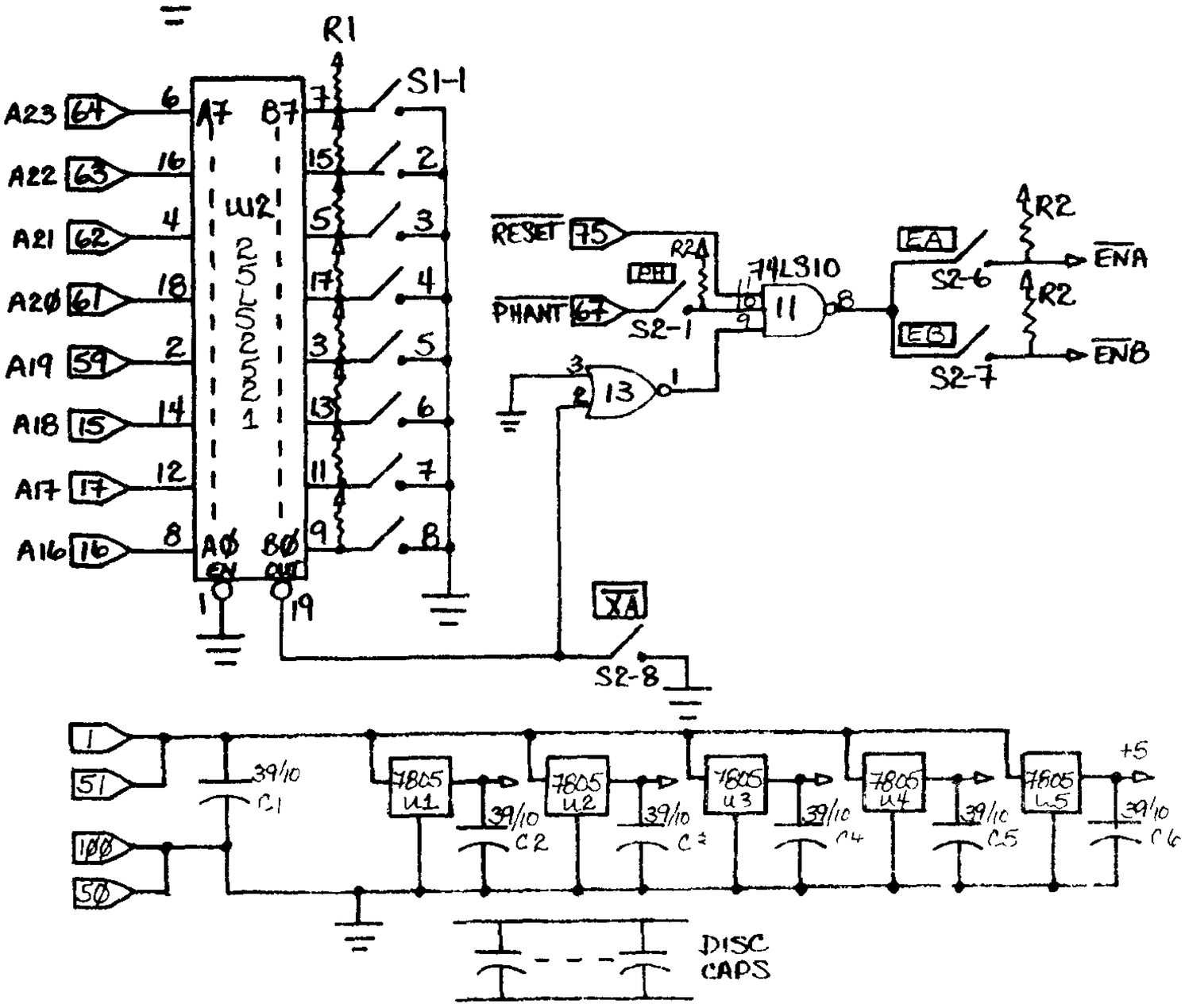


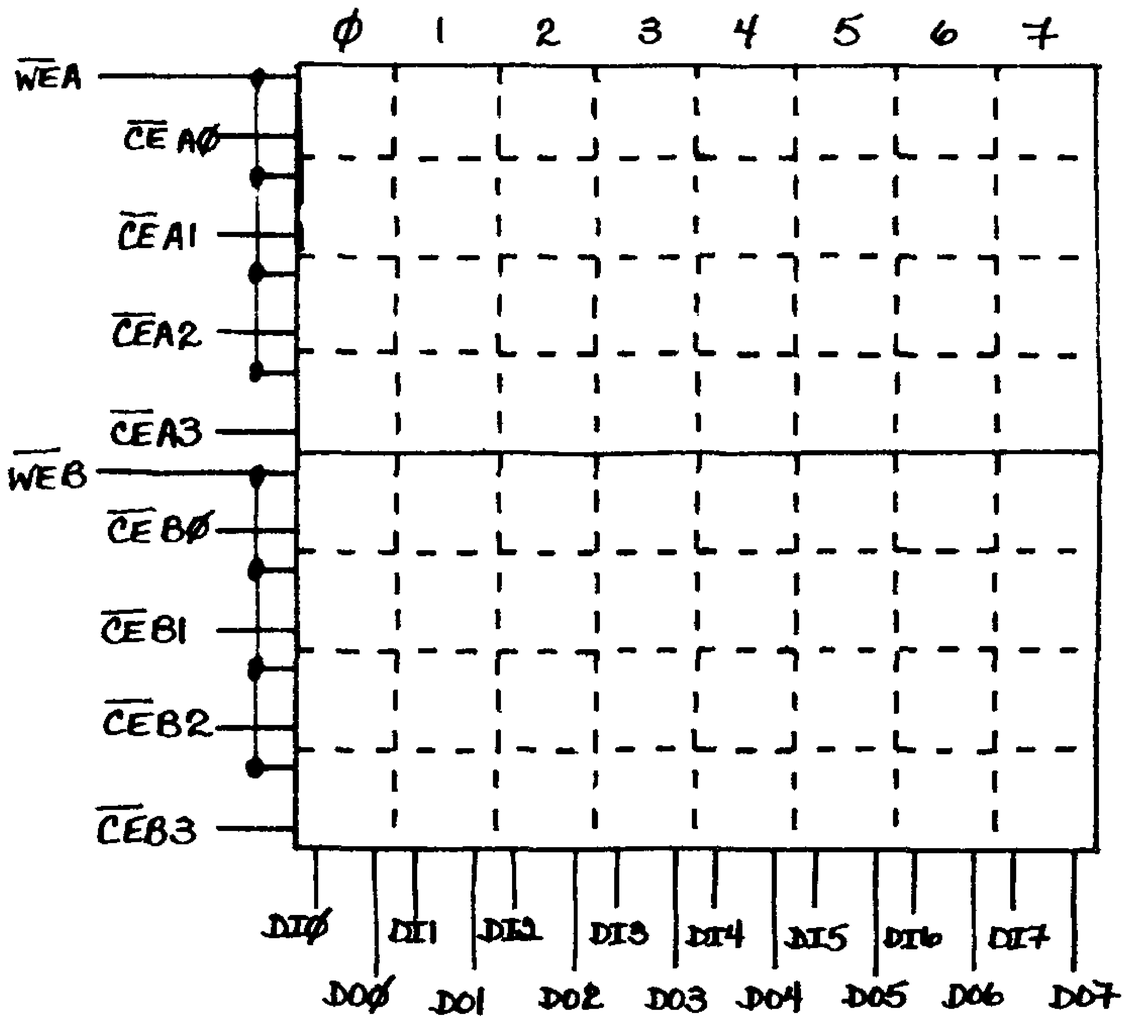




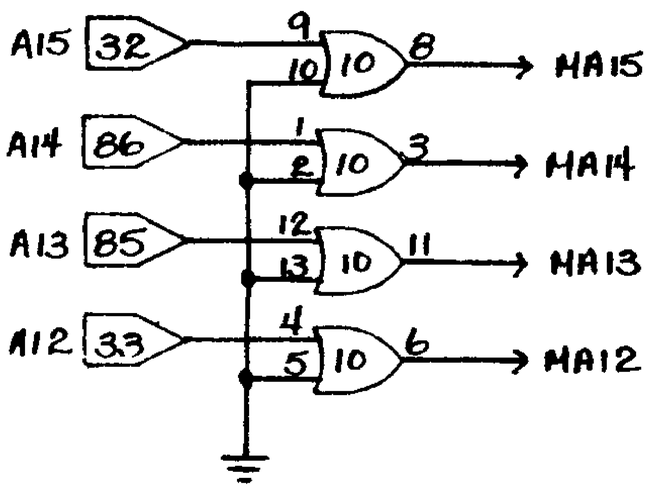


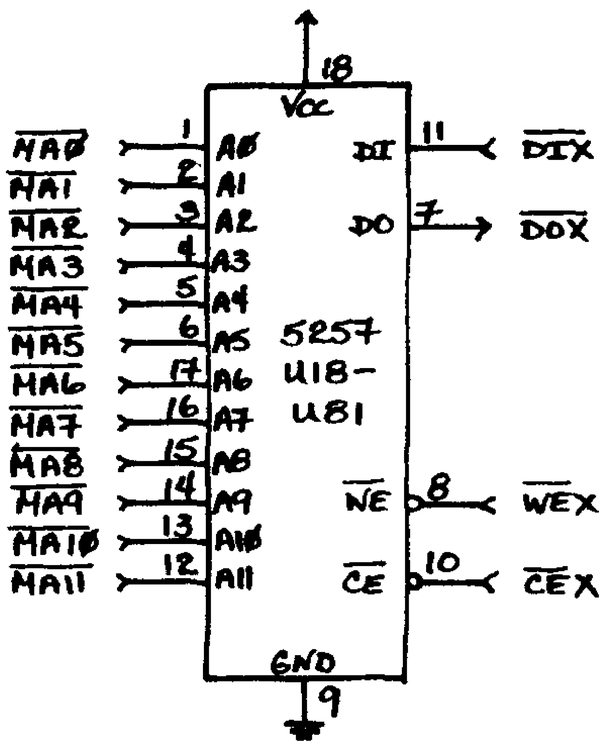
ECONORAM X
S-100 32K EXTENDED ADDRESS
© GODBOUT ELECTRONICS

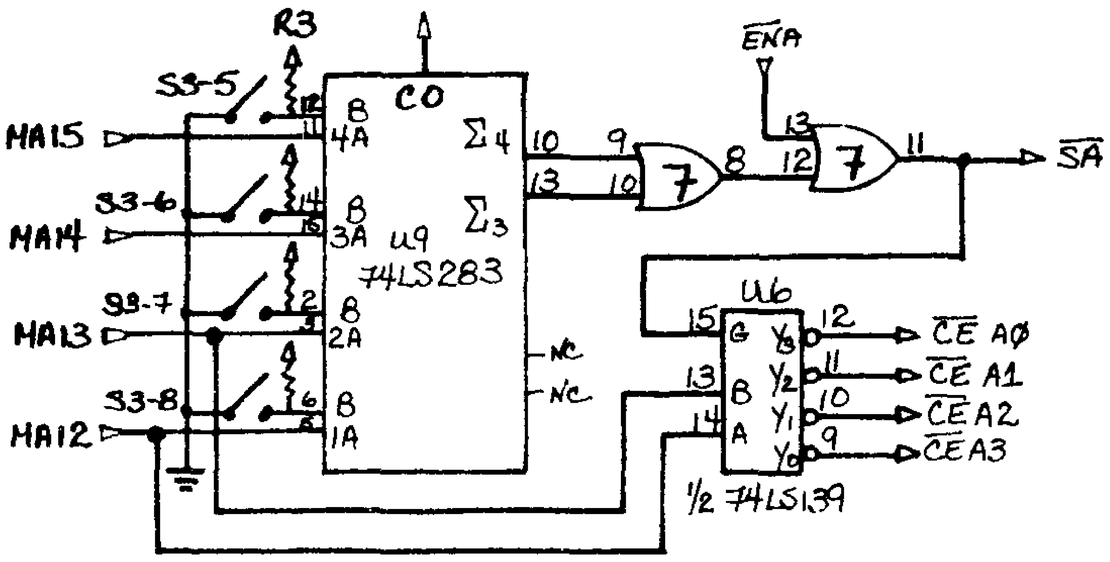


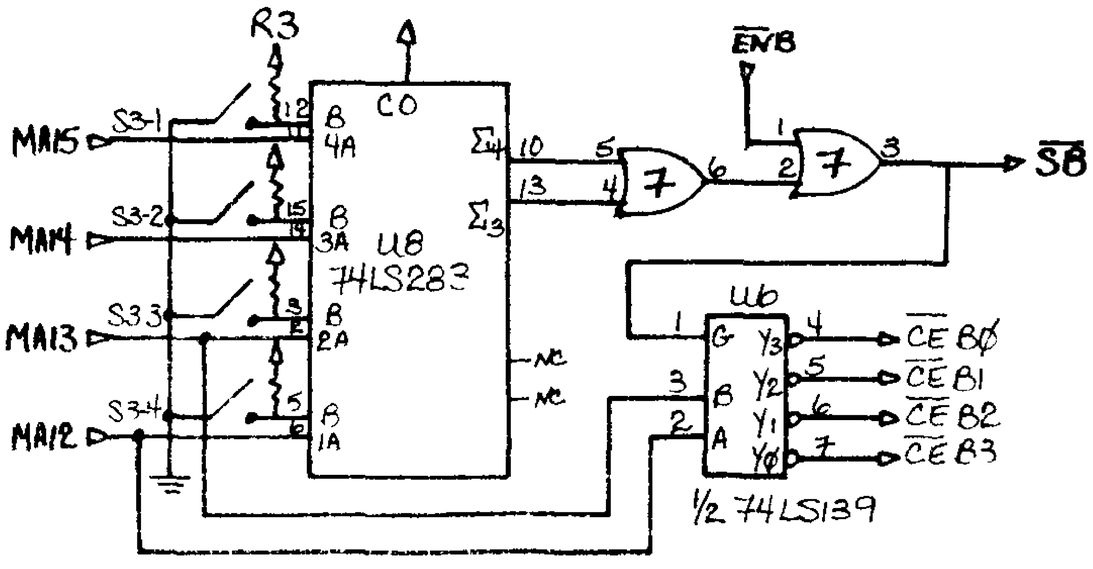


ARRAY CONSISTS OF
64 (4KX1) STATIC RAMS
SIMILAR TO MM5257
OR SM0030B
U18 - U81









PARTS LIST - ECONORAM Xa

(5)	U1-U5	7805
(1)	U6	74LS139
(2)	U7, U10	74LS32
(2)	U8, U9	74LS283
(1)	U11	74LS10
(1)	U12	25LS2521
(1)	U13	74LS02
(2)	U14, U15	74LS04
(1)	U16	81LS96/98
(1)	U17	74LS240
(6)	C1-C6	39 µf 10v tant
(3)	R1-R3	SIP Resistor
(2)	S1, S2	8 position DIP Switch
(64)	U18-U81	MM5257 or SM00308

attained by establishing a sub-set of IEEE 696 which would permit distribution of regulated +5 volts directly to system boards.

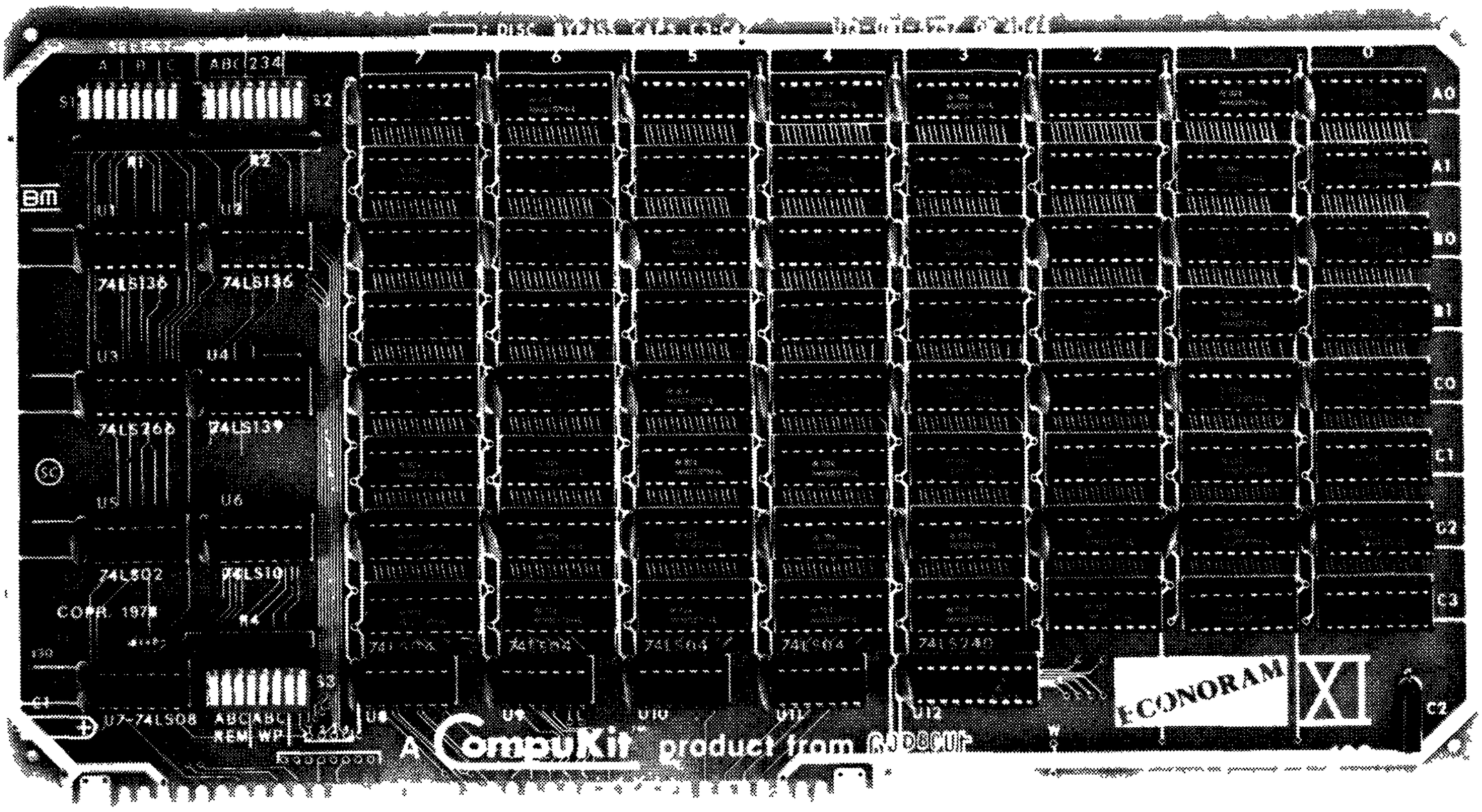
I. NDEF, 3 Lines, Not to be DEFined, are optional signal lines for use by individual manufacturers. These lines MUST be fully defined by any manufacturer using them. They MUST be provided with switches or jumpers to eliminate bus conflicts and their signals MUST be 5 volt TTL logic levels.

J. RFU, 4 Lines, Reserved for Future Use, may not be used for any purpose. These lines are reserved for bus expansion and may be defined in future revisions of IEEE 696.

This completes a brief overview of the functions and operation of the 100 lines specified in IEEE 696/S-100.

CONTINUED page 94

ECONORAM XI™
USER'S MANUAL



32K x 8 STATIC MEMORY
SBC-80 and BLC-80 SERIES

using MM5257/TMS40L44 · 4MHz

130 mac

A CompuKit™ product from GODBOUT

1/79

ABOUT ECONORAM XI

Congratulations on your decision to purchase ECONORAM XI, a 32K x 8 static memory board designed specifically for electrical and mechanical compatibility with the single-board-level-computers, that is the SBC 80 series by Intel and the BLC series by National Semiconductor Corp

All IC sockets and disc bypass capacitors are pre-soldered into place on the board, so the tedious work in putting a kit together has already been done Completion of the remaining assembly steps should take from one to three hours Upon completion, you will discover as thousands of satisfied ECONORAM owners have discovered, the pleasure of using a fine memory board that just works and works and works

As the first company to nationally offer memory kits to computer hobbyists, and now supplying memories to individuals and large concerns, we again thank you for choosing ECONORAM XI Welcome to the club!

TECHNICAL OVERVIEW

This board incorporates proven static memory technology There are currently two popular types of memory being used in products such as this static and dynamic Static memories are the overwhelming choice in applications where speed, complexity, ease of use and reliability must all be considered There is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far easier to implement

The individual memory ICs used on this board are grouped together to form three blocks of memory, two 8K x 8 and one 16K x 8 The 8K blocks are addressable on any 8K boundary, the 16K block on any 16K boundary by setting the starting locations with the on-board DIP switch (no jumpers required) Additional features include a write protect switch for each block, optional advanced write strobe, optional remote memory protect, optional "2 of 8" extra qualifiers, disable switches for each block, plus thorough bypassing of supply lines to suppress transients All this and sockets go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend

+++ Parts List ++++++++++++++++++++

Upon receipt of your kit, check your parts against the list below

- ☐ (1) ECONORAM XI circuit board

INTEGRATED CIRCUITS (note the following parts may have letter suffixes and prefixes along with the key numbers given below)

- ☐ (64) MM5257 or TMS4044 memories (U12 - U81)
- ☐ (2) 74LS136 exclusive OR gate (U1, U3)
- ☐ (1) 74LS266 exclusive NOR gate (U2)
- ☐ (1) 74LS139 dual 1 of 4 decoder (U4)
- ☐ (1) 74LS02 NOR gate (U5)
- ☐ (1) 74LS10 NAND gate (U6)
- ☐ (1) 74LS38 buffer and interface gates (U7)
- ☐ (4) 74LS04 hex inverters (U8 - U11)
- ☐ (1) 74LS240 TRI-STATE® inverters (U12)

OTHER ELECTRONIC COMPONENTS

- ☐ (44) ceramic capacitors*
- ☐ (2) 39uF tantalum capacitors*
- ☐ (3) S I P resistor packs (R1, R2, R4)*
- ☐ (1) 1 8K 1/4 watt resistor (R3)*

MECHANICAL COMPONENTS

- ☐ (76) low profile sockets*
- ☐ (3) DIP switches*
- ☐ (1) instruction booklet

*Supplied already soldered to board

®TRI-STATE a trademark of National Semiconductor Corp

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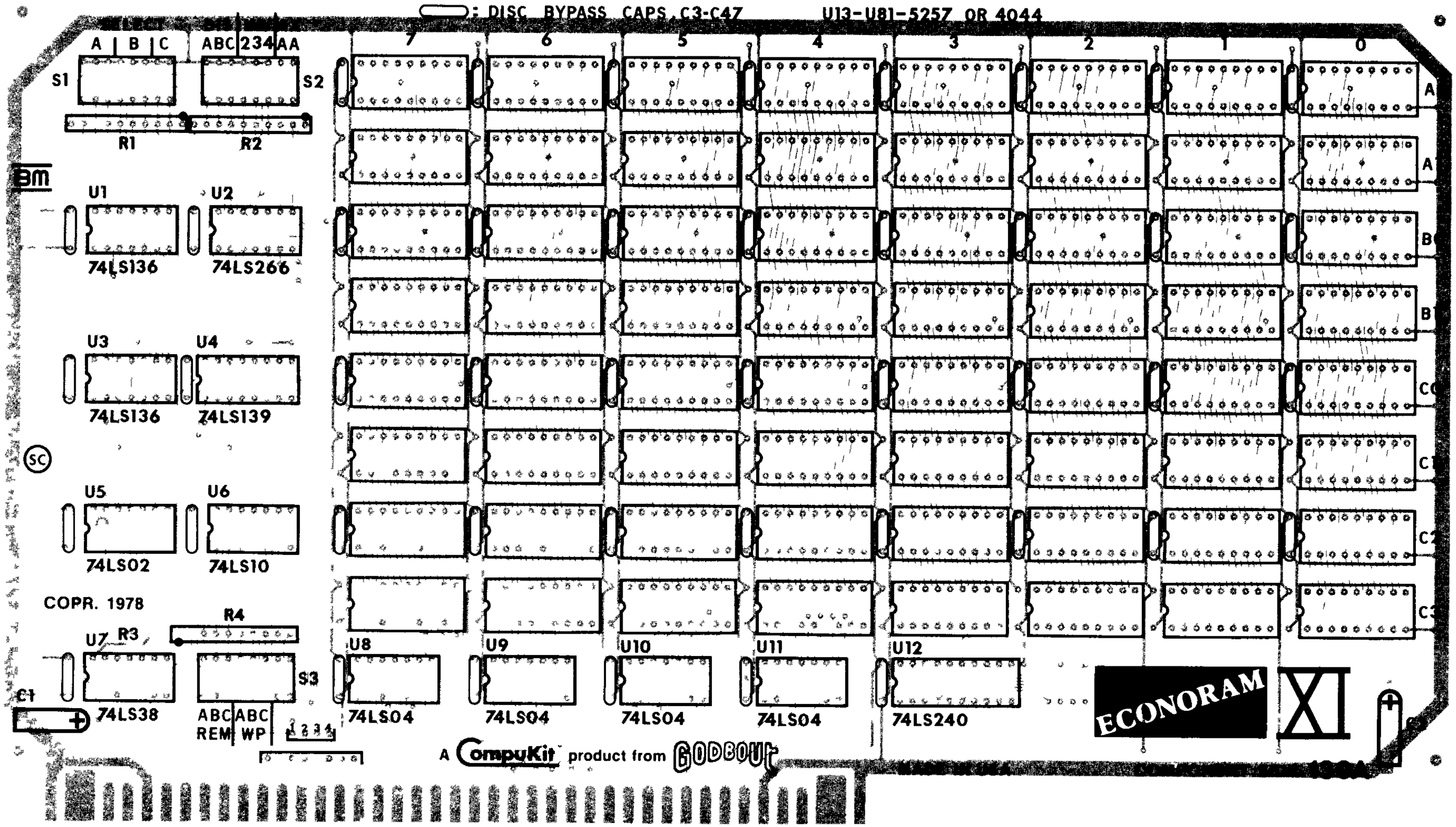


Component Layout

UP

MEMORY ADDRESS ASSIGNMENT

This board is addressable as three separate blocks on their respective boundaries Blocks A and B are 8K, Block C is 16K with switch positions as follows

	ADDRESS SWITCH POSITIONS	8K BLOCK STARTING ADDRESS	16K BLOCK STARTING ADDRESS	DISABLE SWITCH
BLOCK A	S1-1 2 3			S2-1
BLOCK B	S1-4 5 6			S2-2
BLOCK C	S1-7 8 X			S2-3
(0 = OFF)	0 0 0	0000	0000	
	0 0 1	2000		
(1 = ON)	0 1 0	4000	4000	
	0 1 1	6000		
	1 0 0	8000	8000	
	1 0 1	A000		
	1 1 0	C000	C000	
	1 1 1	E000		

In addition, S2 positions 1 - 3 disable blocks A - C respectively as noted above Each block may be disabled (switch on) or enabled (switch off) independently allowing the board to be configured as 8K, 16K, 24K or 32K A *deselected* block is transparent to the system (content of the memory may neither be changed nor read)

MEMORY WRITE PROTECT SWITCHES

DIP switch 3 position 1 - 6 are write enable switches Conversely, they may be used for manual write protection of the memory with *on* enabling and *off* protecting each block as follows

	WRITE ENABLE SWITCH	REMOTE WRITE PROTECT SWITCH
BLOCK A	S3 - 4	S3 - 1
BLOCK B	S3 - 5	S3 - 2
BLOCK C	S3 - 6	S3 - 3

Remote write protect may be implemented by connecting jumper position 4 to any unused buss pin A logic 0 or ground on that buss line with a remote switch or circuit board will write protect each block with the respective remote switch *on* Moreover the remote protect may be active high instead of low by setting S2 position 6 *on* (inv/4) If unused, the remote protect switches and the inv/4 switch should be in the *off* position Active low operating is the preferred mode of operation for this or any other feature

ADVANCED WRITE STROBE

Under normal operation a write cycle on the buss requires at least 2 wait states The main CPU/controller board, however, uses an advance write strobe that eliminates this delay on-board If this strobe is brought out onto the buss on one of the unused buss pins, it may be used by this memory board to eliminate the wait states by connecting the appropriate buss pin to jumper pad #1

For normal CPU configuration switch S2-8 (XA external acknowledge) should be ON and switch S2-7 (AA advance acknowledge) should be OFF Systems using AA (advance acknowledge) turn S2-7 ON and S2-8 OFF

QUALIFIERS

In addition to the normal address qualification this board has two unused qualifiers which may be used, if desired, for systems with more than the normal 64K of memory or other unusual applications Each is implemented by connecting the desired buss pin to jumper pads #2 and/or #3 These are active high (low to disable memory), but may be made active low by placing S2 positions 4 and/or 5 (labeled invert 2, invert 3 respectively) in the *on* position If the extra qualifiers are not used the associated invert switches MUST be in the *off* position

MEMORY

If the memory board seems to be working properly, the Memory Testing Routine can be used to give the board a more thorough workout It is rather slow, but will do the job well

The routine is set up to test 32K from 4000 hex up to 6000 hex This may be changed by entering a different starting address at "STRT (3001 - 3002) and/or a different end address at "END (3004 - high order byte only)

If the memory passes the test, it starts over again You may on the other hand, insert a jump instruction at "MARK to some user routine, or if desired the user may enter an output instruction, or can do a notification routine at "MARK to show successful completion and restart

If the memory fails the test critical information is stored and the routine enters a software "HALT that is a "jump to here at "SHLT Front panel lights, if any will show this state The user may then use the front panel or dump routines to display the following stored failure information

3069*	'FDE	-- D E pair D is the fill character and E is the test character
306B*	'FHL	-- H L pair the failure address
306D*	'FOUT	-- the data expected at this address
306E*	'FIN	-- the data read from the address

*address from Memory Testing Routing listing

The user may replace the 'jump at 'SHLT with a jump to a display or a notification routine

The difference between "FOUT and FIN should indicate which bit is failing indicating which chip or area is causing the problem

The test will find most of the harder to distinguish errors

MEMORY TESTING ROUTINE

```
3000 21 00 40          0010 STRT  LXI   H,40C0H
3003 3E 80             0020 END   MVI   A,80H
3005 32 6E 30          0030       STA   FIN
3008 3E 10             0040       MVI   A,10H
300A 84                0050       ADD   H
300B 4F                0060       MOV   C,A
300C 16 00             0070       MVI   D,0
300E 1E FF             0080       MVI   E,0FFH
3010 22 65 30          0090 DONE  SHLD  STAD
3013 AF                0100       XRA   A
3014 47                0110       MOV   B,A
3015 7B                0120 SCND  MOV   A,E
3016 5A                0130       MOV   E,D
3017 57                0140       MOV   D,A
3018 79                0150       MOV   A,C
3019 2A 65 30          0160       LHLD  STAD
301C 72                0170 FILL  MOV   M,D
301D 23                0180       INX   H
301E BC                0190       CMP   H
301F C2 1C 30          0200       JNZ   FILL
3022 2A 65 30          0210       LHLD  STAD
3025 73                0220 NEXT  MOV   M,E
3026 7B                0230       MOV   A,E
3027 BE                0240       CMP   M
3028 C2 6F 30          0250       JNZ   FAIL
302B 79                0260       MOV   A,C
302C 23                0270       INX   H
302D 94                0280       SUB   H
302E C2 4D 30          0290       JNZ   NDON
3031 B8                0300       CMP   B
3032 44                0310       MOV   B,H
3033 CA 15 30          0320       JZ    SCND
3036 3A 66 30          0325       LDA   STAD+1
3039 00                0330 MARK  NOP
303A 00                0331       NOP
303B 00                0332       NOP
303C 3A 6E 30          0340       LDA   FIN
303F B9                0350       CMP   C
3040 CA 00 30          0360       JZ    STRT
3043 79                0370       MOV   A,C
3044 67                0380       MOV   H,A
3045 2E 00             0390       MVI   L,0
3047 C6 10             0400       ADI   10H
3049 4F                0410       MOV   C,A
304A C3 10 30          0420       JMP    DONE
304D 22 67 30          0430 NDON  SHLD  NXAD
3050 7A                0440 LOPB  MOV   A,D
3051 BE                0450 LOPA  CMP   M
3052 C2 6F 30          0460       JNZ   FAIL
3055 2C                0470       INR   L
3056 C2 51 30          0480       JNZ   LOPA
3059 79                0490       MOV   A,C
305A 24                0500       INR   H
305B BC                0510       CMP   H
305C C2 50 30          0520       JNZ   LOPB
305F 2A 67 30          0530       LHLD  NXAD
3062 C3 25 30          0540       JMP   NEXT
3065                   0550 STAD  DS    2
3067                   0560 NXAD  DS    2
3069                   0570 FDE   DS    2
306B                   0580 FHL   DS    2
306D                   0590 FOUT  DS    1
306E                   0600 FIN   DS    1
306F 22 6B 30          0610 FAIL  SHLD  FHL
3072 32 6D 30          0620       STA   FOUT
3075 7E                0630       MOV   A,M
3076 32 6E 30          0640       STA   FIN
3079 EB                0650       XCHG
307A 22 69 30          0660       SHLD  FDE
307D C3 7D 30          0670 SHLT  JMP SHLT
3080                   0680 *
```

CIRCUIT DESCRIPTION

The heart of ECONORAM XI is the MM5257/TMS4044 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1 memory IC) Unlike standard RAMs those included with your kit are specifically designated by the manufacturer as low power, high speed parts

These ICs are arranged in rows that are 8 ICs wide This way, each row can store 4K x 8 bits of information Paralleling 8 or these rows together produces a total memory storage of 32K x 8 bits *(Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array)*

Now that we have this storage, there are still other aspects we must consider first, addressing a specific location in memory, and second, *writing* data into the memory or *reading* data from the memory

The logic diagram on Pages 8 and 9 show the address circuitry along with the other ECONORAM XI circuitry Each memory IC requires 12 address bits (ADDR0 - ADDR9, ADDRA - ADDRB) to access any one of the 4096 bits available in the IC These address bits are generated by the CPU and are buffered by a number of inverters After buffering, a particular address is presented to all IC address selection pins However, we additionally need to select which particular row of ICs is to react to the given address This requires 4 more address bits (ADDC - F) which are decoded and used to enable the desired row of ICs *(note row markings along the right-hand side of the memory array)*

When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (bufering prevents loading of the data buss) Data to be read onto the data buss from memory passes through 8 TRI-STATE® inverting buss drivers When data is not being read onto the buss, the outputs of these inverters are in a high-impedence or "disconnected ' state

To prevent IC generated switching transient noise problems, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC

This board is guaranteed to operate at 4 MHz over the full temperature range (0-70 C ambient) and to draw less than 3500 mA (3 5 amps) Our typical measured currents were less than 3000 mA at cold start-up, rapidly decreasing to 2400 - 2800 mA, depending on the ambient temperature

It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards

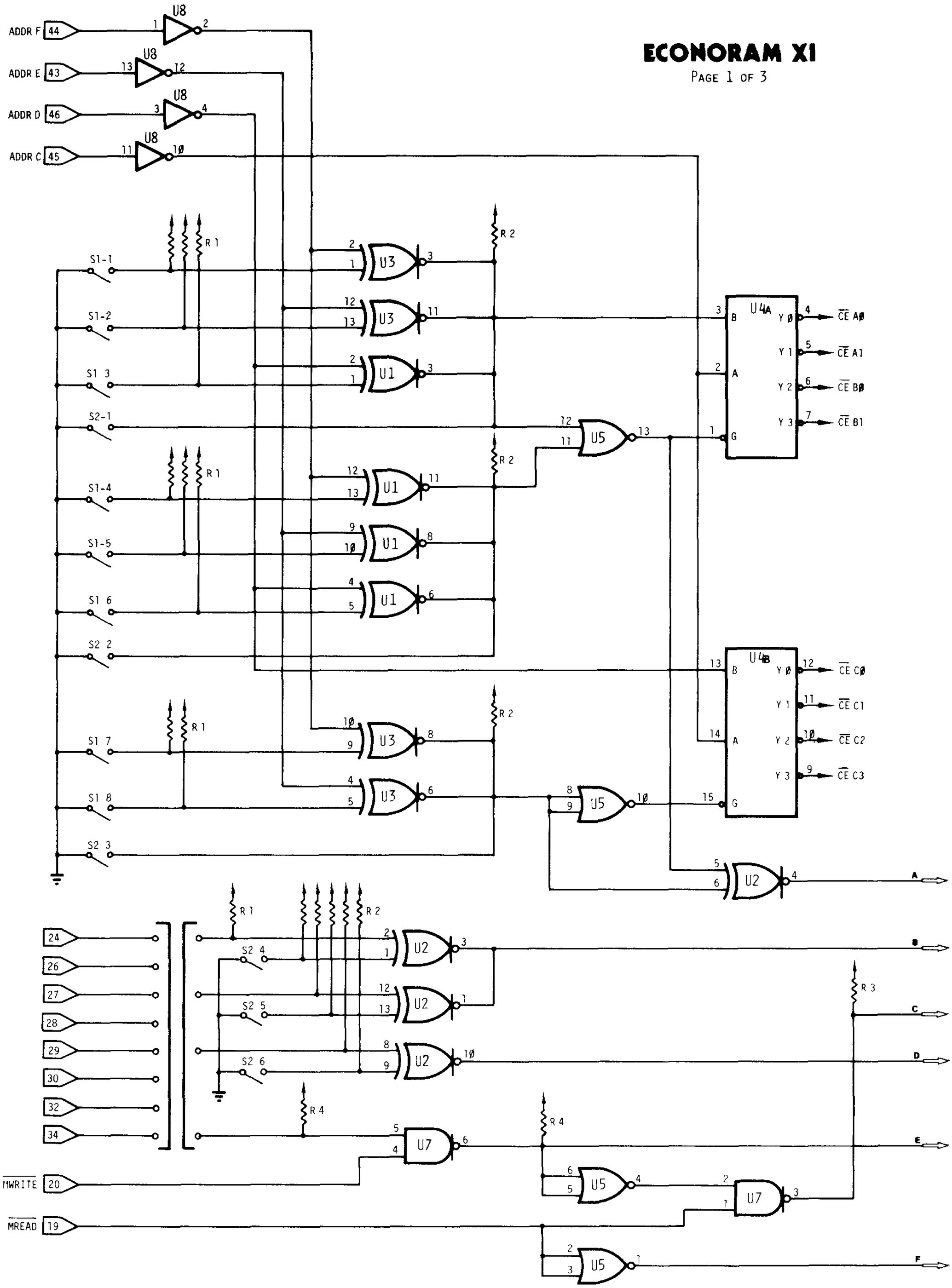
THANK YOU

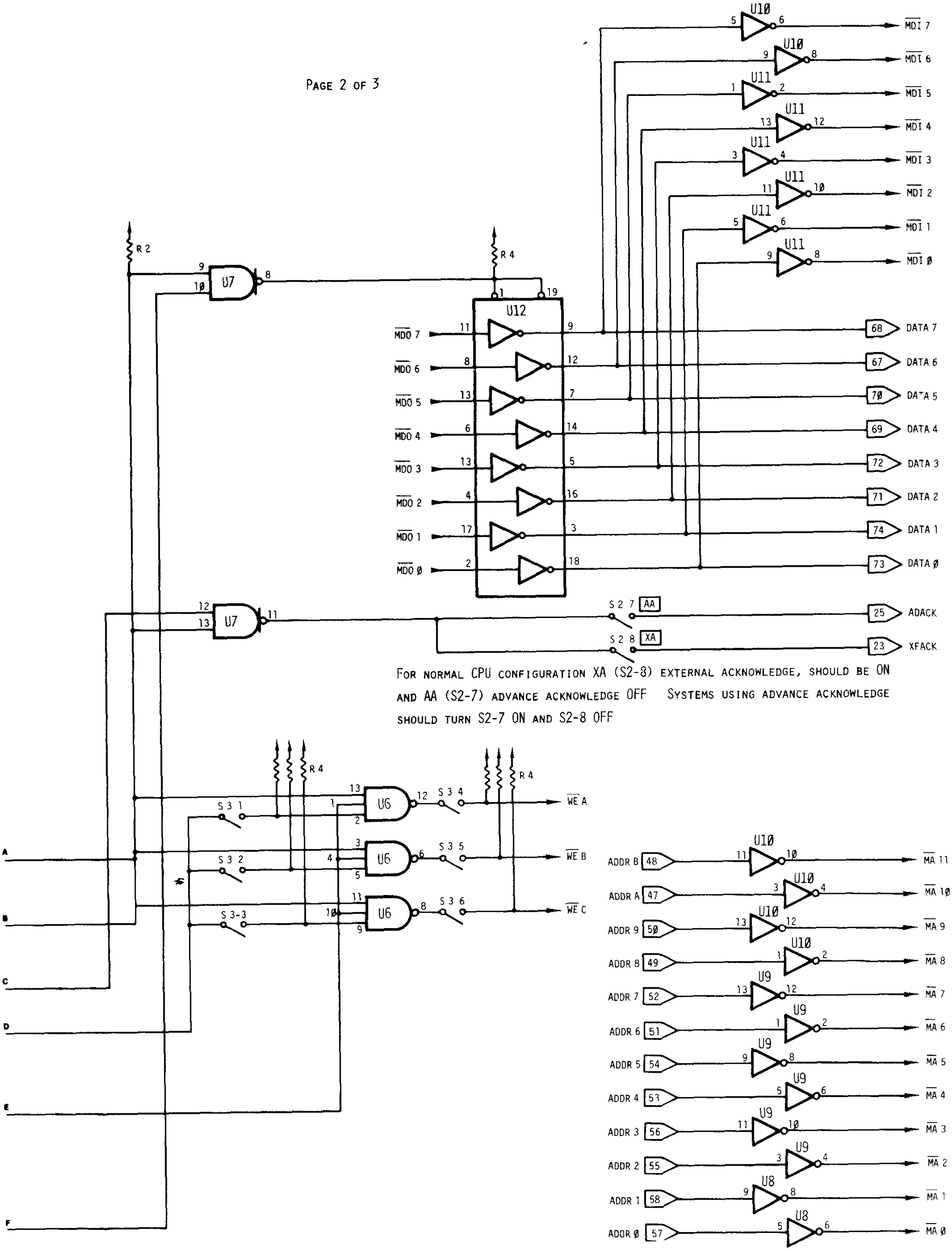
This board is the result of much time, work and experience on the part of a number of people In addition to thanking you for choosing this board, we d like to thank everyone involved for their work on this project

We strive for a board that doesn t just work the first time, but continues to give reliable operation for a long time If we can be of any help to you in applying this board, or if you have any questions, please let us know As always, we solicit your comments letters and new product suggestions

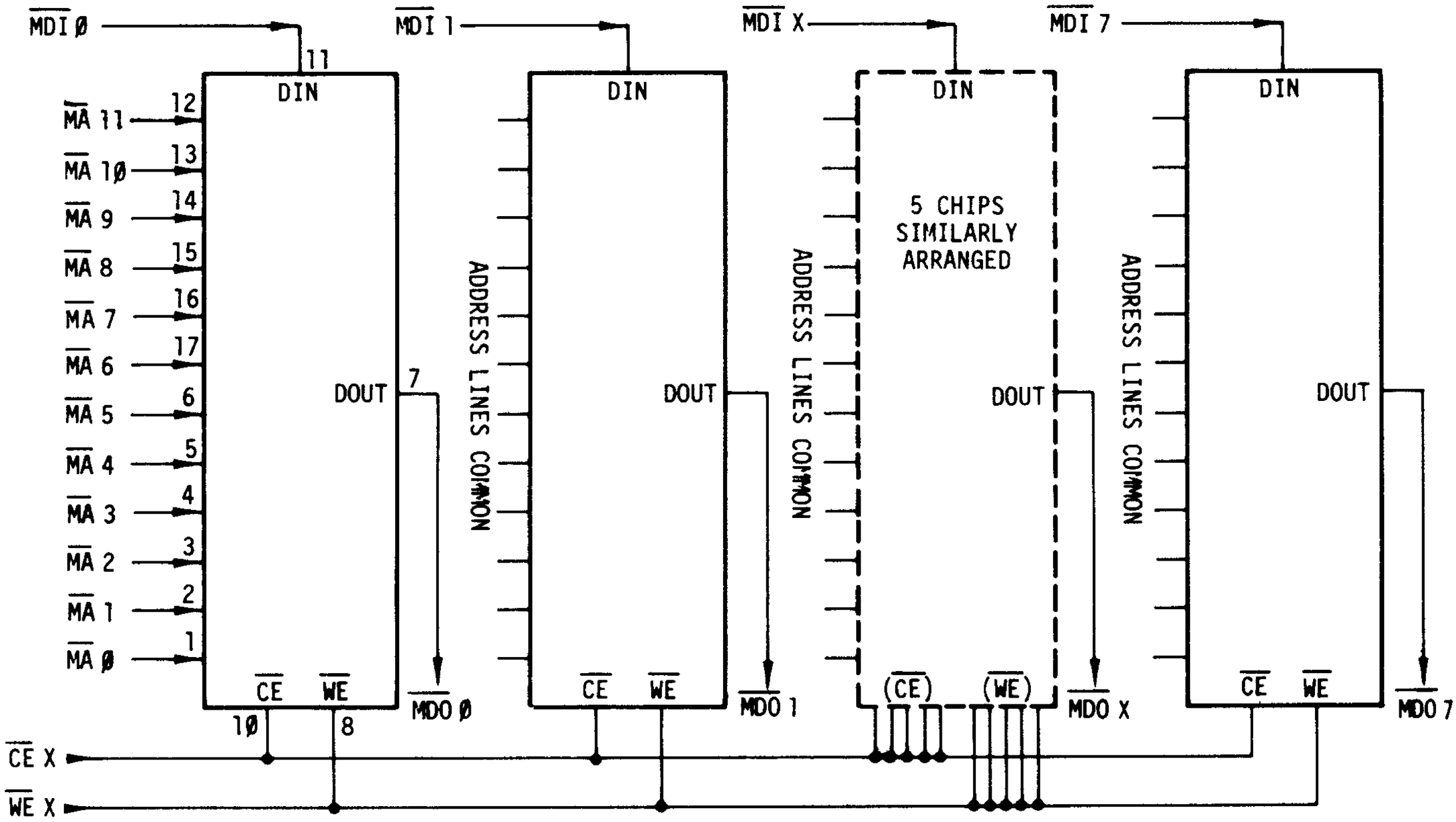
HAPPY COMPUTING!

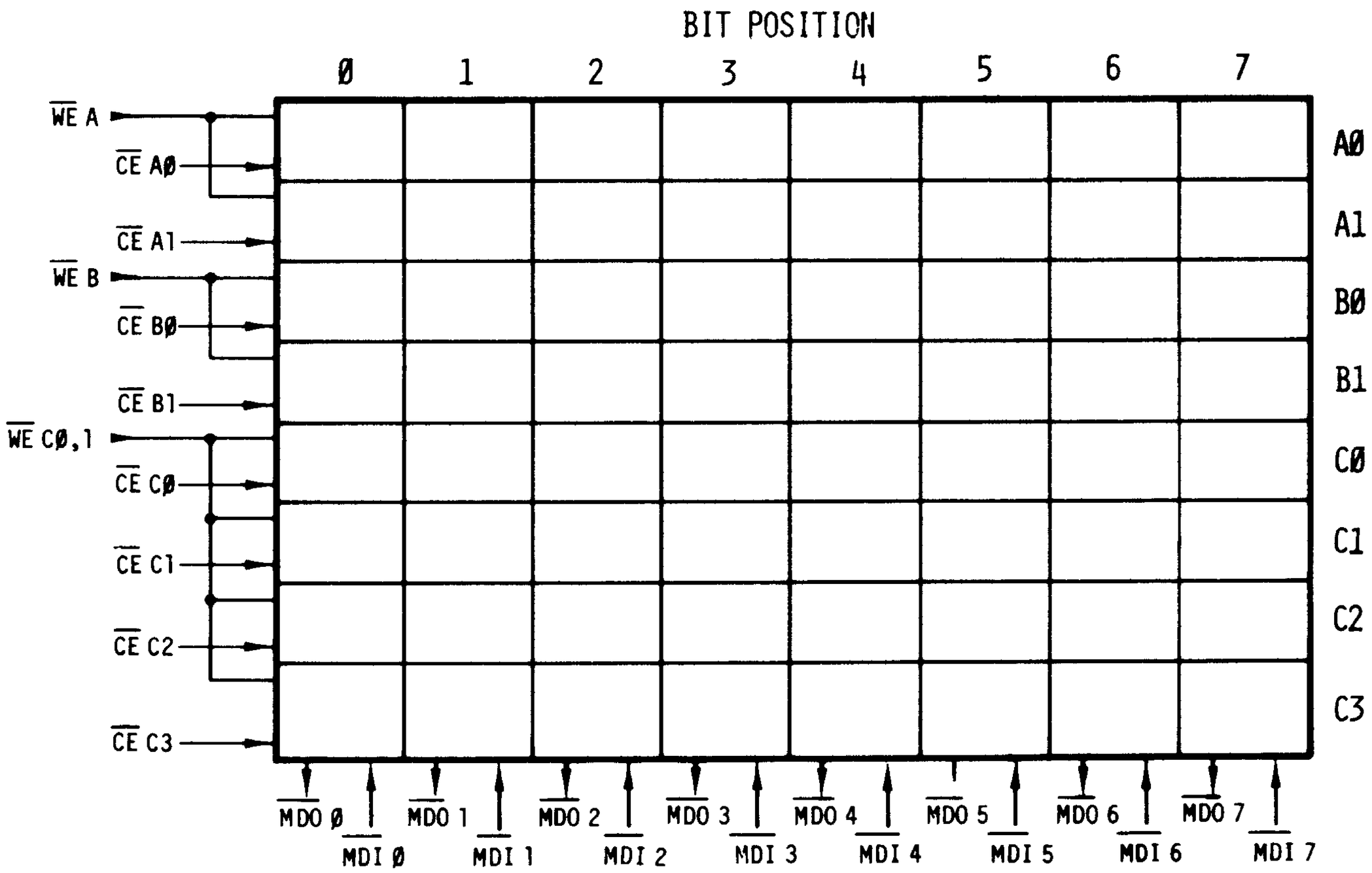
ECONORAM XI


ADDR F 44
ADDR E 43
ADDR D 46
ADDR C 45
U8
S1-1
S1-2
S1 3
S2-1
S1-4
S1-5
S1 6
S2 2
S1 7
S1 8
S2 3
R 1
R 2
U3
U1
U5
U4A
U4B
U2
U7
CE A0
CE A1
CE B0
CE B1
CE C0
CE C1
CE C2
CE C3
A
B
C
D
E
F
R 3
R 4
S2 4
S2 5
S2 6
24
26
27
28
29
30
32
34
MWRITE 20
MREAD 19

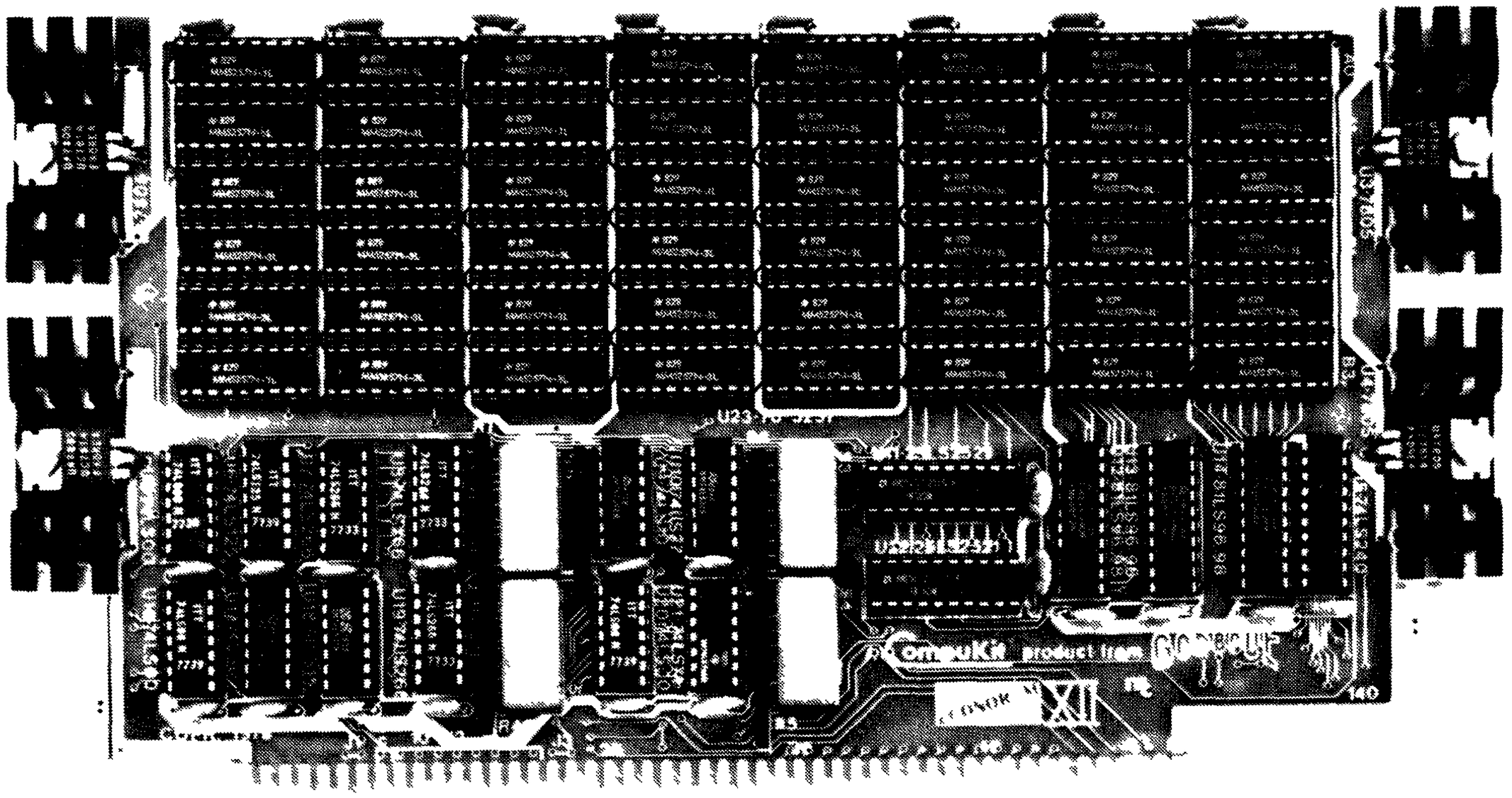


FOR NORMAL CPU CONFIGURATION XA (S2-8) EXTERNAL ACKNOWLEDGE, SHOULD BE ON AND AA (S2-7) ADVANCE ACKNOWLEDGE OFF SYSTEMS USING ADVANCE ACKNOWLEDGE SHOULD TURN S2-7 ON AND S2-8 OFF


MDI Ø
MDI 1
MDI X
MDI 7
DIN
DOUT
11
12
13
14
15
16
17
6
5
4
3
2
1
7
MA 11
MA 1Ø
MA 9
MA 8
MA 7
MA 6
MA 5
MA 4
MA 3
MA 2
MA 1
MA Ø
CE
WE
1Ø
8
MDO Ø
MDO 1
MDO X
MDO 7
ADDRESS LINES COMMON
5 CHIPS
SIMILARLY
ARRANGED
(CE)
(WE)
CE X
WE X


BIT POSITION
Ø
1
2
3
4
5
6
7
WE A
CE AØ
CE A1
WE B
CE BØ
CE B1
WE CØ,1
CE CØ
CE C1
CE C2
CE C3
AØ
A1
BØ
B1
CØ
C1
C2
C3
MDO Ø
MDO 1
MDO 2
MDO 3
MDO 4
MDO 5
MDO 6
MDO 7
MDI Ø
MDI 1
MDI 2
MDI 3
MDI 4
MDI 5
MDI 6
MDI 7

ECONORAM XII™
USER'S MANUAL



bank select
16K/24K x 8 static memory
using MM5257/TMS40L44 • 4MHz
S-100

140

CompuPro™ from GODBOUT

BANK SWITCHING THEORY

The purpose behind Bank switching is to allow the microcomputer user to access and write to more than the typical 64K that most micros can directly address. To allow this, the ECONORAM XII allows chunks of memory to be selectively enabled and disabled by outputting to data bit 0 of a use-specified port, (a "1" or a "0"). For example, if one Bank is specified as Port 40H, outputting a "0" to data bit 0 (Port 40H) will disable the memory associated with that bank. By then outputting a "1" to data bit 0 (port 40H), the memory will then be enabled. In addition, the status of the memory controlled by a certain port (i.e. port 40H) can be sampled to tell if the memory is currently enabled or disabled by inputting from the port (40H) and checking data bit 0. If data bit 0 is a "1", the memory is enabled. If it is a "0", the memory is disabled.
NOTE: Care should be taken to first disable an enabled bank before enabling the disabled bank to insure that no memory conflicts occur.

BANK PORT ADDRESSING

S3

A 7	1
A 6	2
A 5	3
A 4	4
A 3	5
A 2	6
A 1	7
A 0	8

(ON=1)
(OFF=0)

BANK 1

S4

A 7	1
A 6	2
A 5	3
A 4	4
A 3	5
A 2	6
A 1	7
A 0	8

(ON =1)
(OFF=0)

BANK 2

Example: positions 1-8 on=port FFH
positions 1-8 off=port 00H
positions 1-4 on
positions 5-8 off } port F0H

Output '1' to bit '0'-enables the bank
Output '0' to bit '0'-disables the bank

Input '1' from bit '0'-bank is enabled
Input '0' from bit '0'-bank is disabled

SWITCH

S1

BLOCK A	A15	1	Address A-15 (ON="1") (OFF="0")
	A14	2	Address A-14
	A13	3	Address A-13
	A-D15	4	On= disabled OFF= enabled
BLOCK B	A15	5	Address A-15 (ON="1") (OFF="0")
	A14	6	Address A-14
	A13	7	Address A-13
	B-DIS	8	On= disabled OFF= enabled

S2

BLOCK C	A15	1	Address A15 (ON="1") (OFF="0")
	A14	2	Address A14
	A13	3	Address A13
	C-DIS	4	ON= disabled OFF= enabled
	1-EPU	5	BANK 1 enable on power-up
	2-EPU	6	BANK 2 enable on power-up
	1-DPU	7	BANK 1 disable on power-up
	2-DPU	8	BANK 2 disable on power-up

POWER-UP ENABLE/DISABLE

The 2 Banks on the Econoram XII can be selectively enabled or disabled on power-up to eliminate memory conflicts. To enable a BANK on power-up, turn the EPU switch on and the DPU switch off. To have a Bank disabled on power-up, turn the DPU switch on and the EPU switch off.

MEMORY ADDRESS ASSIGNMENT

This board is addressable as three separate 8K x 8 blocks, identified as A, B and C. These three blocks comprise the two Banks, with block A associated with Bank 1 and blocks B and C associated with Bank 2. Addressing of the Banks will be discussed below.

Switch	Position A15	A14	A13	Hex Starting Address	Disable Switch position
BLOCK A S1	1	2	3		4
BLOCK B S1	5	6	7		8
BLOCK C S2	1	2	3		4
	0	0	0	0 0 0 0	
	0	0	1	2 0 0 0	
	0	1	0	4 0 0 0	
	0	1	1	6 0 0 0	
	1	0	0	8 0 0 0	
	1	0	1	A 0 0 0	
	1	1	0	C 0 0 0	
	1	1	1	E 0 0 0	

(MEMORY ADDRESS ASSIGNMENT CONT.)

Each Block may be disabled by putting the associated disable switch (shown on last page) in the on position. A disabled block is transparent to the system and its contents may be neither changed or read.
NOTE: Purchasers of the ECONORAM XII-16K bank select board should disable the 8K block not populated on the board.

POWER-UP ENABLE/DISABLE

The two Banks on the ECONORAM XII can be selectively enabled or disabled on power-up to eliminate memory conflicts. To enable a BANK on power-up, turn the EPU switch on and the DPU switch off. To have a Bank disabled on power-up, turn the DPU switch on and the EPU switch off.

PHANTOM LINE

PHANTOM (Buss pin 67) can be jumpered to disable BANK 1, BANK 2 or both BANKS by simply installing a jumper.

A jumper installed at J4 will enable BANK 1 to be phantomed by the system.

A jumper installed at J3 will enable BANK 2 to be phantomed by the system.

CAUTION

Some manufacturers use the PHANTOM line as a refresh signal for dynamic memories. This will conflict with the PHANTOM feature and cause boards with PHANTOM to fail. If your system has this conflict, it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PAHNTOM feature on this and other boards.

Econoram XII - PARTS LIST

16K and 24K Bank Select Ram for S-100 Bus

(1) Econoram XII Circuit Board

INTEGRATED CIRCUITS

(32) MM5257N-3L (16K KIT)

(48) MM5257N-3L (24K KIT)

(3) 74LS00 Quad NAND (U5, U16, U20)

(1) 74LS02 Quad NOR (U17)

(1) 74LS10 Triple 3 input NAND (U9)

(1) 74LS15 Triple 3 input O.C. AND (U18)

(1) 74LS27 Quad NOR (U10)

(1) 74LS74 Dual D type Flip Flop (U21)

(1) 74LS125 Quad tri-state buffers (U6)

(1) 74LS240 Octal bus Driver (U15)

(3) 74LS266 Quad O.C. X-NOR (U7, U8, U19)

(3) 81LS96/98 Octal Bus Driver (U12, U13, U14)

(2) 25LS521 Octal Comparator (U11, U22)

(4) 7805 + 5 Volt regulator (U1, U2, U3, U4)

OTHER ELECTRONIC COMPONENTS

(5) SIP resistor packs (R1-R5)*

(8) 39uf tantalum capacitors (C1-C8)

(26) Ceramic Bypass Capacitors*

MECHANICAL COMPONENTS

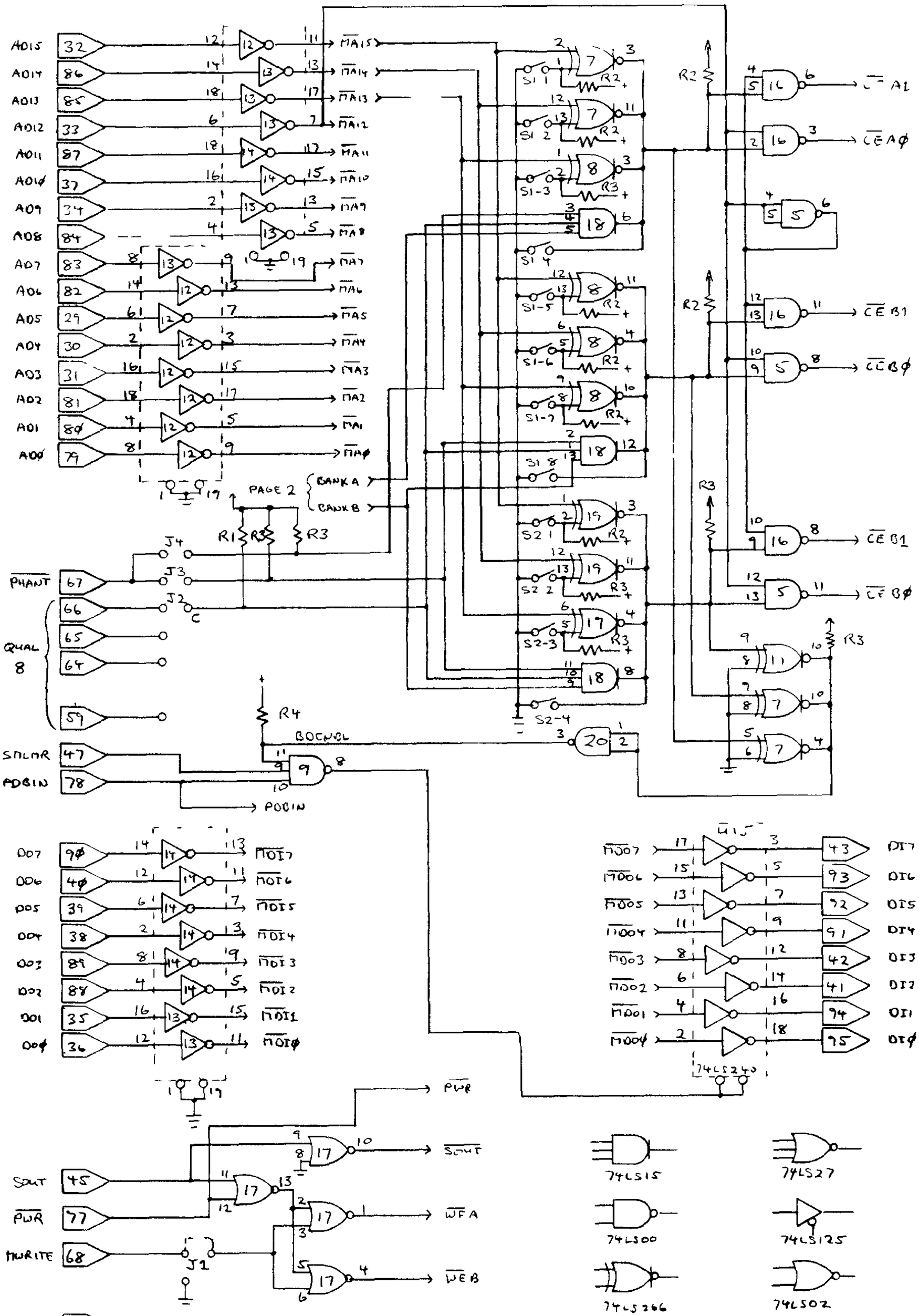
(66) Low Profile sockets*

(4) Dipswitch, 8 position (S1-S4)*

(4) TO-220 Heat Sinks

(4) Sets 6-32 Hardware

* Supplied already soldered to board.


ECONORAM XII
#140 24K X 8 S100 BANK SELECT RAM
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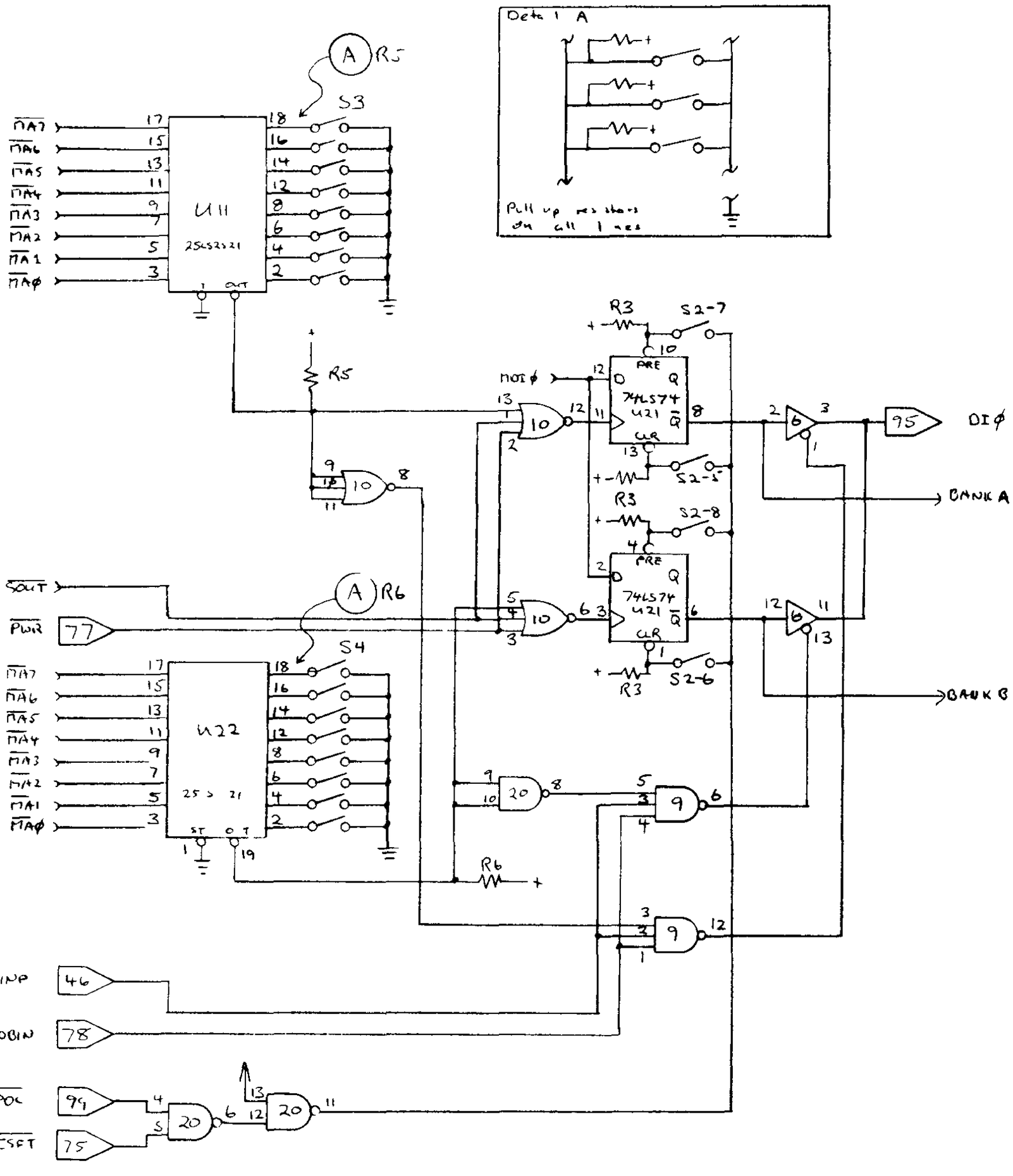
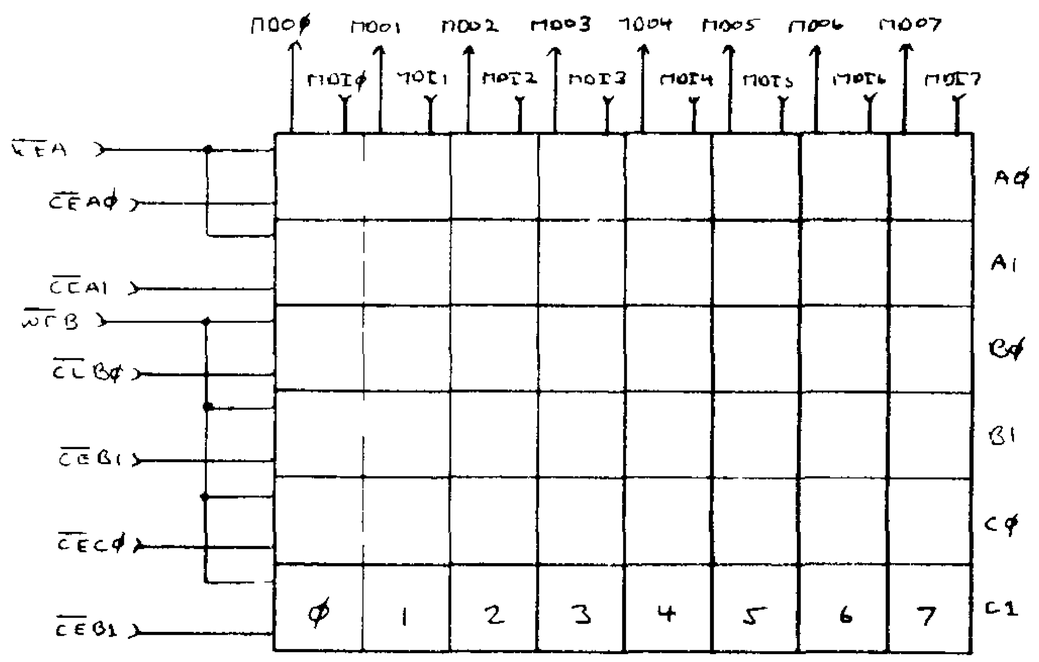
page 1 of 2
74LS15
74LS27
74LS00
74LS125
74LS266
74LS02
74LS240
7805
3 MORE LIKE BEFORE
BANKA
BANKB
PAGE 2
PHANT
QUAL 8
SMEMR
PDBIN
PWR
SOUT
PWRITE
WFA
WEB





140 24KX8 S100 BANK SELECT RAM
ECONORAM XII

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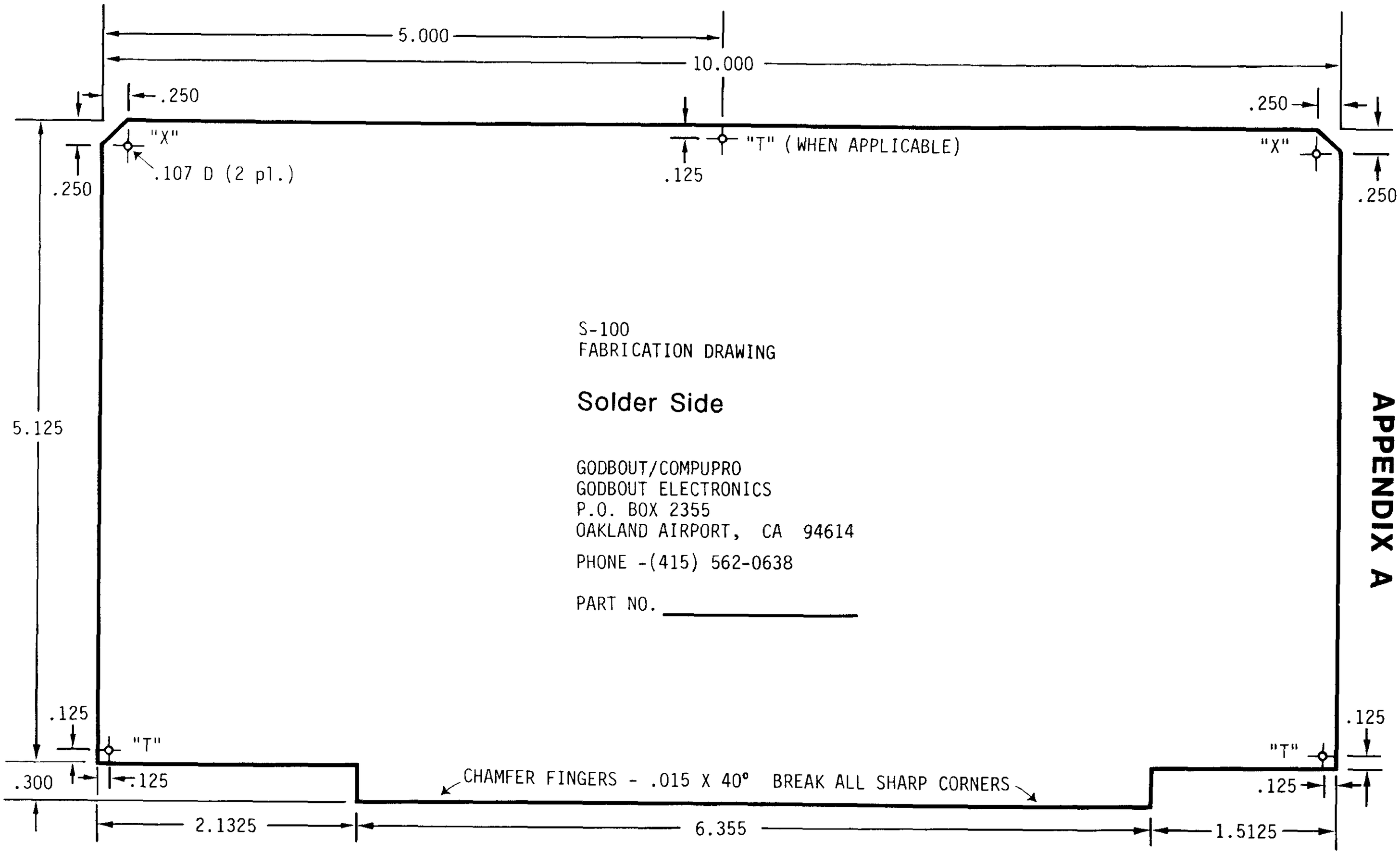
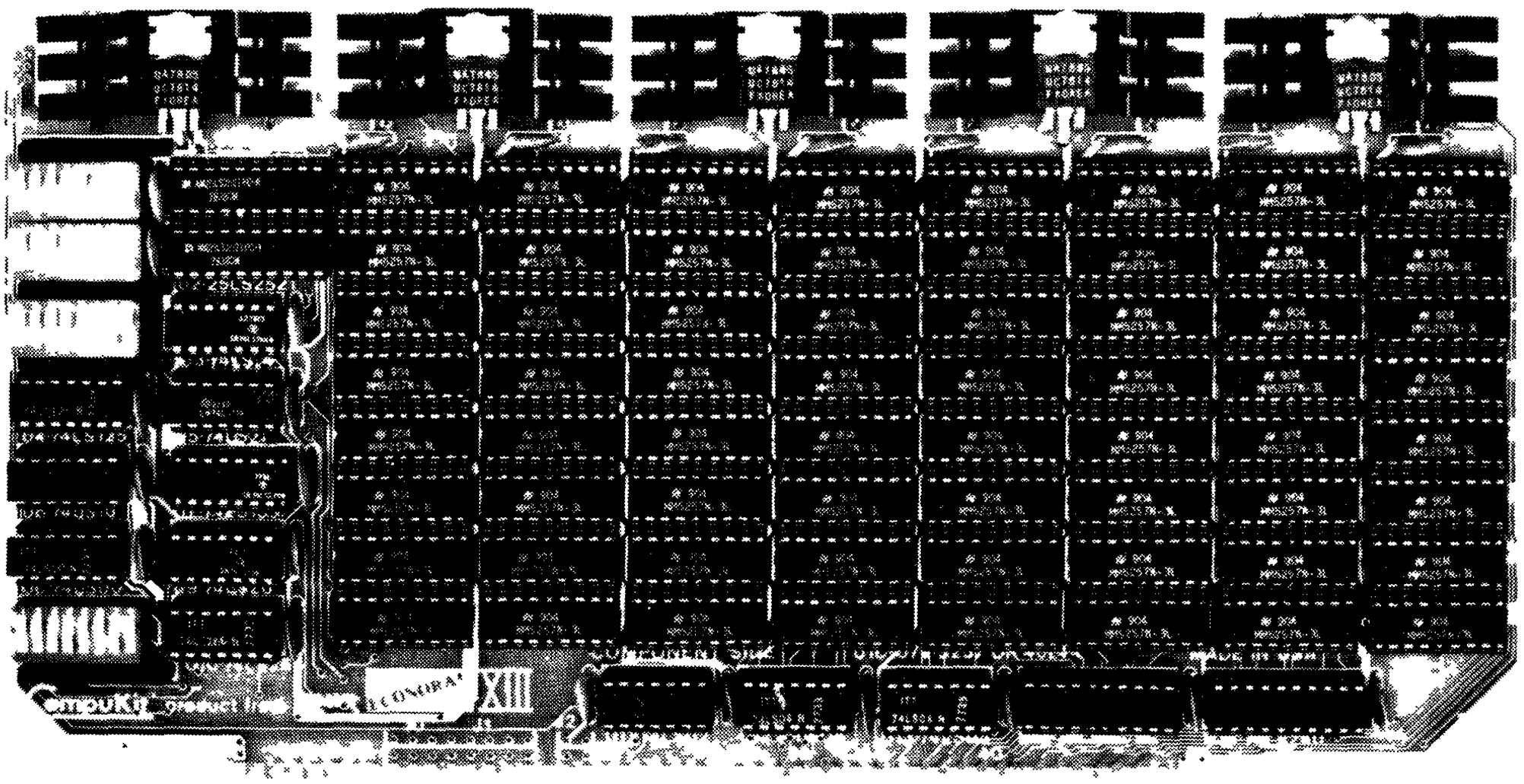


1. BOARD CORNERS ARE REFERENCES FOR ALL DIMENSIONS
2. TOOLING HOLES ("T") ARE LOCATED EXACTLY .125 FROM EDGES
3. FABRICATION TOLERANCE - .005 ON ALL DIMENSIONS.
4. ALL DIMENSIONS IN INCHES.

CONTINUED page 110

ECONORAM XIII™
USER'S MANUAL



bank select
32K x 8 static memory • S-100
using MM5257/TMS40L44 • 4MHz

141

CompuPro™ from GODBOUT

Econoram XIII - PARTS LIST

32K Bank Select Ram for S-100 bus

(1) Econoram XIII Circuit Board

INTEGRATED CIRCUITS

(64) MM5257N-3L 4Kx1 Static Ram

(1) 74LS00 Quad 2 input NAND (U8)

(1) 74LS02 Quad 2 input NOR (U11)

(2) 74LS04 Hex inverter (U12, U13)

(1) 74LS10 Triple 3 input NAND (U6)

(1) 74LS20 Dual 4 input NAND (U9)

(1) 74LS27 Triple 3 input NOR (U5)

(1) 74LS74 Dual "D" Flip Flop (U3)

(1) 74LS125 Quad Tri-State buffer (U4)
(1) 74LS139 Decoder (U7)
(1) 74LS240 Octal Bus Driver (U15)

(1) 74LS266 Quad 2 input X-NOR (U10)

(1) 81LS96/98 Octal Bus Driver (U14)

(2) 25LS2521 Octal Comparator (U1, U2)

(5) 7805 5 Volt Regulator

OTHER ELECTRONIC COMPONENTS

(4) SIP Resistor Packs (R1-R4) *

(10) 39 uf tantalum capacitors (C1-C10)

(24) Ceramic Bypass Capacitors *

MECHANICAL COMPONENTS

(79) Low Profile sockets *

(4) Dipswitch, 8 position (S1-S4)*

(4) TO-220 Heat Sinks

(4) Sets 6-32 Hardware

* supplied already soldered to board.

BANK SWITCHING THEORY

The purpose behind Bank switching is to allow the micro-computer user to access and write to more than the typical 64K that most micros can directly address. To allow this, the ECONORAM XIII allows chunks of memory to be selectively enabled and disabled by outputing to data bit Ø of a use-specified port. (a " 1" or a " Ø "). For example, if one Bank is specified as Port 4ØH, outputing a " Ø" to data bit Ø (Port 4ØH) will disable the memory associated with that bank. By then outputing a " 1" to data bit Ø (port 4ØH), the memory will then be enabled. In addition, the status of the memory controlled by a certain port (i.e. port 4ØH) can be sampled to tell if the memory is currently enabled or disabled by inputing from the port (4ØH) and checking data bit Ø. If data bit Ø is a " 1" , the memory is enabled. If it is a " Ø" , the memory is disabled.

NOTE: Care should be taken to first disable an enabled bank before enabling the disabled bank to insure that no memory conflicts occur.

BANK PORT ADDRESSING

S1

1	2	3	4	5	6	7	8
A Ø	A 1	A 2	A 3	A 4	A 5	A 6	A 7

BANK A
(ON=1)
(OFF=Ø)

S2

1	2	3	4	5	6	7	8
A Ø	A 1	A 2	A 3	A 4	A 5	A 6	A 7

BANK B
(ON=1)
(OFF=Ø)

Example: positions 1-8 on=port FFH
positions 1-8 off=port ØØH
positions 1-4 on port ØFH
positions 5-8 off

Output " 1" to bit " Ø" -enables the bank
Output " Ø" to bit " Ø" -disables the bank

Input " 1" from bit " Ø" -bank is enabled
Input " Ø" from bit " Ø" -bank is disabled

Power-up ENABLE/DISABLE

S3

SWITCH 1 2 3 4	5	6	7	8
	'B'		'A'	
NOT USED	DPU	EPU	DPU	EPU

BANK (A or B)
DPU= Disable on Power-Up
EPU= Enable on Power-Up

CONT.

The 2 Banks on the Econoram XIII can be selectively enabled or disabled on power-up to eliminate memory conflicts. To enable a BANK on power-up, turn the FPU switch on and the DPU switch off. To have a Bank disabled on power-up, turn the DPU switch on and the EPU switch off.

MEMORY ADDRESS ASSIGNMENT

This Board is addressable a two separate 16Kx8 block, with Block A associated with Bank A, and Block B associated with Bank B. Addressing is described below:

S4

SWITCH							
1	2	3	4	5	6	7	8
A	A	A	B	A	A	A	B
D	1	1	D	1	1	P	P
I	4	5	I	4	5	H	H
S			S				

Position	Bank	
(1)	A	ON= disabled
(2)	A	Address A14
(3)	A	Address A15
(4)	B	ON= disabled
(5)	B	Address A14
(6)	B	Address A15
(7)	A	PHANTOM on=enabled
(8)	B	PHANTOM on=enabled

	Position (Switch S4)			HFX STARTING ADDRESS
	A 15	A 14	DISABLE	
BLOCK A	3	2	1	
BLOCK B	6	5	4	
(ON=" Ø")	Ø - ON	Ø - ON		0 0 0 0
	Ø - ON	1 - OFF		4 0 0 0
	1 - OFF	0 - ON		8 0 0 0
(OFF- " 1")	1 - OFF	1 - OFF		C 0 0 0

PHANTOM LINF

PHANTOM (BUS PIN 67) can be switched to disable either or both BANKS for power-on jumps and booting.

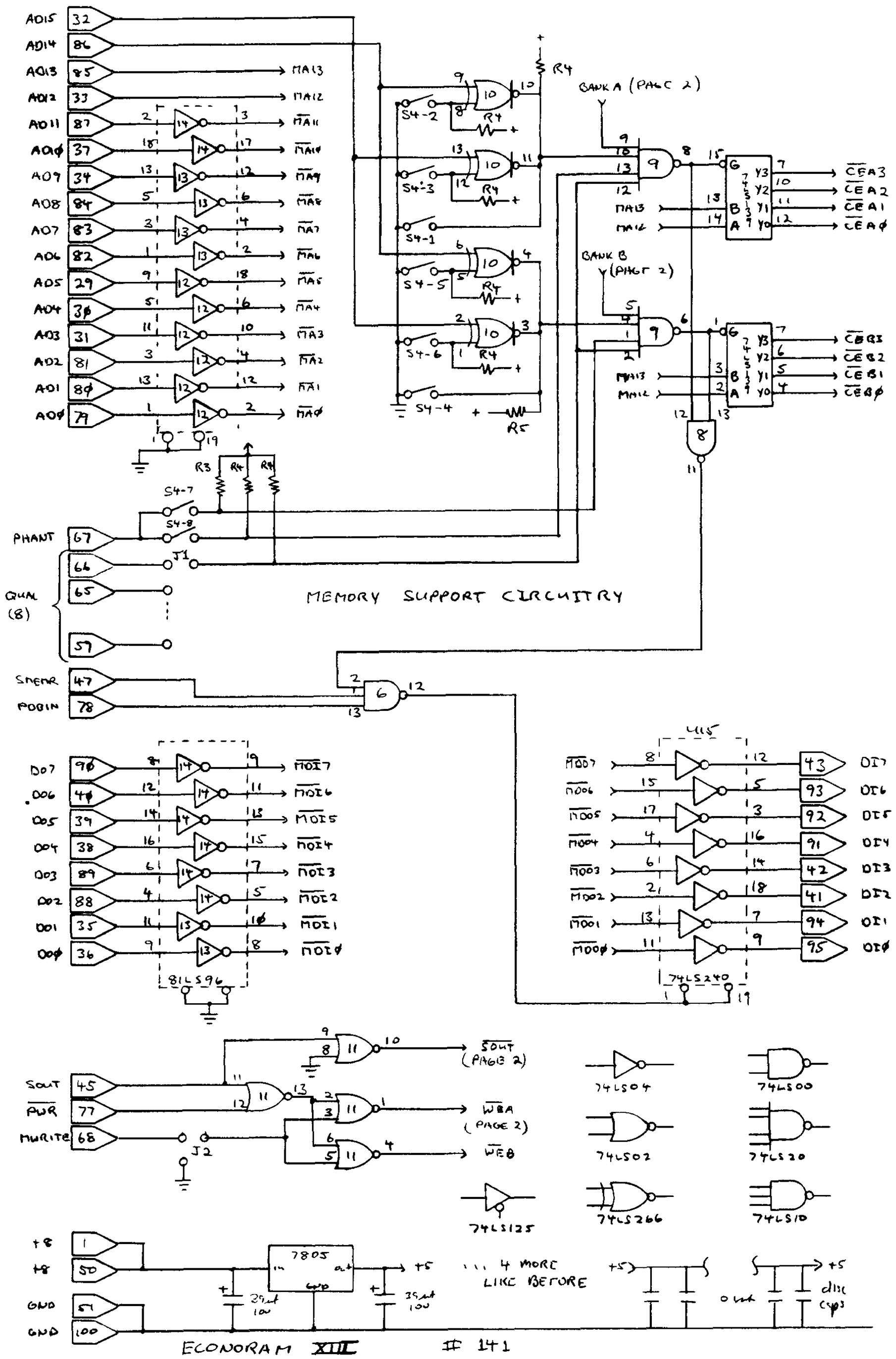
Switching position 7 of S4 " on" will enable PHANTOM on Bank A.

Switching position 8 of S4 " on" will enable PHANTOM on Bank B.

With either position 7 or 8 off, the corresponding BANK will not be disabled by the PHANTOM signal.

CAUTION

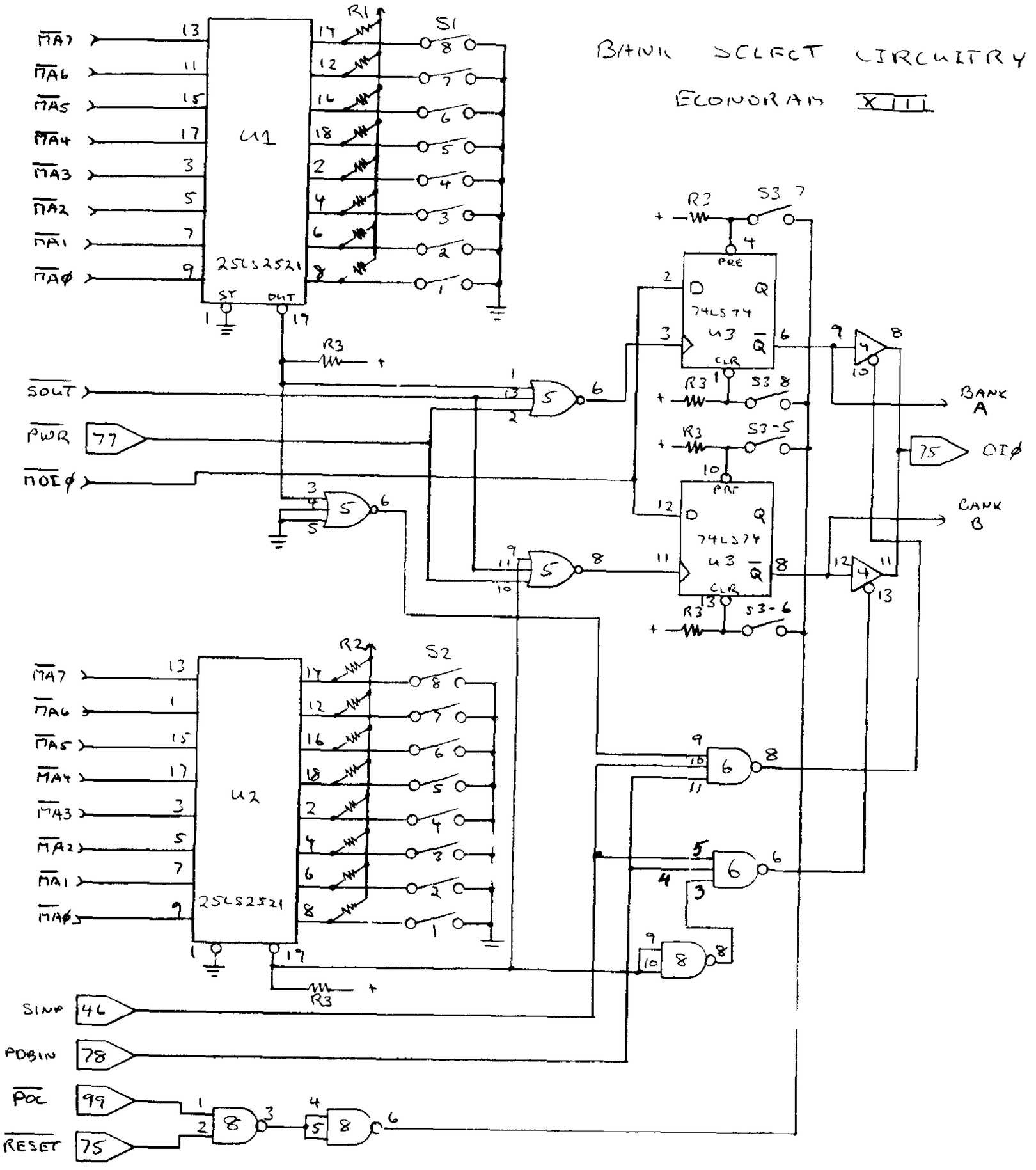
Some manufacturers use the PHANTOM line as a refresh signal for dynamic memories. This will conflict with the PHANTOM feature and cause boards with PHANTOM to fail. If vour system has this conflict, it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards.

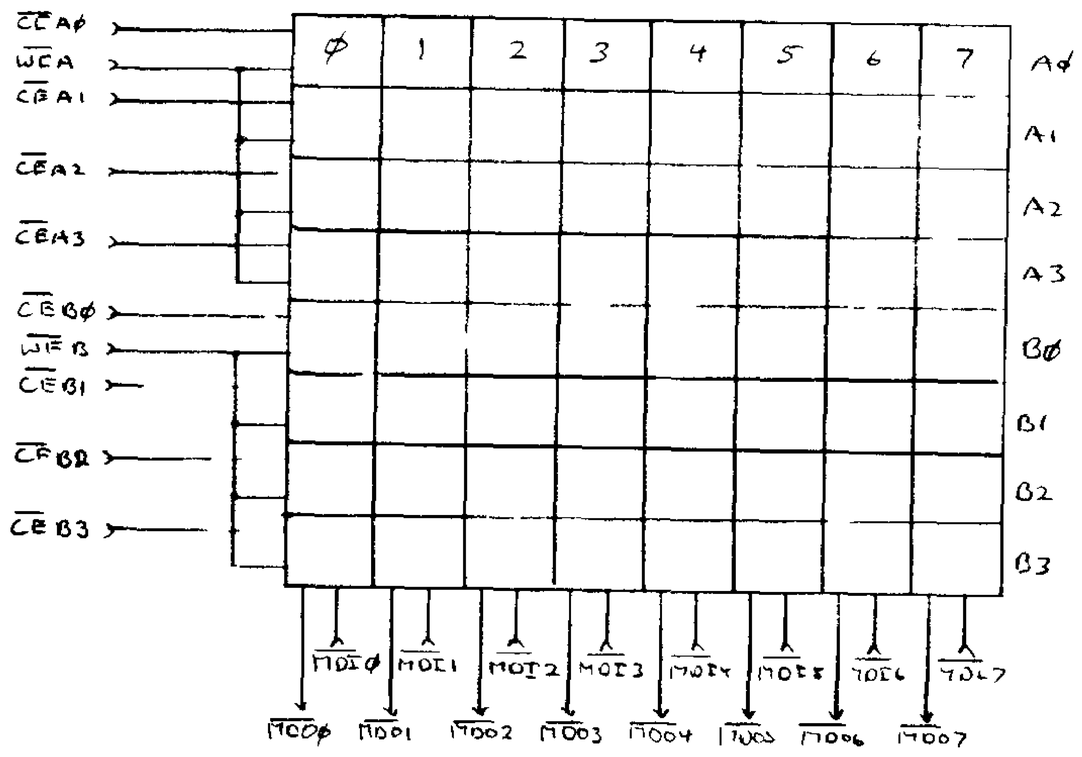


ECONORAM XIIC # 141

32KX8 S100 BANK SELECT RAM © Godbout Electronics 1979

PAGE 1 of 2





ECONORAM XIII

32K x 8 S100 BANK SELECT RAM # 141

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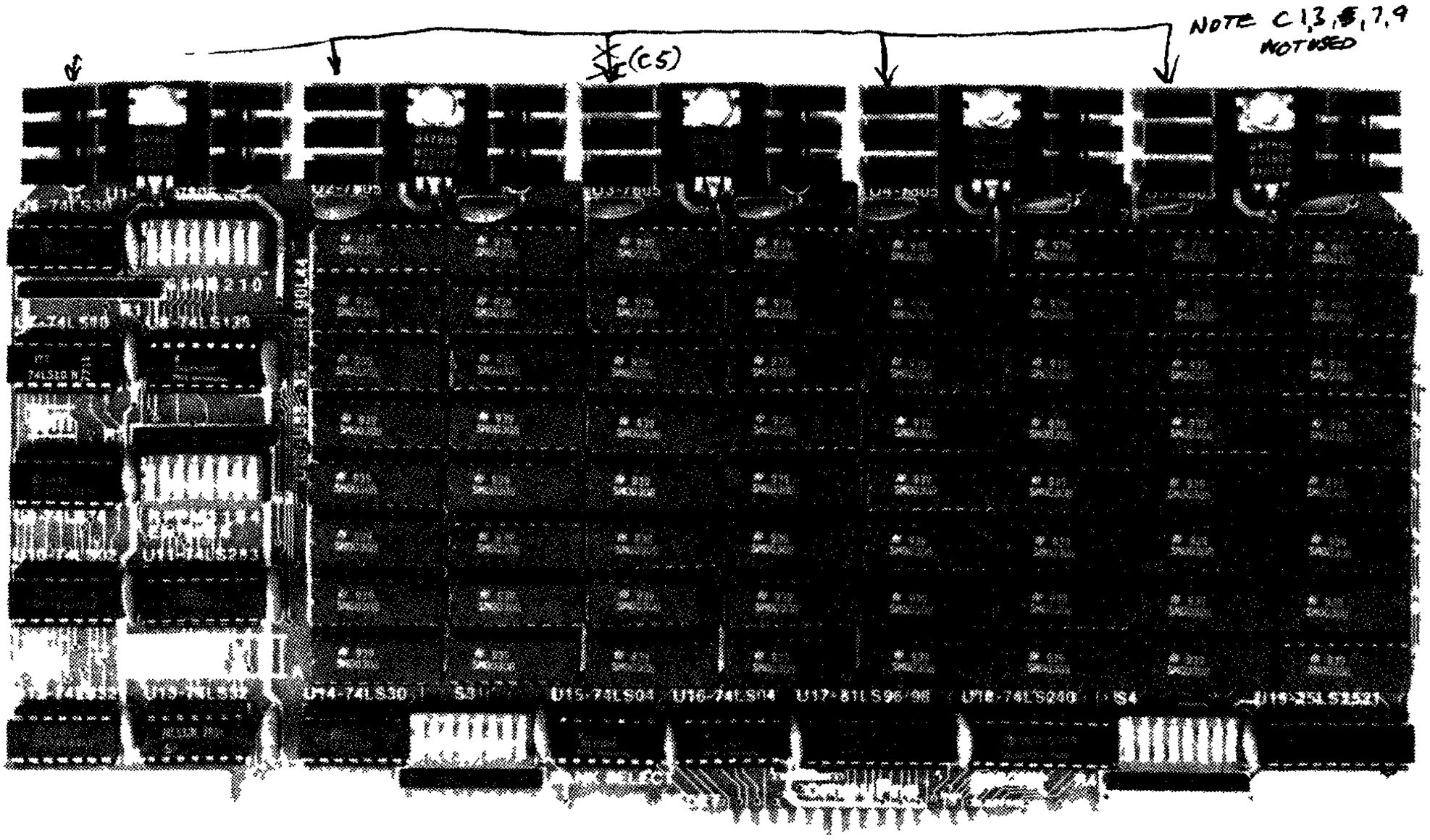
ECONORAM XIIIa™
USER'S MANUAL



IEEE • S-100

32K Bank Select Memory

using MM5257/90L44 • 5 MHz

147
mac

CompuPro™ from GODBOUT

2/80

ABOUT ECONORAM XIIIa

Congratulations on your decision to purchase **ECONORAM XIIIa**, a 32K x 8 memory board designed specifically for electrical and mechanical compatibility with the IEEE S-100 buss standard. The S-100 buss is the professional level choice for commercial, industrial, and scientific applications. This buss provides for ready expansion and modification as the state of the computing art improves. We believe this board, along with the rest of the S-100 portion of the **CompuPro** family, is one of the best memory boards available for that buss.

As amateur radio operators have contributed greatly to communication technology, so too the computer hobbyist has provided the microcomputer industry with many significant developments. In recognition of this fact, we also make this board available in "UNKIT" form for those who enjoy the challenge of assembling and testing a fine computer board.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing the **CompuPro ECONORAM XIIIa**...welcome to the club!

TECHNICAL OVERVIEW

This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this: static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered...there is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement. The individual memory ICs used on this board are grouped together to form a single 32K X 8 block of memory, addressable on any 4K boundary using the on-board Dip switch (no jumpers required). Additional features include a write protect switch; a write strobe selection switch which allows use of this memory in systems with or without a front panel (MWRITE strobe); allowance for use of the PHANTOM* line; thorough capacitor bypassing of supply lines to suppress transients; plus on-board regulation and heatsinking for reliably cool operation. All this and sockets for all ICs go onto a double sided, solder-masked printed circuit board with a complete component-layout legend.

POWER-ON ENABLE/DISABLE

When initial power is applied, and upon receiving a slave reset this board will be either ENABLED or DISABLED depending on the switch setting of S2 positions 1 & 2. To have the board enabled on power-on turn position 1 (PR) ON, and position 2 OFF. To disable board on power-on turn position 1 OFF and position 2 (RE) ON. Do not have both switches ON because the board will come up randomly enabled or disabled.

MEMORY ADDRESS ASSIGNMENT

This board is one large 32K block addressable on any 4K boundary. The dipswitch S2, positions 5-8 are used for selecting the starting address of the block. The starting address is set by "adding" the values shown below the switch when the position is ON. EXAMPLE: To start at 20K, turn ON positions 6 and 8 (16+4). To start at 52K, turn ON positions 5, 6, and 8 (32+16+4). With all switches (5-8) OFF the block will start at 0H.

DISABLING 4K BLOCKS

Because this board is sold partially populated also, the memory rows can be disabled. S1 is used to delete 4K Blocks from the memory space. This is particularly useful for disk operations which may require ROM at E900 or E000. By turning on the appropriate position on S1 the 4K Block associated with that position is removed from the system.

```
S1 POSITION   1 2 3 4 5 6 7 8   ON = DISABLED
BLOCK         7 6 5 4 3 2 1 0   OFF = ENABLED
```

The legend on the right side of the board (A0-A7) corresponds with the positions shown above. FOR EXAMPLE: To populate the board to only 16K, put the RAM chips in rows A0-A3 and turn on positons 5-8 of S1. This will disable rows A4-A7. S2 is still used to select the starting address of the block. Problem: To populate the board with 28K in the upper half of the memory map and leave a hole at E000 (for disk ROM). Set the address switches to start at 8000 (S2-7 ON, 5, 6, & 8 OFF), turn S1-2 ON to disable row A6, and put the RAM chips in all rows but A6. You can leave RAM chips in a disabled row with no problems if you choose to.

BANK SWITCHING THEORY

The purpose behind Bank Switching is to allow the Microcomputer user to access and write to more than the typical 64K that most Micros can directly address. To allow this, the **ECONORAM XIIIa** allows chunks of memory to be selectively enabled and disabled by outputting a data bit (user selectable) to a I/O Port (also user selectable). For example, if the bank is specified as port 40H, and the data bit is bit 0, by outputting a one in data bit 0 to port 40H, the bank will be enabled. Alternately, by outputting a zero to data bit 0 the bank will be disabled, and the board will not be electrically part of your system.
NOTE: Care should be taken to first disable an enabled bank before enabling the disabled bank to insure that no memory conflicts occur.

BANK PORT ADDRESSING

```
S4    1   2   3   4   5   6   7   8      Bank Selection

      A7  A6  A5  A4  A3  A2  A1  A0         ON=1
                                             OFF=0
```

EXAMPLE:

POSITIONS 1-8 ON = PORT FFH

POSITIONS 1-8 OFF = PORT 00H

POSITIONS 1-4 ON \
POSITIONS 5-8 OFF/ = PORT F0H

BANK ENABLE/DISABLE BIT ASSIGNMENT

Once the Bank Port has been selected, one data bit (or more) must be selected to enable or disable the bank. S3 is used to select these data bits as shown below:

```
          1   2   3   4   5   6   7   8     ON=  "1"
S3
          D7  D6  D5  D4  D3  D2  D1  D0    OFF= "0"
```

To disable the bank all 0's must be output to the data bits which have been turned ON. To enable the bank again, a "1" must be output to any of the data bits that have been turned ON. Note that it requires all 0's to be sent to the selected data bits to disable, but only one "1" bit will enable the bank again.

REFERENCE TABLE

SWITCH S1	1	2	3	4	5	6	7	8	ON=DISABLED
BLOCK	(7)	6	5	4	3	2	1	0	OFF=ENABLED

-S1 is used to selectively blank out individual 4K blocks within the main 32K block.

SWITCH S2	1	2	3	4	5	6	7	8	ON=ENABLED
LABEL	P R	R E	P H	M W	3 2	1 6	8	4	OFF=DISABL

-PR enabled causes the board to be enabled on power up or reset.
-RE enabled causes the board to be disabled on power up or reset.
-PH enabled puts the board under the control of the phantom line 67.
-MW enabled grounds the MWRITE line and causes the board to respond to PWR*.
-32, the decimal number that, when enabled, must be summed together to obtain the starting address for the board.
-16 See "32".
-8 See "32".
-4 See "32".

SWITCH S3	1	2	3	4	5	6	7	8	ON=RESPOND
LABEL	7	6	5	4	3	2	1	0	OFF=NORESP

Bank Data Select

-Positions 1 through 8 correspond to data bits 7 through 0 respectively. S3 is used to select which bit(s) the bank select responds to.

SWITCH S4	1	2	3	4	5	6	7	8	ON = "1"
LABEL	7	6	5	4	3	2	1	0	OFF = "0"

Bank Port Address Select

- Positions 1 through 8 correspond to address lines 7 through 0 respectively. S4 selects bank select port address and should reflect the binary equivalent of the desired address.

PHANTOM LINE

Switch S2-3 allows the **ECONORAM XIIIa** to be removed from memory space by a low level on PHANTOM* (Bus Pin 67). With S2-3 ON, memory will disappear when PHANTOM* is asserted. With S2-3 OFF, the board is unaffected by PHANTOM*. NOTE: Since some manufacturers are not conforming to the proposed IEEE S-100 buss standard, insure that your system is using the PHANTOM* line properly before using this feature on your **ECONORAM XIIa.**

MEMORY TESTING

If the memory board seems to be working properly, the MEMORY TESTING ROUTINE can be used to give the board a more thorough workout. It is rather slow; but will do the job well. It can be entered via editor/assembler or front panel switches.

The routine is set up to test 32K from 4000 hex to BFFF hex. This may be changed by entering a different starting address at "STRT" (3001-3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical information is stored and the routine enters a software "HALT" that is a "jump to here" at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure information:

3069*	"FDE"	= D,E pair...D is the fill character, and E is the test character
306B*	"FHL"	= H,L pair...the failure address
306D*	"FOUT"	= the data expected
306E*	"FIN"	= the data read

* address from MEMORY TESTING ROUTINE

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

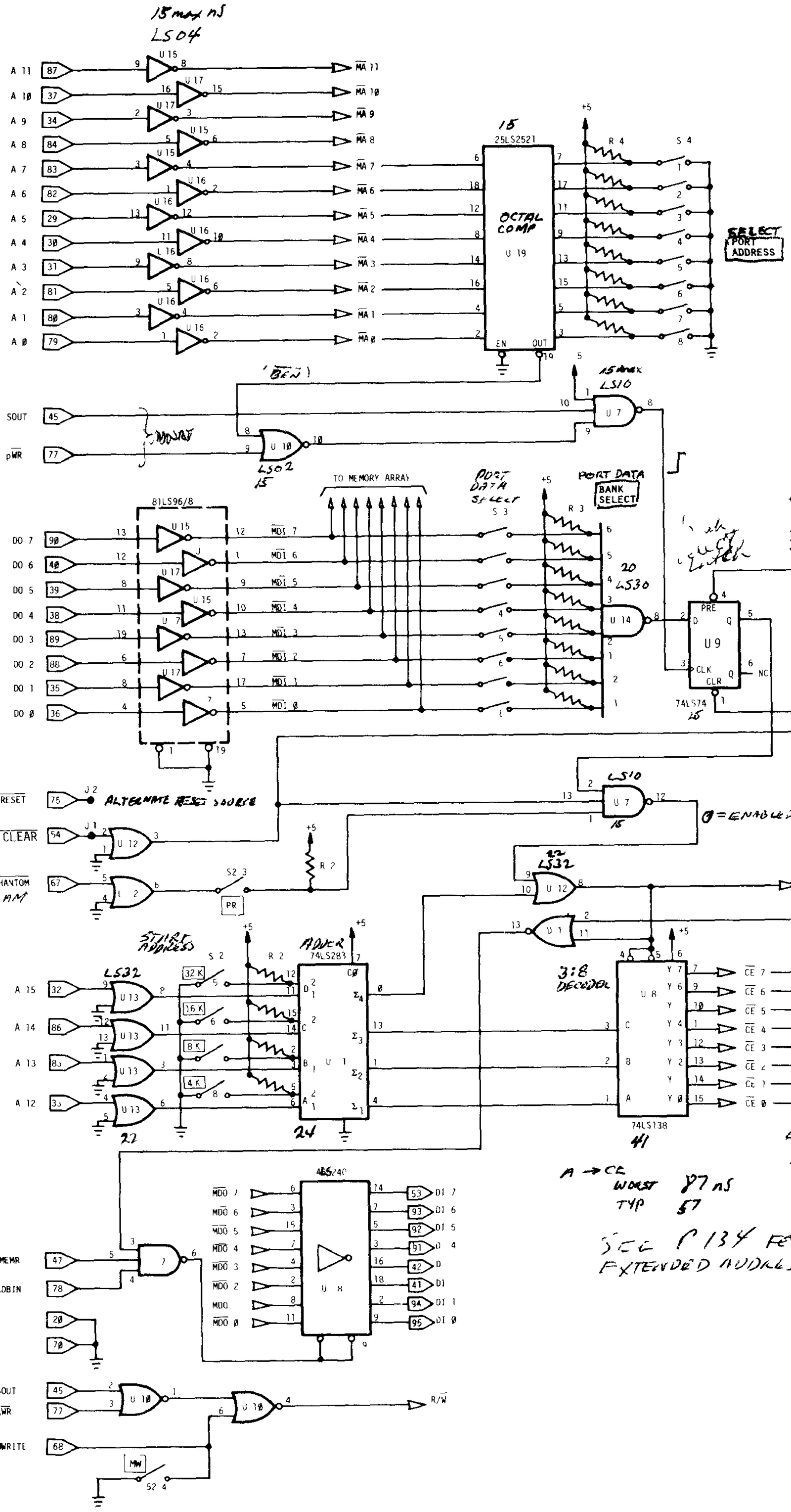
The difference betwen "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

NOTE THAT DATA IN AND DATA OUT ARE INVERTED

MEMORY TESTING ROUTINE

```
3000 21 00 40           0010 STRT LXI  H,40C0H
3003 3E A0              0020 END  MVI  A,0A0H
3005 32 6E 30           0030      STA  FIN
3008 3E 10              0040      MVI  A,10H
300A 84                 0050      ADD  H
300B 4F                 0060      MOV  C,A
300C 16 00              0070      MVI  D,0
300E 1E FF              0080      MVI  E,0FFH
3010 22 65 30           0090 DONE SHLD STAD
3013 AF                 0100      XRA  A
3014 47                 0110      MOV  B,A
3015 7B                 0120 SCND MOV  A,E
3016 5A                 0130      MOV  E,D
3017 57                 0140      MOV  D,A
3018 79                 0150      MOV  A,C
3019 2A 65 30           0160      LHLD STAD
301C 72                 0170 FILL MOV  M,D
301D 23                 0180      INX  H
301E BC                 0190      CMP  H
301F C2 1C 30           0200      JNZ  FILL
3022 2A 65 30           0210      LHLD STAD
3025 73                 0220 NEXT MOV  M,E
3026 7B                 0230      MOV  A,E
3027 BE                 0240      CMP  M
3028 C2 6F 30           0250      JNZ  FAIL
302B 79                 0260      MOV  A,C
302C 23                 0270      INX  H
302D 94                 0280      SUB  H
302E C2 4D 30           0290      JNZ  NDON
3031 B8                 0300      CMP  B
3032 44                 0310      MOV  B,H
3033 CA 15 30           0320      JZ   SCND
3036 3A 66 30           0325      LDA  STAD+1
3039 00                 0330 MARK NOP
303A 00                 0331      NOP
303B 00                 0332      NOP
303C 3A 6E 30           0340      LDA  FIN
303F B9                 0350      CMP  C
3040 CA 00 30           0360      JZ   STRT
3043 79                 0370      MOV  A,C
3044 67                 0380      MOV  H,A
3045 2E 00              0390      MVI  L,0
3047 C6 10              0400      ADI  10H
3049 4F                 0410      MOV  C,A
304A C3 10 30           0420      JMP   DONE
304D 22 67 30           0430 NDON SHLD NXAD
3050 7A                 0440 LOPB MOV  A,D
3051 BE                 0450 LOPA CMP  M
3052 C2 6F 30           0460      JNZ  FAIL
3055 2C                 0470      INR  L
3056 C2 51 30           0480      JNZ  LOPA
3059 79                 0490      MOV  A,C
305A 24                 0500      INR  H
305B BC                 0510      CMP  H
305C C2 50 30           0520      JNZ  LOPB
305F 2A 67 30           0530      LHLD NXAD
3062 C3 25 30           0540      JMP  NEXT
3065                    0550 STAD DS   2
3067                    0560 NXAD DS   2
3069                    0570 FDE  DS   2
306B                    0580 FHL  DS   2
306D                    0590 FOUT DS   1
306E                    0600 FIN  DS   1
306F 22 6B 30           0610 FAIL SHLD FHL
3072 32 6D 30           0620      STA  FOUT
3075 7E                 0630      MOV  A,M
3076 32 6E 30           0640      STA  FIN
3079 EB                 0650      XCHG
307A 22 69 30           0660      SHLD FDE
307D C3 7D 30           0670 SHLT JMP SHLT
3080                    0680 *
```



ECONORAM XIIIA
PART 1 OF 2

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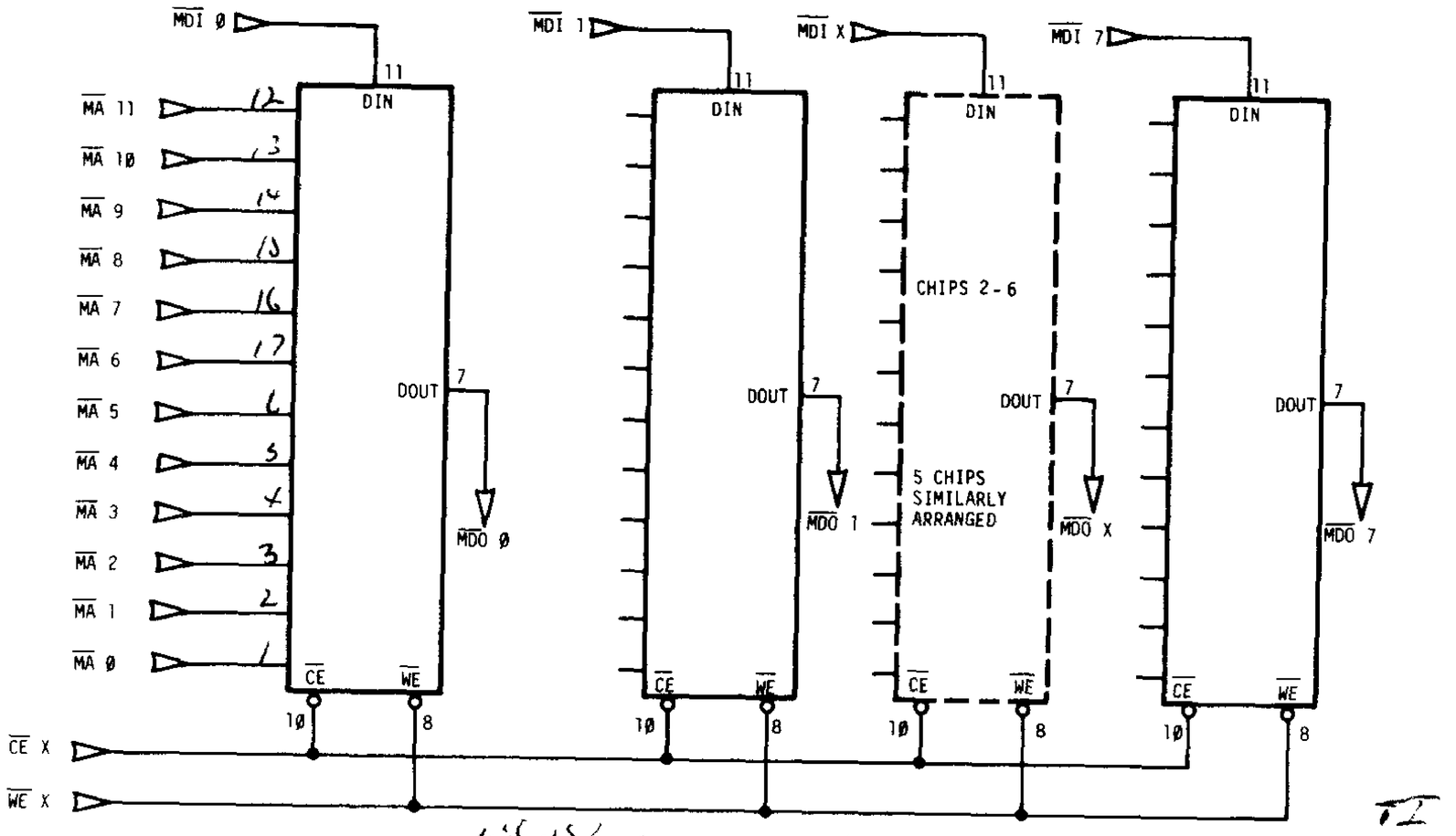
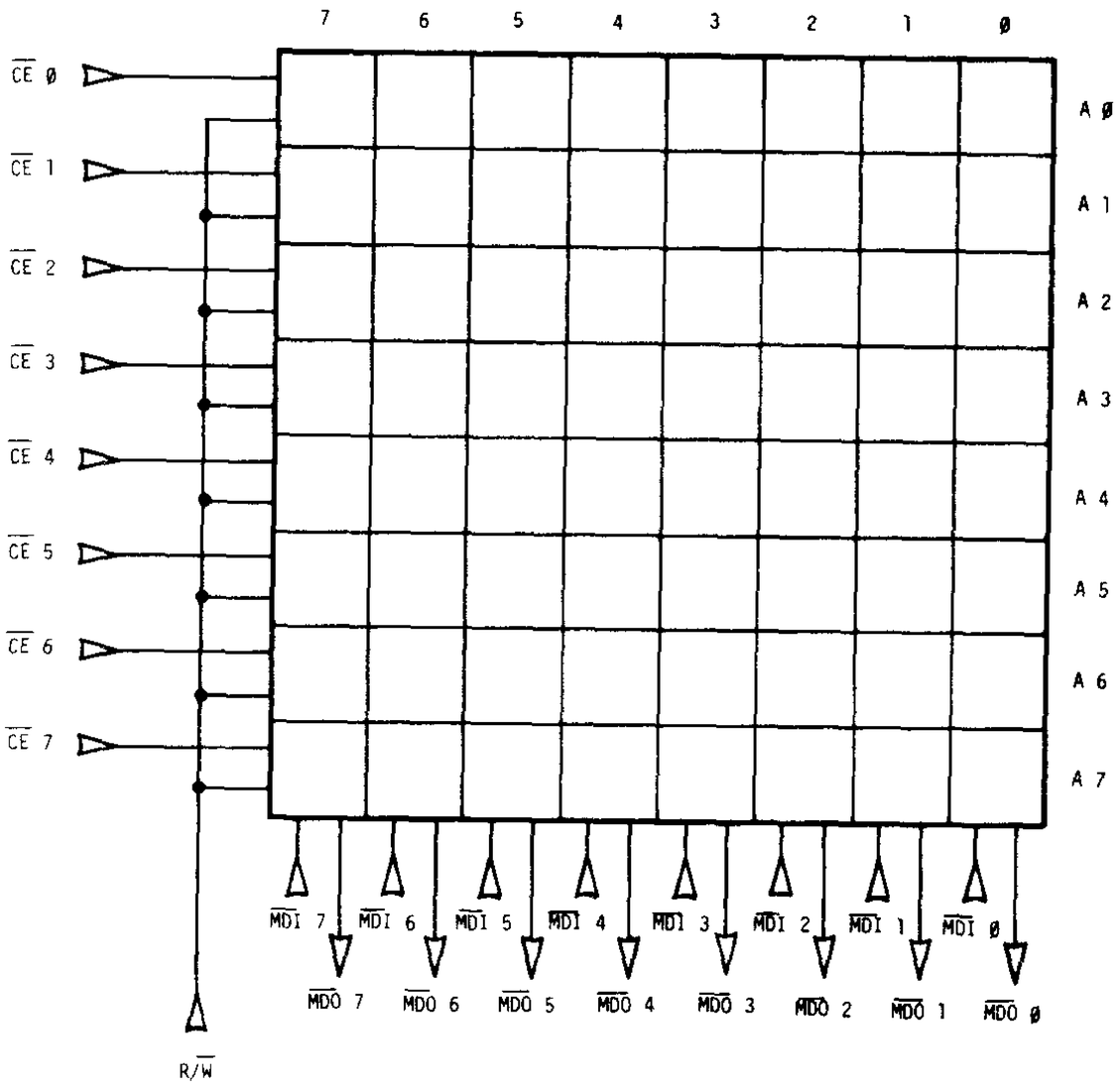


4K x 1

525 7/4044 (250 ns) Seq 2613 (200 ns) 4044 — 45 = 450 ns etc

MK 4104 (200 ns)

TI



~~TMS 9140 (200 ns)~~

NT IM 7141-3 300 ns

FMM 4801G 450 ns

2147 85 ns

2141-5 250 ns

IM 6504 300 ns CMOS

MKA 104 " "

ECONORAM XIIIA
PART 2 OF 2

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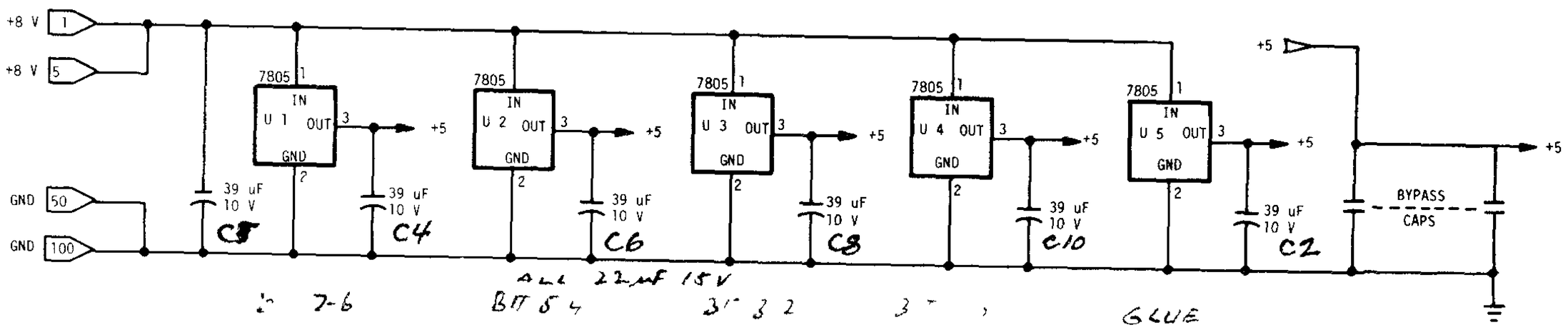
2147 990 mW ACTIVE x 8 = 7.92 W 1.58 A
165 mW STDBY " 396
11.88 W 2.38 A

(7805) 0.2 A)

2 x 2147 ACTIVE ~ 400 mA
+ 14 x " STDBY ~ 460 mA
860 mA/REG



ALL 22 mF 15 V

2-6 BIT 5 4 3 2 1 GLUE

3,5,7,9 NOT USED

CIRCUIT DESCRIPTION

The heart of **ECONORAM XIIIa** is the MM5257/90L44 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts. These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4K x 8 bits of information. Paralleling 8 of these rows together produces a total memory storage of 32K x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array). Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to write data into the memory, or read data from the memory. The schematics show the address circuitry along with the other **ECONORAM XIIIa** circuitry. Each memory IC requires 12 address lines (A0-A11) to access any one of the 4096 bits available in the IC. These address lines are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to react to the given address. This requires 4 more address lines (A12-A15) which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array). When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss). Data to be read on to the data buss from memory passes through 8 TRI-STATE inverting buss drivers; when data is not being read on to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state. This board can be used in a system with more than 64K of memory, and because of this there must be a method to disable the entire board and remove it from the system memory map. Since the CPU can only access 64K of memory with its 16 address lines, the method chosen was to use an I/O port to ENABLE/DISABLE the board. Switch S4 is used to select the I/O port for the board and when the correct port is decoded by U19, U9 latches in the data bit(s), if any bit selected by switch S3 is high, the board will be enabled at the address selected by switch S2 positions 5-8. Conversely if all bits selected by S3 are low upon receiving the output instruction the board will be disabled. The board can be set up to be turned ON or OFF with Preset or Power-on by using switch S2 positions 1 and 2.

U8 is used to select the row of memory enabled during read/write. Switch S1 and NAND gate U6 are used with U8 to select 4K chunks of memory to be removed anywhere on the board. The appropriate position of S1 will disable the corresponding block if it is turned on.

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC.

This board is guaranteed to operate at 4 MHz, or 5 MHz with an 8085 CPU over the full temperature range (0-70 C ambient) and draw less than 3.5 Amps. Also, our typical measured currents were less than 3.0 Amps, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

Parts List

☐ (1) ECONORAM XIIIa circuit board

INTEGRATED CIRCUITS (note the following parts may have letters suffixes and prefixes along with the key numbers given below.)

☐ (64)	MM5257N-3L	4Kx1 static RAM	
☐ (1)	74LS02	quad 2 input NOR	(U10)
☐ (2)	74LS04	hex inverter	(U15, U16)
☐ (1)	74LS10	triple 3 input NAND	(U7)
☐ (2)	74LS30	8 input NAND	(U6, U14)
☐ (2)	74LS32	quad 2 input OR	(U12, U13)
☐ (1)	74LS74	dual "D" flip flop	(U9)
☐ (1)	74LS138	decoder	(U8)
☐ (1)	74LS240	octal buss driver	(U18)
☐ (1)	74LS283	4 bit adder	(U11)
☐ (1)	25LS2521	octal comparator	(U19)
☐ (1)	81LS96/98	octal buss driver	(U19)
☐ (5)	7805	5 volt regulator	(U1-U5)

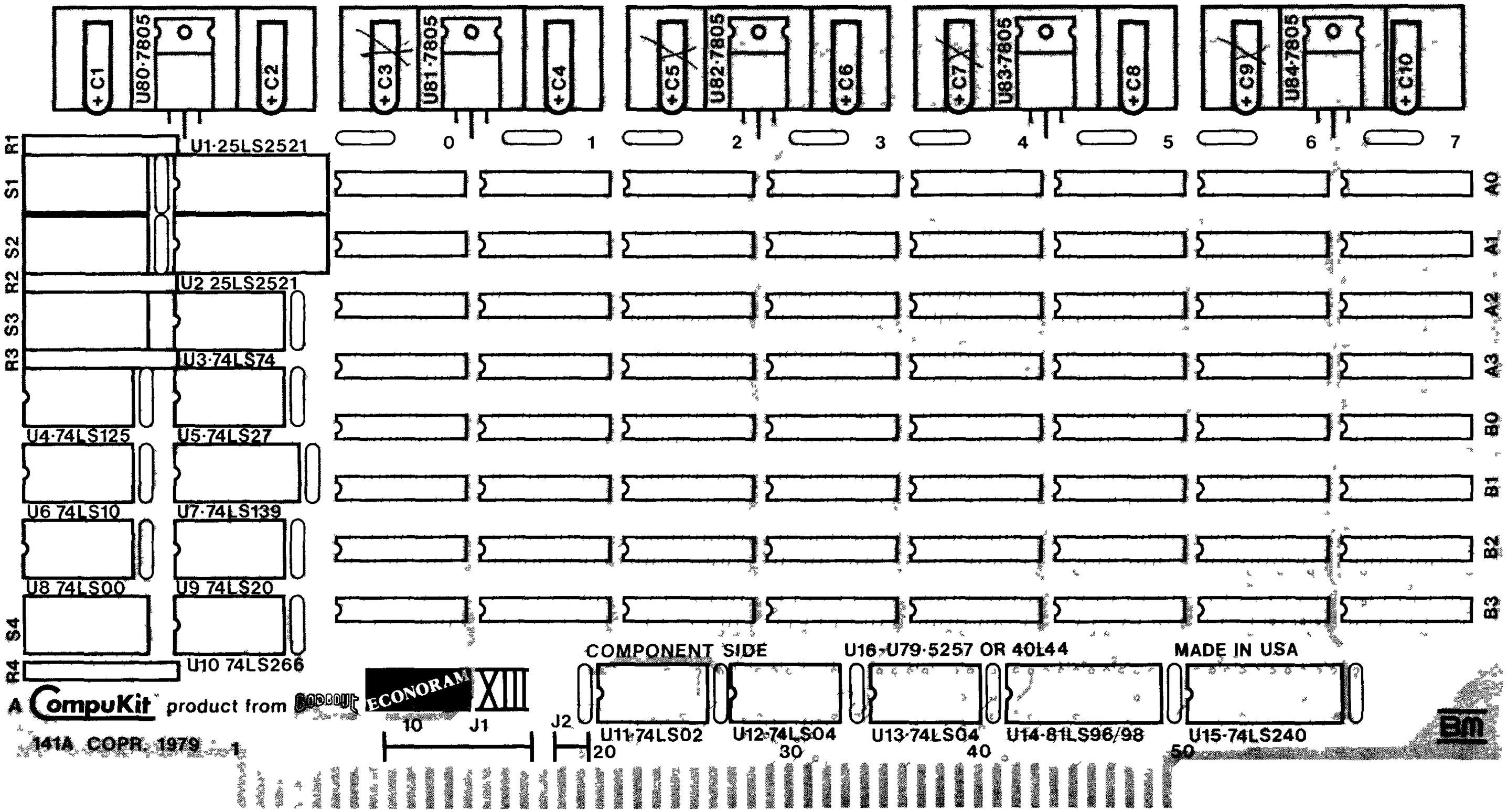
OTHER ELECTRONIC COMPONENTS

☐ (4)	SIP resistor packs	(R1-4)*
☐ (6)	39uf Tantalum Capacitors	(C1-C6)
☐ (20)	Ceramic bypass Capacitors *	C4.C6 C8-C10)

MECHANICAL COMPONENTS

☐ (78)	Low Profile Sockets *	
☐ (4)	Dip Switch, 8 position	(S1-S4)*
☐ (5)	TO-220 Heat Sinks	
☐ (5)	Sets 6-32 Hardware	

* supplied already soldered on the board



Component Layout XIII (rev A)

UP

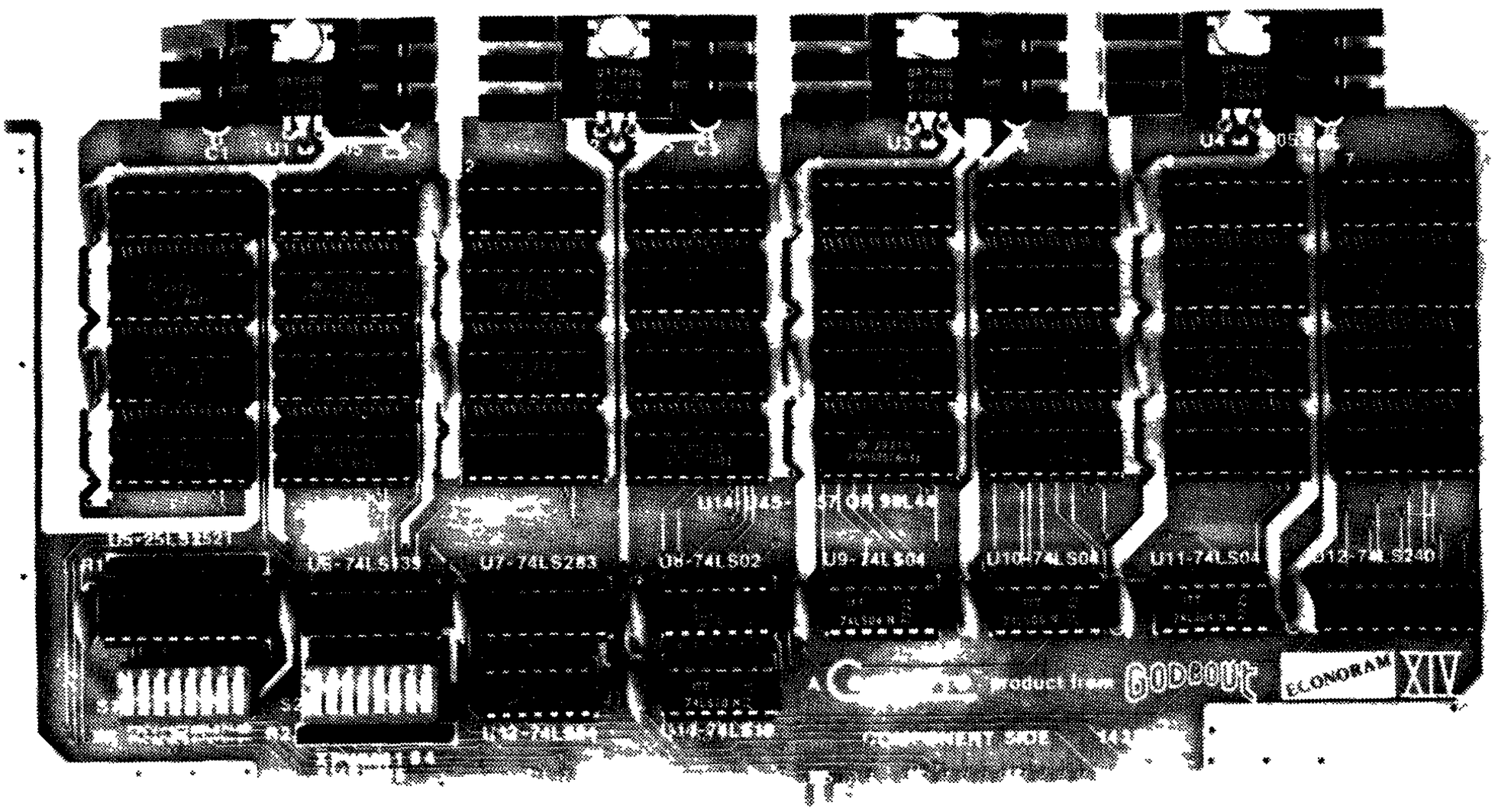
APPENDIX B

IEEE 696/S-100 Pin Assignments

01	+8 Volt	51	+8 Volt
02	+16 Volt	52	-16 Volt
03	XRDY	53	Ground
04	VI 0*	54	SLAVE CLR*
05	VI 1*	55	DMA 0*
06	VI 2*	56	DMA 1*
07	VI 3*	57	DMA 2*
08	VI 4*	58	sXTRQ*
09	VI 5*	59	A 19
10	VI 6*	60	SIXTN*
11	VI 7*	61	A 20
12	NMI*	62	A 21
13	PWRFAIL*	63	A 22
14	DMA 3*	64	A 23
15	A 18	65	NDEF
16	A 16	66	NDEF
17	A 17	67	PHANTOM*
18	SDSB*	68	MWRT
19	CDSB*	69	RFU
20	GROUND	70	GROUND
21	NDEF	71	RFU
22	ADSB*	72	RDY
23	DODSB*	73	INT*
24	PHI	74	HOLD*
25	pSTVAL*	75	RESET*
26	pHLDA	76	pSYNC
27	RFU	77	pWR*
28	RFU	78	pDBIN
29	A 5	79	A 0
30	A 4	80	A 1
31	A 3	81	A 2
32	A 15	82	A 6
33	A 12	83	A 7
34	A 9	84	A 8
35	DO 1	85	A 13
36	DO 0	86	A 14
37	A 10	87	A 11
38	DO 4	88	DO 2
39	DO 5	89	DO 3
40	DO 6	90	DO 7
41	DI 2	91	DI 4
42	DI 3	92	DI 5
43	DI 7	93	DI 6
44	sM1	94	DI 1
45	sOUT	95	DI 0
46	sINP	96	sINTA
47	sMEMR	97	sWO*
48	sHLTA	98	ERROR*
49	CLOCK	99	POC*
50	GROUND	100	GROUND

CONTINUED page 128

ECONORAM XIV™
USER'S MANUAL



IEEE • S-100
16K Memory 24 Bit Address
using MM5257/90L44 • 5MHz

143
mac

CompuPro™ from GODBOUT

2/80

ABOUT ECONORAM XIV

Congratulations on your decision to purchase **ECONORAM XIV**, a 16K x 8 memory board designed specifically for electrical and mechanical compatibility with the IEEE S-100 buss standard. The S-100 buss is the professional level choice for commercial, industrial, and scientific applications. This buss provides for ready expansion and modification as the state of the computing art improves. We believe this board, with the rest of the S-100 portion of the **CompuPro** family, is one of the best boards available for that buss.

As amateur radio operators have contributed greatly to communication technology, so too the computer hobbyist has provided the microcomputer industry with many significant developements. In recognition of this fact, we also make this professional quality board available in "**UNKIT**" form for those who enjoy the challange of assembling and testing a fine computer board.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing a **CompuPro Product** ...welcome to the club!

TECHNICAL OVERVIEW

This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this: static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered...there is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement. The individual memory ICs used on this board are grouped together to form a single 16K x 8 block of memory, addressable on any 4K boundary using the on-board dip switch (no jumpers required). Additional features include a write protect switch; a write strobe selection switch which allows use of this memory in systems with or without a front panel (MWRITE strobe); allowance for use of the PHANTOM* line; extended 24 bit addressing; thorough capacitor bypassing of supply lines to suppress transients; plus on-board regulation and heatsinking for reliably cool operation. All this and sockets for all ICs go onto a double sided, solder-masked printed circuit board with a complete component-layout legend.

BOARD ADDRESSING

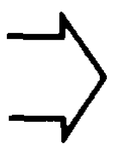
This board is configured as one 16K block. This block may be assigned to any area of memory beginning on a 4K boundary (0K, 4K, 36K etc.) with the only limitation being that it should not overlap any other memory in the system. The board is addressed by flipping S2 positions 5-8 ON or OFF to achieve the desired starting address. With all four switches OFF (S2(5-8)), the block will start at 0H or 0K. To start at 4K, flip switch S2-8 (marked "4" on the legend) ON. To start at 16K or 32K, flip switches S2-6 or S2-7 ON respectively (marked "16" and "32" respectively). To start at 44K, (32K + 8K + 4K) flip switches 32, 8 and 4 ON. In effect, add the switch numbers to give your starting address. Note: If the start of the 16K block is at 52K or above, the residual memory beyond 64K will appear starting at 0K.

EXTENDED ADDRESSING

The ECONORAM XIV has provisions on board for implementing the proposed IEEE S-100 extended address lines, A16-A23. If provided with this option, switch S2 position 1 should be turned OFF to enable the extended address decoder. Switch S1 should be set as shown below.

SWITCH POSITION	FUNCTION	
1	Address A23	
2	Address A22	
3	Address A21	ON = "0"
4	Address A20	
5	Address A19	
6	Address A18	OFF = "1"
7	Address A17	
8	Address A16	

EXAMPLE: To address your Econoram XIV at 370000H, flip positions 3, 4, 6, 7, & 8 OFF and 1, 2, & 5 ON.



NOTE: If not using the extended addressing feature of this board, remove U5 (25LS2521), turn all positions of S1 OFF and turn S2-1 ON.

MEMORY PROTECT SWITCH

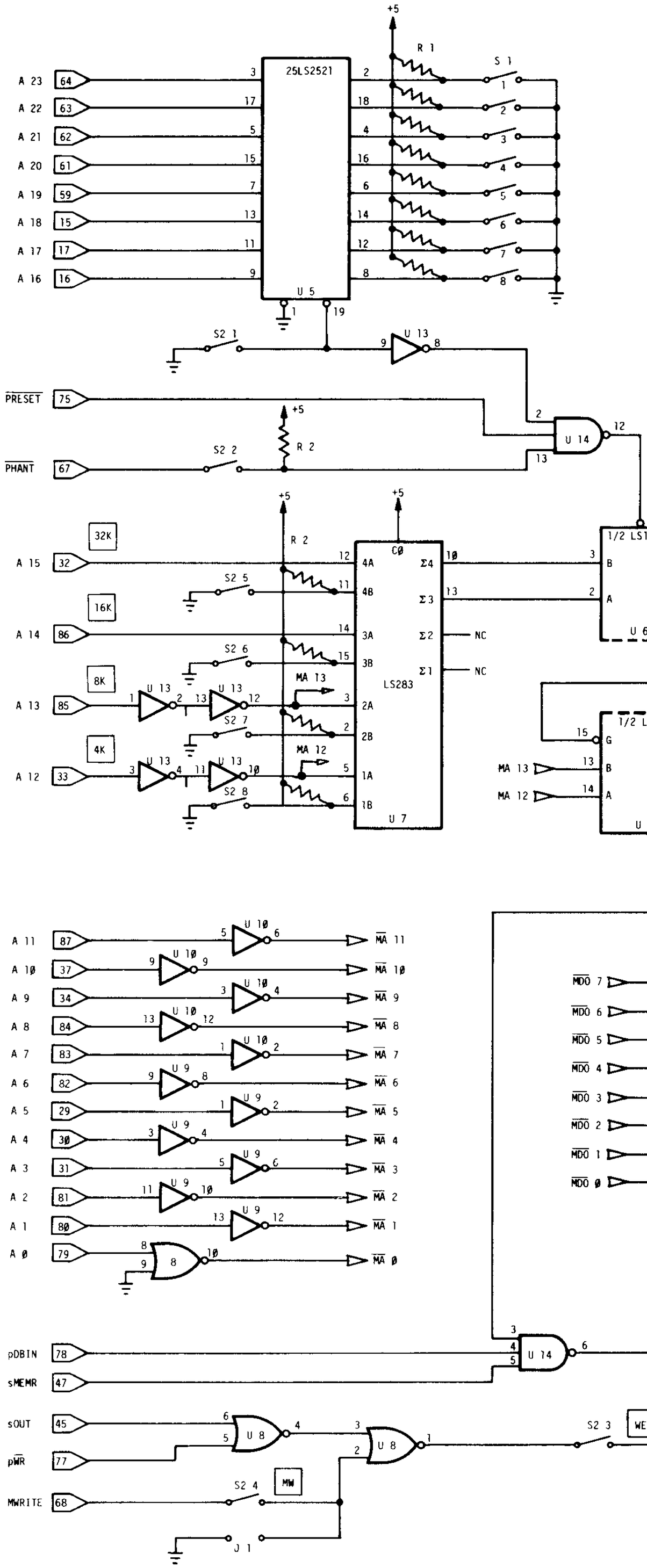
If you desire to "write protect" the contents of your **ECONORAM XIV** board; simply turn OFF switch WE (S2-3). With this switch OFF, the content of the RAM can be read, but not altered. For operation as a standard RAM board, leave switch S2-3 ON.

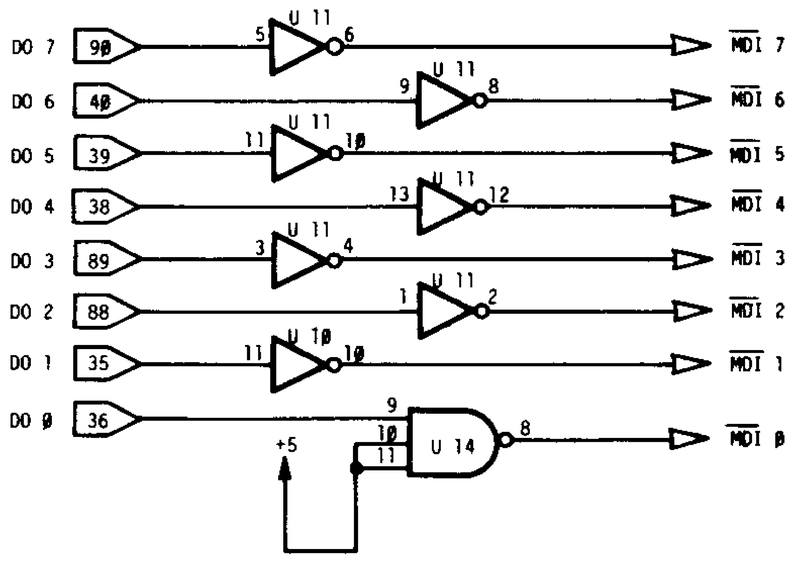
WRITE STROBE SELECTION

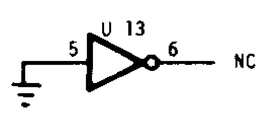
Switch S2 position 4 and jumper J1 allow the **ECONORAM XIV** to be operated in several different modes concerning the signal MWRITE (Pin 68). For systems that have MWRITE implemented, turn Switch MW (S2-4) ON. In systems where MWRITE is grounded, turn MW ON (S2-4), for systems that have a floating MWRITE line, turn MW ON and install a jumper at position J1 (in between U13 and U14).

PHANTOM LINE

Switch S2 position 2 allows the **ECONORAM XIV** to be removed from memory space by a low level on PHANTOM* (Bus Pin 67). With S2-2 ON, memory will disappear when PHANTOM* is asserted. With S2-2 OFF, the board is unaffected by PHANTOM*. NOTE: Since some manufacturers are not conforming to the proposed IEEE S-100 buss standard, insure that your system is using the PHANTOM* line properly before using this feature on your **ECONORAM XIV**.







ECONORAM XIV
PART 1 OF 2
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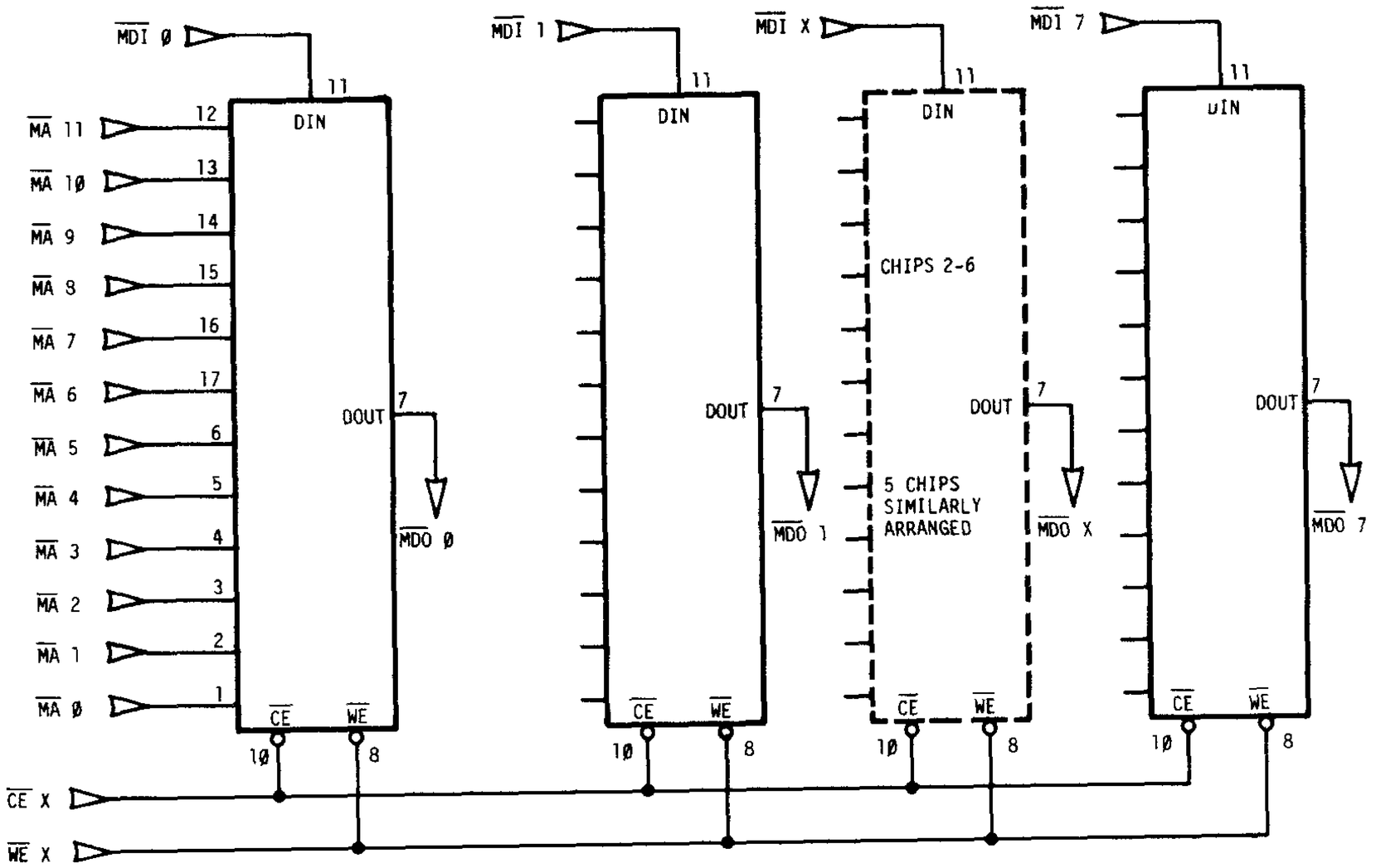

ECONORAM XIV
PART 2 OF 2
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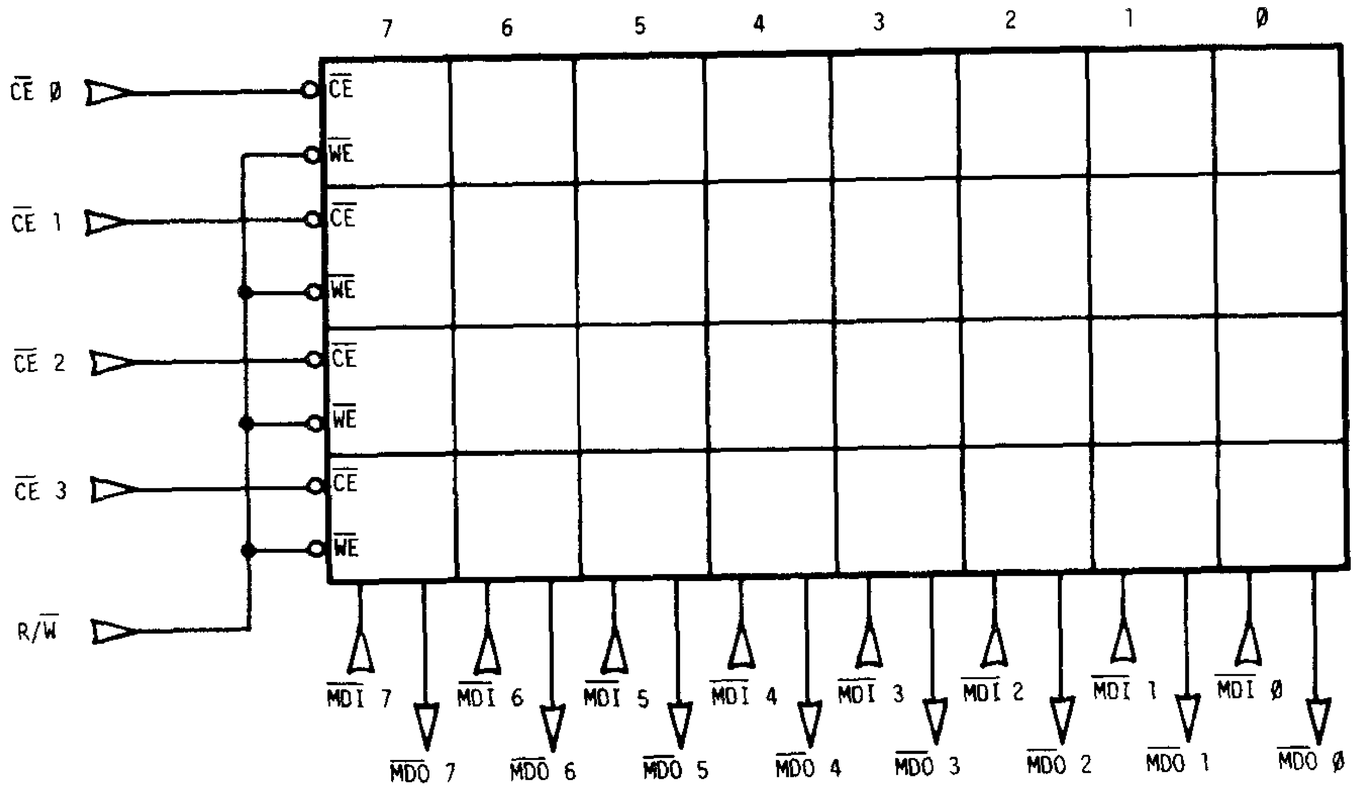
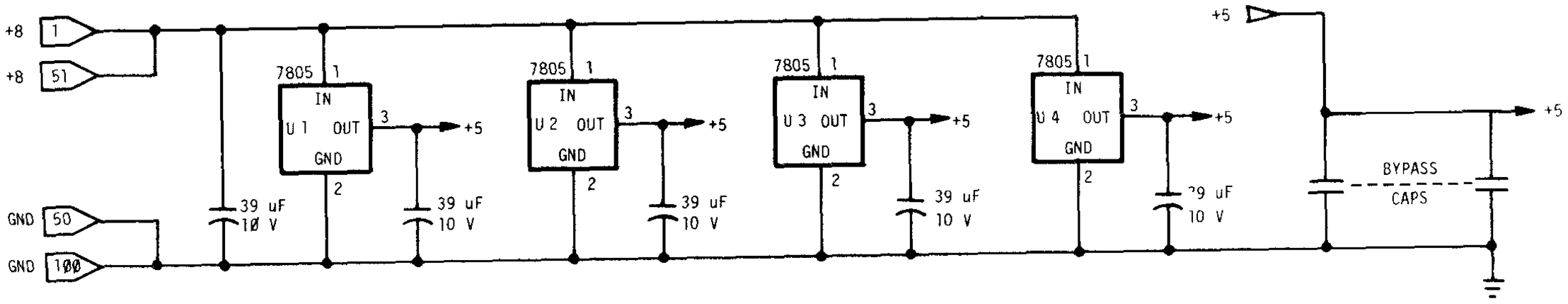




MEMORY TESTING

If the memory board seems to be working properly, the MEMORY TESTING ROUTINE can be used to give the board a more thorough workout. It is rather slow; but will do the job well. It can be entered via editor/assembler or front panel switches.

The routine is set up to test 16K from 4000 hex to 7FFF hex. This may be changed by entering a different starting address at "STRT" (3001-3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical informaton is stored and the routine enters a software "HALT" that is a "jump to here" at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure information:

3069*	"FDE"	= D,E pair...D is the fill character, and E is the test character
306B*	"FHL"	= H,L pair...the failure address
306D*	"FOUT"	= the data expected
306E*	"FIN"	= the data read

* address from MEMORY TESTING ROUTINE

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference betwen "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

MEMORY TESTING ROUTINE

```
3000 21 00 40          0010 STRT LXI  H,40C0H
3003 3E 80             0020 END  MVI  A,80H
3005 32 6E 30          0030      STA  FIN
3008 3E 10             0040      MVI  A,10H
300A 84                0050      ADD  H
300B 4F                0060      MOV  C,A
300C 16 00             0070      MVI  D,0
300E 1E FF             0080      MVI  E,0FFH
3010 22 65 30          0090 DONE SHLD STAD
3013 AF                0100      XRA  A
3014 47                0110      MOV  B,A
3015 7B                0120 SCND MOV  A,E
3016 5A                0130      MOV  E,D
3017 57                0140      MOV  D,A
3018 79                0150      MOV  A,C
3019 2A 65 30          0160      LHLD STAD
301C 72                0170 FILL MOV  M,D
301D 23                0180      INX  H
301E BC                0190      CMP  H
301F C2 1C 30          0200      JNZ  FILL
3022 2A 65 30          0210      LHLD STAD
3025 73                0220 NEXT MOV  M,E
3026 7B                0230      MOV  A,E
3027 BE                0240      CMP  M
3028 C2 6F 30          0250      JNZ  FAIL
302B 79                0260      MOV  A,C
302C 23                0270      INX  H
302D 94                0280      SUB  H
302E C2 4D 30          0290      JNZ  NDON
3031 B8                0300      CMP  B
3032 44                0310      MOV  B,H
3033 CA 15 30          0320      JZ   SCND
3036 3A 66 30          0325      LDA  STAD+1
3039 00                0330 MARK NOP
303A 00                0331      NOP
303B 00                0332      NOP
303C 3A 6E 30          0340      LDA  FIN
303F B9                0350      CMP  C
3040 CA 00 30          0360      JZ   STRT
3043 79                0370      MOV  A,C
3044 67                0380      MOV  H,A
3045 2E 00             0390      MVI  L,0
3047 C6 10             0400      ADI  10H
3049 4F                0410      MOV  C,A
304A C3 10 30          0420      JMP   DONE
304D 22 67 30          0430 NDON SHLD NXAD
3050 7A                0440 LOPB MOV  A,D
3051 BE                0450 LOPA CMP  M
3052 C2 6F 30          0460      JNZ  FAIL
3055 2C                0470      INR  L
3056 C2 51 30          0480      JNZ  LOPA
3059 79                0490      MOV  A,C
305A 24                0500      INR  H
305B BC                0510      CMP  H
305C C2 50 30          0520      JNZ  LOPB
305F 2A 67 30          0530      LHLD NXAD
3062 C3 25 30          0540      JMP  NEXT
3065                   0550 STAD DS   2
3067                   0560 NXAD DS   2
3069                   0570 FDE  DS   2
306B                   0580 FHL  DS   2
306D                   0590 FOUT DS   1
306E                   0600 FIN  DS   1
306F 22 6B 30          0610 FAIL SHLD FHL
3072 32 6D 30          0620      STA  FOUT
3075 7E                0630      MOV  A,M
3076 32 6E 30          0640      STA  FIN
3079 EB                0650      XCHG
307A 22 69 30          0660      SHLD FDE
307D C3 7D 30          0670 SHLT JMP SHLT
3080                   0680 *
```

CIRCUIT DESCRIPTION

The heart of **ECONORAM XIV** is the MM5257/90L44 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts. These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4K x 8 bits of information. Paralleling 4 of these rows together produces a total memory storage of 16K x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array). Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to write data into the memory, or read data from the memory. The schematics show the address circuitry along with the other **ECONORAM XIV** circuitry. Each memory IC requires 12 address lines (A0-A11) to access any one of the 4096 bits available in the IC. These address lines are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to react to the given address. This requires 4 more address lines (A12-A15) which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array). When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss). Data to be read to the data buss from memory passes through 8 TRI-STATE inverting buss drivers; when data is not being read to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state.

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC.

This board is guaranteed to operate at 4 MHz, or 5 MHz with an 8085 CPU over the full temperature range (0-70 C ambient) and draw less than 2.0 Amps. Also, our typical measured currents were less than 1.6 Amps, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

Parts List

☐ (1) Econoram XIV circuit board.

INTEGRATED CIRCUITS (note: the following parts may have letter suffixes and prefixes along with the key numbers given below.)

☐	(32)	MM5257-3L	4Kx1 static RAM	(U14-U45)
☐	(1)	74LS02	Quad 2 input NOR gate	(U8)
☐	(4)	74LS04	Hex inverters	(U9,10,11,13)
☐	(1)	74LS10	Triple 3 input NAND gate	(U14)
☐	(1)	74LS240	Octal TRI-STATE inverters	(U12)
☐	(1)	74LS283	4 bit adder	(U7)
☐	(1)	74LS139	Dual 1 of 4 decoder	(U6)
☐	(4)	7805	Positive 5V regulators	(U1-U4)

OTHER ELECTRONIC COMPONENTS

☐	(5)	39uF tantalum capacitors	(C1-C6)
☐	(16)	Ceramic disk bypass capacitors *	
☐	(1)	2.7K SIP *	

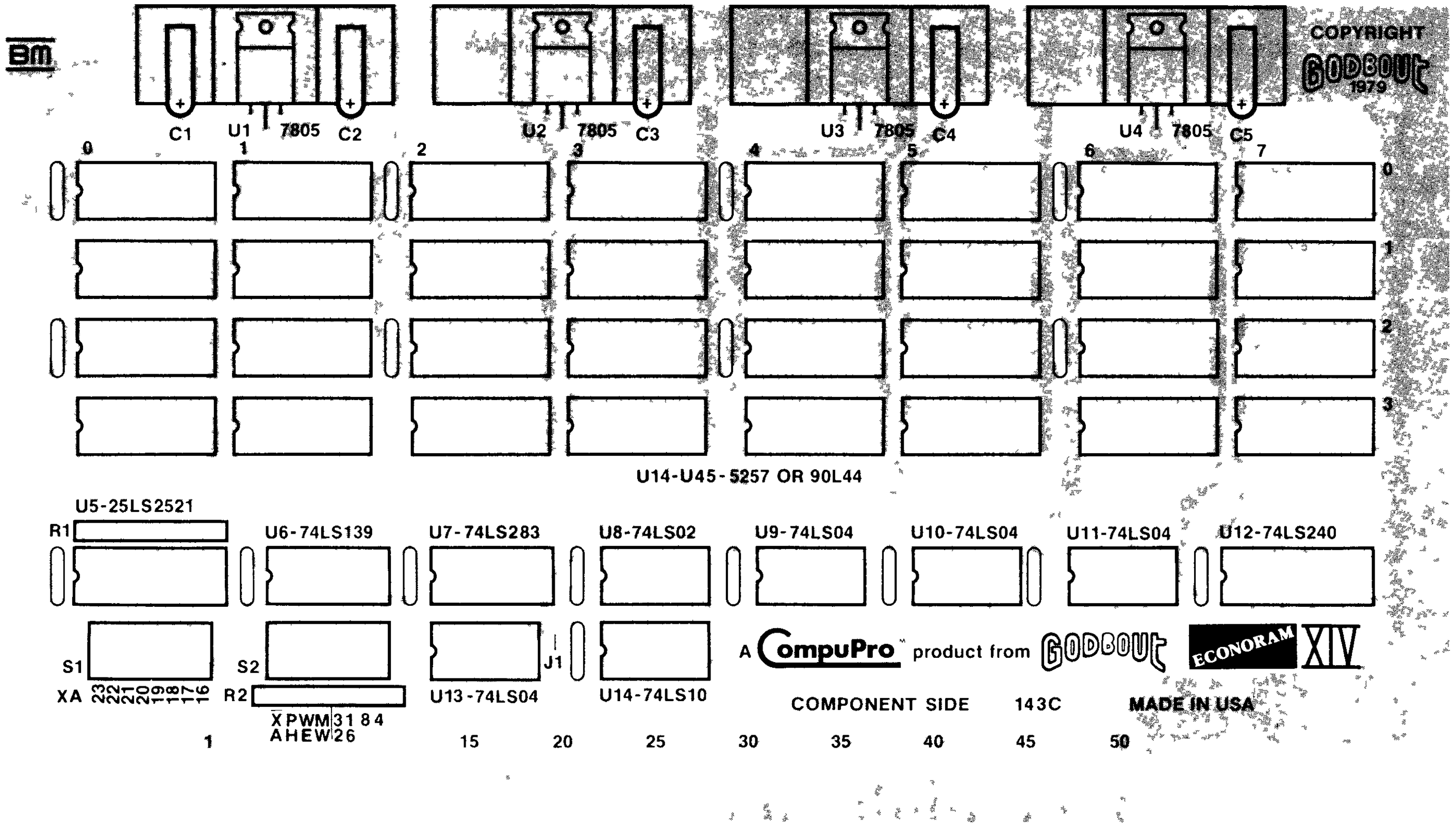
MECHANICAL COMPONENTS

☐	(41)	Low profile sockets *	
☐	(1)	8 pole dip switch	(S1)
☐	(4)	Heat sinks for regulator ICs	
☐	(4)	6-32 bolts	
☐	(4)	6-32 lockwashers	
☐	(4)	6-32 nuts	
☐	(1)	Instruction booklet	

*Supplied already soldered to board

OPTIONAL PARTS FOR EXTENDED ADDRESSING

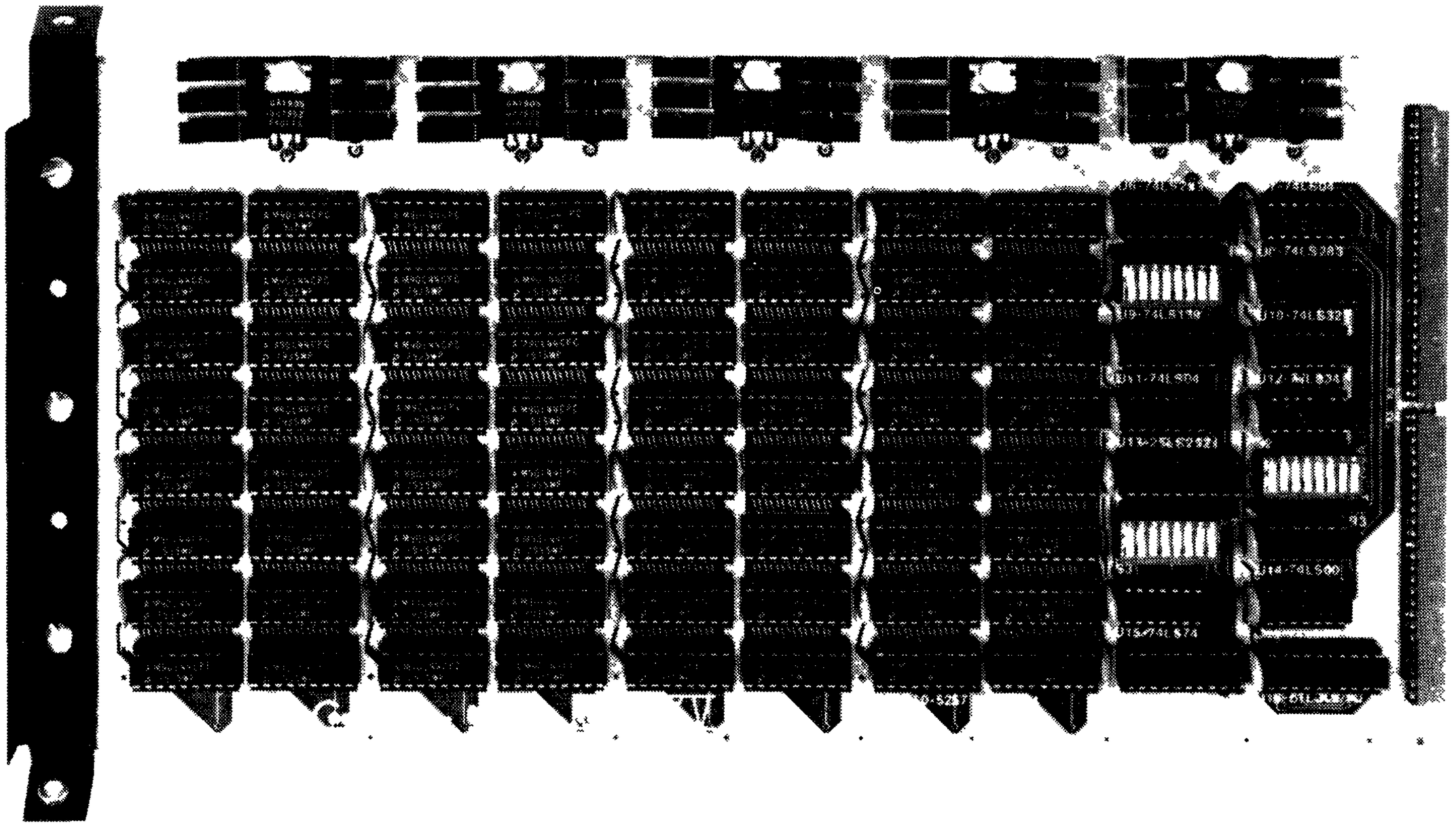
☐	(1)	25LS2521 Octal Comparator	(U5)
☐	(1)	DIP switch	(S1)
☐	(1)	2.7K SIP	(R1)
☐	(1)	Disc Cap	



Component Layout

up

ECONORAM XV™
USER'S MANUAL



32K Bank Select • H8
using MM5257/90L44 • 5MHz

CompuPro™ from GODBOUT

2/80

ABOUT ECONORAM XV

Congratulations on your purchase of the **ECONORAM XV**, a 32K x 8 memory board designed for electrical and mechanical compatability with the Heathkit H-8 computer. This board features two independent 16K blocks, easy switch assigment of blocks to desired memory address locations and switch selectable enables for operation in either bank select or standard mode. It is fully buffered to prevent loading the buss, and has write protect switches for each block.

As amateur radio operators have contributed greatly to communication technology, so too the computer hobbyist has provided the microcomputer industry with many significant developements. In recognition of this fact, we also make this professional quality board available in "**UNKIT**" form for those who enjoy the challange of assembling and testing a fine computer board.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing a **CompuPro Product** ...welcome to the club!

TECHNICAL OVERVIEW

The individual memory chips used on this board are grouped together to form two 16k blocks of memory. Each of these 16K blocks is individually addressable on any 4K boundary. The starting addresses of each block are set by dipswitches on the board. In addition, one or both of the blocks may be operated in page select mode and essentially located at any of the 256 page locations. Write protect switches are also included for each block. Extra heavy duty power supply traces, generous bypassing of supply lines, sockets for all integrated circuits, careful layout and double sided solder-mask printed circuit board with complete component and switch legends make this a versatile memory board which will give exceptionally long and trouble free service.

STATIC MEMORIES

This board incorporates proven static memory technology using industrial design techniques and generous safety factors to ensure extremely reliable operation. Of the currently popular approaches to memory design, static and dynamic, static memories have the overwhelming choice in applications where speed, simplicity, ease of use and reliability must be considered. In order to retain data, dynamic memory must continually be refreshed. This board due to its static design will retain data as long as power is applied. This is of particular interest to those who will be using this board where DMA operations are involved. The static memory requires no refresh, and thefore there is never a conflict between the DMA device and the CPU attempting to refresh memory.

MEMORY ADDRESS ASSIGNMENT

This board is configured as two 16K blocks. Each 16K block may be assigned to any area of memory beginning on 4K boundary (0K, 4K, 32K, etc.). The only limitation is that the assigned locations should not overlap each other or any other memory in your system.

BLOCK ENABLE SWITCHES/ BANK SELECT FEATURES

Each of the two 16K blocks may be used in either the standard or bank select mode. Block A, for example, is enabled in the standard mode by switching dipswitch S3-5 ON and S3-6 OFF. Block A now resides at the address selected by the user with dipswitch S1 positions 1-4. This memory will always be part of the system memory map in this mode. To use block A in the bank mode turn S3-5 OFF and S3-6 ON. The block is now enabled by outputting a 1 in data bit D0 to the port address corresponding to that selected at dipswitch 2, outputting a 0 to data bit D0 will disable the block. Block B is enabld in the normal mode (always in the memory map) by turning S3-7 ON and S3-8 OFF. To use block B in bank mode, turn S3-8 ON and S3-7 OFF. This simple scheme enables the user to manage and utilize a theoretical maximum of 16 megabytes of memory by assigning blocks of memory to various banks and turning them OFF and ON under software control as required. Memory management may now be employed easily and efficiently. Either block may be used in either its standard mode or its bank select mode. The user should not leave both switches ON. The I/O port address for bank select is selected by the user with S2, the user may locate the bank select port for this board at any of the 256 I/O port locations.

BLOCK DISABLE SWITCHES

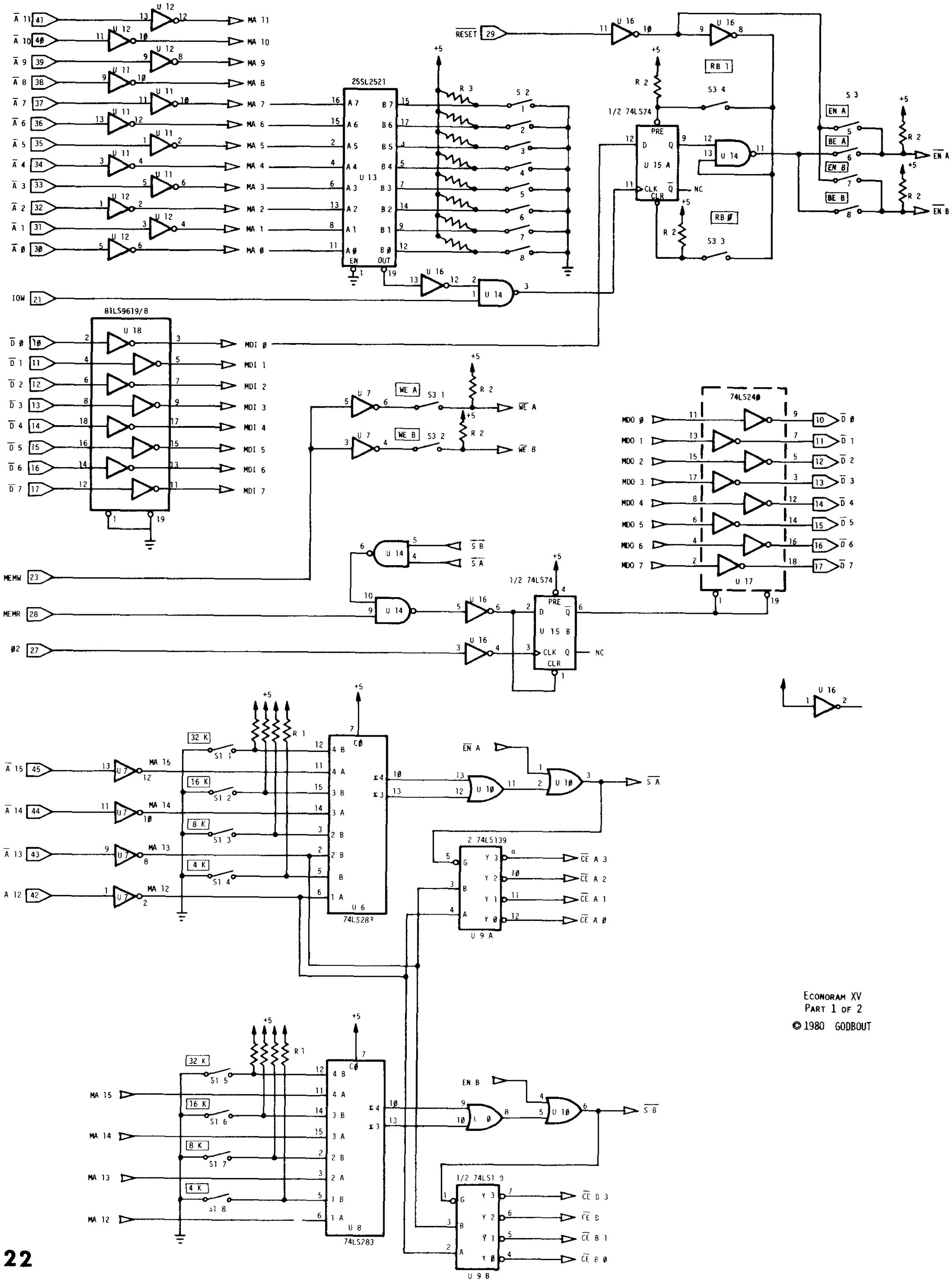
Switch S3 positions 6 through 8 provide 16K block disable functions as well as mode select functions. To disable the 16K block of RAM controlled by Block A, S3-5 and S3-6 should both be turned OFF. To disable Block B, S3-7 and S3-8 should both be turned OFF. Once a block is disabled, it is totally removed from the bus. It can neither be read from nor written to, and it will not conflict with off-board memory sharing the same address space.

WRITE PROTECT ENABLE SWITCHES

Switch S3 positions 1 and 2 provide a write protect feature. That is, in normal operations, both of these switches are ON, and they enable the write signal to blocks A and B of the board. In certain operations you may want to use a portion of this RAM as if it were read only memory (ROM). That is, memory you can read from but not write into once you have initialized it. Switch S3-1 is turned OFF to disable the memory write for block A. S3-2 is turned OFF to disable the memory write for block B. Whenever you want to write into these blocks, the respective switches should be in the ON position.

POWER ON STATUS

When running in Bank Select mode, the **ECONORAM XV** may be set to come up enabled or disabled at power-on or reset. This allows bank select systems to have a known memory map at power-on, before there has been time for the CPU to establish through appropriate I/O instructions which boards are to be enabled or disabled. S3 positions 3 and 4 determine power-on status. Setting S3-3 ON and S3-4 OFF will cause the board to be DISABLED at power-on. Setting S3-3 OFF and S3-4 ON will cause the board to be ENABLED at power-on.


Econoram XV
Part 1 of 2
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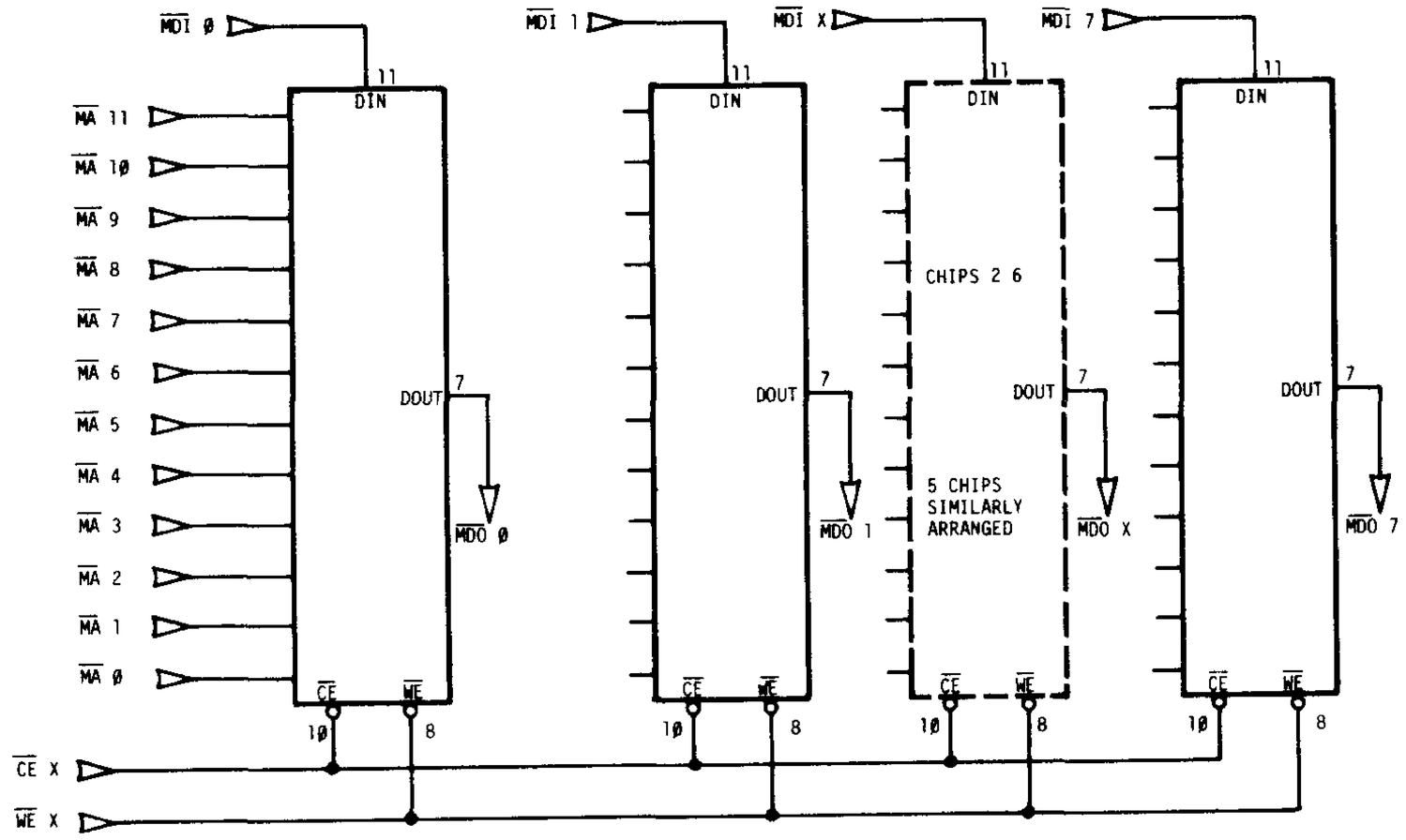

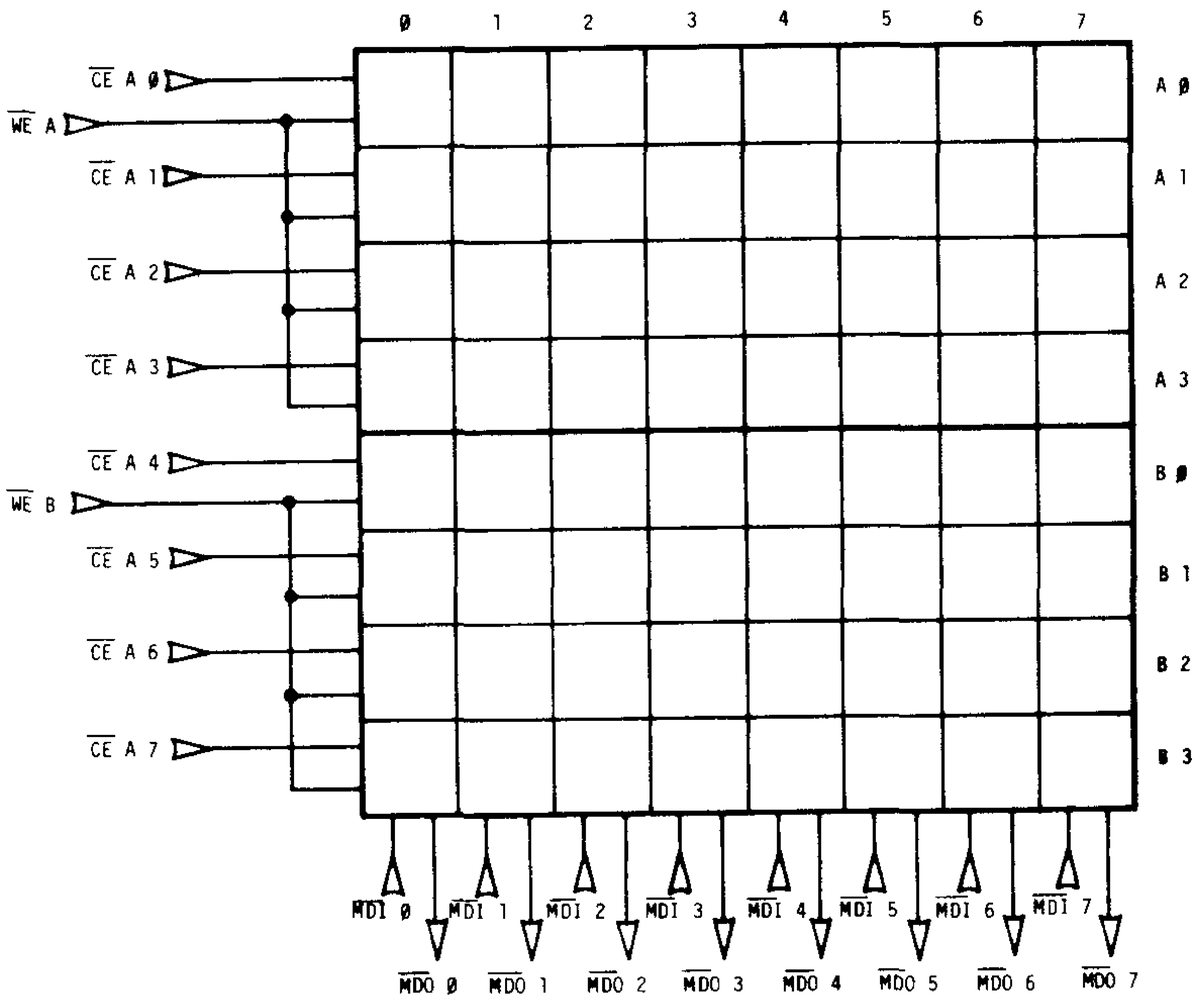

ECONORAM XV
PART 2 OF 2

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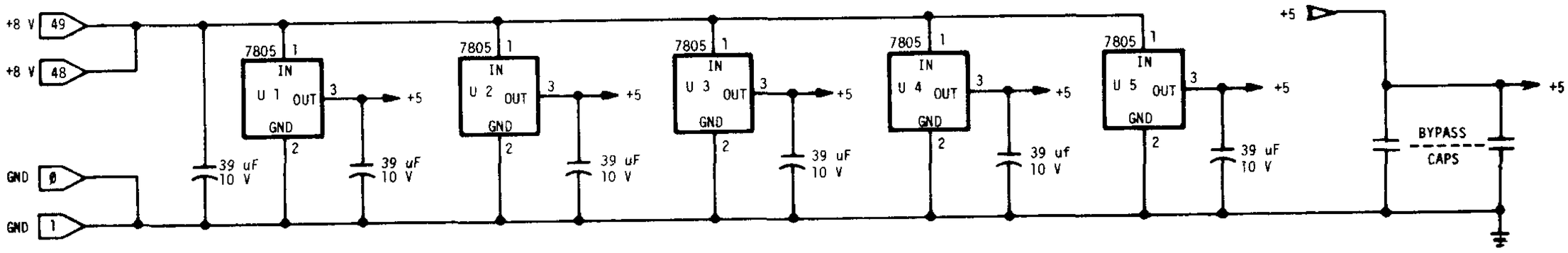


MEMORY TESTING

If the memory board seems to be working properly, the memory testing routine supplied with your Heath H8 can be used to give the board a thorough workout. It can be entered via editor/assembler or front panel.

The MEMORY TESTING ROUTINE included is set up to test 32K from 4000 hex to BFFF hex. This may be changed by entering a different starting address at "STRT" (3001-3002) and/or a different end address at "FND" (3004 - high order byte only). This program may be modified to run on the H8 if desired.

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical informaton is stored and the routine enters a software "HALT" that is a "jump to here" at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or dump routines to display the following stored failure information:

3069*	"FDE"	= D,E pair...D is the fill character, and E is the test character
306B*	"FHL"	= H,L pair...the failure address
306D*	"FOUT"	= the data expected
306E*	"FIN"	= the data read

* address from MEMORY TESTING ROUTINE

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference betwen "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

MEMORY TESTING ROUTINE

```
3000 21 00 40            0010 STRT LXI  H,4000H
3003 3E A0               0020 END  MVI  A,0A0H
3005 32 6E 30            0030      STA  FIN
3008 3E 10               0040      MVI  A,10H
300A 84                  0050      ADD  H
300B 4F                  0060      MOV  C,A
300C 16 00               0070      MVI  D,0
300E 1E FF               0080      MVI  E,0FFH
3010 22 65 30            0090 DONE SHLD STAD
3013 AF                  0100      XRA  A
3014 47                  0110      MOV  B,A
3015 7B                  0120 SCND MOV  A,E
3016 5A                  0130      MOV  E,D
3017 57                  0140      MOV  D,A
3018 79                  0150      MOV  A,C
3019 2A 65 30            0160      LHLD STAD
301C 72                  0170 FILL MOV  M,D
301D 23                  0180      INX  H
301E BC                  0190      CMP  H
301F C2 1C 30            0200      JNZ  FILL
3022 2A 65 30            0210      LHLD STAD
3025 73                  0220 NEXT MOV  M,E
3026 7B                  0230      MOV  A,E
3027 BE                  0240      CMP  M
3028 C2 6F 30            0250      JNZ  FAIL
302B 79                  0260      MOV  A,C
302C 23                  0270      INX  H
302D 94                  0280      SUB  H
302E C2 4D 30            0290      JNZ  NDON
3031 B8                  0300      CMP  B
3032 44                  0310      MOV  B,H
3033 CA 15 30            0320      JZ   SCND
3036 3A 66 30            0325      LDA  STAD+1
3039 00                  0330 MARK NOP
303A 00                  0331      NOP
303B 00                  0332      NOP
303C 3A 6E 30            0340      LDA  FIN
303F B9                  0350      CMP  C
3040 CA 00 30            0360      JZ   STRT
3043 79                  0370      MOV  A,C
3044 67                  0380      MOV  H,A
3045 2E 00               0390      MVI  L,0
3047 C6 10               0400      ADI  10H
3049 4F                  0410      MOV  C,A
304A C3 10 30            0420      JMP   DONE
304D 22 67 30            0430 NDON SHLD NXAD
3050 7A                  0440 LOPB MOV  A,D
3051 BE                  0450 LOPA CMP  M
3052 C2 6F 30            0460      JNZ  FAIL
3055 2C                  0470      INR  L
3056 C2 51 30            0480      JNZ  LOPA
3059 79                  0490      MOV  A,C
305A 24                  0500      INR  H
305B BC                  0510      CMP  H
305C C2 50 30            0520      JNZ  LOPB
305F 2A 67 30            0530      LHLD NXAD
3062 C3 25 30            0540      JMP  NEXT
3065                     0550 STAD DS   2
3067                     0560 NXAD DS   2
3069                     0570 FDE  DS   2
306B                     0580 FHL  DS   2
306D                     0590 FOUT DS   1
306E                     0600 FIN  DS   1
306F 22 6B 30            0610 FAIL SHLD FHL
3072 32 6D 30            0620      STA  FOUT
3075 7E                  0630      MOV  A,M
3076 32 6E 30            0640      STA  FIN
3079 EB                  0650      XCHG
307A 22 69 30            0660      SHLD FDE
307D C3 7D 30            0670 SHLT JMP SHLT
3080                     0680 *
```

ERATTA FOR THE ECONORAM XV

PARTS LIST
ADD THE FOLLOWING:
[] (1) 81LS96/98 OCTAL BUS DRIVER (U18)
CHANGE THE FOLLOWING:
[] (1) 25LS2521 OCTAL COMPARATOR (U13)

SUBSTITUTE THE FOLLOWING:

MEMORY ADDRESS ASSIGNMENT

This board is configured as two 16K blocks. Each 16K block may be assigned to any area of memory on any 4K boundary (0K, 4K, 8K, 12K, 32K, etc.). The only limitation is that the blocks should not overlap. Block A is set by switches S1-1 thru S1-4, and block B is set with switches S1-5 thru S1-8. Each switch is assigned a value which when added yields the block starting address as shown below.

SWITCH S1 POSITION AND VALUE

1	2	3	4	5	6	7	8
32K	16K	8K	4K	32K	16K	8K	4K

EXAMPLE: To give block A a starting address of 0K, positions 1 thru 4 would be OFF. To start at 4K, positions 1 thru 3 would be OFF and position 4 would be ON. To start at 12K, positions 1 and 2 would be OFF and positions 3 and 4 would be on (4K + 8K = 12K). To start at 48K, positions 1 and 2 would be ON and positions 3 and 4 would be OFF (32K + 16K = 48K). The same applies for the B block as well as the A block.

NOTE: If a block has the starting address of 52K or above, the one or more 4K blocks that would exist above 377,377 octal (maximum memory address), will wrap around and start at 0K. If you plan to wrap around the memory or start the memory at lower than 8K, make sure that you disable the front panel ROM in the first 8K of memory.

BLOCK DISABLE SWITCHES

To disable block A, flip switches S3-5 and S3-6 to the OFF position. To disable block B, flip switches S3-7 and S3-8 to the OFF position. A disabled block of memory is totally transparent to the system, and other memory boards may reside in that space.

ADD: BANK SELECT ADDRESSING

The BANK SELECT PORT ADDRESS is set in a binary fashion as shown below with dip switch S2.

POSITION	ADDRESS BIT	
1	ADDRESS A7	
2	ADDRESS A6	
3	ADDRESS A5	ON = "0"
4	ADDRESS A4	
5	ADDRESS A3	
6	ADDRESS A2	OFF = "1"
7	ADDRESS A1	
8	ADDRESS A0	

EXAMPLE: To address the port at 360 octal, positions 1 thru 4 would be OFF and positions 5 thru 8 would be ON. For port 077 octal, positions 1 and 2 would be ON and positions 3 thru 8 would be OFF.

CIRCUIT DESCRIPTION

The heart of **ECONORAM XV** is the MM5257/90L44 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4K x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts. These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4K x 8 bits of information. Paralleling 8 of these rows together produces a total memory storage of 32K x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array). Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to write data into the memory, or read data from the memory. The schematics show the address circuitry along with the other **ECONORAM XV** circuitry. Each memory IC requires 12 address lines (A0-A11) to access any one of the 4096 bits available in the IC. These address lines are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to react to the given address. This requires 4 more address lines (A12-A15) which are decoded and used to enable the desired row of ICs (note row markings along the left hand side of the memory array). When data is to be written into memory, it first passes through 8 inverting buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buss). Data to be read to the data buss from memory passes through 8 TRI-STATE inverting buss drivers; when data is not being read to the buss, the outputs of these inverters are in a high-impedance or "disconnected" state. This board can be used in a system with more that 64K of memory, and because of this there must be a method to disable the entire board and remove it from the system memory map. Since the CPU can only access 64K of memory with its 16 address lines, the method chosen was to use an I/O port to ENABLE/DISABLE the board. Switch S2 is used to select the I/O port for the board and when the correct port is decoded by U13, U15 latches in data bit d0 and if it is high, the bank(s) will be enabled at the address selected by switch S1 . Conversely if data bit d0 is low upon receiving the output instruction the board will be disabled. The board can be set up to be turned ON or OFF with Preset or Power-on by using switch S3 positions 4 and 3.

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurances, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC.

This board is guaranteed to operate at 4 MHz, or 5 MHz with an 8085 CPU over the full temperature range (0-70 C ambient) and draw less than 3.5 Amps. Also, our typical measured currents were less than 3.0 Amps, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

It is interesting to note that static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

Parts List

☐ (1) ECONORAM XV circuit board

INTEGRATED CIRCUITS (note: the following parts may have letter suffixes and prefixes along with the key numbers given below.)

☐	(64)	MM5257-3L	4K x 1 static RAM	
☐	(1)	74LS00	Quad 2 input NAND	(U14)
☐	(4)	74LS04	Hex inverter	(U7,11,12,16)
☐	(1)	74LS32	Quad 2 input OR	(U10)
☐	(1)	74LS74	Dual "D" flip flop	(U15)
☐	(1)	74LS139	Dual decoder	(U9)
☐	(1)	74LS240	Octal buss driver	(U17)
☐	(2)	74LS283	4 bit adder	(U6,U8)
☐	(1)	25LS2521	Octal comparator	(U13)
☐	(5)	7805	5 Volt regulator	(U1-U5)
		81LS96A9		U18

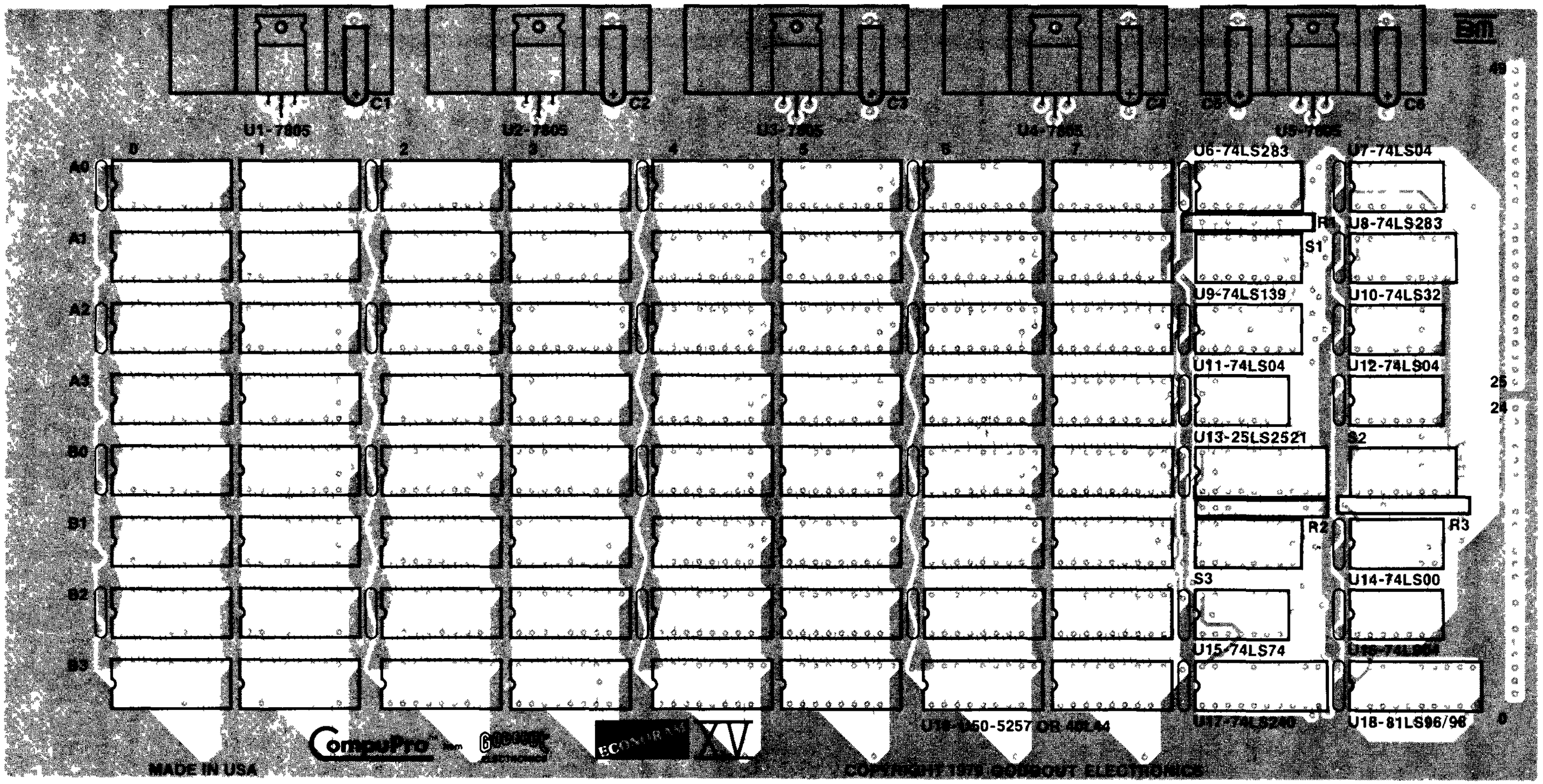
OTHER ELECTRONIC COMPONENTS

☐	(3)	SIP resistor packs	(R1-R3)
☐	(6)	39us 10V tantalum caps.	(C1-C6)
☐	(29)	Ceramic disc caps *	

MECHANICAL COMPONENTS

☐	(77)	Low Profile IC sockets *	
☐	(3)	Dipswitch, 8 position	(S1-S3)
☐	(5)	TO-220 heat sinks	
☐	(10)	Sets, #6 hardware	
☐	(1)	Heathkit bracket	
☐	(2)	25 pin female connectors	
☐	(1)	**ECONORAM XV** instruction booklet	

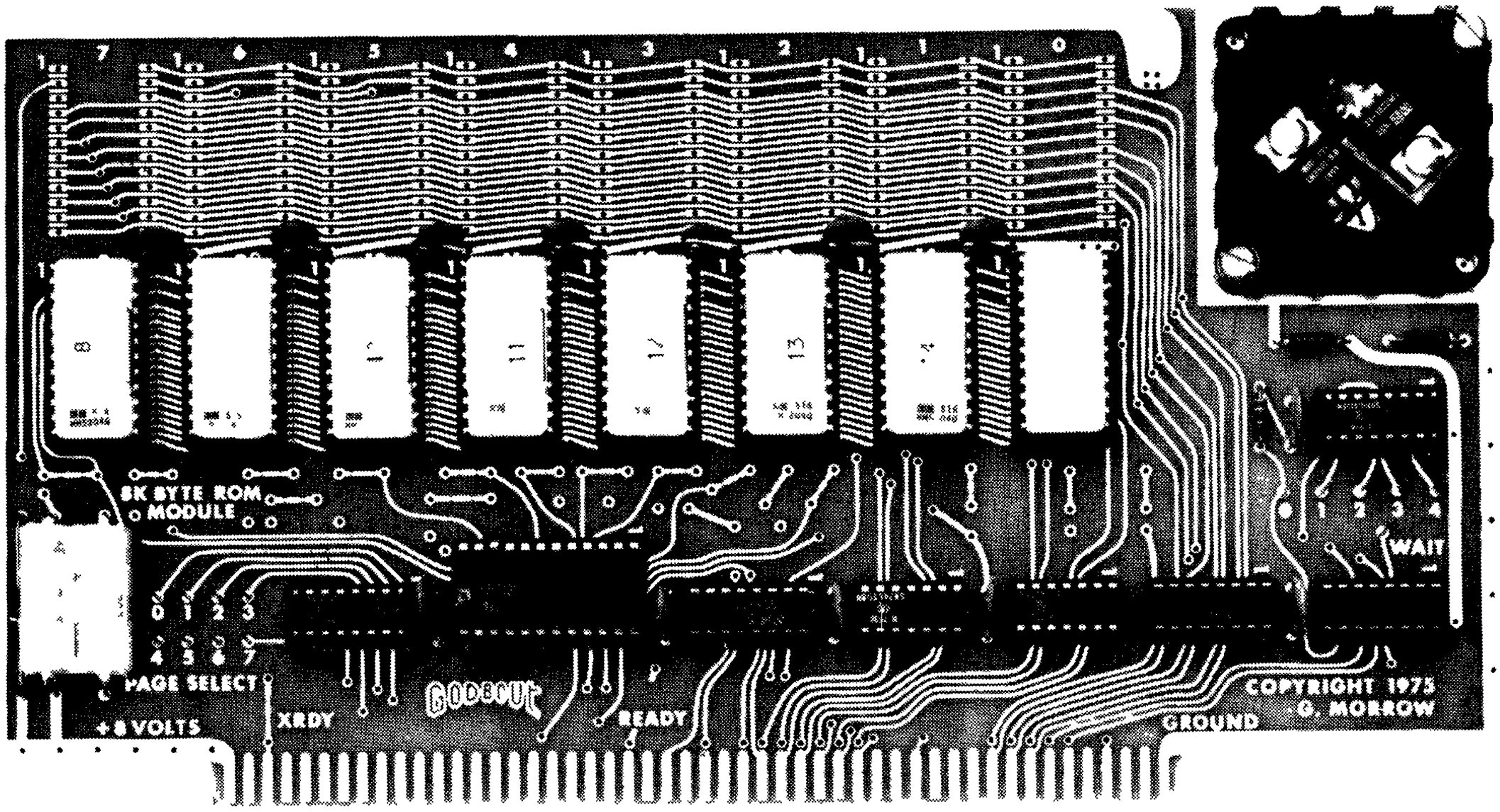
* Supplied already soldered to board



Component Layout

UP

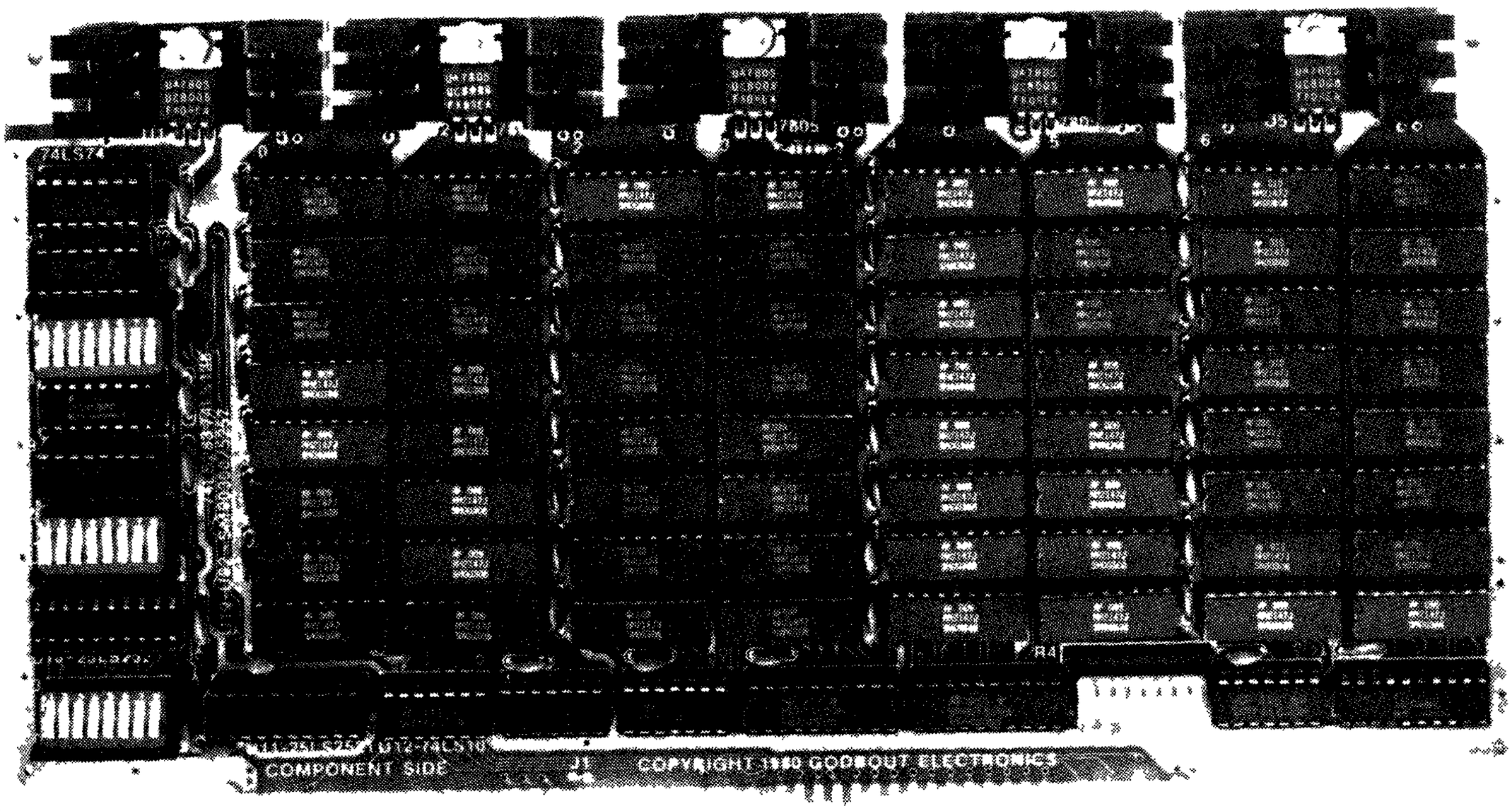
EPROM 5204



MANUAL ON PAGE 5

RAM XX™

USER'S MANUAL



IEEE·696/S-100

32K Static RAM

Extended Addressing and Bank Select

164
£

CompuPro™ from GODBOUT

8/80

129

RAM XX

TECHNICAL OVERVIEW

The RAM XX is a high speed 32K byte static RAM board designed for full compatibility with the proposed IEEE S-100 bus standard of 24 address lines as well as all currently used Bank Select configurations. The user can at will alter the board for either configuration by simply moving one integrated circuit and changing several switch settings. This board is configured as one 32K byte block that can slide throughout its 64K byte page and start on any 4K boundary. In addition, an 8 position DIP switch is provided to disable any or all of the eight 4K byte blocks on this board and create as many windows in this memory as needed to avoid system memory conflicts.

With the RAM XX configured for extended 24 bit addressing, this board fully conforms to the proposed IEEE S-100 Bus standard fully, and allows the user to place the memory in any or all of the 256 - 64K byte pages. With the RAM XX configured for Bank Select mode, the user can select any I/O port as the Bank port and any bit as the Bank control bit. In addition, the user can select whether the board comes up enabled or disabled on power-up.

The RAM XX is shipped as a 16K, 24K, or 32K byte board, with sockets for all 32K bytes of RAM and all support chips. Extra heavy duty power supply traces, generous bypassing of supply lines, sockets for all integrated circuits, careful layout, conservative design techniques, and a double-sided, solder-masked printed circuit board with complete component legends make this a versatile memory board which will give exceptionally long and trouble-free service even in harsh environments.

SWITCH SETTINGS FOR COMPUPRO RAM XX

Switch 1

Switch 1 is used to enable or disable 4K blocks of RAM. When a switch is in the 'ON' position then its associated 4K row is enabled.

Switch Position	Row Number	
1	0	
2	1	
3	2	'ON' enables row
4	3	
5	4	
6	5	'OFF' disables row
7	6	
8	7	

For example, if this board is addressed to start at 0K, flipping positions 2 and 3 OFF will create a window at the 2nd and 8th 4K block of the board.

Switch 2

Switch 2 is used to select the base address of the RAM XX, whether or not the board is used for extended addressing or phantom, and whether or not the board comes up disabled or enabled for a bank select system.

Positions 1 to 4 select the base address of the RAM XX. Each switch position has a decimal number associated with it. To select the proper address for the board, merely add up the decimal numbers until they equal the starting location you want.

Switch Position	Decimal Number
1	4
2	8
3	16
4	32

Starting Location	Starting Address	Starting Location	Starting Address
0K	0000H	32K	8000H
4K	1000H	36K	9000H
8K	2000H	40K	A000H
12K	3000H	44K	B000H
16K	4000H	48K	C000H
20K	5000H	52K	D000H
24K	6000H	56K	E000H
28K	7000H	60K	F000H

For example, if you wanted the board to start at 0 (the zeroeth 4K block), you would leave the switches off. If you wanted the board to start at the 8K address boundary you would turn on switch position 2. If you wanted the board to start at the 28K boundary, you would turn on switches 1, 2 and 3 (4+8+16=28). NOTE: If the 32K bytes of this board are started at address 9000H or greater, the residual memory beyond FFFFH will wrap around and start at 0000H.

Switch position 5 is used to select whether or not you want the RAM XX to respond to extended addressing, meaning bank select or the 8 extended address bits specified in the IEEE S-100 standard (A16-23).

If you are using the RAM XX as a standard or global memory, you should turn switch postion 5 ON. If you are using the RAM XX as an extended address memory, or bank select memory turn switch position 5 OFF.

Switch position 6 is used to enable/disable the RAM XX's response to PHANTOM. If you want the board to respond (deselect) to a PHANTOM, turn switch position 6 ON. If you don't want the RAM XX to respond to PHANTOM, turn switch position 6 OFF.

Positions 7 and 8 determine whether or not the RAM XX comes up enabled or disabled if you are using it as a bank select memory.

If you want the RAM XX to come up enabled when you turn on the computer, turn switch position 7 ON and position 8 OFF. If you want the board to come up disabled, turn switch position 7 OFF and position 8 ON. NOTE: Never leave both positions 7 and 8 either ON or OFF at the same time!

Switch 3

Switch 3 is used to set either the extended address or the bank select port address. If you are using the RAM XX as an extended address memory you should plug the 25LS2521 into position U11 (leaving U5 and U10 blank). Then switch 3 will respond as follows:

Switch Position	Address Bit	
1	A16	
2	A17	
3	A18	ON = '0' (does not match bit)
4	A19	
5	A20	
6	A21	OFF = '1' (matches bit)
7	A22	
8	A23	

If you are using the RAM XX as a bank select board you should plug the 25LS2521 into position U10 (leaving U11 blank), and a 74LS74 into position U5. Then switch 3 will select the bank select port address as follows:

Switch Position	Address Bit	
1	A0	
2	A1	
3	A2	ON = '1'
4	A3	
5	A4	
6	A5	OFF = '0'
7	A6	
8	A7	

Switch 4

If you are using the RAM XX as an extended address memory you can ignore switch 4. If you are using the RAM XX as a bank select board then switch 4 is used to select the data bit that will enable the board when written to the bank select port.

Switch Position	Data Bit	
1	D0	
2	D1	
3	D2	ON = '1'
4	D3	
5	D4	
6	D5	OFF = '0'
7	D6	
8	D7	

Note that if more than one switch is turned on then the board will be selected if <u>any</u> bit matches.

32Kx8 RAM.FOR S-100 BUS

PARTS LIST

(1) RAM XX circuit board

INTEGRATED CIRCUITS (note: the following parts may have letters suffixes and prefixes along with the key numbers given below.)

(64)	MM5257N-3	L 4Kx1 static RAM	
(1)	74LS02	quad 2 input NOR	(U13)
(1)	74LS04	hex inverter	(U14)
(1)	74LS10	triple 3 input NAND	(U12)
(2)	74LS30	8 input NAND	(U7, U17)
(1)	74LS74	dual "D" flip flop	(U6)
(1)	74LS138	decoder	(U8)
(1)	74LS240	octal buss driver	(U18)
(1)	74LS283	4 bit adder	(U9)
(1)	25LS2521	octal comparator	(U11 or U10)
(2)	81LS96/98	octal buss driver	(U15, U16)
(5)	7805	5 volt regulator	(U1-U5)

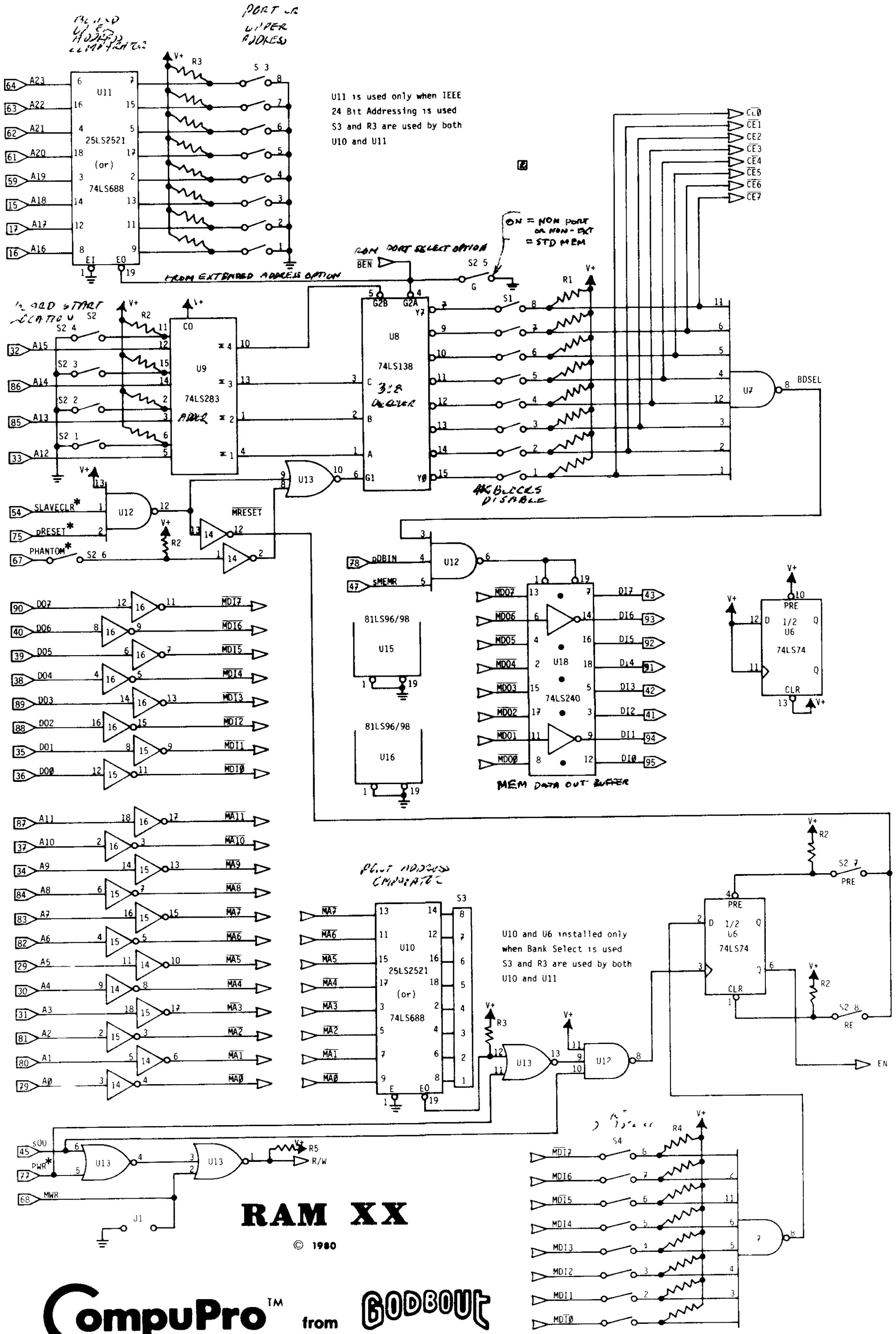
OTHER ELECTRONIC COMPONENTS

(4)	SIP resistor packs	(R1-4)*
(10)	39uf Tantalum Capacitors	(C1-C10)
(45)	Ceramic bypass Capacitors *	
(1)	2.7K ohm resistor 1/4 W *	(R5)

MECHANICAL COMPONENTS

(77)	Low Profile Sockets *	
(4)	Dip Switch, 8 position	(S1-S4)*
(5)	TO-220 Heat Sinks	
(5)	Sets 6-32 Hardware	

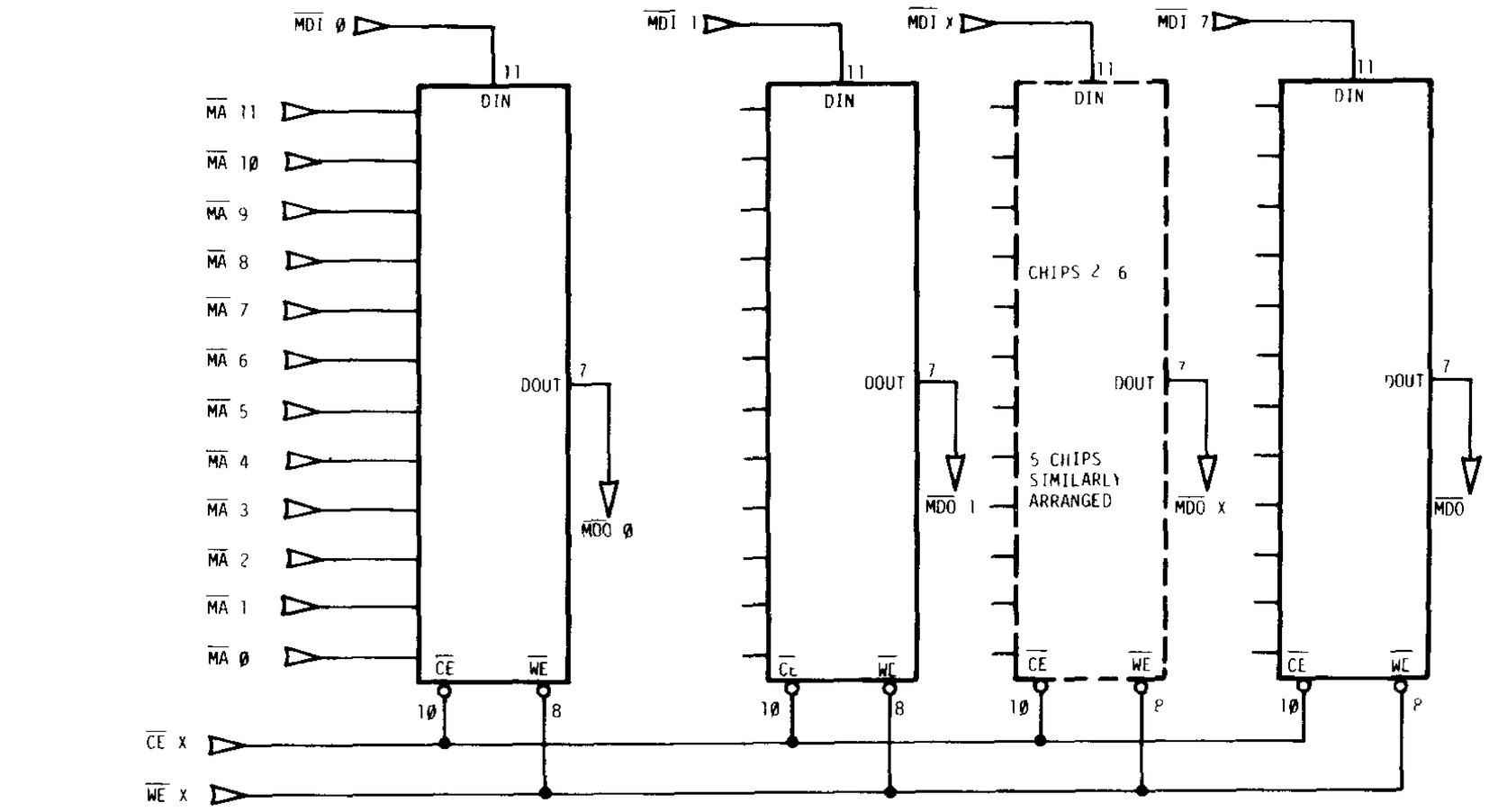
* supplied already soldered on the board

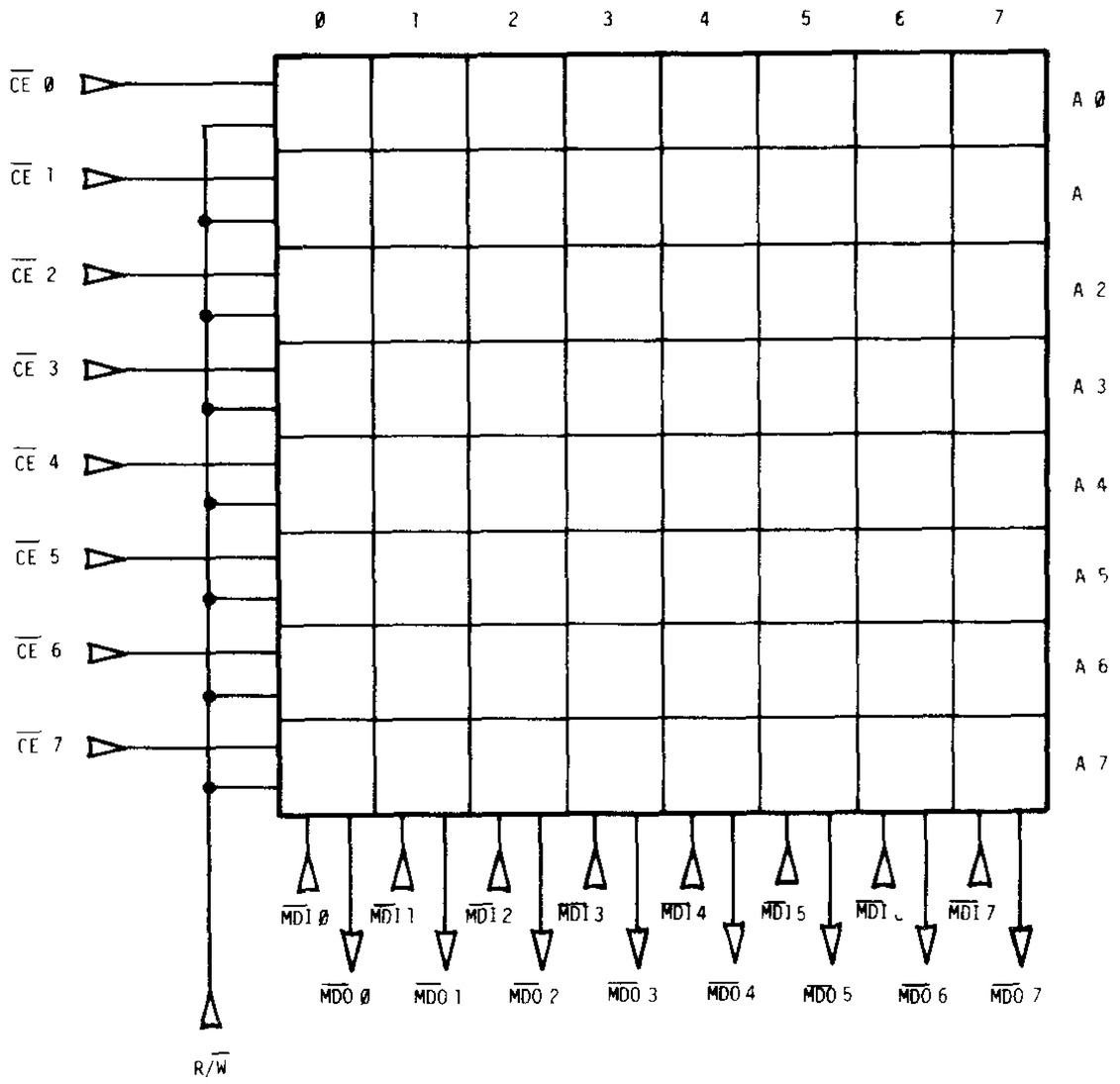


RAM XX

© 1980

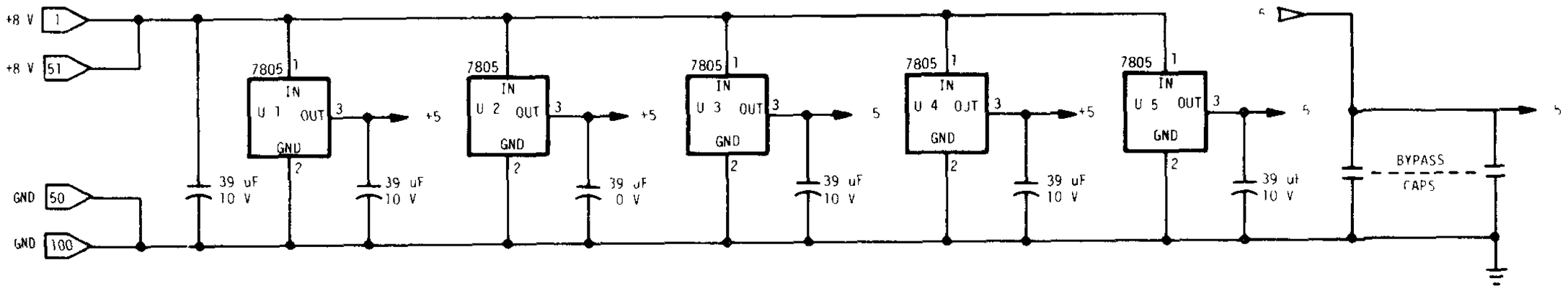
CompuPro™ from GODBOUT ELECTRONICS



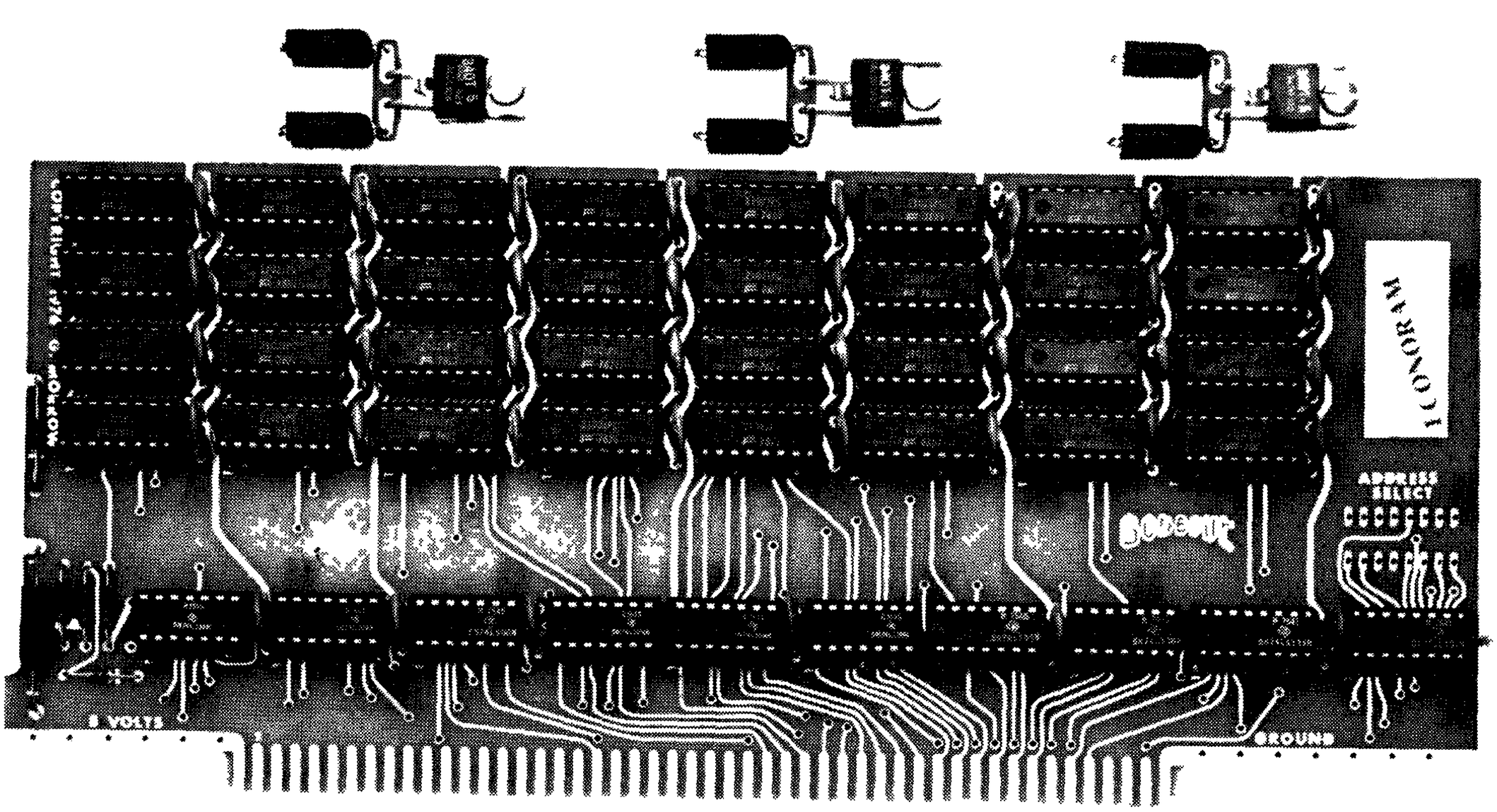


RAM x
PART 2 OF 2

© 1980 ODBOUT

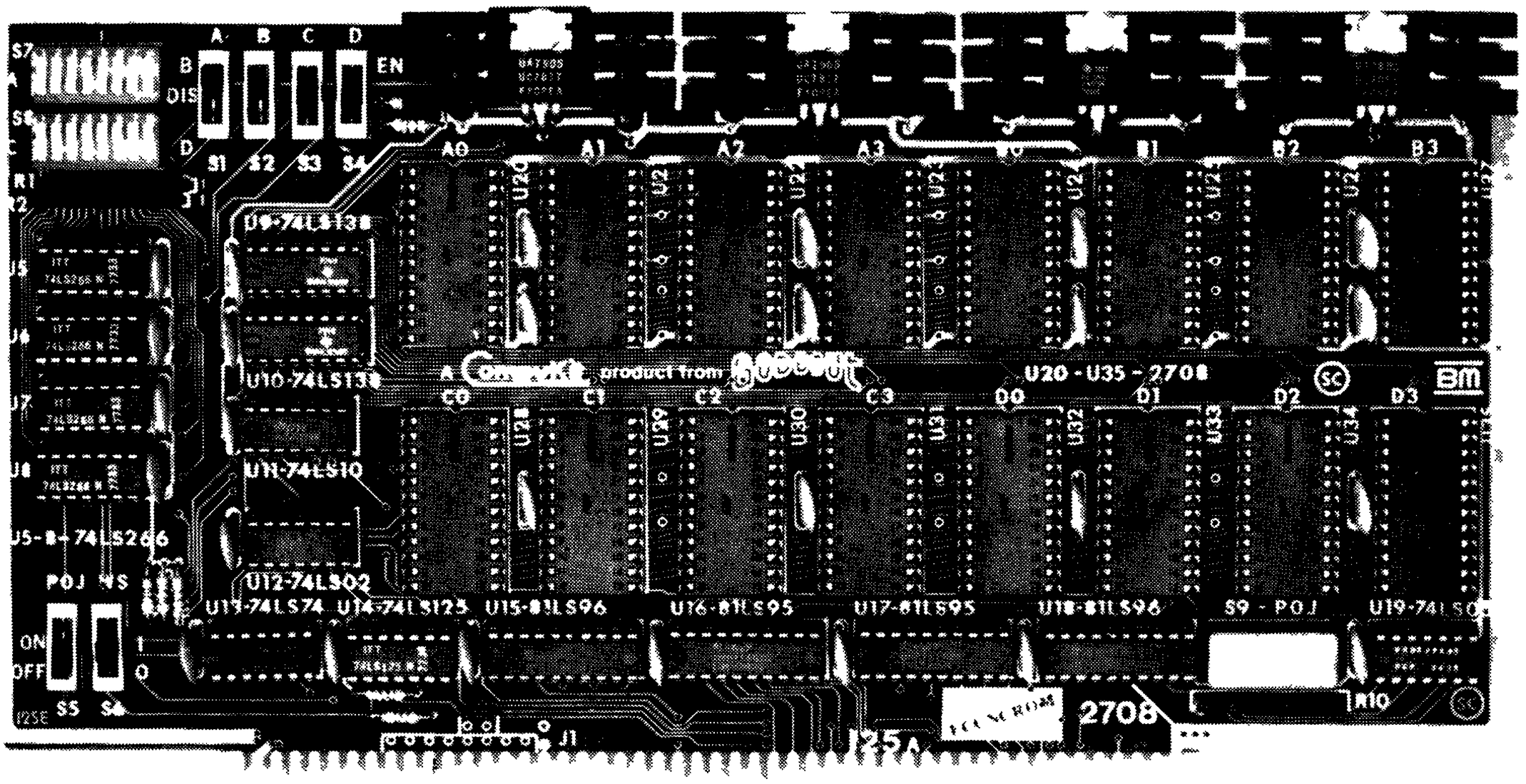


ECONORAM



MANUAL ON PAGE 7

ECONOROM 2708 T.M.
USER'S MANUAL



16K x 8 EPROM memory • S-100
with JUMP START

125 mac

A CompuKit™ product from GODBOUT

1/79

ABOUT ECONOROM 2708

Congratulations on your decision to purchase ECONOROM 2708, a 16K x 8 EPROM board designed specifically for electrical and mechanical compatibility with the proposed IEEE S-100 buss standard The S-100 buss currently is one of the most popular in the industry and by far the most prolific, we believe this board, with the rest of the S-100 portion of the COMPUKIT family is one of the best memory boards available for that buss

We recommend that the parts in this kit be checked against the parts list for completeness and that these instructions be read through carefully before starting Assembly should take from one to four hours, depending on previous experience Upon completion, you will discover as thousands of satisfied COMPUKIT memory owners have discovered, the pleasure of using a fine memory board that just works and works and works

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing ECONOROM 2708 welcome to the club!

TECHNICAL OVERVIEW

This board provides space for up to 16 2708s, one of the most popular high density EPROMS EPROMS give the advantage of retaining stored data when power is removed EPROMS are erasable, that is, after programming they may be erased and reprogrammed with other material The EPROM locations on this board are grouped in four independent 4K blocks The on-board DIP switch (no jumpers required) provides addressing on any 4K boundary Additionally, each 4K block contains an independent disable switch This board also features a wait state selection switch to select zero or one wait state, provision for use of PHANTOM (line 67), a switch addressed power-on-jump feature, thorough capacitor bypassing of supply lines to suppress noise transients, plus on-board regulation and heat-sinking for reliably cool operation All this and presoldered sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend This board provides the user with a highly flexible building block for virtually any S-100 system configuration

Parts List

see errata page 142

Upon receipt of your kit, check your parts against the list below

☐ (1) ECONOROM 2708 circuit board

INTEGRATED CIRCUITS (note the following parts may have letter suffixes and prefixes along with the key numbers given below)

☐ (2) 7905 negative 5V regulator (U1 - U2)
☐ (1) 7812 positive 12V regulator (U3)
☐ (1) 7805 positive 5V regulator (U4)
☐ (2) 74LS138 1 of 8 line decoders (U9 U10)
☐ (1) 74LS266 exclusive NOR gate (U2)
☐ (1) 74LS10 NAND gates (U11)
☐ (1) 74LS02 NOR gate (U12)
☐ (1) 74LS74 dual flip flop (U13)
☐ (1) 74LS125 TRI-STATE® output gates (U14)
☐ (2) 81LS96/98 TRI-STATE® buffer (U15, U18)
☐ (2) 81LS95/97 TRI-STATE® buffer (U16, U17)
☐ (1) 74LS05 hex inverter (U19)

OTHER ELECTRONIC COMPONENTS

☐ (3) SIP resistor packs (R1, R2, R10)*
☐ (27) Disc capacitors (C9-C35)*
☐ (7) 2 7K 1/4 watt resistors (R3-R9) red, violet, red
☐ (4) 39uF 10V tantalum capacitors (C5, C6, C7, C8)
☐ (4) 1 8uF 35V tantalum capacitors (C1, C2, C3, C4)

MECHANICAL COMPONENTS

☐ (3) DIP switches (S7, S8, S9)*
☐ (31) low profile sockets*
☐ (6) slide switches (S1-S6)
☐ (4) sets #6 hardware
☐ (4) TO-220 heat sinks

*Supplied already soldered to board

MEMORY ADDRESS ASSIGNMENT

This board is configured as 4 independent 4K blocks addressable on any 4K boundary Each 4K block is addressed using the following DIP switch positions

Block A	Switch S7 positions 1 - 4
Block B	Switch S7 positions 5 - 8
Block C	Switch S8 positions 1 - 4
Block D	Switch S8 positions 5 - 8

Each area s address is selected as follows
see errata page 142

Switch Number 1 2 3 4 or 6 7 8 9		Hex Address
0 0 0 0		0 0 0 0
0 0 0 1		1 0 0 0
0 0 1 0		2 0 0 0
0 0 1 1	0 = OFF	3 0 0 0
0 1 0 0	1 = ON	4 0 0 0
0 1 0 1		5 0 0 0
0 1 1 0		6 0 0 0
1 0 0 0		7 0 0 0
1 0 0 1		8 0 0 0
1 0 0 1		9 0 0 0
1 0 1 0		A 0 0 0
1 0 1 1		B 0 0 0
1 1 0 0		C 0 0 0
1 1 0 1		D 0 0 0
1 1 1 0		E 0 0 0
1 1 1 1		F 0 0 0

BOARD ENABLE SWITCHES

Slide switches S1 through S4 are board enable switches for blocks A through D, respectively Each switch in the CENTER position *disables* its respective block of memory Putting each switch in the UP position will *enable* the respective block of memory When a block is disabled, it is transparent or invisible as far as the machine is concerned (just as if it were non-existent)

This feature allows the board to be used as a 4K, 8K, 12K or 16K board It also allows the user to have parallel sets of software For example, suppose you need to run some programs in BASIC, switch over to some other language, then get back to BASIC again You may have both languages in blocks occupying the same area of memory When using BASIC, merely disable the block containing the other language When you wish to switch, disable the BASIC block and enable the other Note that if 2 blocks share the same address space, only 1 may be enabled at any time

POWER ON JUMP

The power on jump feature, when enabled, causes the machine to start at some address other than zero after reset or power on clear This is accomplished by driving the PHANTOM line low which should disable all system memory, then putting a jump command onto the data in buss, causing the CPU to jump to the desired address This address can be any multiple of 256 by setting the high order byte of the address on the appropriate DIP switch (switch 9) This feature is *enabled* when slide switch 5 is in the CENTER (ON) position and is *disabled* when this switch is in the DOWN (OFF) position

WAIT STATE SELECT SWITCH

If switch S6 is in the CENTER position, *one* wait state will be added to all memory cycles accessing this board If the switch is in the DOWN position, no wait states will be added

PHANTOM LINE

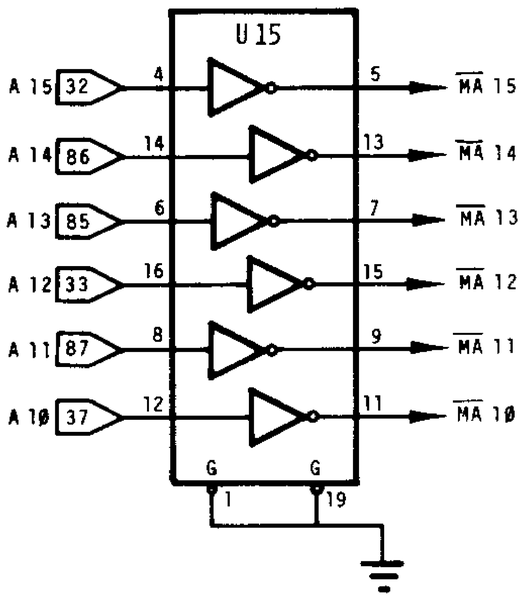
In response to increasing numbers of users who have requested inclusion of "PHANTOM line, (often used for implementing power on jump features) this board is designed for use with active or inactive PHANTOM lines Boards require a jumper J1 to implement this feature

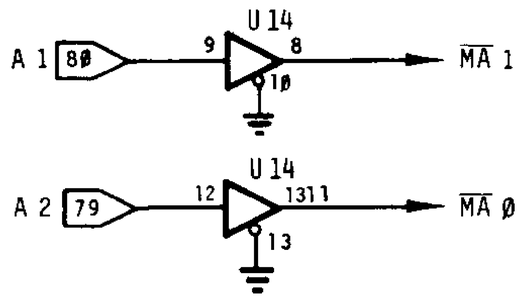
CAUTION

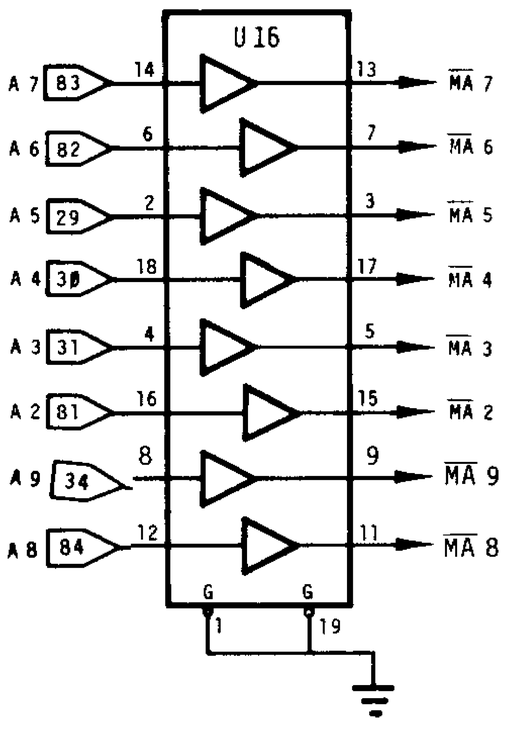
Some manufacturers use the PHANTOM line (buss pin 67) for a refresh signal This will conflict with the PHANTOM feature and cause boards with PHANTOM to fail If your system has this conflict, it *must* be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards The PHANTOM feature is disabled if the jumper (J1) is *not connected* on the trace to buss pin 67 (see Figure 11)

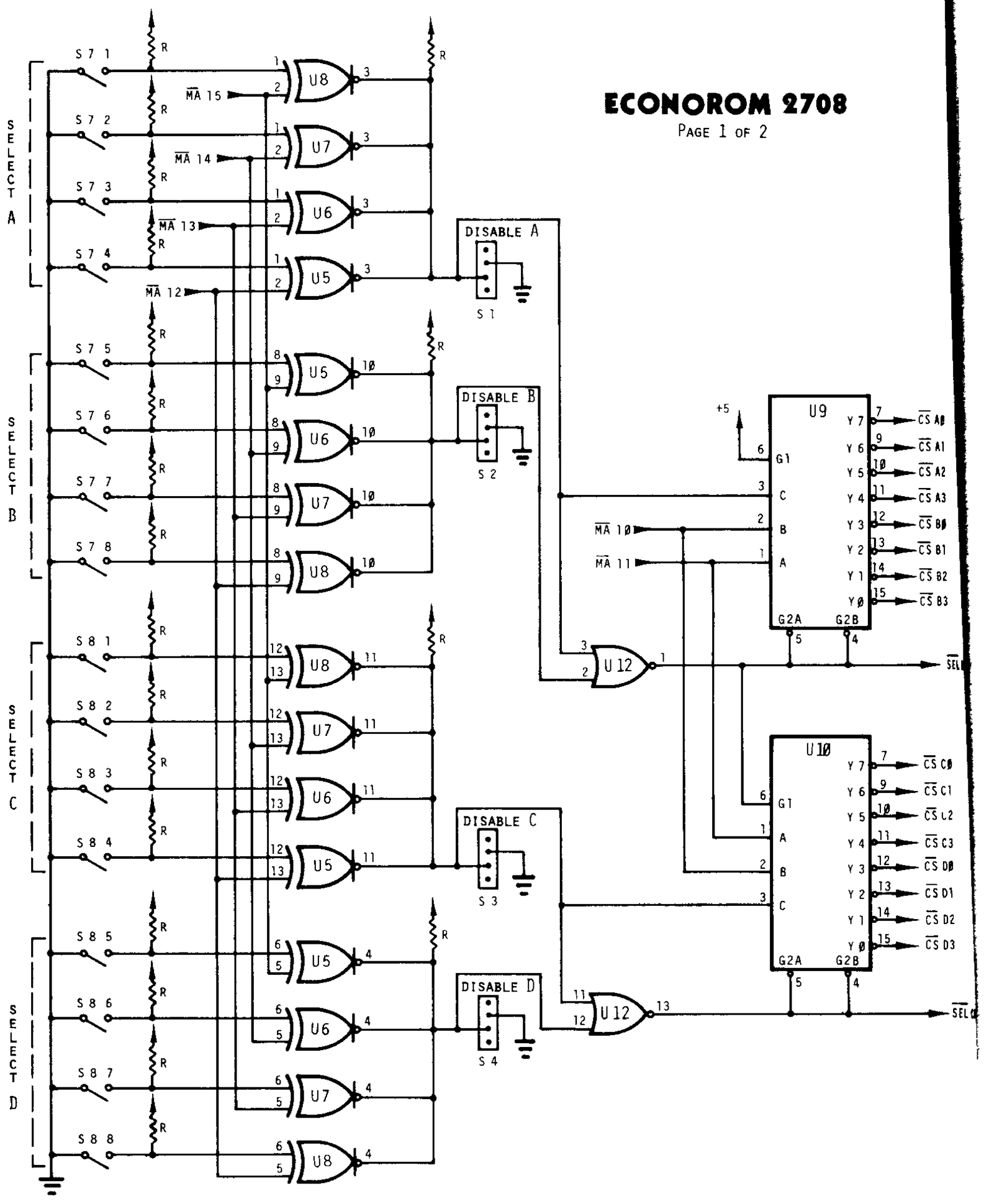
If you want the PHANTOM feature the conflicting refresh signal may be eliminated (IF NOT USED ELSEWHERE IN THE SYSTEM) by cutting the trace connected to buss pin 67 on the CPU board BE SURE OF YOUR SYSTEM CONFIGURATION BEFORE CUTTING ANY TRACES

ECONOROM 2708



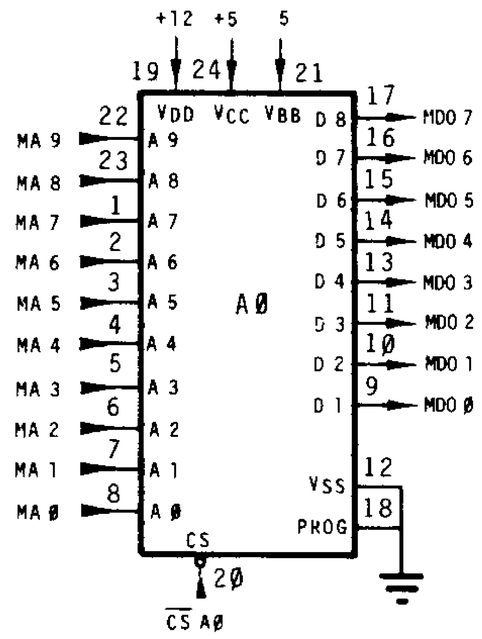


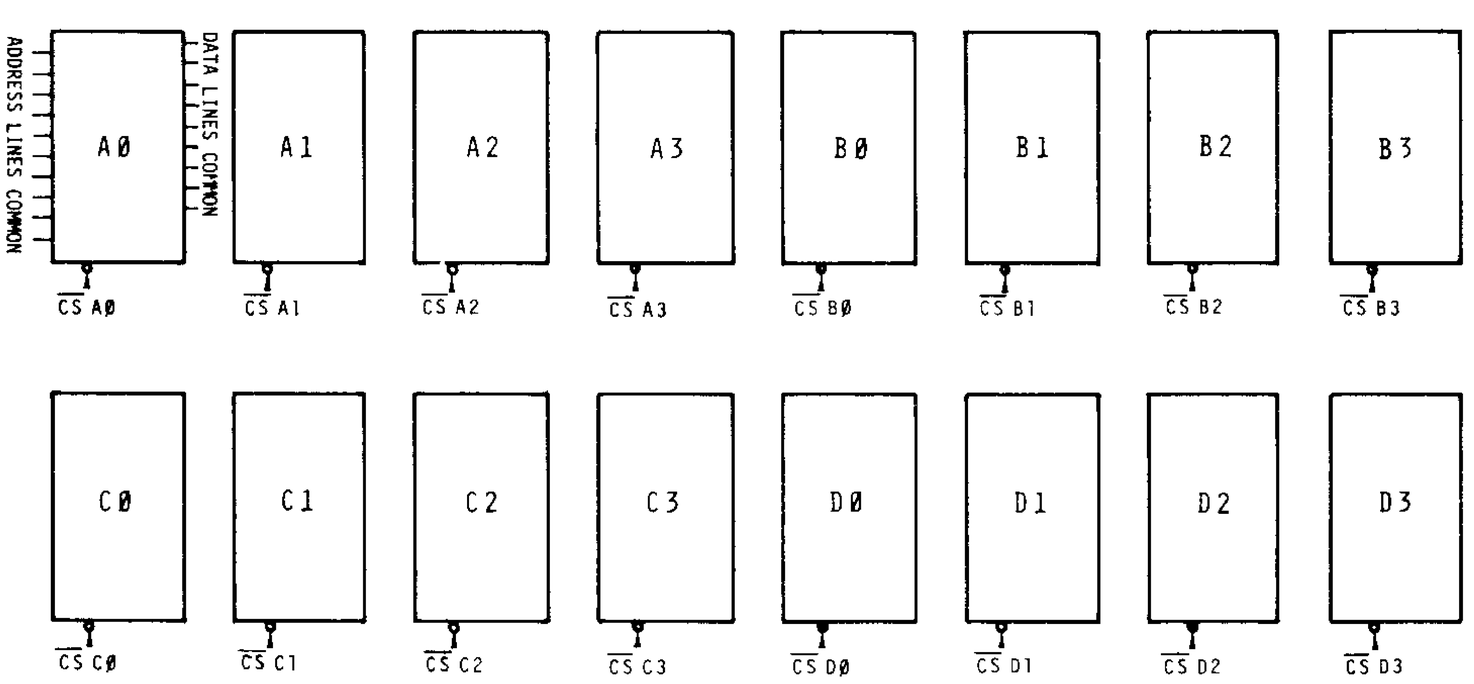


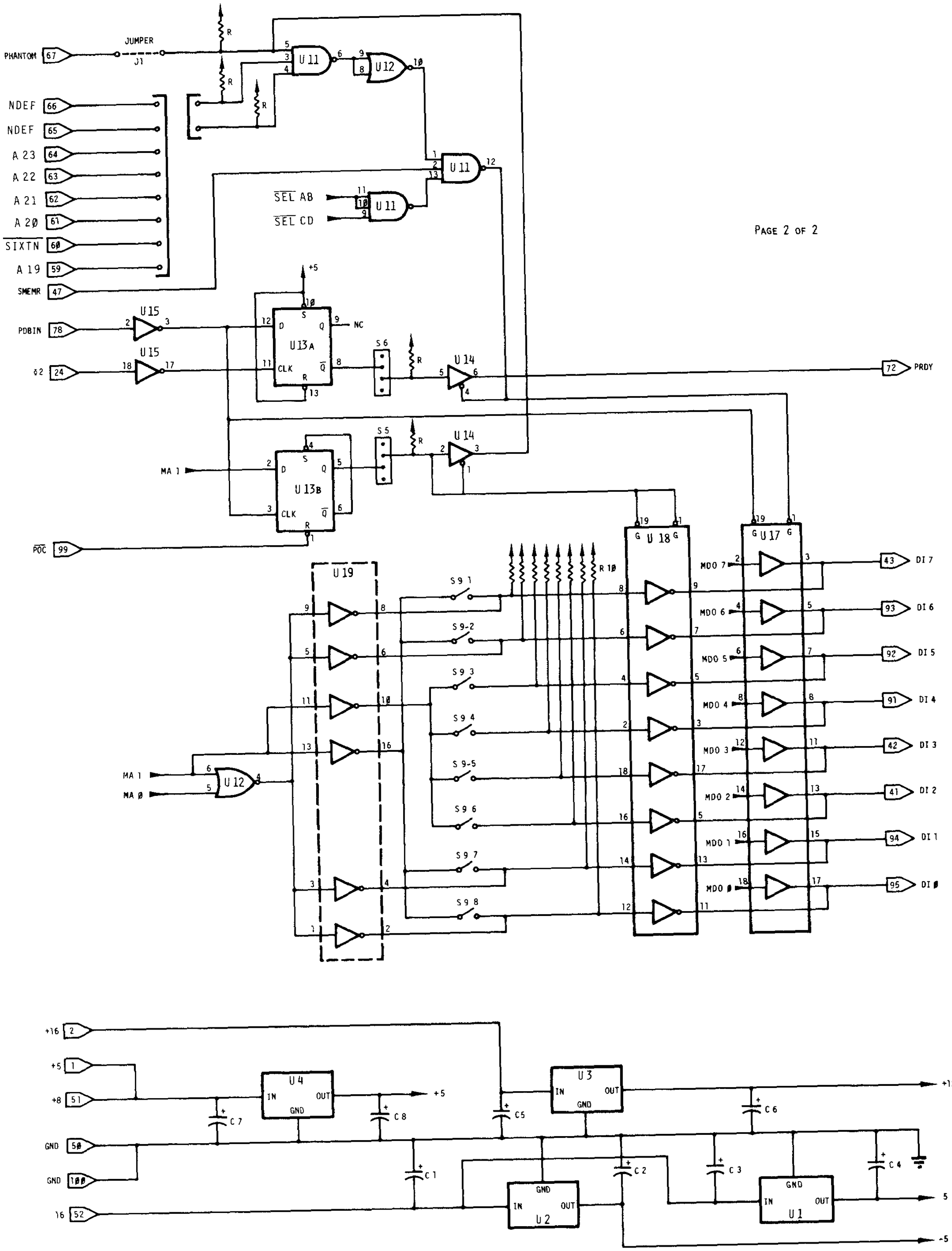


Resistors [R] not otherwise labeled are in SIP R1 or R2

U 2Ø THROUGH U 35 ARE 2708s






PHANTOM 67
JUMPER
J1
R
U 11
U 12
NDEF 66
NDEF 65
A 23 64
A 22 63
A 21 62
A 20 61
SIXTN 60
A 19 59
SMEMR 47
SEL AB
SEL CD
U 11
U 11
+5
PDBIN 78
U15
U13A
NC
S 6
U 14
72 PRDY
Ø2 24
U15
CLK
S 5
U 14
MA 1
U 13B
POC 99
U 19
S 9 1
S 9-2
S 9 3
S 9 4
S 9-5
S 9 6
S 9 7
S 9 8
R 10
U 18
U 17
MDO 7
MDO 6
MDO 5
MDO 4
MDO 3
MDO 2
MDO 1
MDO Ø
43 DI 7
93 DI 6
92 DI 5
91 DI 4
42 DI 3
41 DI 2
94 DI 1
95 DI Ø
MA 1
MA Ø
U 12
+16 2
+5 1
+8 51
GND 50
GND 100
16 52
U 4
U 3
U 2
U 1
C 7
C 8
C 5
C 6
C 1
C 2
C 3
C 4
+12
5
-5

CIRCUIT DESCRIPTION

The heart of ECONOROM 2708 is the 2708 erasable, programmable, read-only memory (EPROM), which has 8K bits of storage configured as 1024 bytes of eight bits each (Thus, each is a "1K x 8" memory IC) These ICs are arranged in blocks of four This way, each block can store 4K x 8 bits of information Four of these blocks together produce a total memory storage of 16K x 8 bits

Now that we have this storage, there are still other aspects we must consider First, *addressing* a specific address in memory, and second, *reading* from memory

The logic diagram on pages 8 and 9 show the address circuitry along with the other ECONOROM circuitry Each memory IC requires 10 address bits (A0-A9) to access any one of the 1024 bytes available in the IC These address bits are generated by the CPU and are buffered on the ECONOROM After buffering, a particular address is presented to all memory address selection pins We must also select which particular IC in any particular block is to react to the given address This requires 6 more address bits (A10-A15) A12 through A15 are decoded and used to *select* the desired block of ICs A10 and A11 are decoded and used to *enable* the desired IC in that block

Data to be read into the data buss from memory passes through 8 TRI-STATE® drivers When data is not being read onto the buss, the outputs of these drivers are in a high impedance or "disconnected" state

To prevent IC generated switching transient noise problems, bypass capacitors are tied across the power lines at regular intervals in the memory array and at every support IC

This board is guaranteed to operate at 2MHz over the full commercial temperature range (0-70° C ambient) and to draw less than 3500 mA (3 5 amps) when used with standard 2708's We have tested these at 4MHz with "standard" 2708's and found them to operate reliably in all cases with one wait state The speed and current will depend directly on the particular 2708's you use

THANK YOU

This board is the result of much time, work and experience on the part of a number of people In addition to thanking you for choosing this board, we'd like to thank everyone involved for their work on this project

We strive for a board that not only works the first time but continues to give reliable operation for a long time If we can be of any help to you in applying this board, or if you have any questions, please let us know As always, we solicit your comments, letters and new product suggestions

HAPPY COMPUTING!

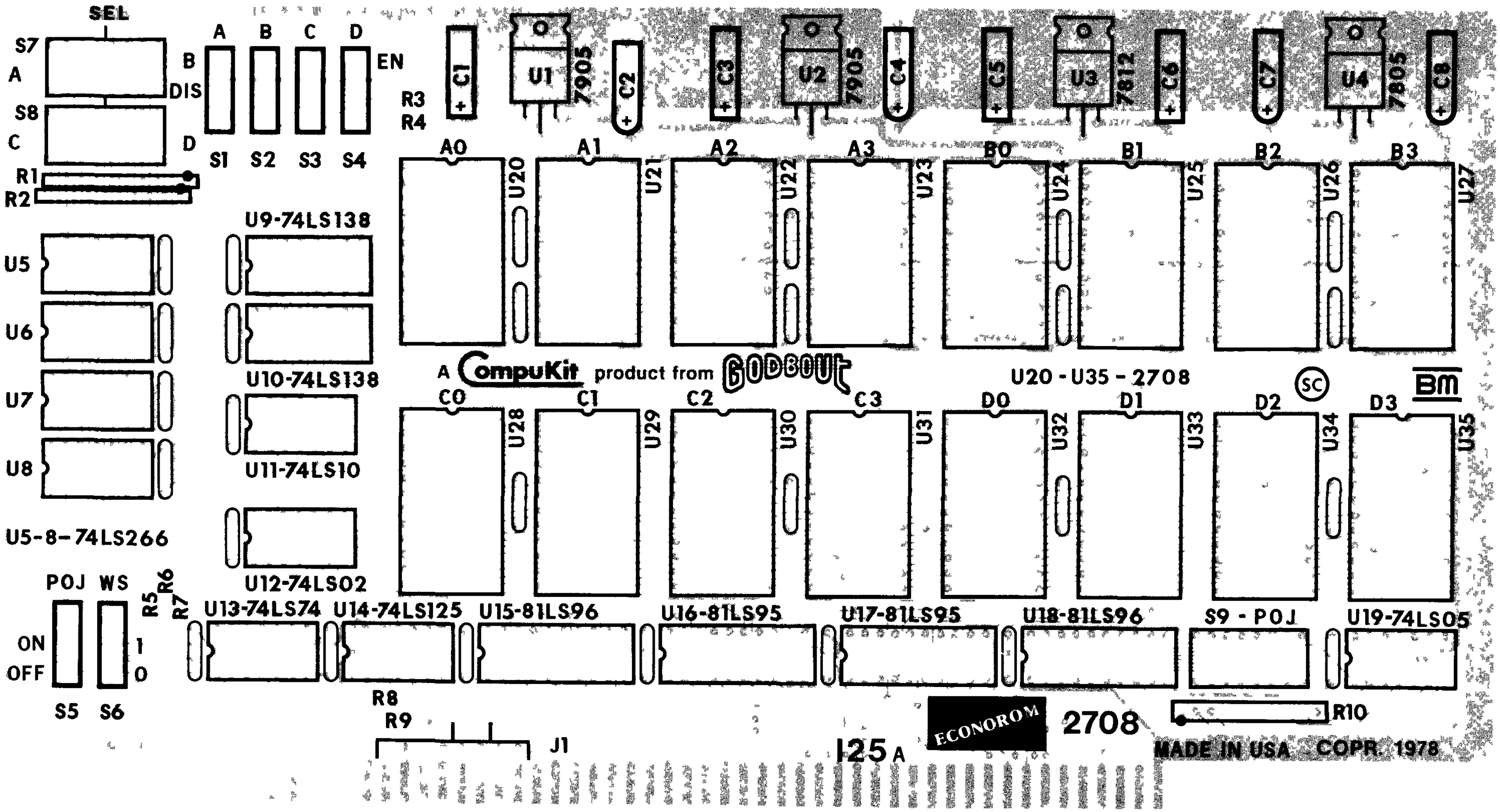
ERRATA ECONOROM 2708

PARTS LIST should read

(4) - 74LS266 at positions U5, U6, U7 & U8
(4) - 39 uF tantalum capacitors at positions C2, C4, C7 & C8
(4) - 1.8 uF 35V tantalum capacitors at positions C1, C3, C5 & C6

MEMORY ADDRESS ASSIGNMENT
should read

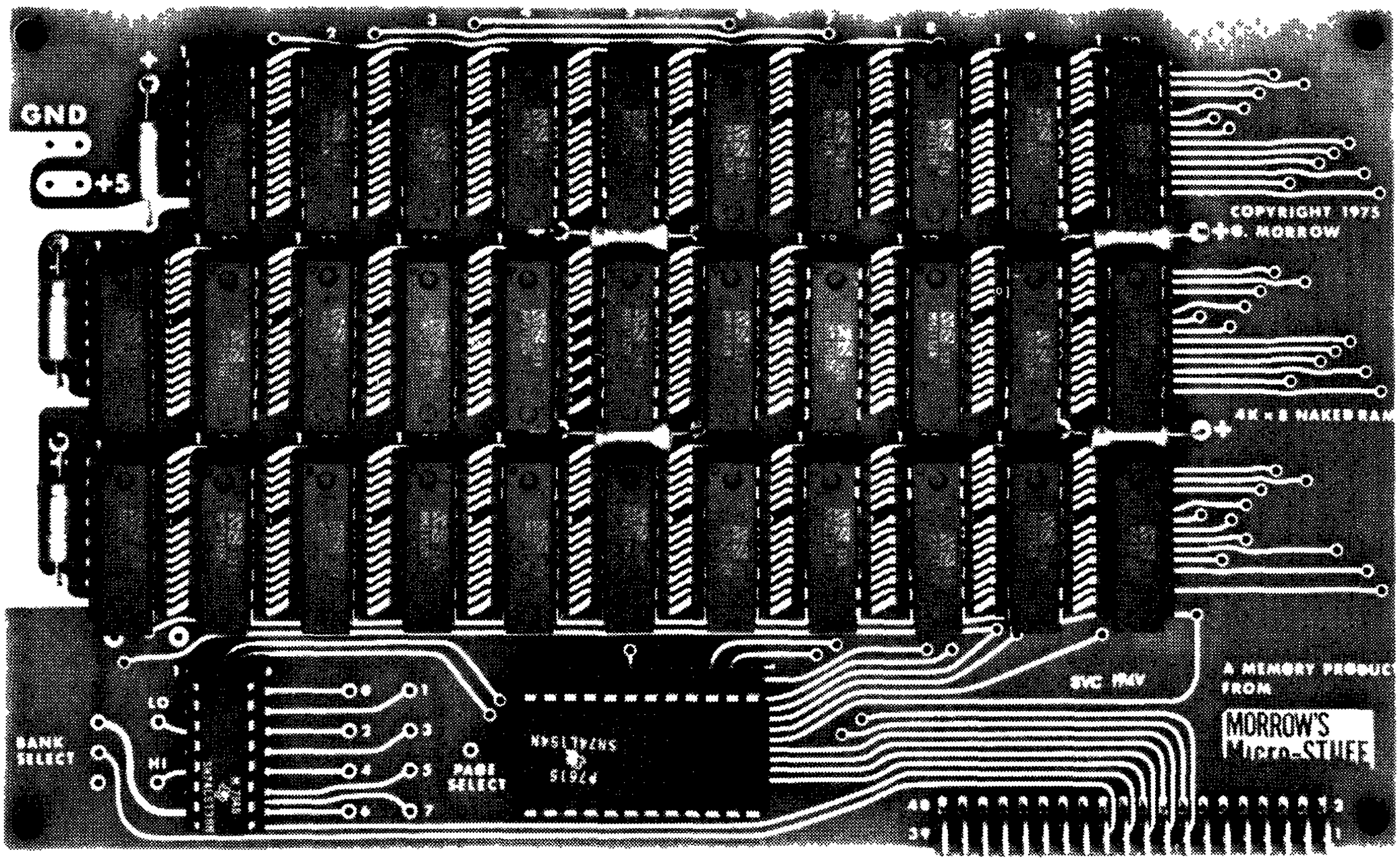
Switch Number 1 2 3 4 or 6 7 8 9		Hex Address
0 0 0 0		0 0 0 0
0 0 0 1		1 0 0 0
0 0 1 0		2 0 0 0
0 0 1 1		3 0 0 0
0 1 0 0		4 0 0 0
0 1 0 1		5 0 0 0
0 1 1 0	0 = OFF	6 0 0 0
0 1 1 1	1 = ON	7 0 0 0
1 0 0 0		8 0 0 0
1 0 0 1		9 0 0 0
1 0 1 0		A 0 0 0
1 0 1 1		B 0 0 0
1 1 0 0		C 0 0 0
1 1 0 1		D 0 0 0
1 1 1 0		E 0 0 0
1 1 1 1		F 0 0 0



Component Layout

UP

JOLT

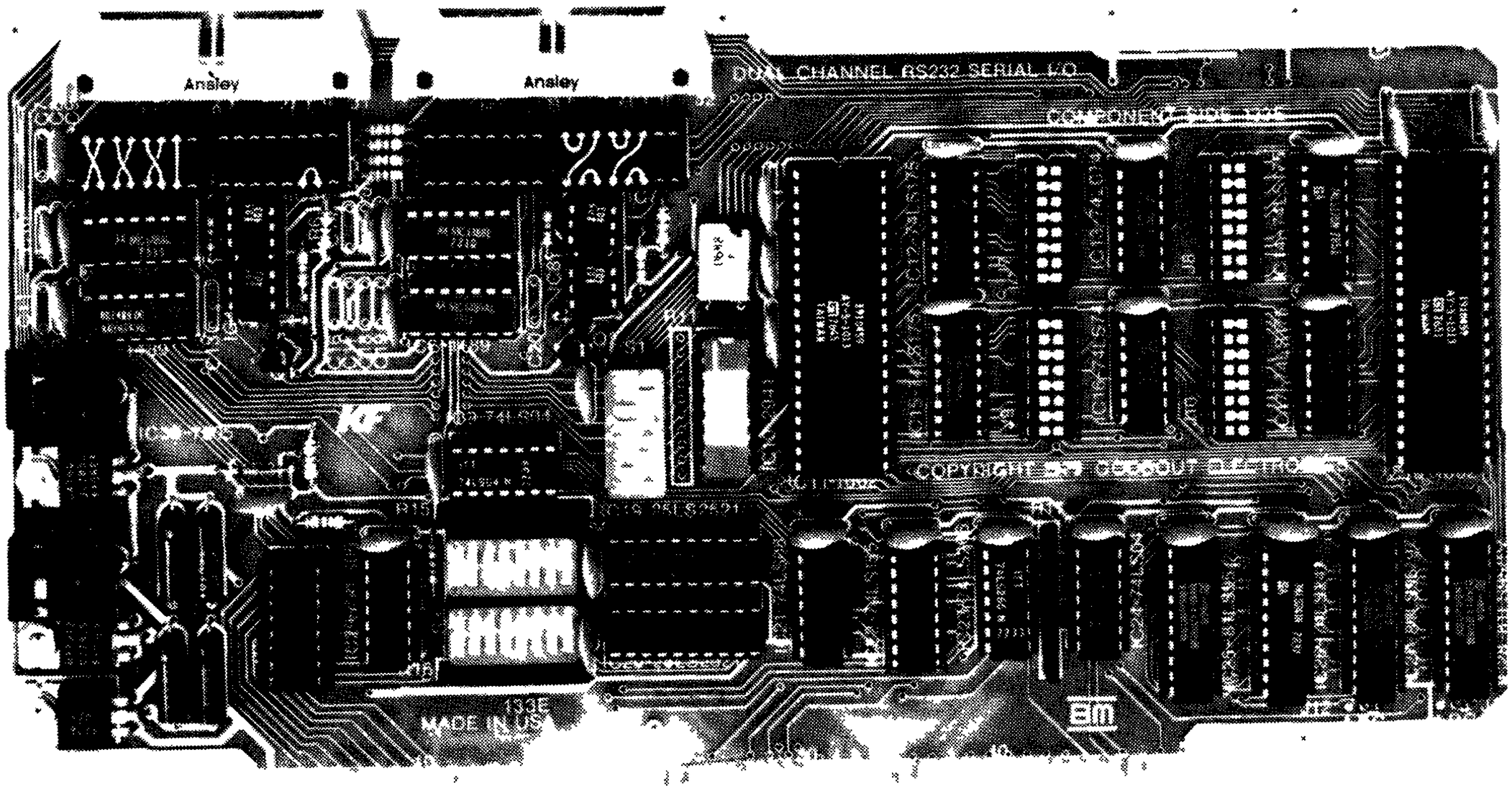


4K x 8 RAM

MANUAL ON PAGE 11

←INTERFACER→™

USER'S MANUAL



IEEE • S-100

Dual Serial RS232C I/O

with full handshake

133G mac

CompuPro™ from GODBOUT

11/80

ABOUT INTERFACER

Congratulations on your decision to purchase the INTERFACER, a dual channel RS-232 serial I/O board designed specifically for full electrical and mechanical compatibility with the IEEE 696/S-100 standard. The S-100 bus is currently one of the most popular in the industry and by far the most prolific. We believe that this board with the rest of the S-100 portion of the CompuPro family, is one of the best boards available for that bus.

Features, such as reliable hardware UARTs, independent channel port selection, crystal controlled dual baud rate generator, full hardware/software programmability, and a convenient interrupt structure allow for maximum flexibility at a reasonable price.

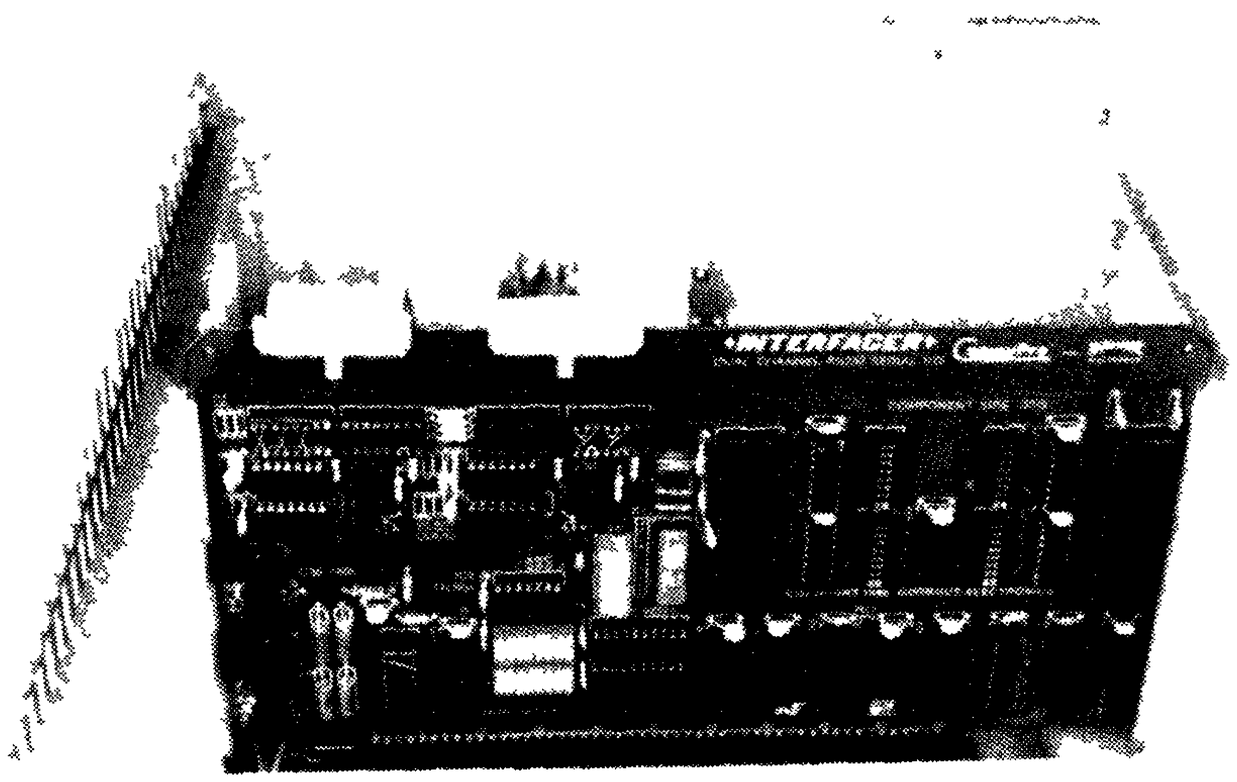
Thank you for choosing a CompuPro product....welcome to the club.

TECHNICAL OVERVIEW

This board incorporates reliable LSI technology UART chips to perform the basic serial-to-parallel and parallel-to-serial conversions necessary for this S-100 dual channel I/O board. By using these UARTs, the CPU is freed of the time consuming drudgery of performing serial I/O operations by software techniques. Because of this, I/O operations are far more reliable and easier to implement.

In addition to the UARTs, several other features are included to make this board extremely flexible and easy to use. These features include an on board crystal controlled dual baud rate generator for reliable baud rates independent of your CPU clock speed, conversion to TTL, current loop and RS-232 levels for interfacing to almost every kind of serial device, and hardware/software programmability for power-on operation and easy parameter modification.

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky TTL and MOS technology integrated circuits for reliably cool operation. All this and sockets for all ICs go onto a double-sided, solder masked printed circuit board with a complete component layout legend.



Shown above is a typical installation using (2) optional Interfacer cable assemblies. These cables consist of an Ansley 609-25S 25 pin "D" connector and an Ansley 609 2601M 26 pin female transition connector.

Individual cable parts or assembled cables in 18 and 30 inch lengths are available from Godbout Electronics

I/O ADDRESS ASSIGNMENT

Each Channel on this board is addressable as a single 2 port block anywhere through the 256 port I/O space. In addition, either or both Channels can be disabled and electrically removed from the I/O space. DIP switch S2 addresses Channel "A" and DIP switch S3 addresses Channel "B". As shipped, both Channels will have the data port residing at the port address, and the status port residing at the port address + 1. If desired, this board may be jumpered so that both Channels have their status ports at the selected address and the data ports at the selected address + 1. This may be accomplished by cutting the trace between points "B" and "C" at J14 (on the solder side of the board) and installing a jumper between points "A" and "B". Both Channels are addressed as follows:

SWITCH POSITION	FUNCTION	
1	ADDRESS A1	
2	ADDRESS A2	
3	ADDRESS A3	"ON" = "0"
4	ADDRESS A4	
5	ADDRESS A5	"OFF" = "1"
6	ADDRESS A6	
7	ADDRESS A7	
8	CHANNEL DIS.	- "ON" = DISABLED
		- "OFF" = ENABLED

Example: To address Channel "A" at the first I/O port address pair 00H and 01H, positions 1 through 7 of switch S2 would be ON and position 8 would be OFF so that the Channel "A" is enabled. This configuration places the data port at 00H and the status port at 01H - assuming that J14 has not been altered from the factory setting.

CONTROL PORT BIT ASSIGNMENT

Outputs to the CONTROL PORT from the CPU are defined as follows:

DATA BIT	NAME	SIGNAL
D0	RxINT E	Receiver interrupt enable
D1	TxINT E	Transmitter interrupt enable
D2	CD	RS232 CD output
D3	CA	RS232 CA output
D4	TSB	Number of stop bits
D5	NP	No parity
D6	EPS	Even parity select
D7	NBI	Number of bit/character

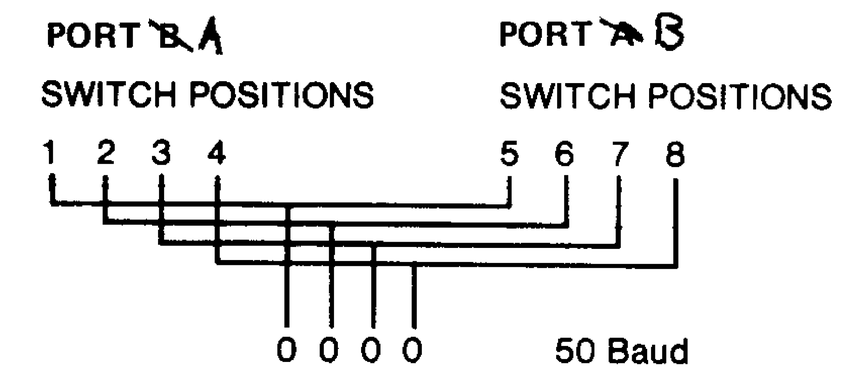
STATUS PORT BIT ASSIGNMENT

Inputs from the STATUS PORT to the CPU are defined as follows:

DATA BIT	NAME	SIGNAL
D0	TBMT	Transmitter buffer empty
D1	DAV	Data available
D2	OPT	Optional status line
D3	PE	Parity error
D4	OR	Over run
D5	FE	Framing error
D6	CC	RS232 CC input
D7	CB	RS232 CB input

BAUD RATE SELECTION

Dip switch S1 is used to select the baud rate for both Channels A and B. Switch positions 1 - 4 set the baud rate for Channel A and positions 5 - 8 set the baud rate for Channel B as shown below.



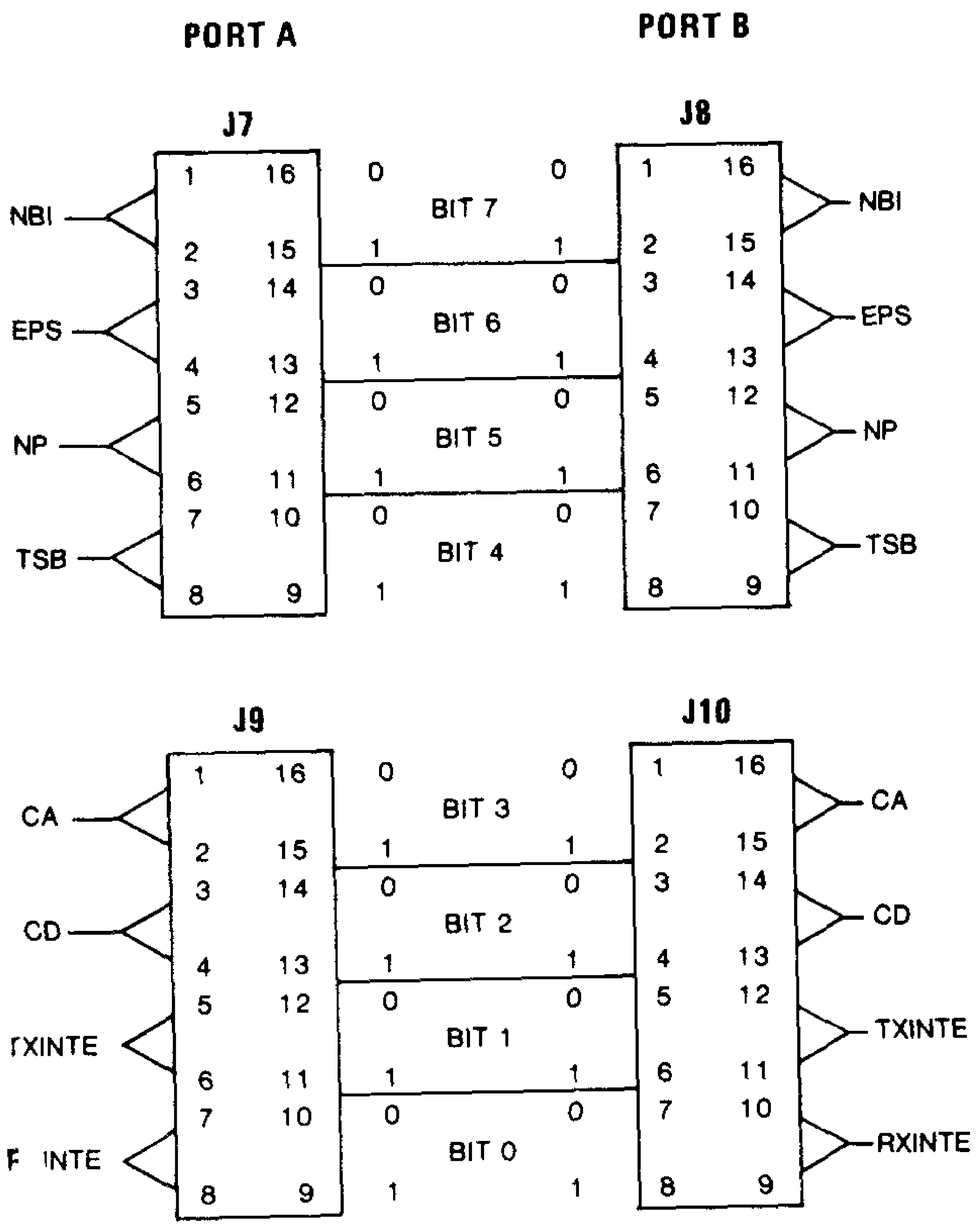
0	0	0	0	50 Baud
1	0	0	0	75 Baud
0	1	0	0	110 Baud
1	1	0	0	134 5 Baud
0	0	1	0	150 Baud
1	0	1	0	300 Baud
0	1	1	0	600 Baud
1	1	1	0	1200 Baud
0	0	0	1	1800 Baud
1	0	0	1	2000 Baud
0	1	0	1	2400 Baud
1	1	0	1	3600 Baud
0	0	1	1	4800 Baud
1	0	1	1	7200 Baud
0	1	1	1	9600 Baud
1	1	1	1	19200 Baud

EXAMPLE: To set Channel "A" to 9600 baud, DIP switch S1 would have position 1 ON and positions 2, 3, and 4 would be OFF. To set Channel "B" to 110 baud, DIP switch S1 would have positions 5, 7, and 8 ON and position 6 OFF.

UART PROGRAMMING

On power-up the control latches are all reset to a defined state as shown below. If the UART parameters for your system configuration are set properly for the reset state, no software initialization is necessary for proper operation of this board. To set the power-up parameters, the proper logic level for the programming header should be chosen from the table and the corresponding header trace should be left intact while the trace with the opposite level should be cut (an X-ACTO knife works great). For example, if odd parity is desired, the table shows that EPS should be a logic "0" and the header diagram indicates that the trace between pins 3 and 14 should remain while the trace between pins 4 and 13 should be cut. NOTE: never leave both traces to a signal line unbroken as this could lead to heating and possible damage to the 74LS175's.

UART PROGRAMMING

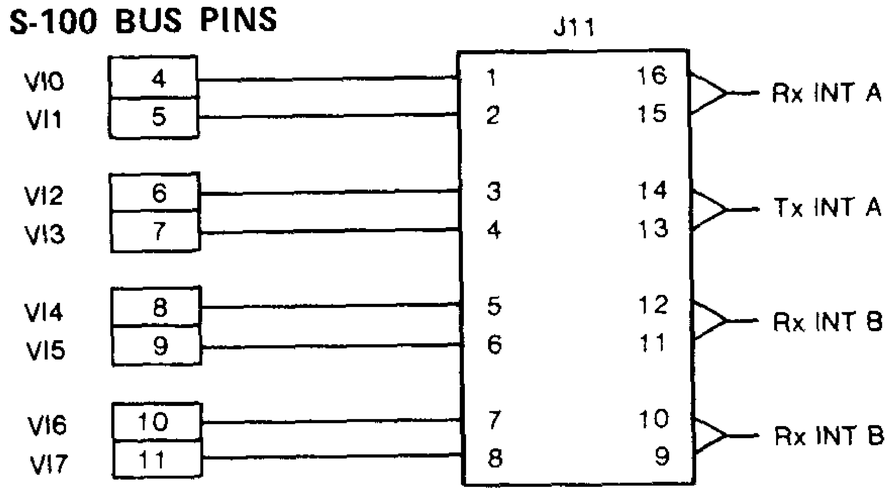


SIGNAL	"0"	"1"
EPS	ODD PARITY	EVEN PARITY
NBI	7 BITS	8 BITS
TSB	1 STOP BIT	2 STOP BITS
NP	PARITY	NO PARITY
TXINTE	DISABLE	ENABLE
RXINTE	DISABLE	ENABLE
CA	SPACING	MARKING
CD	SPACING	MARKING

The state of this board may be altered at any time by outputting a new control word to the Control Port. To change the mask under software control, simply output a "1" to the proper data bit of the Control Port corresponding to the signal that you desire to change. This will flip the logic level of the particular signal to the opposite state (i.e. odd parity will become even parity). Outputting a "0" to a bit will return it to the power-up setting.

VECTORED INTERRUPTS

When enabled and jumpered to the appropriate interrupt pin on the S-100 bus, each port has both a transmit and receive interrupt line. The receive interrupt line (RxINT A or B) is driven low when data is available from the UART and the RXINTE line has been enabled as described in the UART PROGRAMMING section. This line resets to a high impedance state after the data has been fetched from the UART. The transmit interrupt line (TxINT A or B) is driven low when the UART is ready to accept a character from the CPU and the TXINTE line has been enabled as described in the UART PROGRAMMING section. This line resets to a high impedance state when the UART transmitter buffer is full and it cannot accept another character. Note that "sINTA", S-100 bus pin 96, is not monitored by this board and is not needed to implement a useful interrupt scheme.



As with the UART parameters, the vectored interrupts are enabled and disabled as described previously. Outputting a "1" to bits 0 or 1 will disable an enabled interrupt or enable a disabled interrupt. Outputting a "0" will return them to their power-up or reset setting.

SERIAL MODE JUMPERS

The INTERFACER board with its unique serial programming jumpers, allows the user to adapt his board to all standard RS-232 pin configurations and to non-standard current loop configurations. In current loop mode, this board may be set to use the on board current source or an external current source. For example, a teletype requires that the on board current source be used, so the serial mode jumpers (J3/J5 and J4/J6) should be set like the example shown on the following page.

In RS-232 mode, these jumpers may be set so that this board operates in a "master" mode where it behaves as the Data Terminal Equipment (DTE), or it may be set so that the board operates in a "slave" mode where it behaves as the Data Communication Equipment (DCE). Since almost all CRT terminals and serial interface printers operate as the "master" or as the Data Terminal Equipment, then the INTERFACER board must operate as the "slave" or Data Communication Equipment. For example, to connect the INTERFACER to a terminal like an ADM 3A or a Hazeltine, the serial mode jumpers (J3/J5 and J4/J6) should be set in "slave" mode as shown on the following page. To connect the INTERFACER to a Modem is a different set-up because Modems are set to operate as "slaves". When connected to a Modem, the INTERFACER should be set in the "master" mode as shown on the following page.

RS-232C CONTROL LINES

The RS-232 control and data lines are defined as shown below.

PIN#	CIRCUIT	DIR.	DESCRIPTION
1	AA		PROTECTIVE GROUND
2	BA	TO DCE	TRANSMITTED DATA
3	BB	TO DTE	RECEIVED DATA
4	CA	TO DCE	REQUEST TO SEND
5	CB	TO DTE	CLEAR TO SEND
6	CC	TO DTE	DATA SET READY
7	AB		SIGNAL GROUND
8	CF	TO DTE	REC'D LINE SIGNAL DET.
20	CD	TO DCE	DATA TERMINAL READY

Four hardwired RS-232 handshaking signals are provided for interfacing to equipment needing these lines as shown below. These lines may be set to power-up either marking or spacing, and their state may be altered by software commands as described in the UART PROGRAMMING Section.

OUTPUT LINES

DATA BIT	RS-232 LINE	DB25 PIN CONNECTION
D2	CD	20 OR 6 *
D3	CA	4 OR 5 *

INPUT LINES

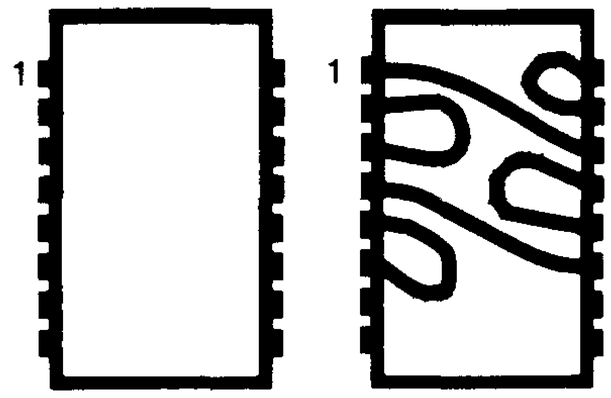
DATA BIT	RS-232 LINE	DB25 PIN CONNECTION
D6	CC	6 OR 20 *
D7	CB	5 OR 4 *

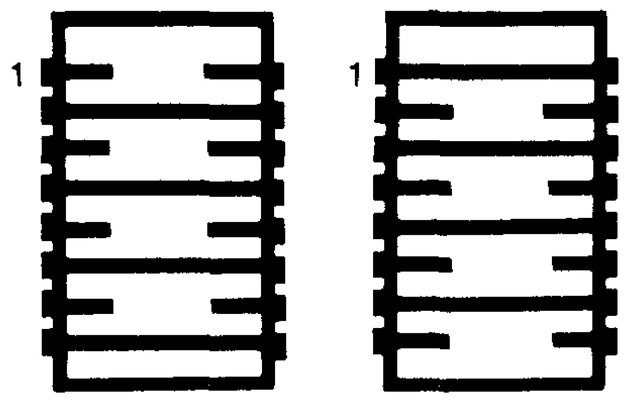
NOTE: Non-starred pin numbers indicate the DB25 pin number when the Serial Mode Jumpers are set for "master" mode. The starred pin numbers indicate the DB25 pin number when the Serial Mode Jumpers are set for "slave" mode.

One optional input line (CF or Rec'd Line Signal Detect) is provided at locations J12 for Channel A and J13 for Channel B. If point "B" is jumpered to point "A", this line will appear on Status Bit D2. By jumpering point "B" to point "C", the "End of Character" output (EOC) from the UART will appear on Status Bit D2.

TYPICAL PROGRAMMING JUMPERS

Current loop - on board current sources EXAMPLE TTY

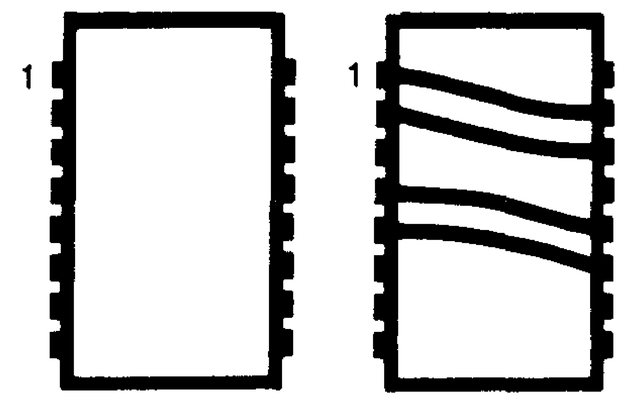


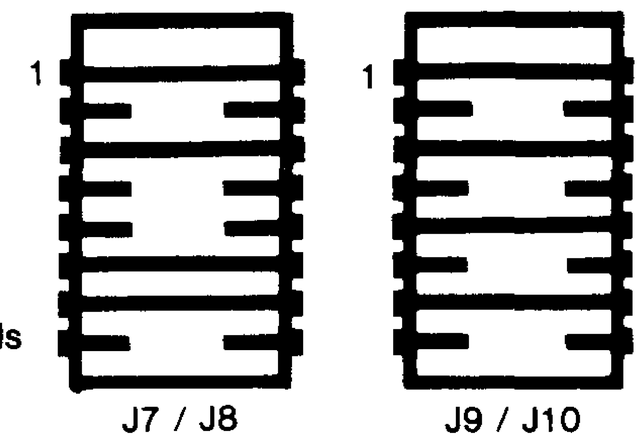


This configuration yields

Even parity
8 data bits
2 stop bits
No parity
Interrupts disabled

Current loop - external current sources

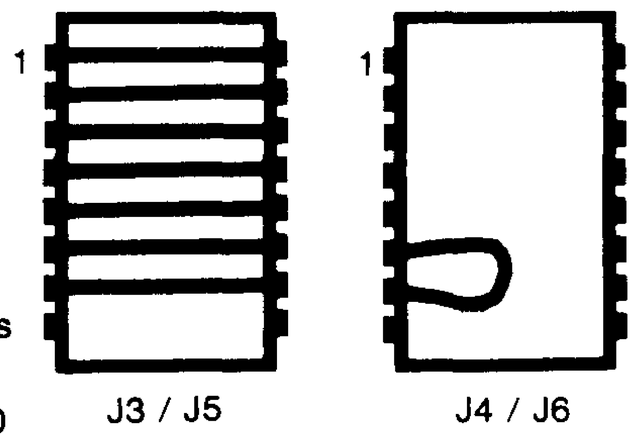




This configuration yields

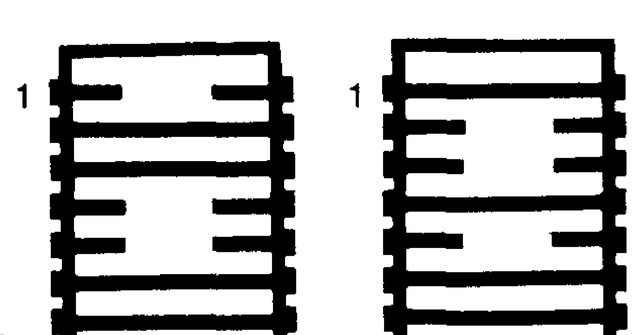
Odd parity
7 data bits
1 stop bit
No parity
Interrupts disabled

RS - 232C - Master mode EXAMPLE Modem



This configuration yields

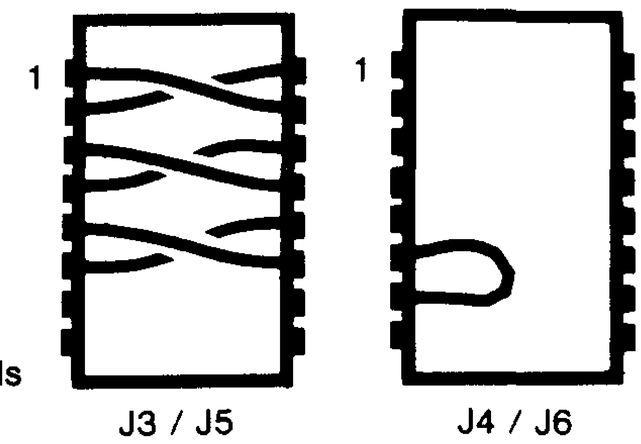
CA "spacing" on pin 4
CD "marking" on pin 20
BA (Tx data) on pin 2
BB (Rx data) on pin 3
CB Status to I/O board on pin 5
CC Status to I/O board on pin 6
CF (Received line signal detector on pin 8)



This configuration yields

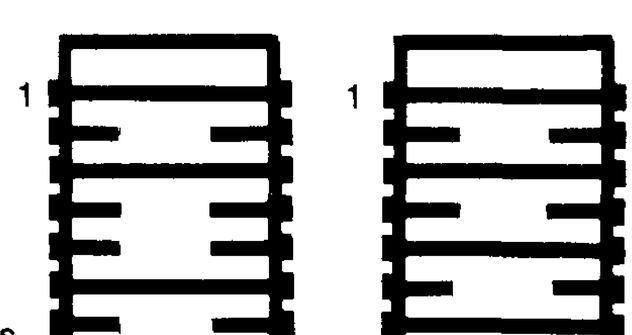
Odd parity
8 data bits
1 stop bit
No parity
Tx Inte enabled
Rx Inte disabled

RS - 232C - Slave mode EXAMPLE CRT Terminal, printer



This configuration yields

CA "spacing" on pin 5
CD "spacing" on pin 6
BA (Tx data) on pin 3
BB (Rx data) on pin 2
CB Status to I/O board on pin 4
CC Status to I/O board on pin 20



This configuration yields

Odd parity
7 data bits
2 stop bit
No parity
Interrupts disabled

BOARD POWER UP AND TESTING

Now the fun part before you install the board in your system, take the time to check these few things over

1 _____ ARE ALL IC S PROPERLY INSERTED?

2 _____ ARE THE BAUD RATE SWITCHES SET TO THE PROPER BAUD RATE FOR YOUR TERMINAL?

3 _____ ARE THE PORTS YOU WANT TO USE PROPERLY ADDRESSED AND ENABLED?

4 _____ IF YOU DON T WANT TO USE A PORT IS IT DISABLED?

5 _____ ARE THE HARDWARE/SOFTWARE PROGRAMMING JUMPERS SET THE WAY YOU REALLY WANT THEM?

6 _____ ARE YOU SURE YOU AREN T TYING TWO OR MORE OF THE PROGRAMMING OUTPUTS TOGETHER?

7 _ ____ ARE THE INTERRUPT JUMPERS SET TO THE PROPER INTERRUPT LINE OR ARE THEY COMPLETELY REMOVED IF NOT BEING USED?

8 _____ IF USING CURRENT LOOP ARE THE PROGRAMMING LINES SET PROPERLY FOR USING EITHER THE ONBOARD CURRENT SOURCE OR THE EXTERNAL SOURCE? (SEE FIGURES A AND B)

9 _____ IF USING RS232 ARE THE PROGRAMMING LINES SET PRO PERLY FOR MASTER OR SLAVE MODE? (SEE FIGURE C AND D)

10 _____ ARE THE OPTION JUMPERS SET THE WAY YOU WANT?

If you have answered 'YES to all of the above - you are ready to proceed

It s now time to power up your board With the power on, verify that the voltages specified earlier are still at their proper levels and that no chips are getting excessively hot (U1, U2, U5, U6 and U10 should be warm) If everything is OK up to this point, enter the I/O board testing routine via either front panel switches or editor/assembler

If the I/O board is working, characters typed on the terminal will be echoed back

I/O BOARD TESTING ROUTINE

THIS PROGRAM INPUTS CHARACTERS FROM A TERMINAL DEVICE AND ECHOES THEM BACK

```
0000              0000 *
0000              0010 *
0000              0020 *
0000              0030 *
0000              0040 *
0000              0050 CONTROL EQU  01H      CONTROL PORT ADDRESS
0000              0060 STATUS  EQU  01H      STATUS PORT ADDRESS
0000              0070 DATA    EQU  00H      DATA PORT ADDRESS
0000              0080 *
0000              0090 *
0000              0100         ORG  0000H
0000              0110 *
0000 3E 00        0120 START   MVI  A 00H    INITIALIZE THE
0002 D3 01        0130         OUT  CONTROL  CONTROL PORT
0004 DB 01        0140 BEGIN   IN   STATUS   INPUT STATUS AND
0006 E6 02        0150         ANI  02H      MASK FOR DAV
0008 CA 04 00     0160         JZ   BEGIN    IF NOTHING/CHECK AGAIN
000B DB 00        0170         IN   DATA     IF DAV  1  INPUT DATA AND
000D 47           0180         MOV  B A      MOVE TO REGISTER B
000E DB 01        0190 LOOP    IN   STATUS   INPUT STATUS AND
0010 E6 01        0200         ANI  01H      MASK FOR TBMT
0012 CA 0E 00     0210         JZ   LOOP     IF NOT READY  CHECK AGAIN
0015 78           0220         MOV  A B      IF TBMT  1  MOVE DATA INTO
0016 D3 00        0230         OUT  DATA     REGISTER A  THEN OUTPUT
0018 C3 04 00     0240         JMP  BEGIN    JUMP FOR NEXT CHARACTER
```

TROUBLESHOOTING

Assuming that your board is having problems and the testing program is not running - *DON T PANIC!!!* A logical approach to troubleshooting will show you that an I/O board is nothing to be frightened of To troubleshoot this board you will either need a scope or a logic probe A frequency counter is handy too

1 Verify that the Baud rate you want is being delivered to the UART With a scope or frequency counter measure the frequency at pins 40 and 17 of the UART Remember that the UART needs a 16x clock so the frequency will be 16 times the Baud rate

example 1200 Baud x 16 = 19 2 KHz
for people with scopes

$$\text{Frequency (Hz)} = \frac{1}{\text{cycle period (seconds)}}$$

2 Verify with scope or logic probe that data reaches pin 20 of the UART when you type a character on your terminal If not - trace back and see where it s being lost

3 Verify that the status bit DAV (pin 19 of the UART) goes high after striking a character from the terminal If it does not and data is getting to the UART you may have a bad UART

4 Verify that your computer is getting the status of the board by running a simple program like the one below

```
LOOP    IN   STATUS   (your status port)
        JMP  LOOP
```

Verify that the line SWE (A or B) pulses low while this program is running (pins 1 and 19 of the status gate U11 or U19) and that the data is getting onto the buss from the buss driver U30 as pin 1 and 19 pulse low and high respectively

5 Verify that the programming latches (U12, 14 15, 17) and the UARTS are receiving their control strobes when the following program is run

```
LOOP    OUT  CONTROL   (your control port)
        JMP  LOOP
```

The line CS (A or B) should strobe low while this program is running (check pin 9 of U12 and U15 *or* U14 and U17)depending on which channel you are currently strobing

6 Verify that data is reaching the UARTS from the host computer by running the following program and observing pin 34 of the UARTS (DS, A or B) strobes low *note* only garbage will be transmitted

```
LOOP    OUT  DATA     (your data port)
        JMP  LOOP
```

7 Verify that data is reaching the computer from the UARTS by running the following program and observing that RDE (A or B) strobes low (pins 4 and 18 of the UARTS) and that pins 1 and 19 of U26 strobe low and high respectively

```
LOOP    IN   DATA     (your data port)
        JMP  LOOP
```

8 Verify that serial data is exiting from UART pin 25 and that it is propigated to the output connector pin through the output level translators (test this while running the I/O board testing routine)

9 If you don t seem to be getting any of the above mentioned control strobes check that either pin 1 of U22 is strobing high or pin 15 is strobing low when running any of the above programs If not either the address is set wrong or there is a defective switch IC or board in the I/O address decoding circuitry Also pin 2 and 14 of U22 should be strobing low to indicate either a pDBIN or PWR

CIRCUIT DESCRIPTION

The heart of this serial I/O board is a MOS/LSI UART similar to the TR1602-B or the TR1863 by Western Digital. These UARTs perform the complete parallel-to-serial and serial-to-parallel conversion, error detection and serial format modification necessary for reliable and flexible serial communication.

This I/O board can be roughly divided into seven major sections; I/O Port Select Logic, Bus Driver Logic, Hardware/Software Programming Logic, Baud Rate Select Logic, Interrupt Logic, Serial Line Level Conversion Logic, and the UARTs.

I/O PORT SELECT LOGIC

Address lines A7-A1 each feed into one input of the 25LS2521 octal comparators (U19, U20) with the other input connected to one switch position of the port select DIP switch. The output of the comparator is gated with the I/O detect logic consisting of X-NOR gate (U23) on sINP and sOUT. When an I/O operation is decoded, and the selected address is on the bus, the control line decoder (U22) is enabled and the proper control signal is output to the UARTs dependent on the 2 select inputs, address A0, and sOUT, and when either pDBIN or pWR* occurs. At the same time, board enable is decoded and the input buffer (U25) is enabled or disabled with sINP.

BUS DRIVER LOGIC

In this section, there will be reference to 2 different buses, the S-100 bus and the internal bi-directional board bus.

The S-100 Data Out line (DO0-DO7) are buffered through octal buffer U25 to drive the internal board bus, which presents the S-100 bus information to the UARTs and the Hardware/ Software Programming Logic to be latched when the processor is not performing an input operation.

The S-100 Data In lines (DI0-DI7) are driven by the 74LS241 octal bus driver (U26) from the internal board bus. The board bus is driven by the UARTs for data and the 81LS95/97 status control buffers. This bus is a TRI-STATE bus, and therefore only one device (either the UARTs or the status buffers) controls the bus at any one time.

HARDWARE/SOFTWARE PROGRAMMING LOGIC

The Hardware/Software Programming Logic consists of U12, U15, J7, and J9 for Channel A and U14, U17, J8 and J10 for Channel B along with one AND gate (U21) and two inverters (U24) for the reset logic. On power-up and reset, all sixteen of the quad 'D' latches (74LS175- U12, U14, U15, U17) are cleared by either power on clear (POC*) or reset (pRESET*). This establishes defined levels on one side of each of the jumper sockets (J7, J8, J9 and J10) which can be wired to each of the four signals on the opposite side of the jumper socket. Since the latches bring out both Q and Q* outputs, each of the 8 control lines per Channel has its own control bit and each bit is brought out both inverted and non-inverted at the same time. This allows each of the control bits to be set either high or low for the particular system configuration needed on power-up. By outputting a '1' to any of the control bits, the particular control line's level will be inverted. This occurs when the clock inputs of the control latches are toggled by the I/O decoder (U22) causing the current data bus data to be latched. This new data causes the jumper sockets levels to change and the control bit to change along with them. One note of caution: NEVER never wire any output of a latch to another latch output or leave both programming shunts unbroken as this could lead to heating and possible damage to the 74LS175s.

BAUD RATE SELECT LOGIC

The Baud Rate Select Logic is by far the simplest section of the board. The complete circuitry consists of the baud rate generator (BR2941-L or BR1941-L, U10), a 5.0688 MHz crystal (X1), DIP switch S1, and the resistor/ zener minus 5 volt regulator (R12 and D3). The baud rate generator contains a crystal oscillator and two programmable dividers to obtain the two independant baud clocks for the UARTs (CLKA and CLKB). The baud rate is set in a binary fashion on DIP switch S1 with positions 1 - 4 for Channel A and positions 5 - 8 for Channel B. Resistor R12 and zener diode D3 provide the - 5 volt substrate bias for the BR2941-L (not needed for the BR1941-L). NOTE: Holes for SIP R11 have been provided in the event that a baud rate generator without internal pullups is provided. R11 will only be provided if needed.

INTERRUPT LOGIC

The interrupt logic consists of four AND gates (U16) and four open collector inverters (U29). When a particular interrupt has been enabled by bringing the necessary enable bit high either by power-up programming or altering the mask under software control, the AND gates can pass their status onto the inverters. When either the Data Available (DAV) or Transmitter Buffer Empty (TBMT) signals go high from the UART, this level is passed by the AND gates to the inverters. The high level on the inverter input pulls the output out of the high impedance state and drives the bus low. The processor acknowledges this interrupt by either reading from or writing data to the UART, which returns the inverter output and the bus line to the high impedance state.

SERIAL LINE LEVEL CONVERSION LOGIC

The Level Conversion Logic consists of two main parts; the RS232 - TTL level converters and the current loop and TTL level converters. Since both Channels are the same, we will only discuss Channel A. All the signals from the Channel A connector (J1) are brought out to jumper sockets J3 and J4 for user programming.

All RS232 level signals are taken from J3 and are either fed from or fed to the two level converters U1 and U2 (1488 - 1489). The 1488 converts TTL level signals to the +12 and -12 volt levels of an RS232 line. Holes for disc capacitors (C7-C9 and C14-C16) are provided on the outputs of these drivers to limit slew rate to less than 30V/uSEC for compatibility with the EIA RS-232-C specifications. For very short cable lengths, you might want to install disc caps with a value no greater than 400pf. For very long cables, we advise that no caps be installed due to the cable capacitance already limiting slew rate. The 1489 converts the RS232 levels back to TTL levels for the UARTs and the status bits. Holes are provided on the board for adding the response control capacitors (C10-C13 and C17-C20) for increased noise immunity.

The current loop and TTL signals all enter and exit through J4. The +IN and -IN signals are designed to feed opto-isolator U3 either through the on board current source (R2) or directly from an external current source. The output of the opto-isolator is combined with the TTL IN signal, inverted (U9) and ANDed (U21) with the level converted RS232 data and fed to the UART (U11) via SIA. Transmit data "A" (TxDA) is inverted (U29), fed through the jumper socket J4 to the TTL out line, and drives the LED of opto-isolator U4. The output of U4 is buffered by transistor Q1 (with diode D1 to clip negative spikes) and fed to J4 where it user either the internal current source (R1) or an external source and drives the +OUT and -OUT lines.

UARTs

The UARTs (U11, U18) take the data from the internal board bus, the serial parameters from the Hardware/Software Programming Logic, The baud clock from the Baud Rate Select Logic and the control signals from the I/O Port Select Logic and outputs serial data to the Serial Line Level Conversion Logic.

The UARTs also take serial data from the Conversion Logic and with the previously mentioned sections yield data and status to the internal board bus for driving the S-100 bus. In summary, as stated at the beginning of this section, the UARTs are the heart of this board.

Parts List

Upon receipt of your kit, check your parts against the list below

☐ 1 - Circuit board

INTEGRATED CIRCUITS (NOTE: the following parts may have letter suffixes & prefixes along with the key numbers given below.)

☐ 2 - TR1602-B or AY-5-1013 UARTs (U11, U18)
☐ 1 - BR2941-L or BR1941-L Baud rate generator (U10)
☐ 2 - 1488/75488 TTL to RS232 converter (U1, U5)
☐ 2 - 1489/75489 RS232 to TTL converter (U2, U6)
☐ 1 - 74LS241 octal buss driver (U26)
☐ 1 - 81LS95 octal buss driver (U25)
☐ 2 - 81LS95/97 octal buss driver (U27, U28)
☐ 4 - 74LS175 quad "D" latches (U12, U14, U15, U17)
☐ 1 - 74LS266 quad X-NOR with o.c outputs (U23)
☐ 1 - 74LS05 hex o c inverter (U29)
☐ 2 - 74LS04 hex inverters (U9, U24)
☐ 1 - 74LS155 decoder (U22)
☐ 2 - 25LS2521 octal comparators (U19, U20)
☐ 2 - 74LS74 dual "D" flip flop (U13, U16)
☐ 1 - 74LS08 quad 2 input AND (U21)
☐ 4 - MCT-2 or similar opto-isolator (U3, U4, U7, U8)
☐ 1 - 7805 positive 5V regulator (U30)
☐ 1 - 7812 positive 12V regulator (U32)
☐ 1 - 7912 negative 12V regulator (U31)

OTHER ELECTRONIC COMPONENTS

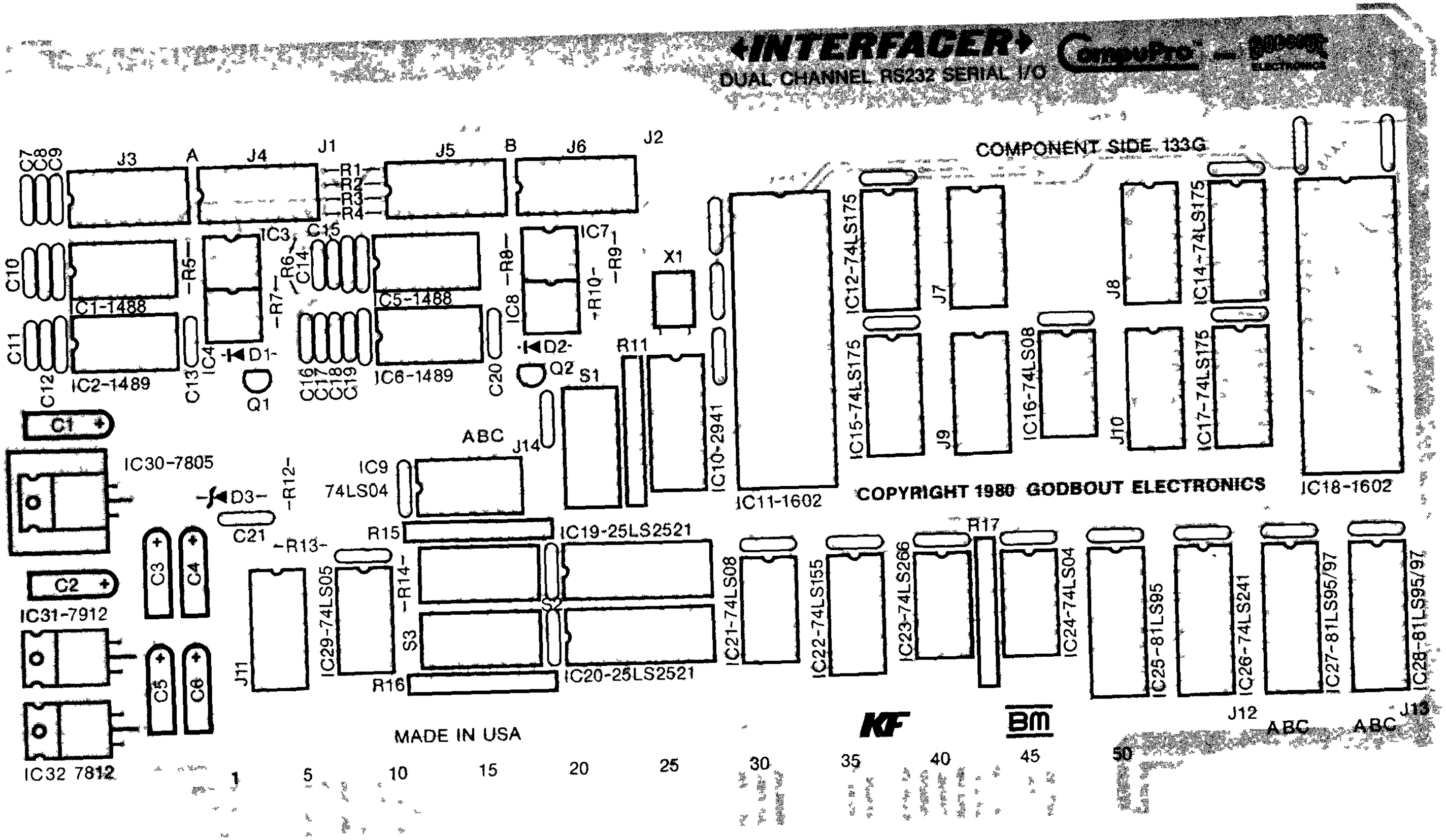
☐ 2 - NPN transistors (Q1,Q2)**
☐ 2 - Signal diodes, 1N914, 809-36 or similar (D1,D2)**
☐ 1 - 5V zener diode, 1N751A or similar (D3)**
☐ 4 - Single inline resistor packs (R11,* R15, R16, R16)**
☐ 4 - 560 ohm ¼ watt resistors (R1, R2, R3, R4)**
☐ 2 - 470 ohm ¼ watt resistors (R5, R8)**
☐ 2 - 4 7K ohm ¼ watt resistors (R7, R10)**
☐ 5 - 2 7K ohm ¼ watt resistors (R12, R13, R14, R6, R9)**
☐ 1 - 5 0688 MHz crystal (Z1)
† ☐ 2 - 39uF 10V tantalum capacitors (C1, C2)
† ☐ 4 - 1 8uF 35V tantalum capacitors (C3, C4, C5, C6)
☐ 31 - ceramic disc bypass capacitors**

MECHANICAL COMPONENTS

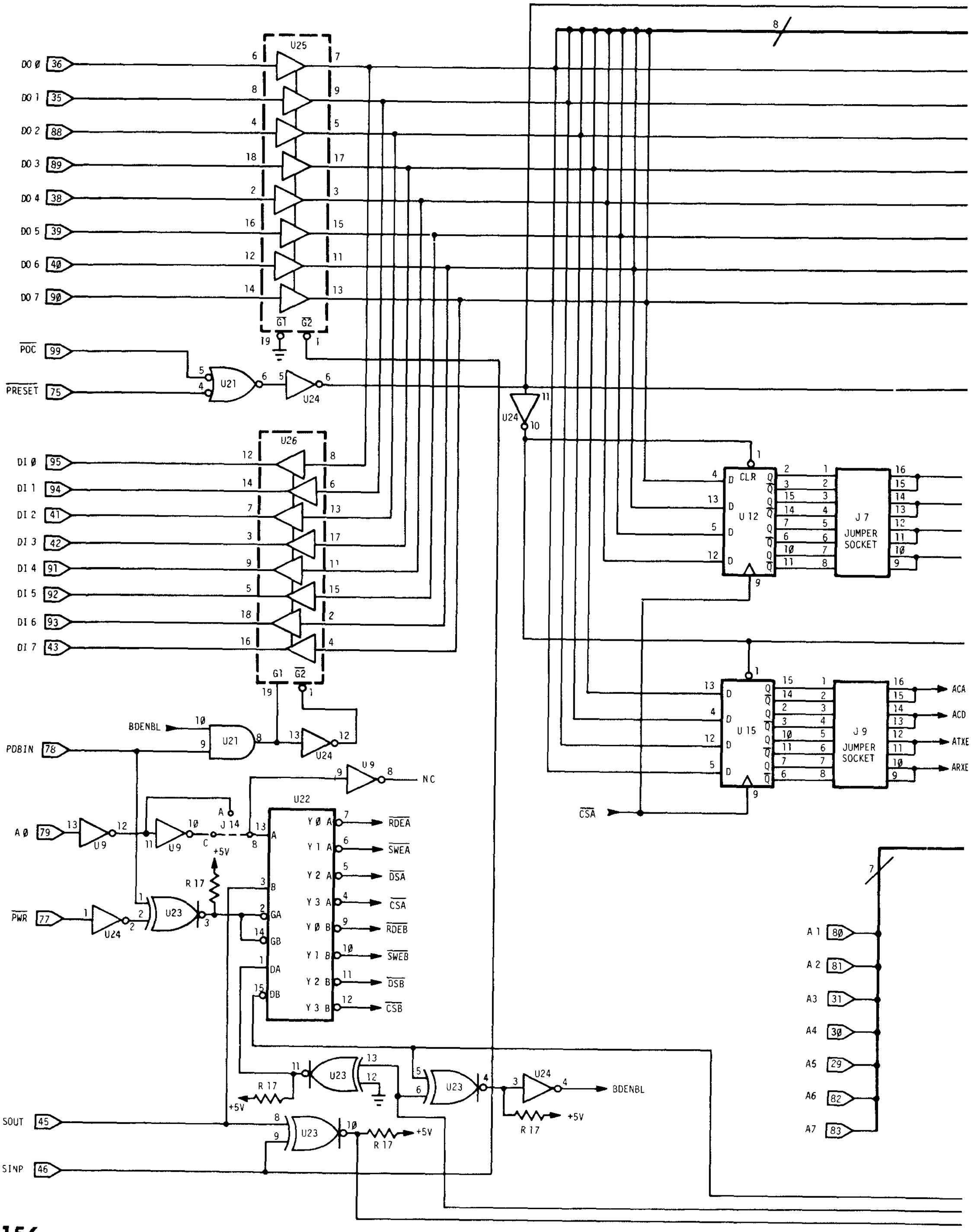
☐ 36- low profile sockets**
☐ 3 - 8 pole DIP switches**
☐ 1 - heat sink for U30
☐ 3 - sets of 6-32 hardware
☐ 2 - 26 pin I/O connectors
☐ 5 - 16 pin DIP platforms
☐ 4 - 16 pin AMP dip shunts
☐ 1 - Instruction booklet

*Note R11 may not be installed or needed on some boards
**Supplied already soldered to the board

† NOTE: Line changes



Component Layout


U25
DO Ø 36
DO 1 35
DO 2 88
DO 3 89
DO 4 38
DO 5 39
DO 6 4Ø
DO 7 9Ø
G1 G2
POC 99
PRESET 75
U21
U24
U26
DI Ø 95
DI 1 94
DI 2 41
DI 3 42
DI 4 91
DI 5 92
DI 6 93
DI 7 43
BDENBL
PDBIN 78
U9
NC
U22
A Ø 79
J 14
+5V
R 17
PWR 77
U23
RDEA
SWEA
DSA
CSA
RDEB
SWEB
DSB
CSB
SOUT 45
SINP 46
BDENBL
U12
CLR
J 7
JUMPER SOCKET
U 15
J 9
ACA
ACD
ATXE
ARXE
A 1 8Ø
A 2 81
A3 31
A4 3Ø
A5 29
A6 82
A7 83

U 11
UART A
1602
AY 5 1013
OR SIMILAR

U 18
UART B
1602
AY 5 1013
OR SIMILAR

U 27
U 28
U 14
U 17
J8 JUMPER SOCKET
J 10 JUMPER SOCKET
J 12
J 13
U 19
25LS2521
U 20
25LS2521
U 10
2941
1941
OR SIMILAR
R 12
R 15
R 16
S 1
S 2
S 3
D3

DAVA
TBMTA
ACB
ACC
OPA
SWEA
RDFA
TXDA
SIA
+5V
12V
CLKA

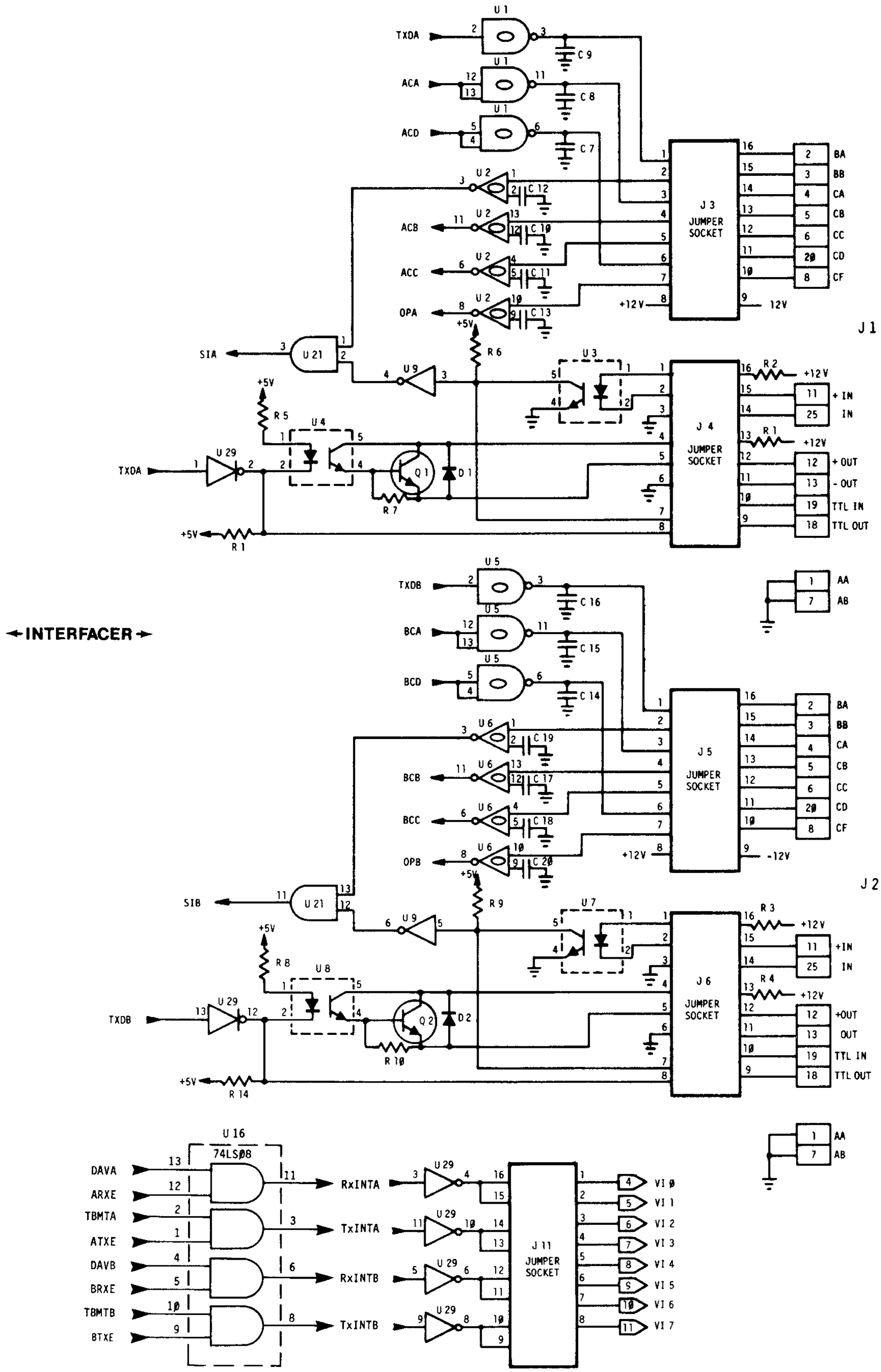
DAVB
TBMTB
BCB
BCC
OPB
SWEB
RDFB
TXDB
SIB
CLKB

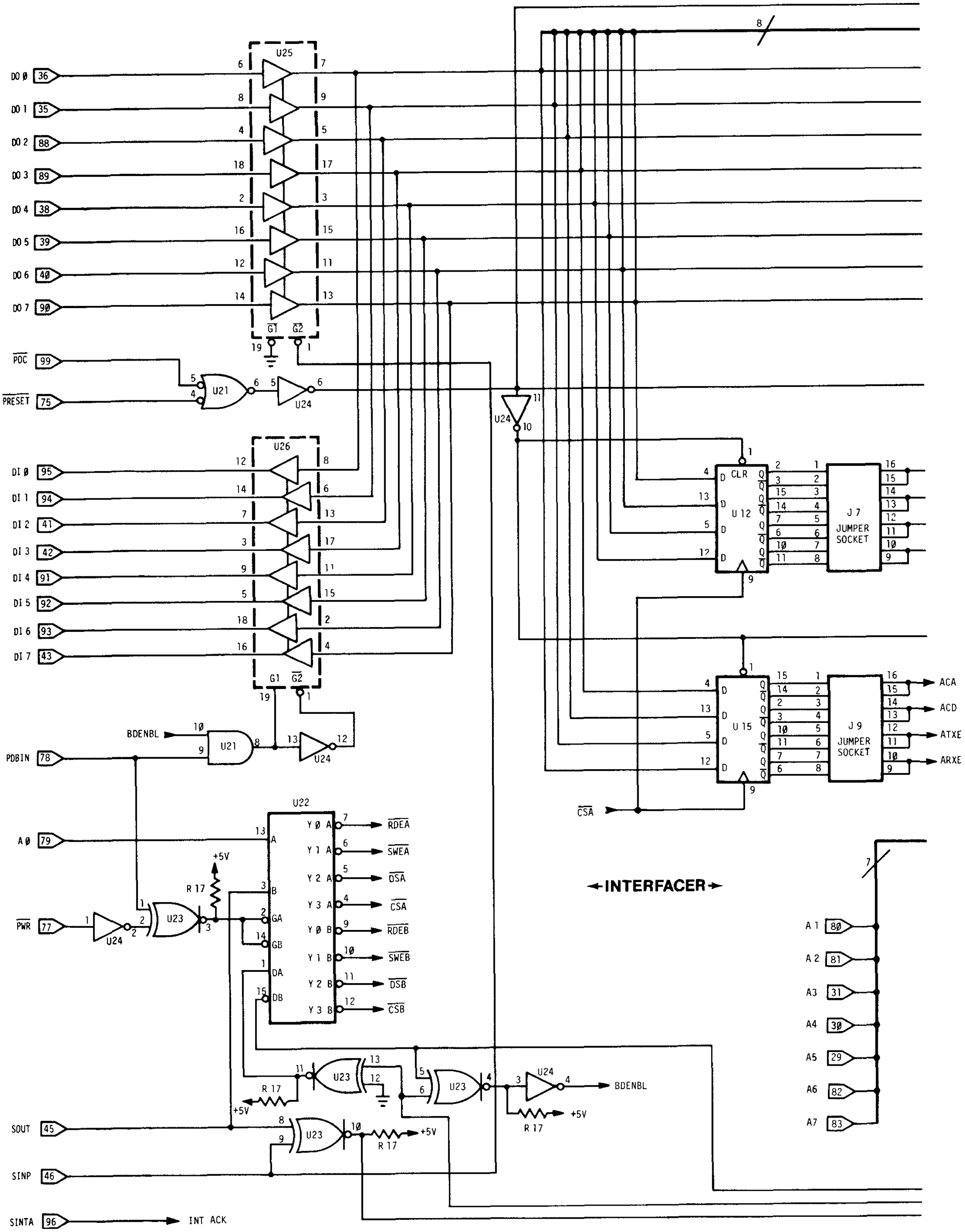
BCA
BCD
BTXE
BRXE

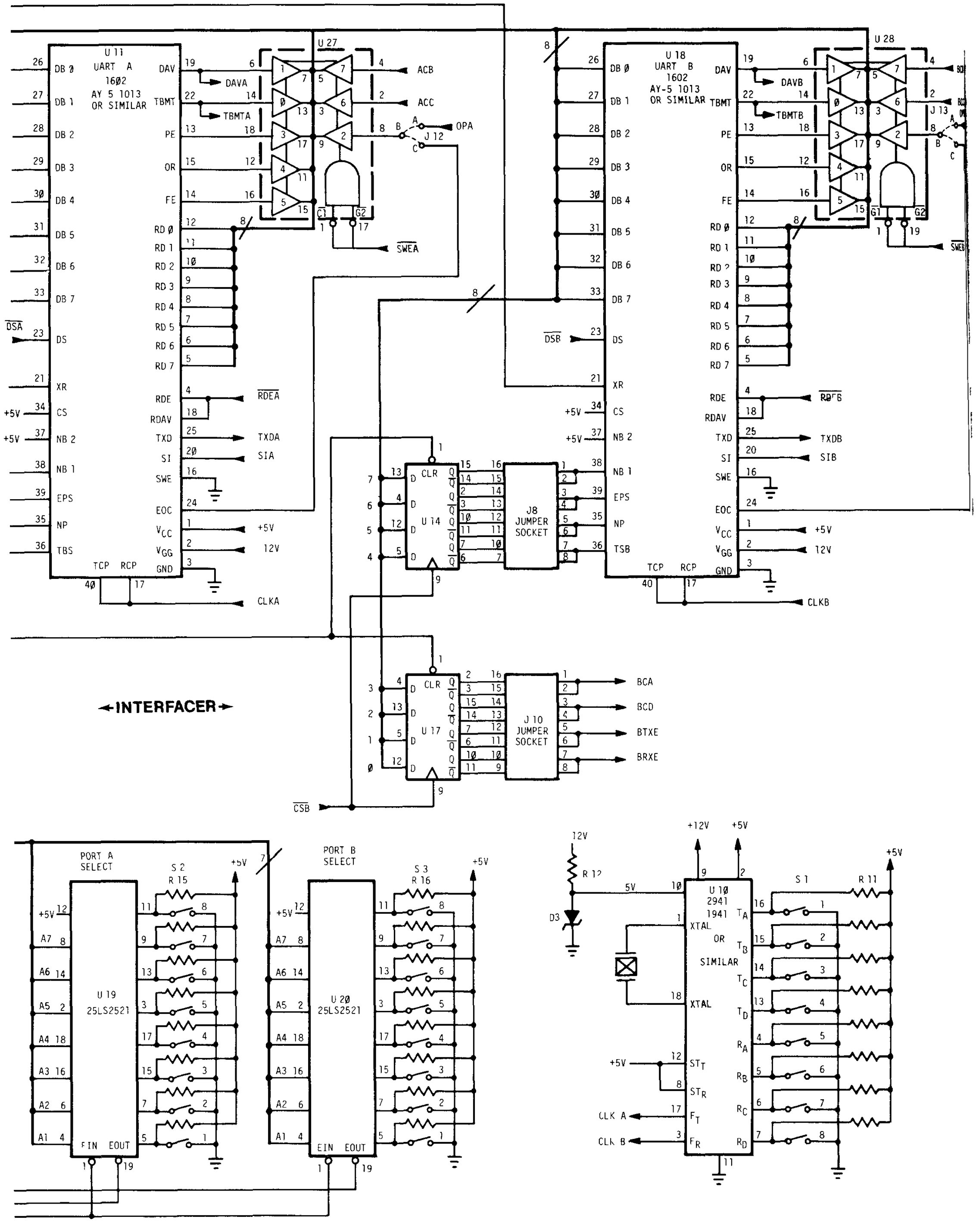
DSA
DSB
CSB

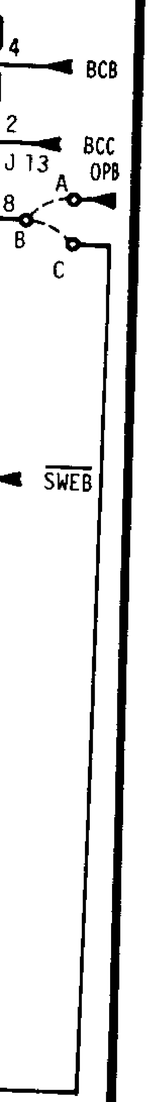
PORT A SELECT
PORT B SELECT

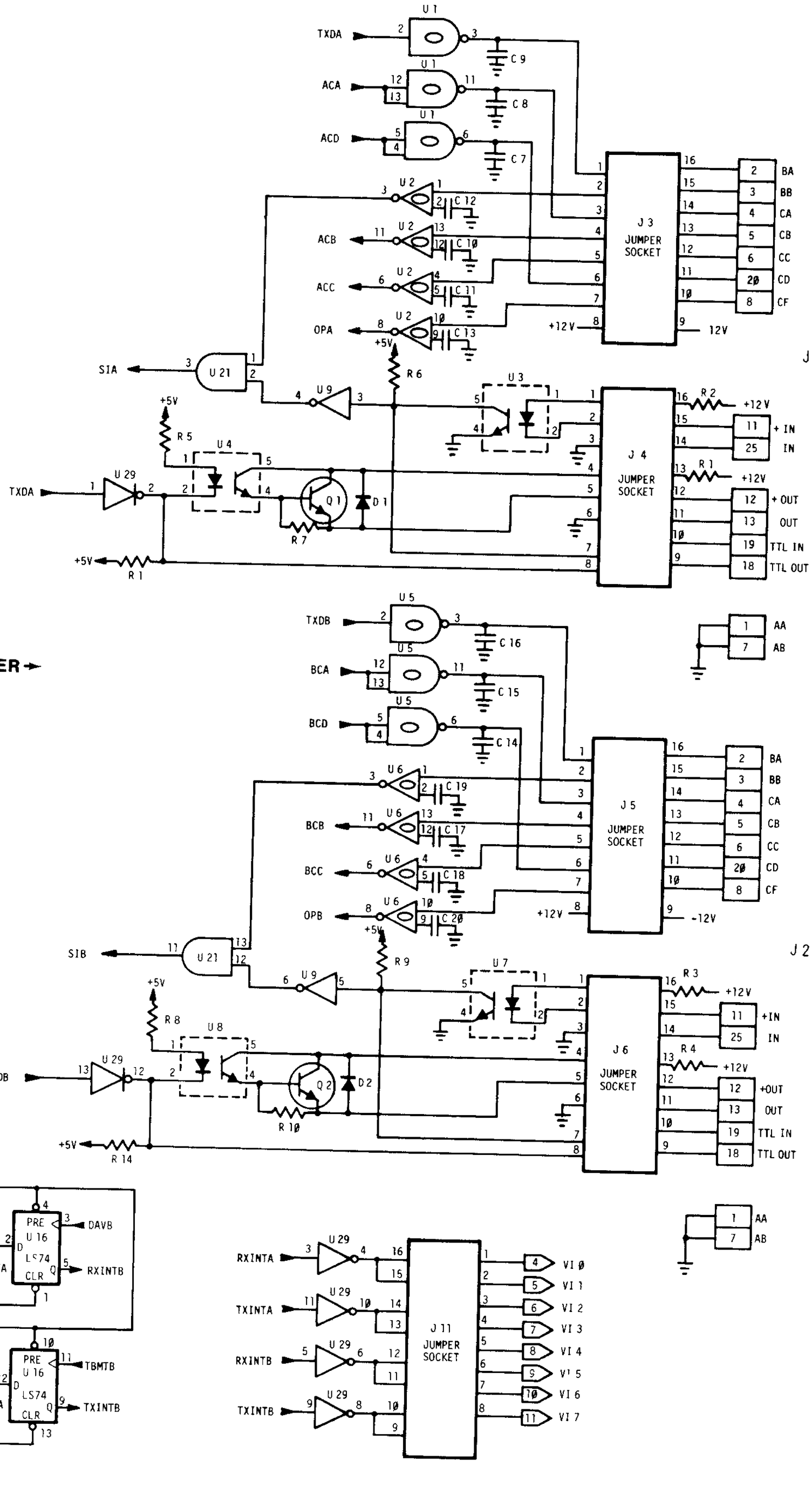
CLK A
CLK B


U 1
TXDA
ACA
ACD
C 9
C 8
C 7
U 2
ACB
ACC
OPA
C 12
C 10
C 11
C 13
+5V
R 6
SIA
U 21
U 9
J 3
JUMPER SOCKET
+12V
12V
BA
BB
CA
CB
CC
CD
CF
J 1
U 3
U 4
U 29
R 5
R 7
Q 1
D 1
R 1
R 2
R 4
+IN
IN
+OUT
- OUT
TTL IN
TTL OUT
J 4
POC
PRESET
DO Ø
DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
DI Ø
DI 1
DI 2
DI 3
DI 4
DI 5
DI 6
DI
PDBI
A
SC
S
SI
INTERFACER
U 5
TXDB
BCA
BCD
C 16
C 15
C 14
U 6
BCB
BCC
OPB
C 19
C 17
C 18
C 20
SIB
U 21
U 9
R 9
U 7
U 8
U 29
R 8
R 10
Q 2
D 2
R 14
R 3
R 4
+IN
+OUT
OUT
J 5
J 6
J 2
AA
AB
U 16
74LSØ8
DAVA
ARXE
TBMTA
ATXE
DAVB
BRXE
TBMTB
BTXE
RxINTA
TxINTA
RxINTB
TxINTB
J 11
JUMPER SOCKET
VI Ø
VI 1
VI 2
VI 3
VI 4
VI 5
VI 6
VI 7


U25
DO Ø 36
DO 1 35
DO 2 88
DO 3 89
DO 4 38
DO 5 39
DO 6 4Ø
DO 7 9Ø
G1 G2
POC 99
PRESET 75
U21
U24
U26
DI Ø 95
DI 1 94
DI 2 41
DI 3 42
DI 4 91
DI 5 92
DI 6 93
DI 7 43
BDENBL
PDBIN 78
U22
A Ø 79
PWR 77
R 17
+5V
Y Ø A
Y 1 A
Y 2 A
Y 3 A
Y Ø B
Y 1 B
Y 2 B
Y 3 B
RDEA
SWEA
DSA
CSA
RDEB
SWEB
DSB
CSB
U12
CLR
J 7
JUMPER
SOCKET
U 15
J 9
ACA
ACD
ATXE
ARXE
INTERFACER
A 1 8Ø
A 2 81
A3 31
A4 3Ø
A5 29
A6 82
A7 83
SOUT 45
SINP 46
SINTA 96
INT ACK

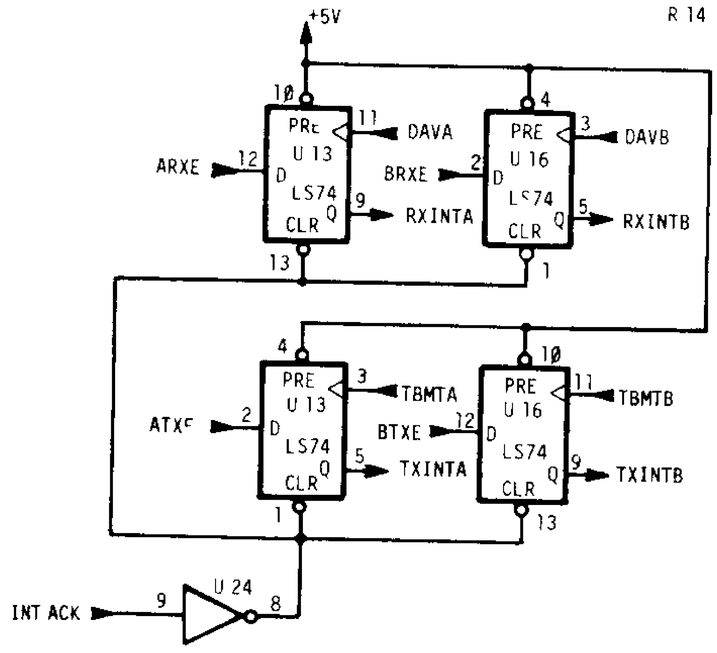

U 11
UART A
1602
AY 5 1013
OR SIMILAR
U 18
UART B
1602
AY-5 1013
OR SIMILAR
U 27
U 28
DB Ø
DB 1
DB 2
DB 3
DB 4
DB 5
DB 6
DB 7
DSA
DSB
DS
XR
CS
NB 2
NB 1
EPS
NP
TBS
TSB
TCP
RCP
DAV
TBMT
PE
OR
FE
RD Ø
RD 1
RD 2
RD 3
RD 4
RD 5
RD 6
RD 7
RDE
RDAV
TXD
SI
SWE
EOC
VCC
VGG
GND
DAVA
TBMTA
DAVB
TBMTB
ACB
ACC
OPA
J 12
SWEA
SWEB
RDEA
RDEB
TXDA
TXDB
SIA
SIB
+5V
12V
CLKA
CLKB
J8
JUMPER
SOCKET
U 14
J 10
JUMPER
SOCKET
U 17
CLR
CSB
BCA
BCD
BTXE
BRXE
INTERFACER
PORT A
SELECT
PORT B
SELECT
S 2
R 15
S 3
R 16
U 19
25LS2521
U 20
25LS2521
FIN
EOUT
EIN
S 1
R 11
R 12
D3
U 10
2941
1941
XTAL
OR
SIMILAR
CLK A
CLK B


4
BCB
2
J 13
BCC
OPB
A
8
B
C
SWEB


U 1
TXDA
2
3
C 9
U 1
ACA
12
13
11
C 8
U 1
ACD
5
4
6
C 7
U 2
3
1
2
C 12
ACB
11
U 2
13
12
C 10
ACC
6
U 2
4
5
C 11
OPA
8
U 2
10
9
C 13
+5V
J 3
JUMPER
SOCKET
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
2
3
4
5
6
20
8
BA
BB
CA
CB
CC
CD
CF
+12V
12V
J 1
SIA
3
U 21
1
2
4
U 9
3
R 6
+5V
R 5
U 4
1
5
U 29
TXDA
1
2
2
4
Q 1
D 1
R 7
+5V
R 1
U 3
5
1
4
2
3
J 4
JUMPER
SOCKET
16
15
14
13
12
11
10
9
R 2
+12V
11
25
+ IN
IN
R 1
+12V
12
13
19
18
+ OUT
OUT
TTL IN
TTL OUT

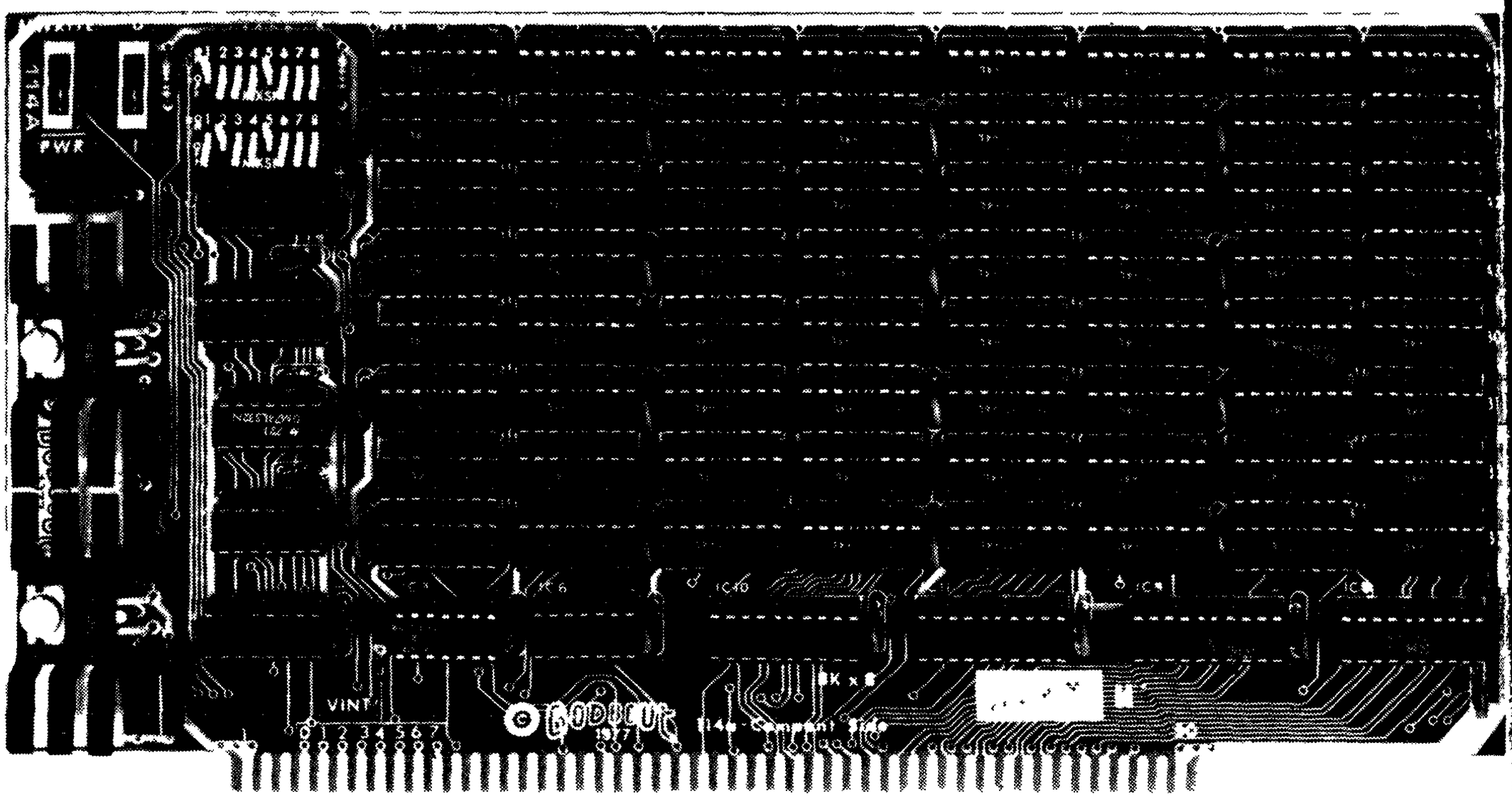
←INTERFACER→

U 5
TXDB
2
3
C 16
U 5
BCA
12
13
11
C 15
U 5
BCD
5
4
6
C 14
U 6
3
1
2
C 19
BCB
11
U 6
13
12
C 17
BCC
6
U 6
4
5
C 18
OPB
8
U 6
10
9
C 20
+5V
J 5
JUMPER
SOCKET
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
2
3
4
5
6
20
8
BA
BB
CA
CB
CC
CD
CF
+12V
-12V
J 2
SIB
11
U 21
13
12
6
U 9
5
R 9
+5V
R 8
U 8
1
5
U 29
TXDB
13
12
2
4
Q 2
D 2
R 10
+5V
R 14
U 7
5
1
4
2
3
J 6
JUMPER
SOCKET
16
15
14
13
12
11
10
9
R 3
+12V
11
25
+IN
IN
R 4
+12V
12
13
19
18
+OUT
OUT
TTL IN
TTL OUT
1
7
AA
AB


+5V
10
PRE
U 13
D
LS74
CLR
Q
11
DAVA
ARXE
12
9
RXINTA
13
4
PRE
U 16
D
LS74
CLR
Q
3
DAVB
BRXE
2
5
RXINTB
1
4
PRE
U 13
D
LS74
CLR
Q
3
TBMTA
ATXE
2
5
TXINTA
13
10
PRE
U 16
D
LS74
CLR
Q
11
TBMTB
BTXE
12
9
TXINTB
1
INT ACK
9
U 24
8

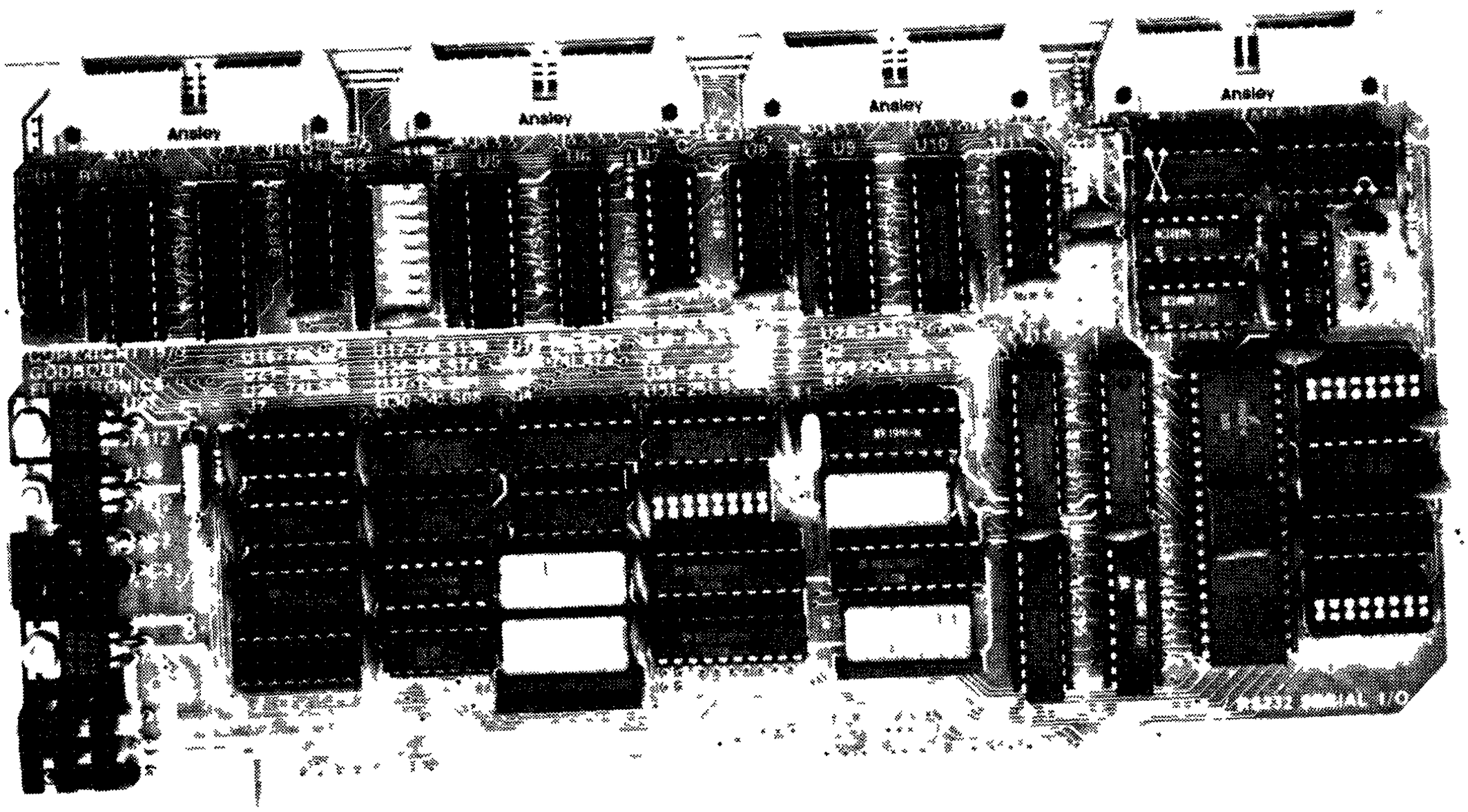
RXINTA
3
U 29
4
16
15
TXINTA
11
U 29
10
14
13
RXINTB
5
U 29
6
12
11
TXINTB
9
U 29
8
10
9
J 11
JUMPER
SOCKET
1
2
3
4
5
6
7
8
4
5
6
7
8
9
10
11
VI Ø
VI 1
VI 2
VI 3
VI 4
VI 5
VI 6
VI 7

ECONORAM II



MANUAL ON PAGE 15

←INTERFACER II→™
USER'S MANUAL



3 Parallel & 1 Serial I/O • S-100
RS232 • with full handshake

150D mac

CompuPro™ from GODBOUT

ABOUT THE INTERFACER II

Congratulations on your decision to purchase the INTERFACER II, a triple parallel/ single channel RS-232 serial I/O board designed specifically for full electrical and mechanical compatibility with the IEEE 696/S100 standard. The S-100 bus is the professional level choice for commercial, industrial and scientific applications. We believe that this board with the rest of the S-100 portion of the CompuPro family, is one of the best boards available for that bus.

Features, such as full RS232 handshaking, crystal controlled baud rate generator, a reliable hardware UART, three full duplex parallel I/O ports with handshaking and interrupts and a selectable rate interrupt clock allow for maximum flexibility at a reasonable price.

Thank you for choosing a CompuPro product....welcome to the club.

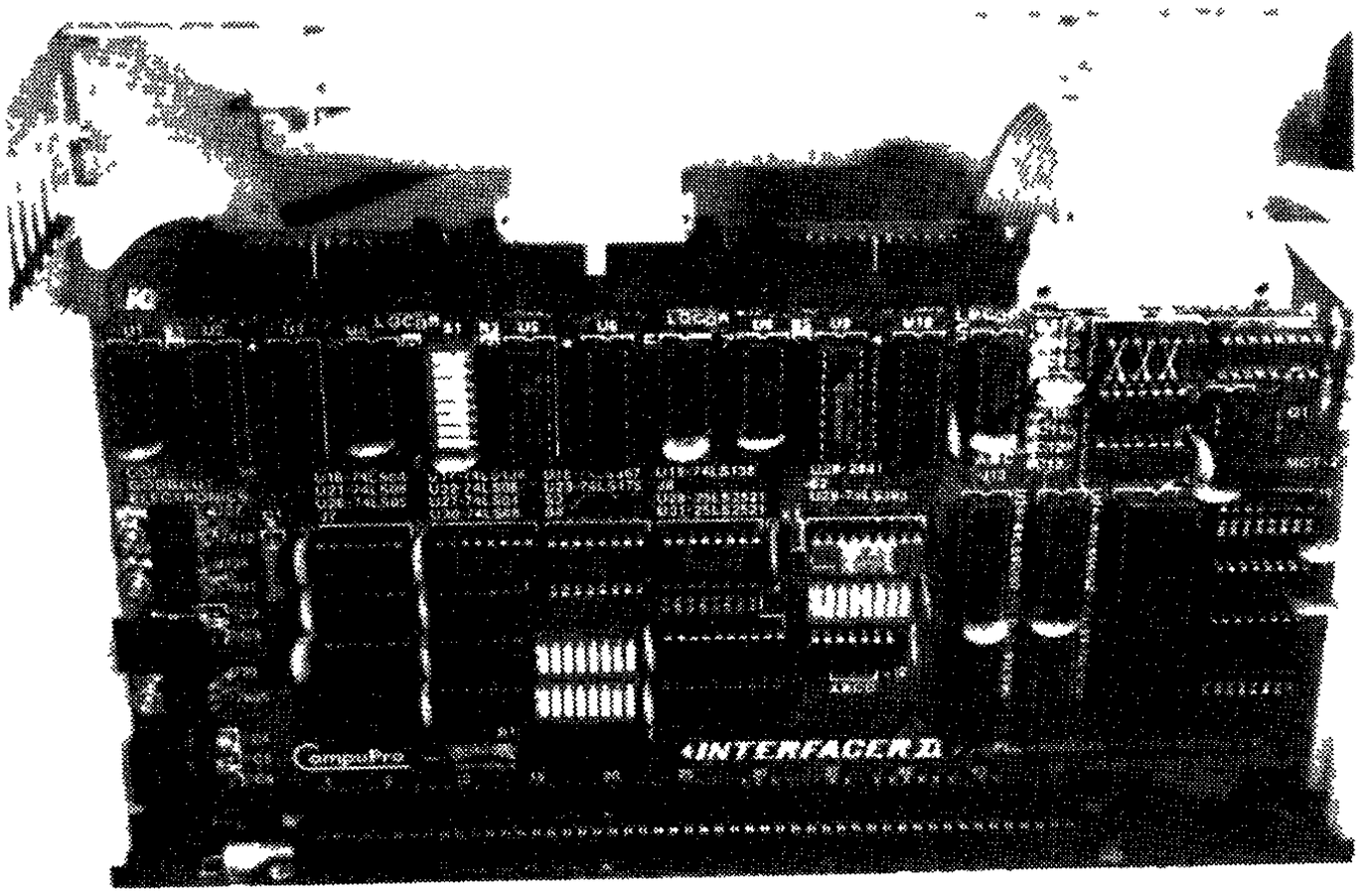
TECHNICAL OVERVIEW

The serial section of Interfacer II incorporates a reliable LSI technology UART chip to perform the basic serial-to-parallel and parallel-to-serial conversions necessary for serial communication. By using the UART, the CPU is freed of the time consuming drudgery of performing serial I/O operations by software techniques. Because of this, I/O operations are far more reliable and easier to implement.

In addition to the UART, several other features are included to make this board extremely flexible and easy to use These features include an on board crystal controlled baud rate generator for reliable Baud rates independent of your CPU clock speed, conversion to TTL, current loop and RS-232 levels for interfacing to almost every kind of serial device, and hardware/software programmability for power-on operation and easy parameter modification.

The parallel section of the INTERFACER II consists of three full duplex latched parallel ports for I/O data and one port for status and interrupt control. The use of TTL latches rather than a MOS parallel interface chip negates the need for mode selection and initialization, and allows each port to have strobe, attention and enable bits, an input interrupt, and 16 true data lines for a three port total of 48 true data lines

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky TTL and MOS technology integrated circuits for reliably cool operation. All this and sockets for all ICs go onto a double-sided, solder masked printed circuit board with a complete component layout legend.



Shown above is a typical installation using (2) optional Interfacer cable assemblies These cables consist of an Ansley 609-25S 25-pin 'D' connector and an Ansley 609-2601M 26-pin female transistion connector

Individual cable parts or assembled cables in 18 and 30 inch lengths are available from Godbout Electronics

I/O ADDRESS ASSIGNMENT

The serial Channel on this board is addressable as a single 2 port block anywhere through the 256 port I/O space In addition, this Channel can be disabled and electrically removed from the I/O space. DIP switch S3 addresses the two port block. The Channel will have the data port residing at the port address, and the status port residing at the port address + 1. The Channel is addressed as follows.

SWITCH POSITION	FUNCTION	
1	ADDRESS A1	
2	ADDRESS A2	
3	ADDRESS A3	'ON' = '0'
4	ADDRESS A4	
5	ADDRESS A5	'OFF' = '1'
6	ADDRESS A6	
7	ADDRESS A7	
8	CHANNEL DIS	'ON' = DISABLED 'OFF'= ENABLED

EXAMPLE: To address the serial channel at the first I/O port address pair 00H and 01H, positions 1 through 7 of switch S3 would be ON and position 8 would be OFF so that the Channel is enabled. This configuration places the data port at 00H (even address) and the status port at 01H (odd address).

BAUD RATE SELECTION

Dip switch S1 is used to select the Baud rate for the serial Channel. Switch positions 1 - 4 set the Baud rate for both the receiver and transmitter sections of the serial Channel as shown below.

ON = '0'
OFF = '1'

SWITCH POSITION 1 2 3 4	BAUD RATE
0 0 0 0	50 BAUD
1 0 0 0	75 BAUD
0 1 0 0	110 BAUD
1 1 0 0	134.5 BAUD
0 0 1 0	150 BAUD
1 0 1 0	300 BAUD
0 1 1 0	600 BAUD
1 1 1 0	1200 BAUD
0 0 0 1	1800 BAUD
1 0 0 1	2000 BAUD
0 1 0 1	2400 BAUD
1 1 0 1	3600 BAUD
0 0 1 1	4800 BAUD
1 0 1 1	7200 BAUD
0 1 1 1	9600 BAUD
1 1 1 1	19200 BAUD

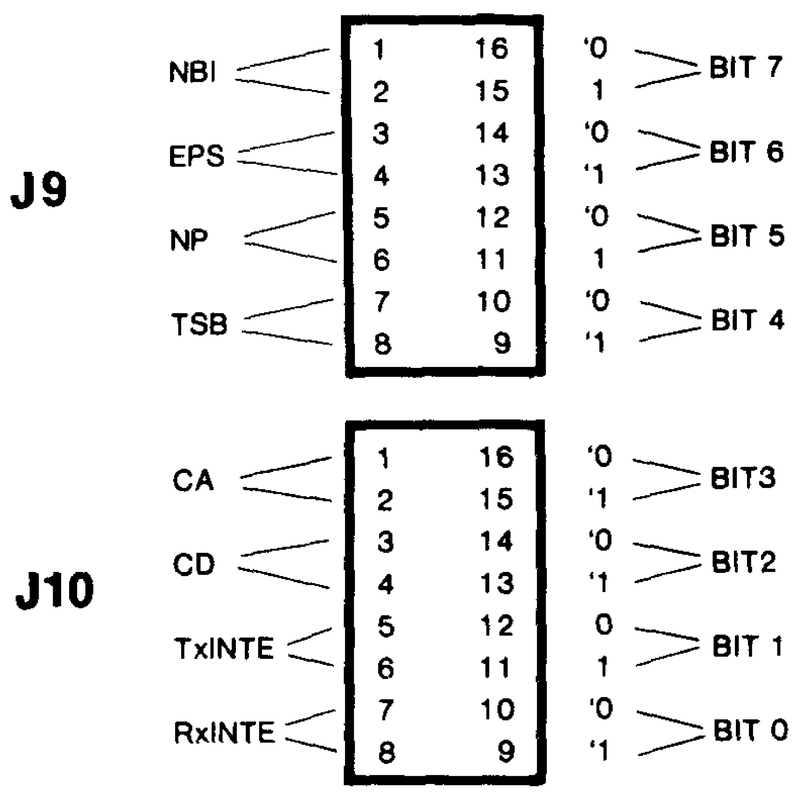
EXAMPLE To set the serial Channel to 9600 baud, DIP switch S2 would have position 1 ON and positions 2, 3, and 4 would be OFF. To set the serial Channel to 110 baud, DIP switch S2 would have positions 1, 3, and 4 ON and position 2 would be OFF.

UART PROGRAMMING

On power-up the control latches are all reset to a defined state as shown below. If the UART parameters for your system configuration are set properly for the reset state, no software initialization is necessary for proper operation of this board. To set the power-up parameters, the proper logic level for the programming header should be chosen from the table and the corresponding header trace should be left intact while the trace with the opposite level should be cut (an X-ACTO knife works great). For example, if odd parity is desired, the table shows that EPS should be a logic '0' and the header diagram indicates that the trace between pins 3 and 14 should remain while the trace between pins 4 and 13 should be cut.*NOTE: never leave both traces to a signal line unbroken as this could lead to heating and possible damage to the 74LS175's.*

The state of this board may be altered at any time by outputting a new control word to the Control Port. To change the mask under software control, simply output a '1' to the proper data bit of the Control Port corresponding to the signal that you desire to change. This will flip the logic level of the particular signal to the opposite state (i.e. odd parity will become even parity). Outputting a '0' to a bit will return it to the power-up setting.

UART PROGRAMMING



SIGNAL	'0'	'1'
EPS	ODD PARITY	EVEN PARITY
NBI	7 BITS	8 BITS
TSB	1 STOP BIT	2 STOP BITS
NP	PARITY	NO PARITY
TxINT E	DISABLED	ENABLED
RxINT E	DISABLED	ENABLED
CA	"SPACING"	"MARKING"
CD	"SPACING"	"MARKING"

VECTORED INTERRUPTS

When enabled and jumpered to the appropriate interrupt pin on the S-100 bus, the serial Channel has both a transmit and receive interrupt line The receive interrupt line (RxINT) is driven low when data is available from the UART and the RXINTE line has been enabled as described in the UART PROGRAMMING section This line resets to a high impedance state after the data has been fetched from the UART. The transmit interrupt line (TxINT) is driven low when the UART is ready to accept a character from the CPU and the TXINTE line has been enabled as described in the UART PROGRAMMING section This line resets to a high impedance state when the UART transmitter buffer is full and it cannot accept another character. Note that 'sINTA', S-100 bus pin 96, is not monitored by this board and is not needed to implement a useful interrupt scheme

	S-100 BUS	PINS	J7			
VI0	4	—	1	16	—	INT J1
VI1	5	—	2	15	—	INT J2
VI2	6	—	3	14	—	INT J3
VI3	7	—	4	13	—	NC
VI4	8	—	5	12	—	TMRI
VI5	9	—	6	11	—	NC
VI6	10	—	7	10	—	RxINT
VI7	11	—	8	9	—	TxINT

To enable an interrupt which is initially disabled or disable an interrupt that is initially enabled by the UART programming dip shunt (see UART Programming), a logical '1' should be output to the Interrupt Enable Bit of the Control Port.

STATUS PORT BIT ASSIGNMENT

Inputs from the status port to the CPU are defined as follows

DA	DATA BIT	NAME	SIGNAL
	D0	TBMT	Transmitter buffer empty
	D1	DAV	Data available
	D2	OPT	Optional status line
	D3	PE	Parity error
	D4	OR	Over run
	D5	FE	Framing error
	D6	CC	RS232 CC input
	D7	CB	RS232 CB input

CONTROL PORT BIT ASSIGNMENT

Outputs to the control port from the CPU are defined as follows

DA	DATA BIT	NAME	SIGNAL
	D0	RxINT E	Receiver interrupt enable
	D1	TxINT E	Transmitter interrupt enable
	D2	CD	RS232 CD output
	D3	CA	RS232 CA output
	D4	TSB	Number of stop bits
	D5	NP	No parity
	D6	EPS	Even parity select
	D7	NBI	Number of bits/character

SERIAL MODE JUMPERS

The INTERFACER II board with its unique serial programming jumpers, allows the user to adapt his board to all standard RS-232 pin configurations and to non-standard current loop configurations In current loop mode, this board may be set to use the on board current source or an external current source For example, a teletype requires that the on board current source be used, so the serial mode jumpers (J5 and J6) should be set like the example shown on the following page In RS-232 mode, these jumpers may be set so that this board operates in a 'master mode where it behaves as the Data Terminal Equipment (DTE), or it may be set so that the board operates in a 'slave mode where it behaves as the Data Communication Equipment (DCE) Since almost all CRT terminals and serial interface printers operate as the 'master' or as the Data Terminal Equipment, then the INTERFACER II board must operate as the 'slave or Data Communication Equipment For example, to connect the INTERFACER II to a terminal like an ADM 3A or a Hazeltine the serial mode jumpers (J5 and J6) should be set in 'slave mode as shown on the following page To connect the INTERFACER II to a modem is a different set-up because modems are set to operate as 'slaves' When connected to a Modem the INTERFACER II should be set in the 'master mode as shown on the following page

RS-232C CONTROL LINES

The RS-232 control and data lines are defined as shown below

PIN#	CIRCUIT	DIR	DESCRIPTION
1	AA		PROTECTIVE GROUND
2	BA	TO DCE	TRANSMITTED DATA
3	BB	TO DTE	RECEIVED DATA
4	CA	TO DCE	REQUEST TO SEND
5	CB	TO DTE	CLEAR TO SEND
6	CC	TO DTE	DATA SET READY
7	AB		SIGNAL GROUND
8	CF	TO DTE	REC D LINE SIGNAL DET
20	CD	TO DCE	DATA TERMINAL READY

Four hardwired RS-232 handshaking signals are provided for interfacing to equipment needing these lines as shown below These lines may be set to power-up either marking or spacing, and their state may be altered by software commands as described in the UART PROGRAMMING Section

OUTPUT LINES

DATA BIT	RS-232 LINE	DB25 PIN CONNECTION
D2	CD	20 OR 6 *
D3	CA	4 OR 5 *

INPUT LINES

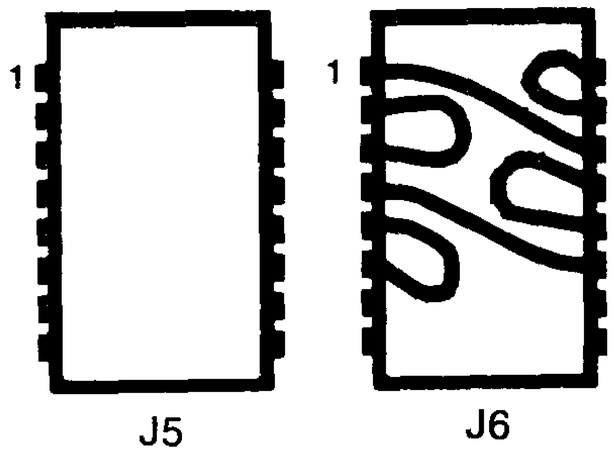
DATA BIT	RS-232 LINE	DB25 PIN CONNECTION
D2(OPT)	CF	8*
D6	CC	6 OR 20 *
D7	CB	5 OR 4 *

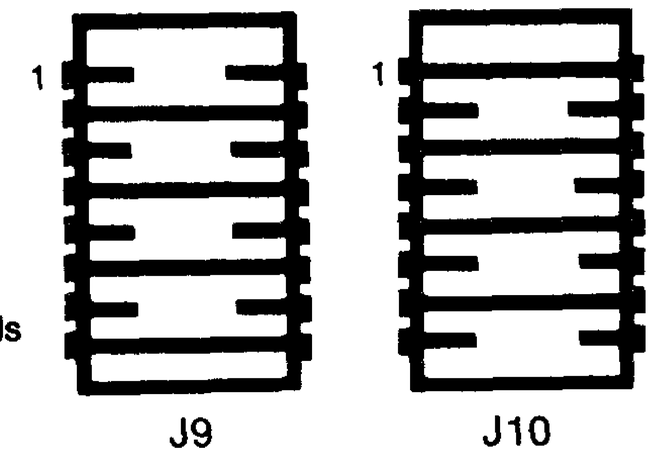
NOTE Non-starred pin numbers indicate the DB25 pin number when the Serial Mode Jumpers are set for master mode The starred pin numbers indicate the DB25 pin number when the Serial Mode Jumpers are set for slave mode

One optional input line (CF or Rec d Line Signal Detect) is provided at locations J13 If point 'B is jumpered to point A , this line will appear on Status Bit D2 By jumpering point B to point 'C , the 'End of Character output EOC) from the UART will appear on Status Bit D2

TYPICAL PROGRAMMING JUMPERS

Current loop - on board current sources EXAMPLE. TTY

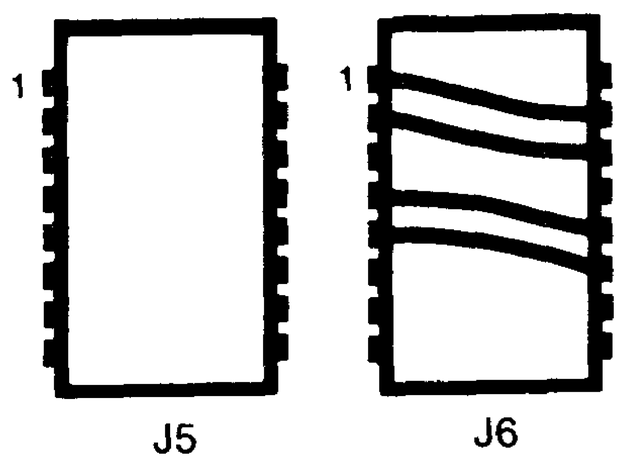


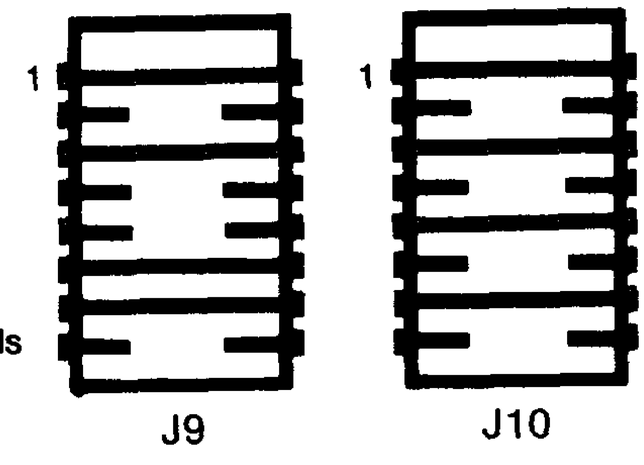


This configuration yields

Even parity
8 data bits
2 stop bits
No parity
Interrupts disabled

Current loop - external current sources

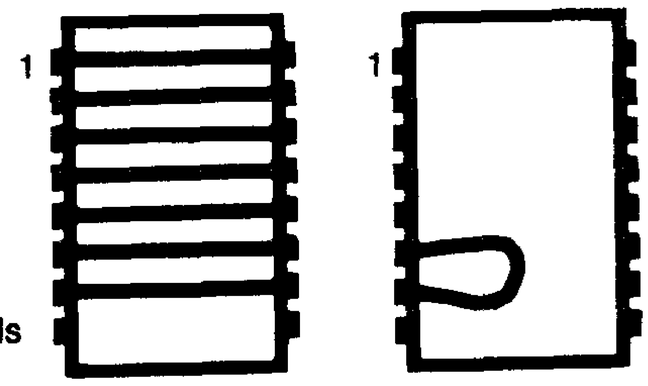




This configuration yields

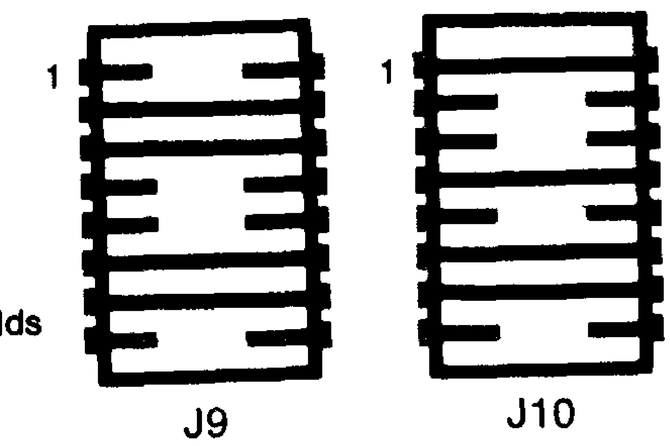
Odd parity
7 data bits
1 stop bit
No parity
Interrupts disabled

RS - 232C - Master mode EXAMPLE Modem



This configuration yields

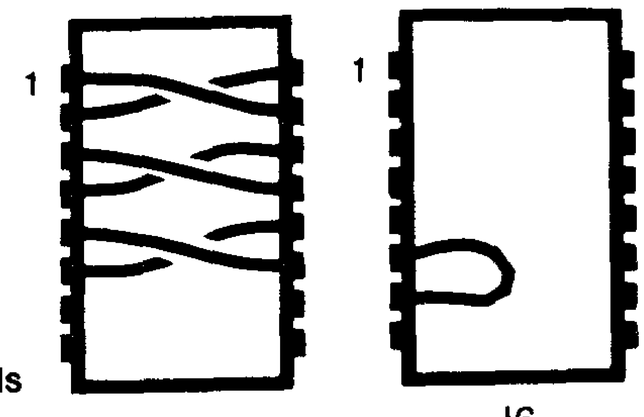
CA "spacing" on pin 4
CD "marking" on pin 20
BA (Tx data) on pin 2
BB (Rx data) on pin 3
CB Status to I/O board on pin 5
CC Status to I/O board on pin 6
CF (Received line signal detector on pin 8)



This configuration yields

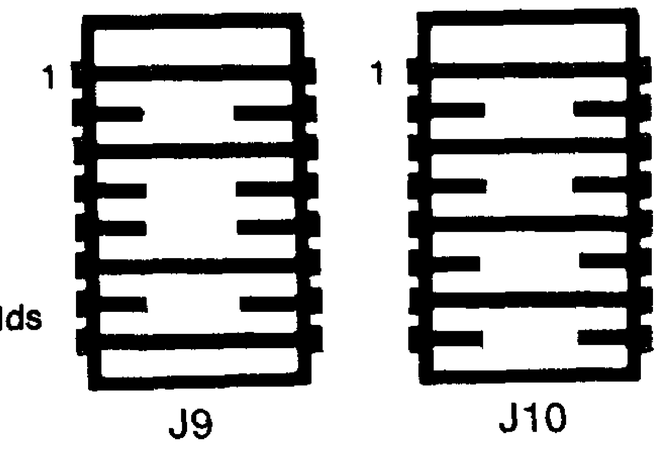
Odd parity
8 data bits
1 stop bit
No parity
Tx Inte enabled
Rx Inte disabled

RS - 232C - Slave mode EXAMPLE CRT Terminal, printer



This configuration yields

CA "spacing" on pin 5
CD "spacing" on pin 6
BA (Tx data) on pin 3
BB (Rx data) on pin 2
CB Status to I/O board on pin 4
CC Status to I/O board on pin 20



This configuration yields

Odd parity
7 data bits
2 stop bit
No parity
Interrupts disabled

PARALLEL SECTION

I/O ADDRESS ASSIGNMENT

The parallel Channels on the INTERFACER II board are addressed as any single four port block anywhere through the 256 port I/O space and can be disabled and electrically removed from the I/O space Dip switch S4 addresses the block with Channel 0 (J1) at the switch address, Channel 1 (J2) at the switch address + 1, Channel 2 (J3) at the switch address + 2, and the Status/Interrupt Control Port at the switch address + 3 Addressing is as shown below

SWITCH POSITION	FUNCTION	
1	NOT USED	
2	ADDRESS A2	
3	ADDRESS A3	ON = "0"
4	ADDRESS A4	OFF = "1'
5	ADDRESS A5	
6	ADDRESS A6	
7	ADDRESS A7	
8	BLOCK DISABLE -	ON = DISABLED
		OFF= ENABLED

EXAMPLE To address the block starting at C8H, switch positions 3,6,7 & 8 would be OFF and 2,4 & 5 would be ON In this configuration, Channel 0 (J1) would be at port C8H, Channel 1 (J2) would be at port C9H, Channel 2 (J3) would be at CAH, and the Status/Interrupt Control Port would be at CBH.

STATUS PORT BIT ASSIGNMENT

Inputs to the processor from the Status Port are defined as follows

DATA BIT	NAME	SIGNAL
D0	DAV0	DATA AVAILABLE CHANNEL 0
D1	TKN0	DATA TAKEN CHANNEL 0
D2	DAV1	DATA AVAILABLE CHANNEL 1
D3	TKN1	DATA TAKEN CHANNEL 1
D4	DAV2	DATA AVAILABLE CHANNEL 2
D5	TKN2	DATA TAKEN CHANNEL 2
D6	NOT USED	
D7	NOT USED	

INTERRUPT CONTROL PORT BIT ASSIGNMENT

Outputs from the processor to the Interrupt Control Port are defined as follows

DATA BIT	NAME	SIGNAL
D0	INTEJ1	INTERRUPT ENABLE CHANNEL 0
D1	INTEJ2	INTERRUPT ENABLE CHANNEL 1
D2	INTEJ3	INTERRUPT ENABLE CHANNEL 2
D3	TMRIE	TIMER INTERRUPT ENABLE
D4-D7	NOT USED	

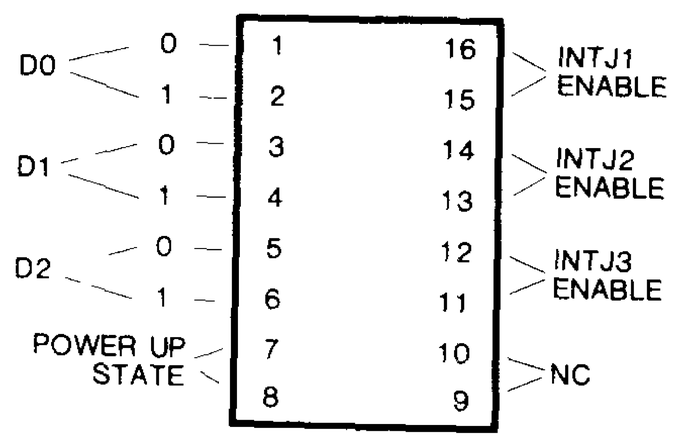
PARALLEL VECTORED INTERRUPTS

When enabled and jumpered to the appropriate interrupt pin on the S-100 bus, the parallel block has three separate interrupts that occur when data is strobed into each of the three input Channels The interrupt lines, INTJ1, INTJ2, and INTJ3, are driven low when J1, J2, and J3 respectively are strobed with input data. These lines are reset to a high impedance state as soon as the data is taken from the appropriate Channel

As with the serial section of this board, the parallel interrupts are also Hardware/ Software programmable with a user definable power on setting Jumper socket J8 is used to set the power-up or reset parameters by programming the DIP shunt from the figure below On power-up or reset, the logic levels shown on the left side of the jumper socket are available for either enabling or disabling the interrupts Since a logic '1' enables the particular input interrupt and a logic '0' disables the interrupt, jumpering the appropriate level across the socket will make the board assume a known state after power-up or reset The proper way to program this setting is to punch out the not wanted trace of the shunt with an X-ACTO or similar knife and leave the trace intact that has the proper level

To alter the programmed setting under software control, the user should output a logic '1' to the proper bit of the Interrupt/ Control Port shown in the figure or the bit assignment table This will disable an enabled interrupt and enable a disabled interrupt Outputting a logic '0' to the same bit will return it to the users power-up or reset configuration

J8



DATA BIT	PORT	CONNECTOR
D0	0	J1
D1	1	J2
D2	2	J3

	S 100 BUS PINS		J7			
VI0	4	—	1	16	—	INT J1
VI1	5	—	2	15	—	INT J2
VI2	6	—	3	14	—	INT J3
VI3	7	—	4	13	—	NC
VI4	8	—	5	12	—	TMRI
VI5	9	—	6	11	—	NC
VI6	10	—	7	10	—	RxINT
VI7	11	—	8	9	—	TxINT

PORT CONTROL LINES

INPUT STROBE LINE

The strobe line on each input Channel is used to latch data from an external device into the input register when a 74LS374 or 74LS373 latch is used This line also sets the status flag (DAVx) so that the processor can tell if data has been entered

If a 74LS374 is used as the input register, a transition on the strobe line latches the data and sets the status flag (DAVx) The strobe polarity select switch should be set as described below so that the peripheral's data is valid during the strobe's transition With the select switch (S1-2, S1-4, and S1-6) ON, a low to high transition on strobe will latch the data With the select switch OFF, a high to low transition on strobe will latch the data

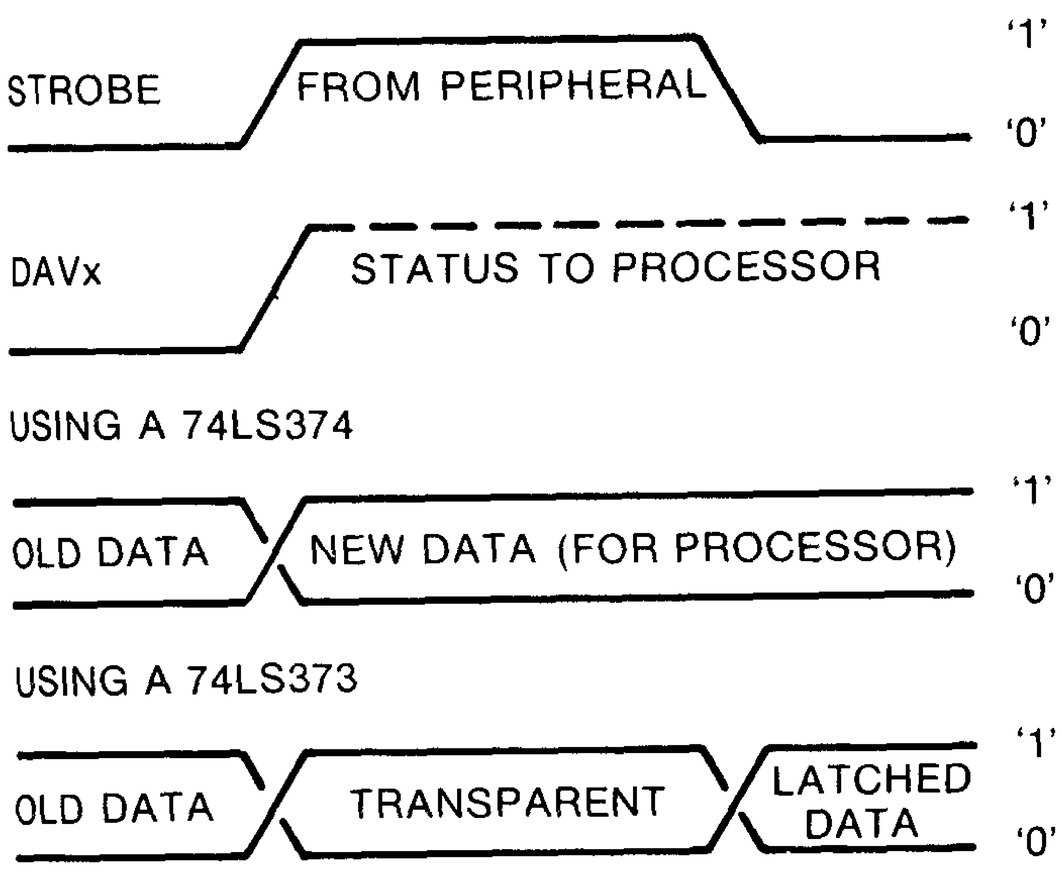
If a 74LS373 is used as the input register, the strobe line can assume two different modes The first mode is similar to the latched mode of the 74LS374 described above except that during the strobe pulse the data is transparent through latch to the processor At the end of the strobe pulse, the data will be latched and stable for the processor to access With the strobe select switch (S1-2, S1-4, and S1-6) ON, a positive going strobe pulse will latch the data at the end of the pulse With the select switch OFF, a negative going strobe pulse will latch the data at the end of the pulse The second mode is the fully transparent mode where the data is never latched but is available for inputting at any time by the processor This mode is useful whenever the data has no strobe bit associated with it This mode is entered when the strobe line is left open with the strobe select switch ON See the timing diagrams below for a visual representation of the input data and the strobe relationships

NOTE In the diagrams below, the strobe is provided by the external device and the incoming data is shown as what is available to the processor in relation to the strobe pulse

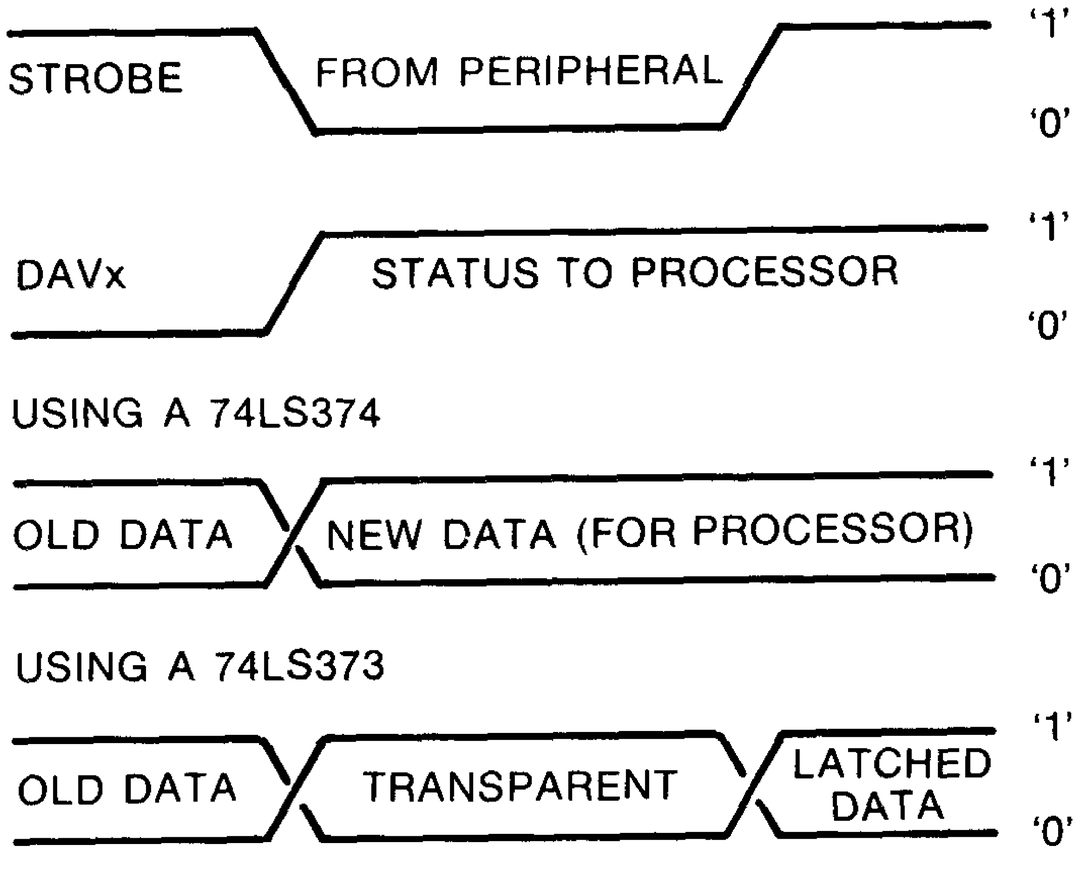
INPUT EXAMPLES

Some examples of typical applications might include connecting a ASCII keyboard or a set of sense switches to one of the input Channels of the INTERFACER II A keyboard usually has a strobe line to indicate that it has current valid data on its data outputs therefore, using one of the 74LS374 latches would be best The keyboard data lines would be connected accordingly to input data lines of the parallel Channel and the keyboard strobe line would be connected to the Channel STROBE input The Strobe Select switch would be ON for a positive keyboard strobe, and OFF for a negative keyboard strobe If connecting some sense switches to the input lines, a 74LS373 would be the best choice because there are usually no strobe lines associated with switches The switches should be connected to the input lines so that they ground the inputs (no pullup resistors are needed since they are supplied on the board) and the STROBE LINE should be left floating with the Strobe Select switch ON This allows the processor to input the data from the switches at any time Another example of an input signal that usually does not h e a strobe associated with it would be the Busy line and r status bits from a printer or other device.

WITH THE STROBE SELECT SWITCH 'ON':



WITH THE STROBE SELECT SWITCH 'OFF':



OUTPUT ENABLE LINE

The OUTPUT ENABLE LINE on each Channel is used to Tri-State the output register and enable the Q and Q* output flags as described below By Tri-Stating the output register, the user may bus the output data from several different sources onto the same 8 data lines In this mode, the TKNx status bit will stay high until the ouput register goes active, at which point the TKNx status bit will go low. If the output register is active at all times, (most applications will be this way) the TKNx status bit will stay low at all times.

When the Polarity Select Switch (S1-3, S1-5, and S1-7) is ON, the OUTPUT ENABLE LINE must be low to enable the output register. With the Select Switch OFF, the OUTPUT ENABLE LINE must be high or left open to enable the output register

ATTENTION LINE

The ATTENTION LINE is used to inform an external device that new data is now available for it This line may be jumpered (J14, J15, and J16) to provide any one of four different outputs. With the Common jumpered to either Q or Q*, and the OUTPUT ENABLE LINE set so that the output of the register is Tri-Stated, then the ATTENTION LINE will go high (Q) or low (Q*) when data is strobed into the output register and the TKNx status bit will go high. When the OUTPUT ENABLE LINE level is changed to enable the data, then the ATTENTION LINE will return to its original level and the TKNx status bit will go low. In this mode, the OUTPUT ENABLE LINE is used to transfer the data out of the register and reset the attention flag Since the level of the ATTENTION LINE may be sampled by the processor through the status port (TKNx), a high speed handshaking data transfer can occur.

With the Common tied to either the 'L' or the 'R', the ATTENTION LINE becomes a positive (R) or negative (L) going strobe pulse with a width of the system PWR* strobe (between 150 and 1000ns) In this mode, the the OUTPUT ENABLE LINE should be set so that the data is active at all times, rendering the TKNx status bit low at all times. This mode is best used when the external device needs the data strobed into it. See the diagrams below for the output data timing using either a 74LS373 or a 74LS374 as an output register

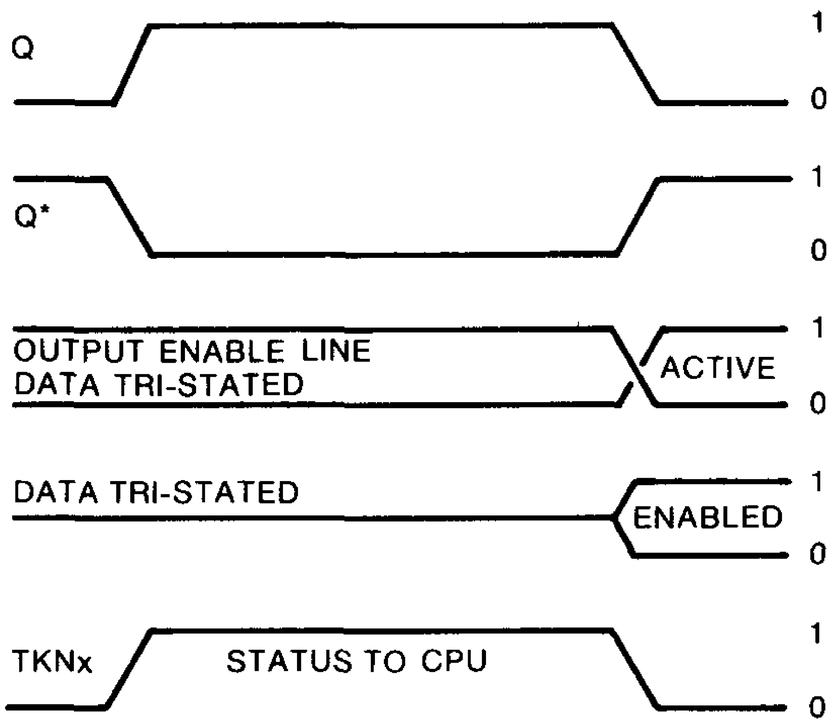
NOTE· Example (1) below shows the Q and Q* output lines (one of which will be tied to 'C' for driving the ATTENTION LINE), the OUTPUT ENABLE LINE with both polarities shown (the user must select the proper level to Tri-State and activate the data as described above and shown in the figure), the TKNx status line as read by the processor, and the state of the output data (either Tri-Stated or enabled)

Example (2) shows the state of the output data in the output register using either a 74LS373 or 74LS374 in relation to the strobes in Examples (1) and (3) NOTE The transparent time on the 74LS373 contains new valid data since the S-100 bus supplies valid data during this time

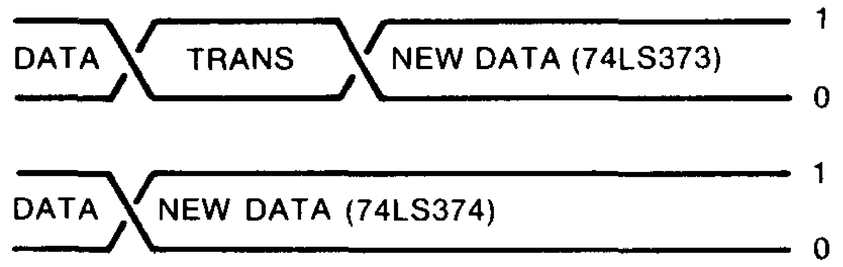
Example (3) shows both the 'L' and 'R' output pulses (one of which is tied to the 'C' or Common line for generating a pulse on the ATTENTION LINE), the state of the new output data (either new or old data), and the TKNx status line which is low to the proccessor at all times (assuming that the data is held active at all times with the OUTPUT ENABLE LINE)

OUTPUT DATA TIMING

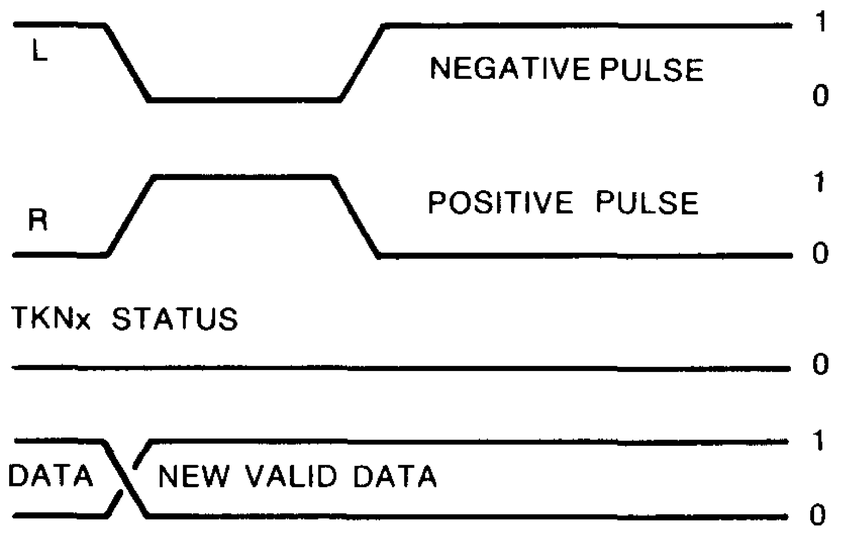
EXAMPLE (1)



EXAMPLE (2)



EXAMPLE (3)



OUTPUT EXAMPLES

Some examples of typical applications might include connecting a parallel printer or some LED's to the output lines A parallel printer might require that 7, 8, or more data lines be connected in addition to a strobe line. In many cases, the strobe (L or R) connected to the ATTENTION LINE will be sufficiently long for the printer and can be connected directly with the proper polarity for correct printer operation Some printers might require a longer strobe than the system PWR* pulse width, therefore a longer strobe can be made by switching a data bit from one of the other parallel output channels on and off via software to act as a strobe If only 7 data lines are required for the printer, then the eighth data line from the same channel may be used with the software being tailored to provide a strobe pulse of almost any length

PROGRAMMABLE TIMER INTERRUPT

The INTERFACER II is equipped with a simple programmable/fixed rate interrupt source for timing. By enabling the timer through the Interrupt Control Port and jumpering the interrupt to the appropriate vectored interrupt line on the bus, a rate timer is established. The basic interrupt rate is set by positions 5 - 8 of Dip switch S2 as shown below. Further reductions in the basic rate are obtained by re-jumpering J12 as described below.

SWITCH POSITION 5 6 7 8	INTERRUPT RATE
0 0 0 0	50 INT/SEC.
1 0 0 0	75 INT/SEC.
0 1 0 0	110 INT/SEC.
1 1 0 0	134.5 INT/SEC.
0 0 1 0	150 INT/SEC.
1 0 1 0	300 INT/SEC.
0 1 1 0	600 INT/SEC.
1 1 1 0	1200 INT/SEC.
0 0 0 1	1800 INT/SEC.
1 0 0 1	2000 INT/SEC.
0 1 0 1	2400 INT/SEC.
1 1 0 1	3600 INT/SEC.
0 0 1 1	4800 INT/SEC.
1 0 1 1	7200 INT/SEC.
0 1 1 1	9600 INT/SEC.
1 1 1 1	19200 INT/SEC.

ON = '0' OFF = '1'

The above basic rate can be reduced by a factor of 2, 4, or 8 by cutting the trace at J12 from 'A' to common on the solder side of the board, and installing a jumper between common and 'B', 'C', or 'D' for a reduction of 2, 4, or 8.

EXAMPLE: To set the interrupt rate to 9600 INT/SEC., DIP switch S2 would have position 5 ON and positions 6, 7, and 8 would be OFF

EXAMPLE. To set the interrupt rate to 110 INT/SEC., DIP switch S2 would have positions 5, 7, and 8 ON and position 6 would be OFF

EXAMPLE: To set the interrupt rate to 25 INT/SEC., (50 INT/SEC. divided by 2) DIP switch S2 would have positions 4-8 ON and a jumper installed between common and 'B' of J12 as described above.

The timer control bit is initially disabled after power-up or reset and must be initialized to be made operational. This is accomplished by outputting a logic '1' to the Interrupt/Control Port bit D3. The timer can be disabled by outputting a '0' to the control bit in the same fashion that it was enabled.

The proper response to a timer interrupt is to disable the timer as described above and then immediately re-enable it. This removes the interrupt from the bus in preparation for the next timer interrupt.

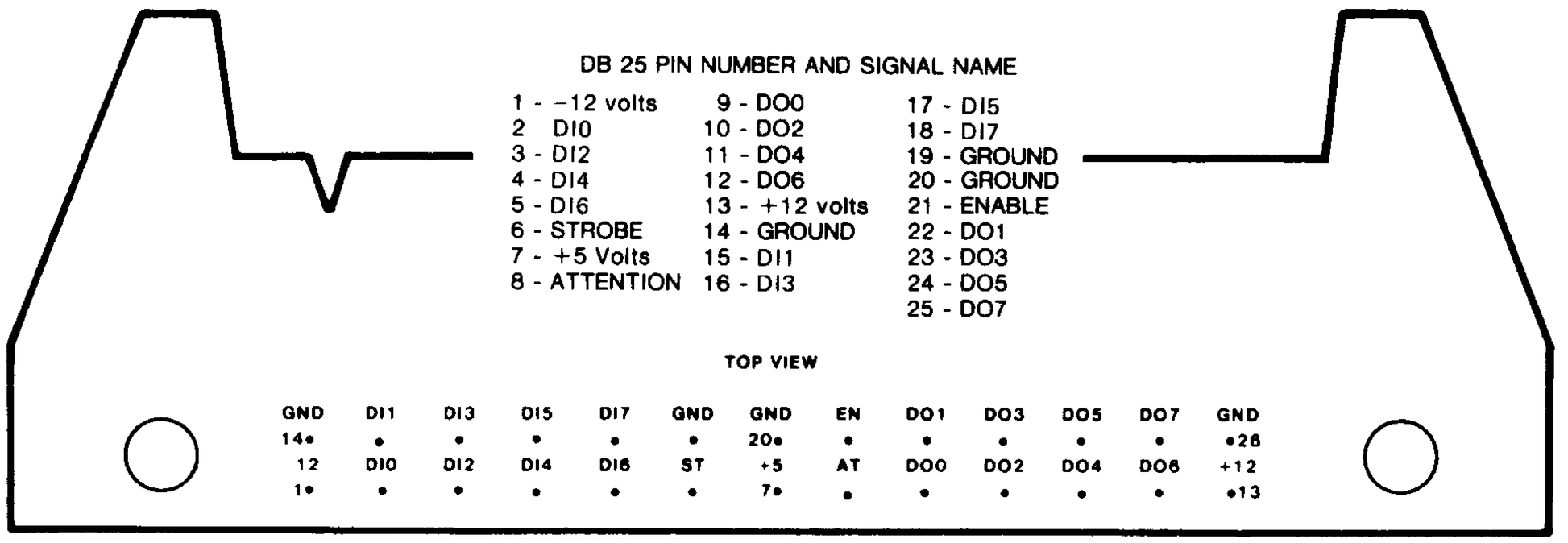
	S-100 BUS	PINS	J7			
VI0	4	—	1	16	—	INT J1
VI1	5	—	2	15	—	INT J2
VI2	6	—	3	14	—	INT J3
VI3	7	—	4	13	—	NC
VI4	8	—	5	12	—	TMRI
VI5	9	—	6	11	—	NC
VI6	10	—	7	10	—	RxINT
VI7	11	—	8	9	—	TxINT

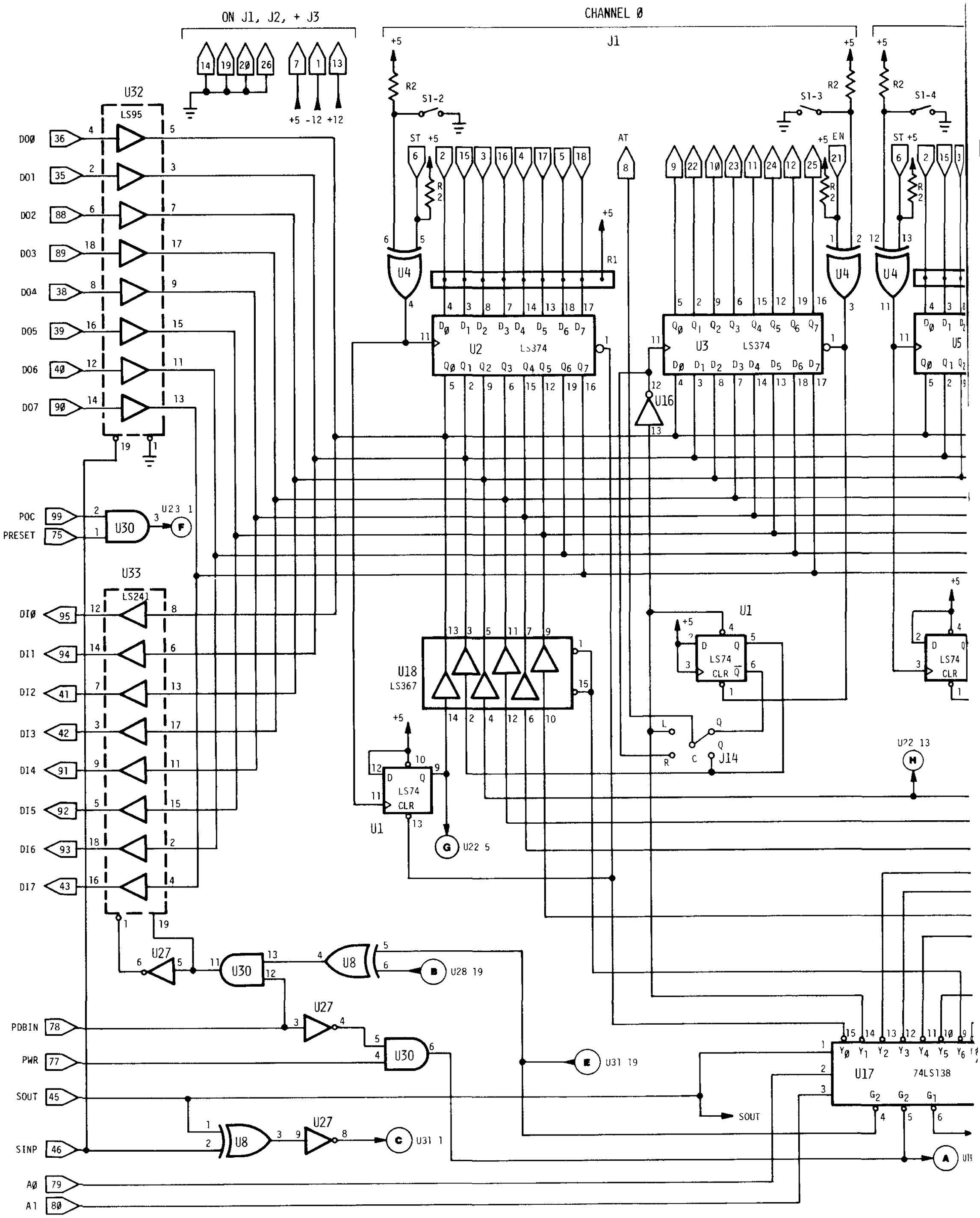
I/O CONNECTOR PINOUTS

A small amount of current is available for powering external devices such as a keyboard or A to D converter at each port connector. The total current available is shown below:

+ 5 volts @ 200 ma	TOTAL FOR
+12 volts @ 50 ma	ALL 3 PARALLEL
−12 volts @ 50 ma	CONNECTORS

CONNECTOR PINOUT - PARALLEL I/O PORT




ON J1, J2, + J3
CHANNEL Ø
J1
14 19 20 26 7 1 13
+5 -12 +12
U32
LS95
DØØ 36
DØ1 35
DØ2 88
DØ3 89
DØ4 38
DØ5 39
DØ6 40
DØ7 90
POC 99
PRESET 75
U30
U23 1
F
U33
LS241
DIØ 95
DI1 94
DI2 41
DI3 42
DI4 91
DI5 92
DI6 93
DI7 43
R2
S1-2
S1-3
S1-4
ST +5
EN
AT
R1
U4
U2 LS374
U3 LS374
U5
U16
U18 LS367
U1 LS74 CLR
U27
U8
U30
B U28 19
E U31 19
C U31 1
G U22 5
H U22 13
J14
PDBIN 78
PWR 77
SOUT 45
SINP 46
AØ 79
A1 80
U17 74LS138
A U19

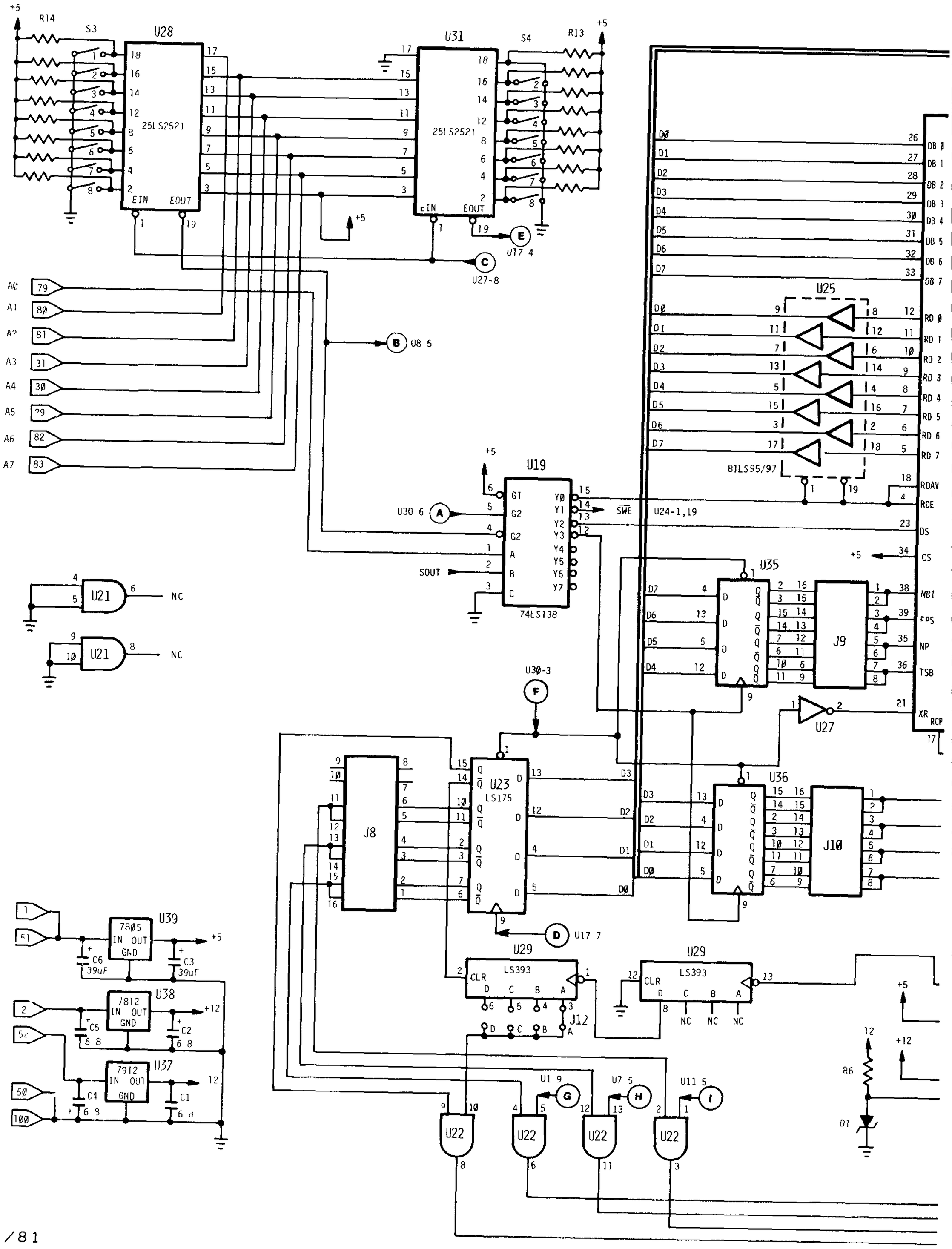
CHANNEL 1

J2

CHANNEL 2

J3

+5
R2
S1 5
+5 EN
AT
R3
U4
U5
U6 LS374
U8
U16
U9 LS374
S1 6
ST +5
R5
U10 LS374
S1 7
EN
R7
R2
R3
R5
U7
U11
LS74
CLR
J15
J16
U22 1
U23 9
U19 5
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
TO OTHER PAGE
NC


+5
R14
S3
U28
25LS2521
EIN
EOUT
U31
S4
R13
A0
A1
A2
A3
A4
A5
A6
A7
79
80
81
31
30
29
82
83
B U8 5
C U27-8
E U17 4
U19
74LS138
U30 6
A
SOUT
SWE
U24-1,19
U25
81LS95/97
RDAV
RDE
DS
CS
NBI
FPS
NP
TSB
XR
RCP
U35
J9
U36
J10
U27
U21
NC
U39
7805
U38
7812
U37
7912
C6 39uF
C3 39uF
C5 6.8
C2 6.8
C4 6.8
C1 6.8
U30-3
F
J8
U23
LS175
D3
D2
D1
D0
D U17 7
U29
LS393
CLR
J12
NC
R6
D1
U1 9
G
U7 5
H
U11 5
I
U22
TCP

DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
TO OTHER PAGE

←INTERFACER II→

U34
1602
1863
TBMT
DAV
EOC
PE
OR
FE
+5
-12
SWE
GND
TXD
SI
TCP
RCP

U24
DAV TBMT
D0
D1
D2
D3
D4
D5
D6
D7
SWE
U19-14

U12
NC
C9
C8
C7

U30
U13
C13
C10
C12
C11

R13
U27
U14
*R8
U15
Q1
D2
*R11
*R10
*R9

J5
J6
J7
J4
BA
BB
CA
CB
CC
CD
CF
+IN
-IN
+OUT
-OUT
TTL IN
TTL OUT
AA
AB
VI0
VI1
VI2
VI3
VI4
VI5
VI6
VI7

X1
U20
2941
FT
FR
STT
STR
+5V
+12V
5V
TA
TB
TC
TD
RA
RB
RC
RD
S2

U21
DAV
TBMT

U26

BOARD POWER-UP AND TESTING

CHECKING-OUT YOUR BOARD

Now for the fun part BEFORE you install the board in your system, take the time to check these few things over

- ☐ 1 ARE ALL THE JUMPERS AND DIP SHUNTS PROPERLY INSERTED?
- ☐ 2 ARE THE BAUD RATE SWITCHES SET TO THE PROPER BAUD RATE FOR YOUR TERMINAL?
- ☐ 3 ARE THE PORTS YOU WANT TO USE PROPERLY ADDRESSED AND ENABLED?
- ☐ 4 IF YOU DON T WANT TO USE A PORT IS IT DISABLED?
- ☐ 5 ARE THE HARDWARE/SOFTWARE PROGRAMMING JUMPERS SET THE WAY YOU REALLY WANT THEM?
- ☐ 6 ARE YOU SURE YOU AREN T TYING TWO OR MORE OF THE PROGRAMMING OUTPUTS TOGETHER?
- ☐ 7 ARE THE INTERRUPT JUMPERS SET TO THE PROPER INTERRUPT LINE OR ARE THEY COMPLETELY REMOVED?
- ☐ 8 IF USING CURRENT LOOP ARE THE PROGRAMMING LINES SET PROPERLY FOR USING EITHER ON-BOARD CURRENT SOURCE OR THE EXTERNAL SOURCE?
- ☐ 9 IF USING RS232 ARE THE PROGRAMMING LINES SET PROPERLY FOR MASTER OR SLAVE MODE?
- ☐ 10 ARE THE OPTION JUMPERS SET THE WAY YOU WANT?
- ☐ 11 ARE THE PARALLEL INTERRUPT MASK JUMPERS SET THE WAY YOU WANT?
- ☐ 12 ARE THE POLARITY SELECT SWITCHES SET PROPERLY?

If you have answered yes to all of the above, you are ready to install the board in your system Enter the serial testing routine via either the front panel switches, editor assembler, or any means available

SERIAL I/O TESTING ROUTINE

```
0000                0050 CONTROL EQU  01H      CONTROL PORT ADDRESS
0000                0060 STATUS  EQU  01H      STATUS PORT ADDRESS
0000                0070 DATA    EQU  00H      DATA PORT ADDRESS
0000                0080*
0000                0090*
0000                0100         ORG  0000H
0000                0110*
0000 3E 00          0120 START   MVI  A 00H    INITIALIZE THE
0002 D3 01          0130         OUT  CONTROL  CONTROL PORT
0004 DB 01          0140 BEGIN   IN   STATUS   INPUT STATUS AND
0006 E6 02          0150         ANI  02H      MASK FOR DAV
0008 CA OE          0160         JZ   BEGIN    IF NON/CHECK AGAIN
000B DB 00          0170         IN   DATA     IF DAV 1 INPUT DATA &
000D 47             0180         MOV  B A      MOVE TO REGISTER B
000E DB 01          0190 LOOP    IN   STATUS   INPUT STATUS AND
0010 E6 01          0200         ANI  01H      MASK FOR TBMT
0012 CA 0E          0210         JZ   LOOP     IF NOT READY CHECK AGAIN
0015 78             0222         MOV  A B      IF TBMT-1 MOVE DATA INTO
0016 D3 00          0230         OUT  DATA     REGISTER A THEN OUTPUT
001B C3 04          0240         JMP  BEGIN    JUMP FOR NEXT CHARACTER
```

PARALLEL I/O TESTING ROUTINE

```
0000                0000 STATUS  EQU  0F3H     STATUS PORT ADDRESS
0000                0010 PORT0   EQU  0F0H     PORT 0 - CONN J1
0000                0020 PORT1   EQU  0F1H     PORT 1 - CONN J2
0000                0030 PORT2   EQU  0F2H     PORT 2  CONN J3
0000                0040*
0000                0050*
0000                0060         ORG  0000H
0000                0070
0000 3E 00          0080 START   MVI  A 00H    CLEAR THE
0002 D3 F3          0090         OUT  STATUS   INTERRUPT MASK
0004 DB F3          0100 BEGIN   IN   STATUS   INPUT STATUS AND MASK
0006 E6 01          0110         ANI  01H      FOR PORT 0 DATA AVL
0008 CA 04 00       0120         JZ   BEGIN    IF NONE / TRY AGAIN
000B DB F0          0130         IN   PORTO    INPUT DATA AND
000D 47             0140         MOV  B A      STORE IN REG B
000E DB F3          0150 LOOP    IN   STATUS   INPUT STATUS AND MASK
000E E6 02          0160         ANI  01H      FOR DATA ACCEPTED
0012 C2 OE 00       0170         JNZ  LOOP     RECHECK IF NOT ACCEPTED
0015 78             0180         MOV  A B      RETRIEVE DATA AND
0016 D3 F0          0190         OUT  PORTO    OUTPUT TO PORT 0
0018 C3 04 00       0200         JMP  BEGIN    START AGAIN
```

IF YOU EXPERIENCE A MALFUNCTION

SERIAL SECTION TESTING

1 Verify that the Baud rate you want is being delivered to the UART With a scope or frequency counter, measure the frequency at pins 40 and 17 of the UART Remember that the UART needs a 16x clock, so the frequency will be 16 times the Baud rate

EXAMPLE 1200 Baud x 16 = 19 2KHz
for people with scopes

$$\text{Frequency (Hz)} = \frac{1}{\text{cycle period (seconds)}}$$

2 Verify with scope or logic probe that data reaches pin 20 of the UART when you type a character on your terminal If not - trace back and see where it's being lost

3 Verify that the status bit DAV (pin 19 of the UART) goes high after striking a character from the terminal If it does not, and data is getting to the UART, you may have a bad UART

4 Verify that your computer is getting the status of the board by running a simple program like the one below

```
LOOP  IN   STATUS     (your status port)
      JMP  LOOP
```

Verify that the line SWE pulses low while this program is running (pins 1 and 9 of the status gate U24) and that the data is getting on to the buss from the buss driver U33 as pin 1 and 19 pulse low and high, respectively

5 Verify that the programming latches (U35, U36) and the UART are receiving their control strobes when the following program is run

```
LOOP  OUT  CONTROL    (your control port)
      JMP  LOOP
```

The line CS should strobe low while this program is running (check pin 9 of U35 and U36)

6 Verify that data is reaching the UART's from the host computer by running the following program and observing that pin 34 of the UART (DS) strobes low NOTE: Only garbage will be transmitted

```
LOOP   OUT  DATA        (your data port)
       JMP  LOOP
```

7 Verify that data is reaching the computer from the UART by running the following programs and observing that RDE strobes low (pins 4 and 18 of the UART) and that pins 1 and 19 of U33 strobe low and high, respectively

```
LOOP   IN   DATA        (your data port)
       JMP  LOOP
```

8 Verify that serial data is leaving the UART pin 25 and is propagated to the output connector pin through the output level translators Test this while running the I/O board testing routine.

9 If you don't seem to be getting any of the above mentioned control strobes, check pin 4 of U19 for a low strobe when running any of the above programs If not, either the address is set wrong or there is a defective switch, I C or board in the I/O address decoding circuitry Also, pin 5 of U19 should be strobe low to indicate either a pDBIN or pWR

PARALLEL SECTION TESTING

1 Verify that pin 11 of the input 74LS374 pulses high when the input is strobed

2 Verify that pins 15, 13, 11 and 9 of U17 strobe low when you input from ports 0, 1, 2, and 3 respectively

3 Verify that pins 14, 12, 10 and 7 of U17 strobe low when you output from ports 0, 1, 2, and 3 respectively

4 If you haven't been getting the strobes in the two previous steps, check for port enable strobing low on pin 4 and check for pWR and pDBIN strobing low on pin 5 of U17

CIRCUIT DESCRIPTION

THE SERIAL SECTION

The heart of the Serial Section of this board is a MOS LSI UART. The UART performs the complete parallel to serial and serial to parallel conversion, error detection, and serial format modification necessary for reliable and flexible serial communication The Serial Section can be divided into seven subsections. I/O Port Select Logic, Bus Driver Logic, Hardware/Software Programming Logic, Baud Rate Select Logic, Interrupt Logic, Serial Line Level Conversion Logic, and the UART.

I/O PORT SELECT LOGIC

Address line A1 thru A7 each feed into one input of the 25LS2521 octal comparator (U28) with the other input connected to a position on the Channel select dip switch (S3). The input of the comparator is gated by the I/O detect logic consisting of an X-OR gate (U8) with sINP and sOUT as its inputs. When the I/O operation is decoded and the selected address is on the bus, the control line decoder (U19) is enabled. The proper strobe lines are decoded by U19 with address A0 and sOUT, and are strobed to the UART during pWR* or pDBIN

BUS DRIVER LOGIC

Data from the S-100 bus is buffered onto the internal bi-directional data bus by octal buffer U32 whenever sINP is not high Data from the internal bi-directional bus is buffered onto the S-100 bus by U33 whenever a valid board enable and a pDBIN strobe both occur.

HARDWARE/SOFTWARE PROGRAMMING LOGIC

The Hardware/Software Programming logic consists of U35, U36, J9, and J10 Quad 'D' type latches (U35, U36, 74LS175) are reset by either POC or pRESET to a known state This establishes defined levels on one side of the jumper sockets (J9, J10) which can be wired to each of the four signal lines on the opposite side of the jumper socket. Since the latches bring out both Q and Q* outputs, each of the eight control lines can be tied either high or low for any power-on or reset parameter setting The control strobe output of U19 allows writing into these latches for software modification of the eight parameters by outputting a '1' to the bit corresponding to the parameter to be changed. Outputting a '0' to the bit will return it to its initial setting

BAUD RATE SELECT LOGIC

The Baud Rate Select Logic is the simplest section of the board and consists of the baud rate generator (23), a 5 0688 MHz crystal (X1), one half of dip switch S2, and the minus 5 volt regulator (R6 and D1) The baud rate is set in a binary fashion on positions 1-4 of S2 for both the transmit and receive sections of the UART. Positions 5-8 of S2 select the base interrupt rate for the interrupt timer

INTERRUPT LOGIC

The Interrupt Logic consists of two AND gates (U21) and two open collector inverters (U26). When the Hardware/Software programming logic is set so that the interrupts are enabled, a high level on either DAV or TBMT will generate a DATA AVAILABLE or TRANSMITTER BUFFER EMPTY interrupt through the open collector inverters. When the interrupt is processed and either the data read or written, the interrupt is removed from the bus.

SERIAL LINE LEVEL CONVERSION LOGIC

The Serial Line Level Conversion Logic consists of two main parts: the RS-232 - TTL level converters and the current loop and TTL level converters. All the signals from the channel connector J4 are brought out to jumper sockets J5 and J6 for user programming. All RS-232 level signals are taken from J5 and are fed to and from level converters U13 and U14 (1489 and 1488). The 1488 (the industry standard EIA RS-232-C line driver) converts the TTL level signals to the +12 and -12 volt signals to drive the transmitted data (TxD) and two RS-232 handshaking signals CA and CD. Holes for disc capacitors (C7-C9) are provided on the output of these drivers to limit slew rate to less than 30V/uSEC for compatibility with the RS-232-C specifications. For very short cables, capacitors with values up to 400 pF may be installed. For very long cables, no capacitance should be added due to the capacitance of the cables already limiting the slew rate. The 1489 (industry standard EIA RS-232-C line receiver) converts the +12 and -12 volt levels back to TTL levels for the UART and the 3 handshaking lines CB, CC, and CF (OPT.). Holes are provided on the board for adding the response control capacitors (C10-C13) for increased noise immunity.

The current loop and TTL level signals all enter and exit thru J6. The +IN and -IN signals are designed to feed opto-isolator U14 either through the on-board current source (R10), or directly from an external current source. The output of the opto-isolator is combined with the TTL IN signal, inverted (U27), ANDed (U30) with the data from the RS232 level converted data, and fed to the UART (U34) serial input line (SI). Transmit data (TxD) is inverted (U27), fed to J6 for TTL data and drives the LED of opto-isolator U15. The output of U15 is buffered by Q1-D2-R11 and fed to J6 where is uses either the on-board current source (R9) or an external current source to drive the +OUT and -OUT lines.

UART

The UART (U34) takes the parallel input data from the internal bus, serial parameters from the programming logic, the baud clock, and outputs serial data for the level conversion logic. It also takes the serial input data from the level converters, the baud clock, and the serial parameters, to yield parallel converted data for the internal bus as well as status through status buffer U24 and interrupts for use by the host processor.

THE PARALLEL SECTION

The parallel section consists of five major subsections: the I/O Port Select Logic, the Status Port, Interrupt Logic/Interrupt Mask Port, the Port Latches, and the Interrupt Timer.

I/O PORT SELECT LOGIC

Address line A2 thru A7 each feed one input of the 25LS2521 octal comparator (U31) with the other input connected to a section of the port select DIP switch S4. The input of the comparator is gated by the I/O detect logic described in the serial section. The output of the comparator enables the port decoder (U17), which generates the proper strobe pulses for the six latches, the status port and the interrupt mask port depending on the three select inputs (A0, A1, and sOUT) and when either a pWR* or pDBIN occurs.

STATUS PORT

The Status Port gates its information onto the internal bus with Hex Tri-State buffer (U18) when pin 9 of the port decoder (U17) strobes low. Data bits D0, D2, and D4 carry the status information from the input port on J1, J2, and J3 respectively. A high level on these lines indicates that data has been strobed into the input buffer and has not been read by the processor. Data bits D1, D3, and D5 carry the attention bit status from channels J1, J2, and J3 respectively. A high level on these lines indicates that the processor has output data to the ports that has not yet been accepted by the external device. A low on this input indicates that the data has been accepted. This bit has no significance when the output register is enabled at all times since the attention flag is being held clear. The status port always resides as the last port in the block of four parallel channels.

INTERRUPT LOGIC/INTERRUPT MASK PORT

The Interrupt Logic consists a quad 'D' type latch (U23), three 'D' type flip flops (U16 and U22a), four 2 input AND gates (U22), and four open collector inverters (U26). The quad latch is cleared on power-up or reset to a known state that can be jumpered across J8 to the inputs of the AND gates to act as enables for the interrupts. The latch can also be written into from the internal bus when strobed by decoder U17, allowing the alteration of the interrupt mask under software control Data bits D0, D1, and D2 control the interrupt enables for the channels on J1, J2, and J3 respectively. Data bit D3 controls the starting and stopping of the timer and will be discussed in a following section. A strobe bit from any of the input channels will set the appropriate 'D' flip flop, and if enabled will provide a high level to the O.C. inverter which drives the interrupt lines. When the input data is read from the latch, the 'D' flip flop is cleared and the interrupt is removed from the S-100 bus.

PORT LATCHES

The port latches (U2, U3, U5, U6, U9, and U19) accept data either from the internal bus or from an external device. 'D' flip flops U1, U7, and U11 act as the status flip flops for the above latches. When the input strobe passes thru the polarity select X-OR gates, the selected transition will latch the incoming data into the 74LS373 or LS374 and set the status flip flop. When this data is read by the processor, the enable strobe gates the data onto the internal bus and clears the status flag. When the processor outputs data to an output register, the clock inputs of the latch and the attention flip flop are strobed, the output strobes are generated and the attention line is set (if the output is not enabled), and the data is latched The attention flip flop is cleared when the output enable line enables the output register. The output strobes are as long as the pWR* strobe in the computer system.

INTERRUPT TIMER

The Interrupt Timer consists of one half of the baud rate generator (U20), a dual 4 bit counter (U29), an AND gate (U22) and an open collector inverter (U29). The output of the baud rate generator is divided by 16 by one half of the counter and the output is fed to the other half for further dividing and clearing. After power-up or reset, the second counter is held cleared until a '1' is written into the interrupt mask register bit D3. When enabled, the counter will increment and when the jumpered output goes high (J12), an interrupt is generated. When recognized, the enable counter should be cleared (removing the interrupt from the bus) by outputting a '0' and then a '1' to the interrupt mask bit D3. This action resets the counter and readys it for another interrupt.

Parts List

☐	(1)	Circuit board	

INTEGRATED CIRCUITS (Note: the following parts may have letter suffixes and prefixes along with key numbers given below).

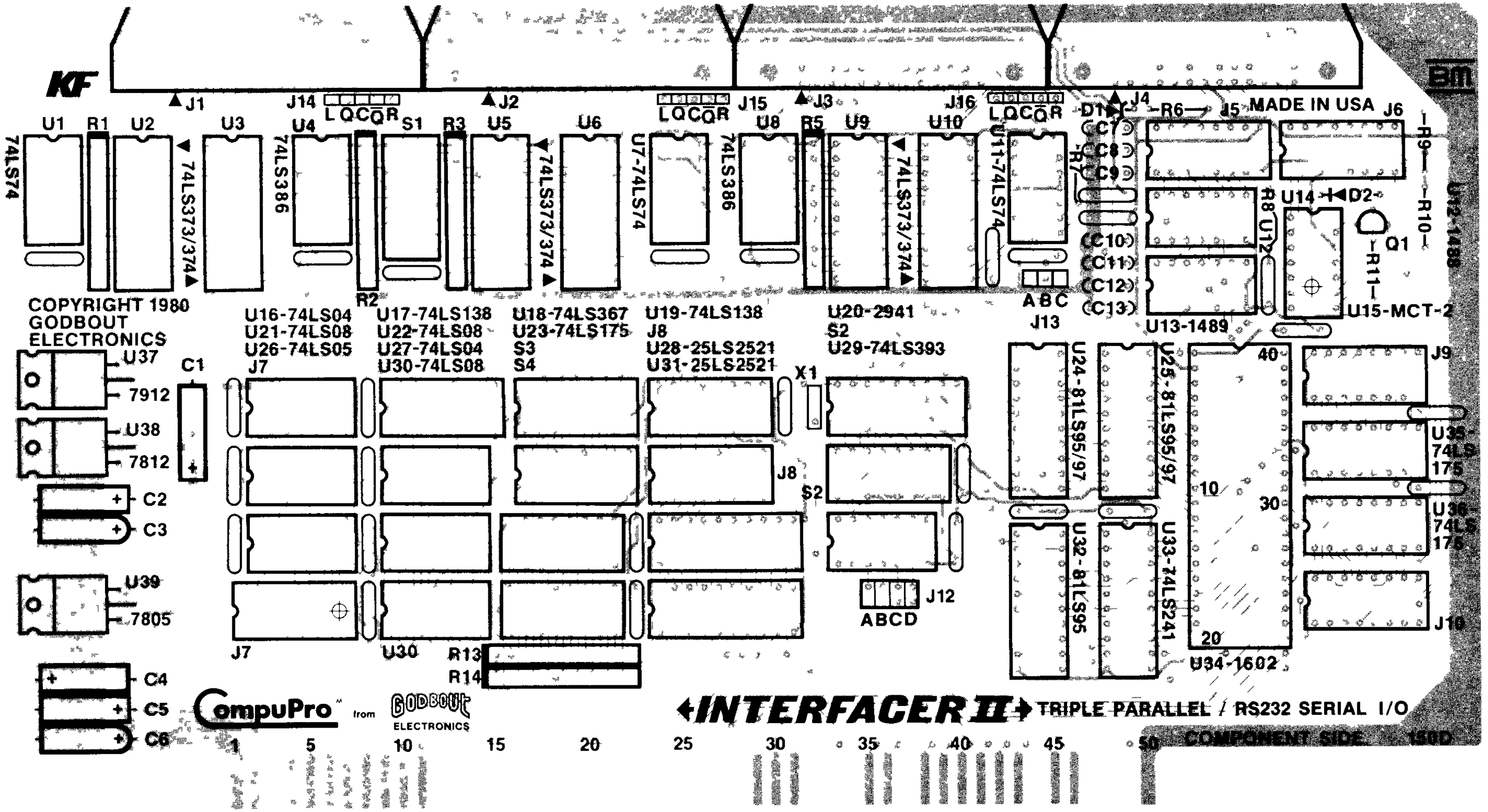
☐	(2)	74LS04 hex inverter	U16, U27
☐	(1)	74LS05 hex o.c. inverter	U26
☐	(3)	74LS08 quad AND gate	U21, U22, U30
☐	(3)	74LS74 dual 'D' flop	U1, U7, U11
☐	(2)	74LS138 3-8 decoder	U17, U19
☐	(3)	74LS175 quad 'D' latch	U23, U35, U36
☐	(1)	74LS241 octal bus driver	U33
☐	(1)	74LS367 hex bus driver	U18
☐	(3)	74LS373 octal latch	U2, U5, U9
☐	(3)	74LS374 octal 'D' latch	U3, U6, U10
☐	(2)	74LS386 quad X-OR gate	U4, U8
☐	(1)	74LS393 dual 4 bit counter	U29
☐	(2)	81LS95/97 octal bus driver	U24, U25
☐	(1)	81LS95 octal bus driver	U32
☐	(2)	25LS2521 octal comparator	U28, U31
☐	(1)	1602/1863 UART	U34
☐	(1)	2941 baud rate generator	U20
☐	(1)	1488 RS232 driver	U12
☐	(1)	1489 RS232 receiver	U13
☐	(2)	MCT-2 opto isolator	U14, U15
☐	(1)	7805 + 5V regulator	U39
☐	(1)	7812 + 12V regulator	U38
☐	(1)	7912 - 12V regulator	U37

OTHER ELECTRICAL COMPONENTS

☐	(1)	NPN transistor - 2N3904	Q1*
☐	(1)	1N914/806-36 signal diode	D2*
☐	(1)	1N751A 5V Zener diode	D1*
☐	(6)	SIPS resistor pack	R1, R2, R3, R5, R13, R14*
☐	(1)	470 ohm resistor	R8*
☐	(2)	560 ohm resistor	R9, R10*
☐	(3)	2.7K resistor	R6, R7, R12*
☐	(1)	4.7K resistor	R11*
☐	(1)	5 0688 MHz crystal	X1
☐	(4)	1.8 uF 35V tantalum cap	C1, C2, C4, C5
☐	(2)	39 uF 10V tantalum cap	C3, C6
☐	(27)	disc caps*	

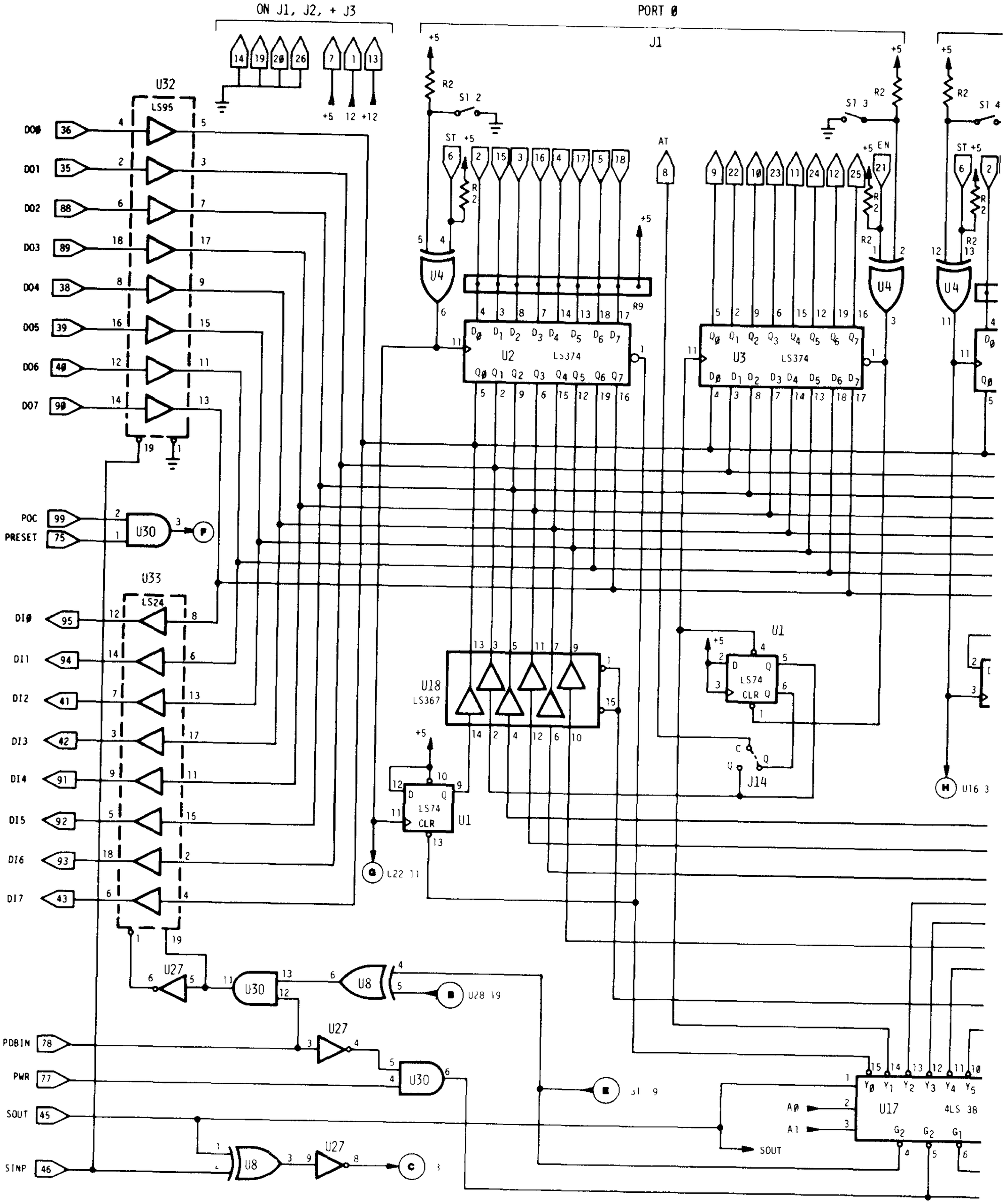
MECHANICAL COMPONENTS

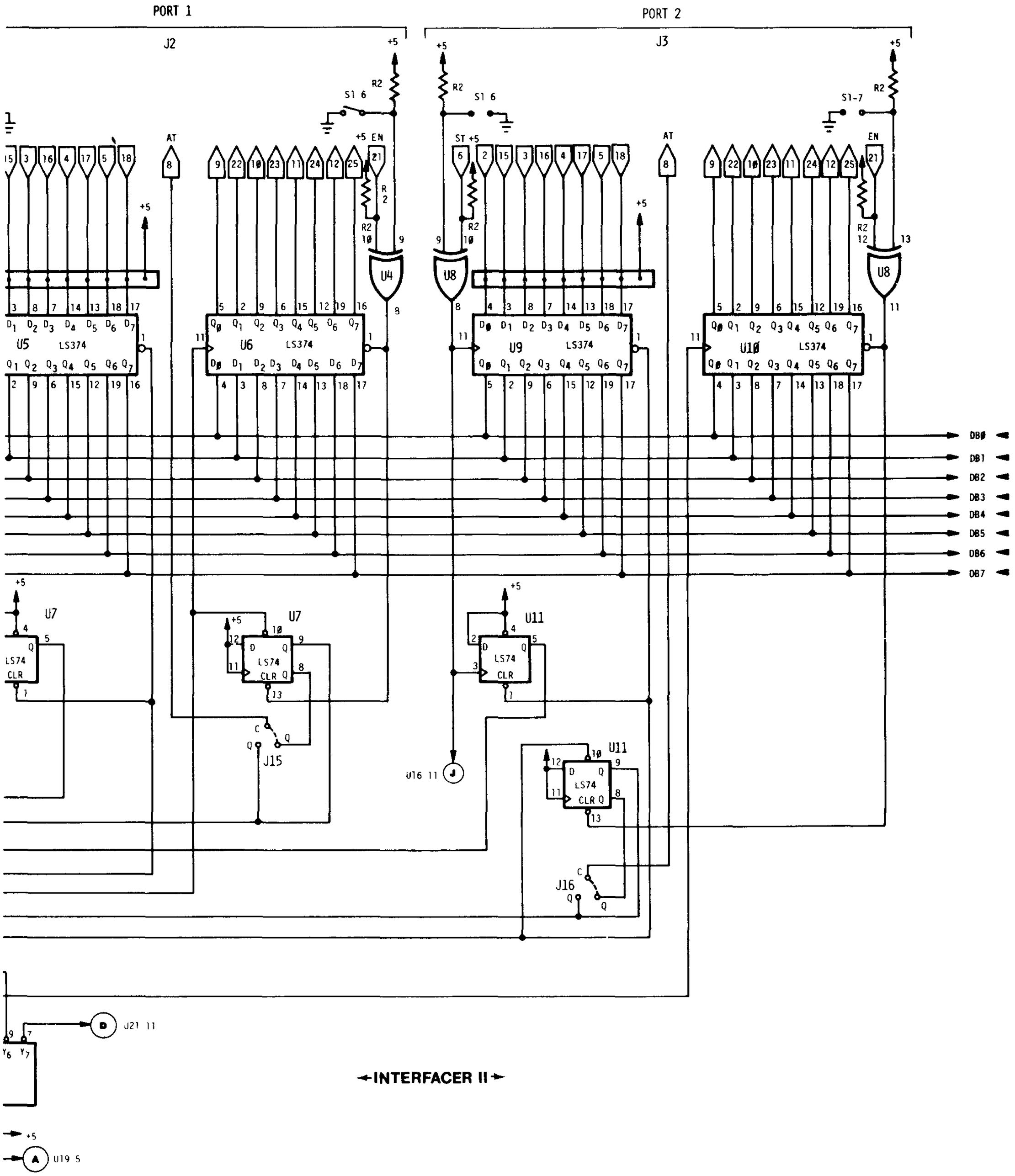
☐	(40)	low profile sockets*	
☐	(4)	dip switches 8-pin	S1, S4
☐	(1)	heat sink for U39	
☐	(3)	sets 6-32 hardware	
☐	(4)	26-pin I/O connector	J1 - J4
☐	(3)	16-pin dip platform	J5 - J7
☐	(3)	16-pin dip shunt	J8 - J10
☐	(1)	instruction book	



Component Layout

up


ON J1, J2, + J3
14 19 20 26 7 1 13
+5 12 +12
PORT Ø
J1
U32
LS95
DØØ 36
DØ1 35
DØ2 88
DØ3 89
DØ4 38
DØ5 39
DØ6 40
DØ7 90
POC 99
PRESET 75
U30
U33
LS24
DIØ 95
DI1 94
DI2 41
DI3 42
DI4 91
DI5 92
DI6 93
DI7 43
PDBIN 78
PWR 77
SOUT 45
SINP 46
U27
U8
U18
LS367
U2
LS374
U3
LS374
U4
LS74
CLR
U1
J14
AT
+5 EN
R2
R9
ST +5
U17
4LS 38
U16 3
U22 11
U28 19
31 9
SOUT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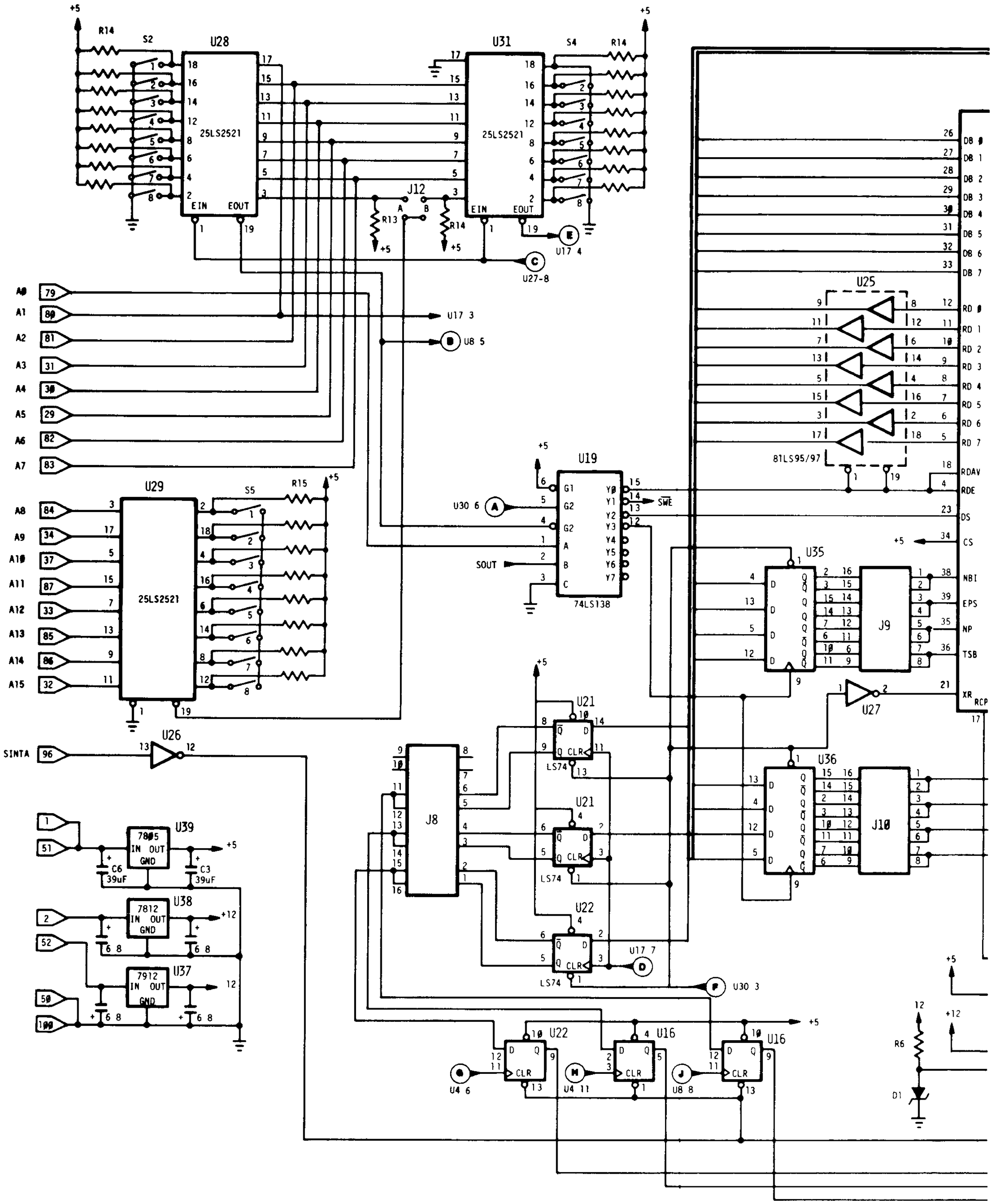
PORT 2
J2
J3
U5 LS374
U6 LS374
U9 LS374
U10 LS374
U4
U8
S1 6
S1-7
R2
AT
EN
ST +5
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
U7
U11
LS74
CLR
J15
J16
U16 11
J21 11
U19 5
INTERFACER II


+5
R14
S2
U28
25LS2521
EIN
EOUT
U31
S4
J12
A
B
R13
R14
U17 4
U27-8
U17 3
U8 5
A0
A1
A2
A3
A4
A5
A6
A7
U29
S5
R15
A8
A9
A10
A11
A12
A13
A14
A15
U26
SINTA
U39
7805
IN OUT
GND
C6
39uF
C3
39uF
U38
7812
U37
7912
+12
12
U19
74LS138
U30 6
SOUT
SWE
U21
LS74
U22
J8
J9
J10
U35
U36
U27
U17 7
U30 3
U4 6
U4 11
U8 8
U16
81LS95/97
DB 0
DB 1
DB 2
DB 3
DB 4
DB 5
DB 6
DB 7
RD 0
RD 1
RD 2
RD 3
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EPS
NP
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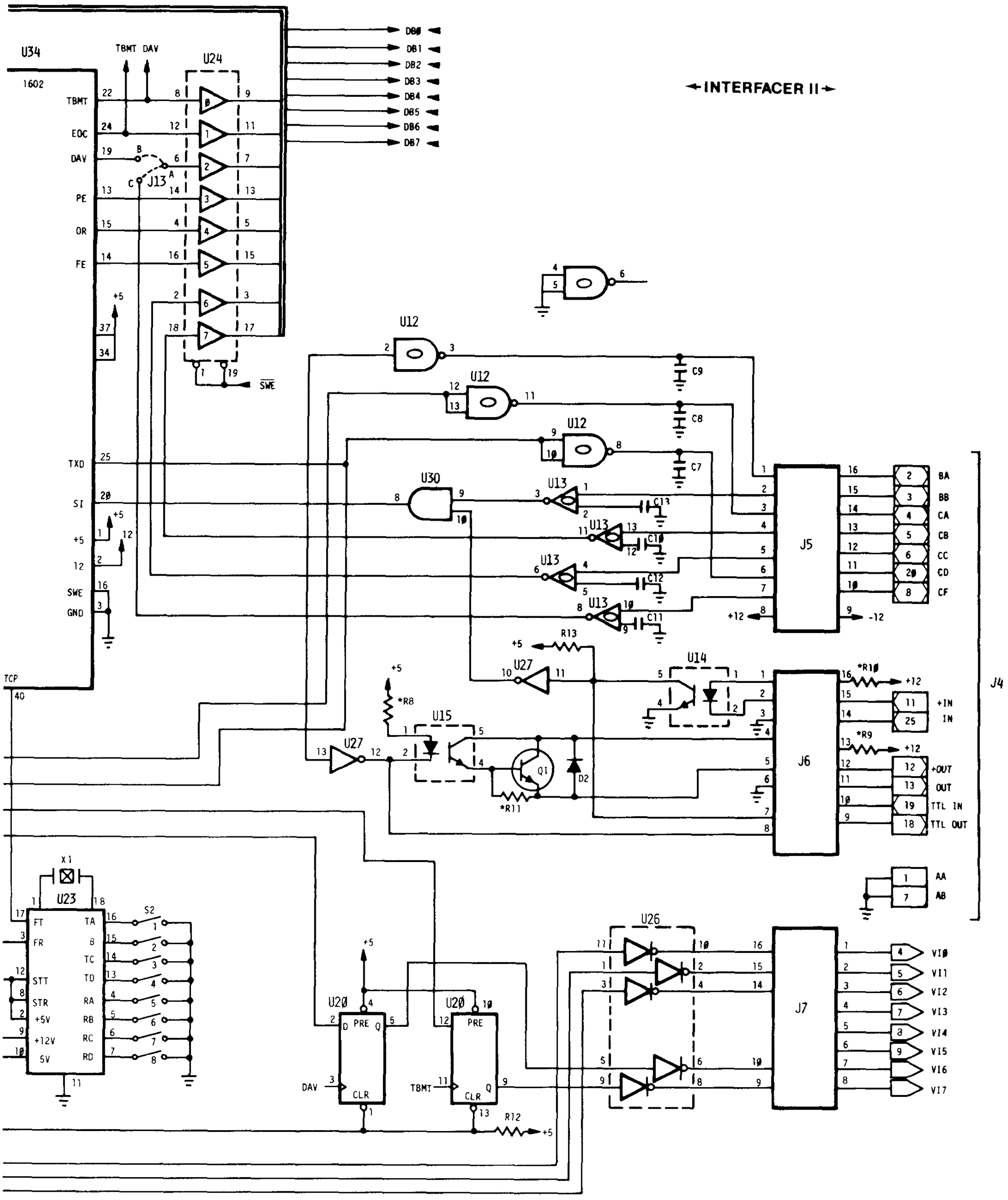
XR
RCP
R6
D1


U34
1602
TBMT
EOC
DAV
PE
OR
FE
TXD
SI
+5
12
SWE
GND
TCP
40
TBMT DAV
U24
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
J13
SWE
U12
C9
C8
C7
U30
U13
C13
C10
C12
C11
J5
BA
BB
CA
CB
CC
CD
CF
+12
-12
R13
U27
U14
*R8
U15
Q1
D2
*R11
*R10
*R9
J6
+IN
IN
+OUT
OUT
TTL IN
TTL OUT
J4
X1
U23
FT
FR
STT
STR
+5V
+12V
5V
TA
B
TC
TD
RA
RB
RC
RD
S2
U20
PRE
CLR
DAV
TBMT
R12
U26
J7
VI0
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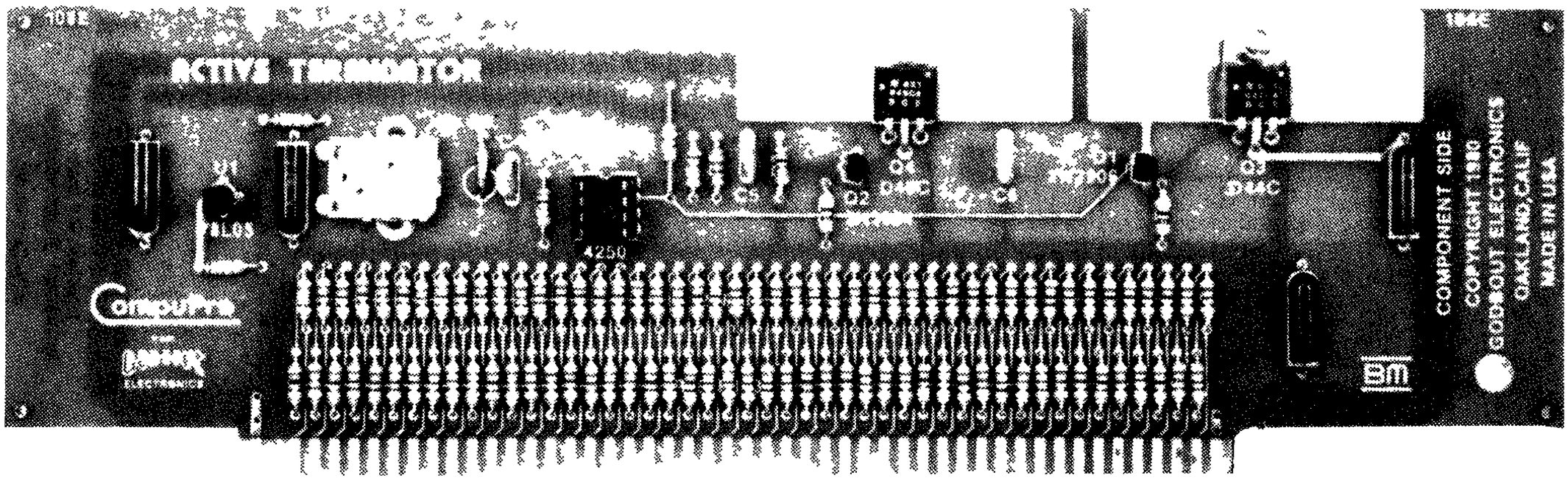
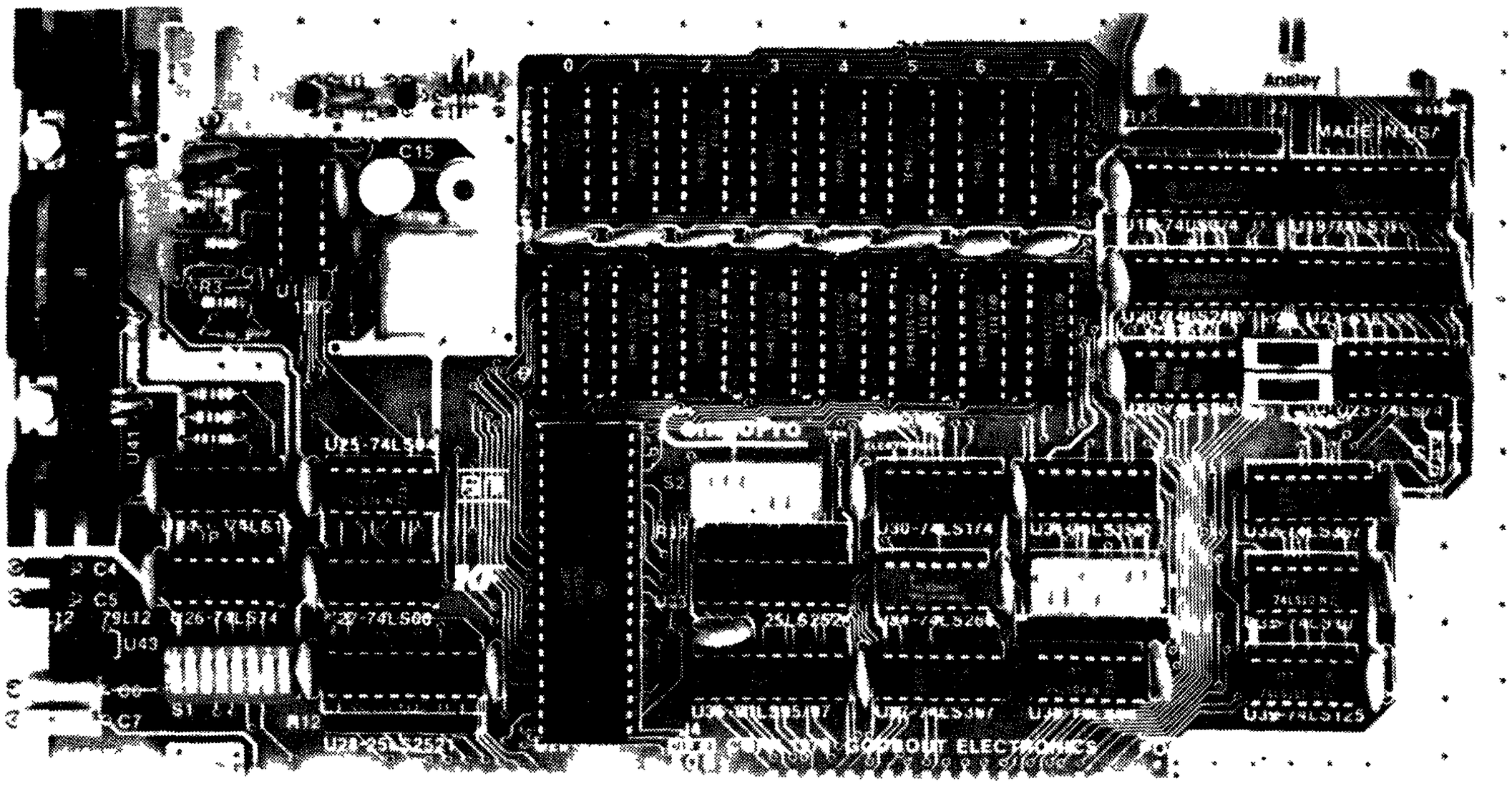
VI2
VI3
VI4
VI5
VI6
VI7
AA
AB

ACTIVE TERMINATOR



MANUAL ON PAGE 217

SPECTRUM
USER'S MANUAL



IEEE S-100

Full Function Graphics Board

with 8 K RAM & PARALLEL I/O

using 6847

144
mac

CompuPro™ from GODBOUT

ABOUT SPECTRUM

Congratulations on your purchase of SPECTRUM - a color graphics board designed specifically for full electrical and mechanical compatibility with the IEEE S-100 bus standard. The S-100 bus is the professional level choice for commercial, industrial and scientific applications. This bus provides for ready expansion and modification as the state of the computing art improves. We believe that this board with the rest of the S-100 portion of the CompuPro family is one of the best boards available for that bus.

Features, such as 8K of fast, low power static RAM, 24 bit addressing, a full duplex parallel port and a 75 ohm, RS-170 video output allow for maximum flexability at a reasonable price.

Thank you for choosing a CompuPro Product.... welcome to the club.

TECHNICAL OVERVIEW

This board incorporates proven static memory technology for the 8K x 8 screen memory of the 6847 color graphics generator. With the 6847, the user can select 10 different color modes of operation- from full alphanumerics with semigraphics to high density graphics.

Upon power-up, the SPECTRUM board behaves as a standard high speed 8K static RAM board - capable of running at 4Mhz with a Z-80 and 5Mhz with an 8085 or 8088. When graphics are required, the user alters the board programming through the Graphics Control Port. This port not only controls the board's operation as a RAM board or a graphics board, but graphics density, color set and alphanumerics/semi-graphics mode.

A 75 ohm video output is provided through an RCA type jack for direct connection to a color monitor, or through a four pin connector that can directly mate to any F.C.C. approved modulator. A programable wait state is provided in color grahics mode to compensate for the restricted timing requirements when the 6847 is in operation. 24 bit addressing is provided so that the graphics RAM can be removed from base page memory, and finally, a full duplex parallel port with full handshaking is provided for interfacing to keyboards, joysticks, LED's or anything requiring parallel data.

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky and MOS technology integrated circuits for reliably cool operation. All this and sockets for all IC's go onto a double sided, solder masked printed circuit board with a complete component layout legend.

MEMORY ADDRESS ASSIGNMENT

This board is addressable as one single 8K block, positionable on any 8K boundary as shown below.

SWITCH POSITION	FUNCTION
S3-1	ADDRESS A15
S3-2	ADDRESS A14
S3-3	ADDRESS A13
S3-4	MEMORY DISABLE
S3-5	WRITE ENABLE
S3-6	PHANTOM ENABLE
S3-7	PHASE 2 CLOCK SELECT
S3-8	WAIT STATE DISABLE

STARTING ADDRESS	SWITCH POSITION S3-1	S3-2	S3-3
0000H	ON	ON	ON
2000H	ON	ON	OFF
4000H	ON	OFF	ON
6000H	ON	OFF	OFF
8000H	OFF	ON	ON
A000H	OFF	ON	OFF
C000H	OFF	OFF	ON
E000H	OFF	OFF	OFF

The RAM on this board can be disabled and electrically removed from memory space by placing switch S3-4 in the ON position. For normal operation, switch S3-4 should remain OFF.

WRITE ENABLE SWITCH

Switch position S3-5 can be used to write protect the 8K block of memory. With S3-5 in the OFF position, the contents of the memory can be read, but cannot be written into. For normal operation, this switch should remain ON.

PHANTOM SWITCH

Switch position S3-6 can be used to PHANTOM the memory on this board out of memory space. With S3-6 in the ON position, a low level on the PHANTOM* line (pin 67) will disable the 8K block. For operation of this board in a mode where PHANTOM* has no effect, S3-6 should be kept OFF.

WAIT STATE SWITCH

Switch position S3-8 is used to disable the wait state circuit when running in graphics mode. In 2Mhz systems, this board is fast enough to run with no wait states - even in graphics mode. However, in systems running at 4 and 5Mhz, a wait state is required in graphics mode to insure reliable data transfer. Therefore, 2Mhz systems should run with S3-8 in the ON position (wait state disabled), and 4Mhz and up systems should have S3-8 turned OFF and the proper clock phase selected with S3-7. In all systems running at 5Mhz and below, this board will run with zero wait states in RAM mode.

With the wait state enabled, S3-7 should be set to provide the proper clock phase to the wait state generator. Typically, S3-7 should be in the OFF position when used with most S-100 standard CPU boards, however, some of the older processors might require it in the ON position. If you are getting reliable data transfers at greater than 3 Mhz, S3-7 is probably in the right position.

S3-7	CLOCK PHASE
ON	NORMAL PHASE 2 CLOCK
OFF	INVERTED PHASE 2 CLOCK

NOTE: If shipped with the high speed optional SM00308 or similar RAM chips, this board will run up to 8 Mhz without wait states in both RAM and GRAPHICS modes.

EXTENDED 24 BIT ADDRESSING

This board implements the proposed IEEE S-100 extended address lines A16 thru A23. With this feature, the user can place the RAM on this board in a location other than base page. As shipped, this board is set to use the extended address lines when decoding the board's location in the memory map. To disable this feature, a jumper must be installed at location J2 (in between U26 and U27 in the lower left corner of the board. When disabled, we suggest that you remove U28 (25LS2521) and place all 8 switches of S1 in the OFF position. Addressing is as shown below.

SWITCH POSITION	FUNCTION	
S1-1	ADDRESS A23	
S1-2	ADDRESS A22	
S1-3	ADDRESS A21	"ON" = "0"
S1-4	ADDRESS A20	
S1-5	ADDRESS A19	
S1-6	ADDRESS A18	"OFF" = "1"
S1-7	ADDRESS A17	
S1-8	ADDRESS A16	

PORT ADDRESS SELECTION

The SPECTRUM board contains two I/O ports to increase its flexability to the user. A full duplex parallel port (8 lines in and 8 lines out) is provided to interface to any type of parallel device. In addition, a Status/Control port is provided to observe the status of the parallel port and the graphics chip, and control the modes of the graphics display.

Switch S2 is used to select the address of the two ports, with the pair addressable at any location in the I/O map on any two port boundary. The Status/Control port resides at the selected address on S2, and the Data port resides at the selected address + 1.

SWITCH POSITION	FUNCTION	
S2-1	ADDRESS A7	"ON" = "0"
S2-2	ADDRESS A6	
S2-3	ADDRESS A5	
S2-4	ADDRESS A4	"OFF" = "1"
S2-5	ADDRESS A3	
S2-6	ADDRESS A2	
S2-7	ADDRESS A1	
S2-8	PORT DISABLE	"ON" = DISABLED

EXAMPLE: If the ports are set for F0H (1-4 and 8 OFF, 5-7 ON), then the Status/Control port will be at port F0H, and the Data port will be at port F1H.

STATUS/CONTROL PORT BIT ASSIGNMENT

The bit assignment for the Status and Control ports are as shown below. In depth descriptions of these bits will be covered in further sections.

DATA BIT	STATUS WORD	CONTROL WORD
D0	DAV	GM0
D1	DNT	GM1
D2	UNDEF.	GM2
D3	UNDEF.	A*/G
D4	UNDEF.	CSS
D5	UNDEF.	R*/G
D6	HS*	UNDEF.
D7	FS*	UNDEF.

THE DATA LINES

The parallel port on this board provides 8 input lines and 8 output lines for the user.

The 8 input lines (DI0-DI7) allow a full byte of TTL level data to be sampled by the processor when it is strobed into the input register U18 (74LS374) by an external strobe signal. All 8 lines are pulled to 5 volts through the pullup resitors in SIP R13, and are therefore read as a "1" if left disconnected.

The 8 output lines (DO0-DO7) are not only capable of sinking 24 Ma., but can be tri-stated through the use of the OUTPUT ENABLE LINE as described below. When new data is strobed into the output register, it is reflected on the ATTENTION LINE also described below.

INPUT STROBE LINE

The strobe line on the input port is used to latch new data into the input register. This line also sets the DAV status flag so that the processor can tell if data has been entered. Since the latch and the status flag are set on a level transition, the strobe polarity select switch (S4) should be set so that your data is valid at this time. With the select switch (S4) set in the center position, a low to high transition on the strobe line will latch the data and set the flag. With the select switch set in the left or right edge position, a high to low transition on the strobe line will latch the data and set the flag.

OUTPUT ENABLE LINE

The OUTPUT ENABLE LINE performs two different functions depending on the input level and the level select switch (S5). In handshaking operations, it is used not only to enable the output register U19 (74LS374), but to reset the attention bit (DNT) and inform the processor that data has been taken from the latch. In strobed operations, the OUTPUT ENABLE LINE is used to enable the output of the register at all times, and the ATTENTION LINE changes mode as described below. The polarity of this line is selectable via the level select switch (S5). When the select switch is in the center position, a low level signal on the ENABLE LINE will enable the output register. With S5 in either the left or right edge position, a high level on the ENABLE LINE will enable the output register. When the output register is enabled, the ATTENTION LINE becomes a strobe line, and when TRI-STATED, the ATTENTION LINE becomes a level selectable flag bit.

ATTENTION LINE

The ATTENTION bit is used to inform an external device that data is available. This bit operates in one of two modes in conjunction with the ENABLE LINE. In strobed operation, the ATTENTION LINE becomes an active high strobe bit when Q is jumpered to C, and the Q* to C trace is cut. The width of this pulse is the width of the system write strobe, PWR* (typically between 200 and 500 nanoseconds). In handshake operation, the data output register is normally TRI-STATED and the ATTENTION LINE changes level to inform the external device to perform a data transfer by enabling the output register. In addition, the DNT status bit goes high to inform the processor that the ATTENTION bit has been set. The ATTENTION LINE resets to the original level when the output register changes from TRI-STATE to enabled, and the DNT status bit is cleared. As shipped, the ATTENTION LINE is set to be negative true. To change this to a positive true level, cut the trace between C and Q* at J5, and jumper C and Q together.

I/O CONNECTOR PINOUTS

In addition to the 16 data lines and 3 control lines provided at the port connector, a small amount of current is available at the +5, +12, and -12 volt pins for powering external devices such as a keyboard or A to D converter. The total current is shown below, and care must be taken not to exceed these rating and over-heat the regulators.

+ 5 volts @ 150 ma.
+12 volts @ 40 ma.
-12 volts @ 40 ma.

DB-25 PIN NUMBER AND SIGNAL NAME

1- -12 VOLTS	9- DATA OUT 0	17- DATA IN 5
2- DATA IN 0	10- DATA OUT 2	18- DATA IN 7
3- DATA IN 2	11- DATA OUT 4	19- GROUND
4- DATA IN 4	12- DATA OUT 6	20- GROUND
5- DATA IN 6	13- +12 VOLTS	21- ENABLE
6- STROBE	14- GROUND	22- DATA OUT 1
7- +5 VOLTS	15- DATA IN 1	23- DATA OUT 3
8- ATTENTION	16- DATA IN 3	24- DATA OUT 5
		25- DATA OUT 7

COLOR GRAPHICS MODES

The SPECTRUM board initially powers-up as an 8K RAM board, and consequently must be told to enter the color graphics mode. To accomplish this, a logic "1" must be sent to data bit 5 of the CONTROL port. To exit from graphics mode back to RAM mode, a logic "0" should be sent to data bit 5 of the CONTROL port or the reset switch on your computer may be pressed which clears the CONTROL port to the power-up state.

Once in graphics mode, the CONTROL port may be altered to enter into any of the nine available modes of operation described below.

DATA BIT						MODE
D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	RAM MODE
1	X	0	X	X	X	ALPHA/SEMIGRAPHICS
1	0	X	X	X	X	COLOR SET A
1	1	X	X	X	X	COLOR SET B
1	X	1	0	0	0	64 X 64 COLOR GRAPHICS
1	X	1	0	0	1	128 X 64 GRAPHICS
1	X	1	0	1	0	128 X 64 COLOR GRAPHICS
1	X	1	0	1	1	128 X 96 GRAPHICS
1	X	1	1	0	0	128 X 96 COLOR GRAPHICS
1	X	1	1	0	1	128 X 192 GRAPHICS
1	X	1	1	1	0	128 X 192 COLOR GRAPHICS
1	X	1	1	1	1	256 X 192 GRAPHICS

"X" = don't care

ALPHA/SEMIGRAPHICS MODE

The 6847 contains an internal character generator capable of displaying 64 ASCII characters, which may be displayed in normal or inverted video on a character by character basis. Also, the 6847 is capable of entering a course graphics mode called SEMIGRAPHICS 4, in which a rectangle of eight by twelve dots is divided into four parts. The luminance of each of the four parts (L0 - L3), and the color of the rectangle (C0 - C2) is controlled as shown below.

ALPHANUMERICS CHARACTER SET

HEX DATA	ASCII CHAR	HEX DATA	ASCII CHAR	HEX DATA	ASCII CHAR	HEX DATA	ASCII CHAR
00H	@	10H	P	20H	(SP)	30H	0
01H	A	11H	Q	21H	!	31H	1
02H	B	12H	R	22H	"	32H	2
03H	C	13H	S	23H	#	33H	3
04H	D	14H	T	24H	$	34H	4
05H	E	15H	U	25H	%	35H	5
06H	F	16H	V	26H	&	36H	6
07H	G	17H	W	27H	'	37H	7
08H	H	18H	X	28H	(	38H	8
09H	I	19H	Y	29H	)	39H	9
0AH	J	1AH	Z	2AH	*	3AH	:
0BH	K	1BH	[	2BH	+	3BH	;
0CH	L	1CH	\	2CH	,	3CH	<
0DH	M	1DH	]	2DH	-	3DH	=
0EH	N	1EH	^	2EH	.	3EH	>
0FH	O	1FH	<-	2FH	/	3FH	?

NOTE: To display ASCII data in ALPHA mode on your SPECTRUM board, a 40H bias must be subtracted from ASCII codes 40H thru 7FH to form the compacted 6 bit code for the 6847's internal character generator.

ALPHA/SEMIGRAPHICS DATA FORMAT

The alphanumeric data shown above should be configured as shown below in the sample data word. To display a standard video character, data bit 6 should be a "0". For an inverted character, data bit 6 should be a "1". To display alphanumeric characters, data bit 7 should be a "0", and to enter SEMIGRAPHICS 4 mode, data bit 7 should be a "1".

DATA BIT	ALPHA FORMAT	SEMIGRAPHICS FORMAT
D0	DATA 0	L0
D1	DATA 1	L1
D2	DATA 2	L2
D3	DATA 3	L3
D4	DATA 4	C0
D5	DATA 5	C1
D6	INVERT	C2
D7	0	1

SEMIGRAPHICS FORMAT

```
 ---------      -----------------------
| L3 | L2 |    |D7|D6|D5|D4|D3|D2|D1|D0|
|____|____|    |--|--|--|--|--|--|--|--|
|    |    |    |1 |C2|C1|C0|L3|L2|L1|L0|
| L1 | L2 |     -----------------------
 ---------        "L" = "0" = COLOR OFF
                  "L" = "1" = COLOR ON
```

COLOR BITS C2 C1 C0	INTENSITY LX	COLOR SELECTED
X X X	0	BLACK
0 0 0	1	GREEN
0 0 1	1	YELLOW
0 1 0	1	BLUE
0 1 1	1	RED
1 0 0	1	BUFF (GRAY)
1 0 1	1	CYAN
1 1 0	1	MAGENTA
1 1 1	1	ORANGE

COLOR GRAPHICS BIT MAPPING

Modes described above as COLOR GRAPHICS modes will have their data bits mapped out on the screen as described below. The pixels are mapped across the screen, starting with byte 0 of the graphics RAM, from the upper left corner of the T.V. picture - across then down - to the lower right corner of the picture.

PIXEL NUMBER

```
 -----------
|E3|E2|E1|E0|
 -----------
```

COLOR MAP

```
 -----------------------
| E3  | E2  | E1  | E0  |
 -----------------------
|C1|C0|C1|C0|C1|C0|C1|C0|
 -----------------------
```

CSS = "0" C1	C0	COLOR	CSS = "1" C1	C0	COLOR
0	0	GREEN	0	0	BUFF (GRAY)
0	1	YELLOW	0	1	CYAN
1	0	BLUE	1	0	MAGENTA
1	1	RED	1	1	ORANGE
BORDER = GREEN			BORDER = BUFF (GRAY)		

GRAPHICS BIT MAPPING

Modes described above as GRAPHICS modes will have their data bits mapped out on the screen as described below. The pixels are mapped across the screen, starting with byte 0 of the graphics RAM, from the upper left corner of the T.V. picture - across then down - to the lower right corner of the picture. In this mode, each data bit maps directly into a pixel as shown.

PIXEL/INTENSITY MAP

```
 -----------------------
|L7|L6|L5|L4|L3|L2|L1|L0|    INTENSITY BIT
|--|--|--|--|--|--|--|--|
|D7|D6|D5|D4|D3|D2|D1|D0|    DATA BIT
 -----------------------
```

CSS = "0" LX	COLOR	CSS = "1" LX	COLOR
0	BLACK	0	BLACK
1	GREEN	1	BUFF (GRAY)
BORDER = GREEN		BORDER = BUFF (GRAY)	

COLOR GRAPHICS MODE DESCRIPTION SUMMARY

HORIZ.	VERT.	BITS/PIXEL	MAX/RAM	GM2	GM1	GM0
64 X	64	2	1K BYTE	0	0	0
128 X	64	2	2K BYTES	0	1	0
128 X	96	2	3K BYTES	1	0	0
128 X	192	2	6K BYTES	1	1	0

GRAPHICS MODE DESCRIPTION SUMMARY

HORIZ.	VERT.	BITS/PIXEL	MAX/RAM	GM2	GM1	GM0
128 X	64	1	1K BYTE	0	0	1
128 X	96	1	1.5K BYTES	0	1	1
128 X	192	1	3K BYTES	1	0	1
256 X	192	1	6K BYTES	1	1	1

USING THE 6847 STATUS BITS

The 6847 provides two status lines to inform the user that it is currently scanning a nonactive portion of the display. This provides a convienient way for the user to update the display without causing any noticable flicker or tearing of the picture. To accomplish this, the user must test the HS* and the FS* signals from the status port. Care must be taken to test these bits properly, as they are active low signals.

NAME	MEANING AND DESCRIPTION	DATA BIT	PULSE WIDTH
HS*	HORIZONTAL SYNC PERIOD	D6	4.9us
FS*	VERTICAL SYNC PERIOD	D7	1.6ms

INITIAL ADJUSTMENTS

As shipped, the SPECTRUM board should require no initial adjustments. However, as components age and change values, the initial adjustment of variable capacitor C15 may need to be altered in order to provide the proper colors described in a previous section. At this point, the user should fill the screen with some large areas of solid color. For example, in SEMIGRAPHICS mode, fill two lines with each color so that all 8 colors are visible, and adjust C15 so that the proper colors appear in the proper locations.

If the optional 10K ohm resistor R5 has been installed, it may be adjusted with an oscilloscope until the clock signal (pin 8, U25) is a square wave. If an oscilloscope is unavailable, adjust it until ALPHANUMERIC characters are as clear as possible. At this point, no other adjustments need to be made on the board.

PICTURE ADJUSTMENTS

For the best possible picture, minor adjustments will probably need to be made to the color monitor or television.

Monitors will most likely require adjustment of the Video Level control and the Video Offset control (if provided) for the sharpest picture. The Tint control should be adjusted if C15 did not provide enough range, and the Color control should be adjusted for the most attractive color saturation and picture quality possible. Brightness and Contrast should be adjusted to provide the clearest characters and most pleasing display.

Color televisions with R.F. modulators should follow the same instuctions as above, except that the Video Level adjustment will probably be on the R.F. modulator unit.

VIDEO OUTPUT CONNECTORS

1. J1 - RCA JACK

RCA connector J1 provides 75 ohm video output for connection to a video monitor or television that requires a composite video signal. Care should be taken to insure a clean signal by using coaxial cable for the interconnection. The signal provided by this output is approximately 1.5 volts peak to peak, with sync tips at 0 volts, black at 0.7 volts and white at 1.5 volts. Keep in mind that these values are only approximate, and that component variations will cause these levels to shift a small amount.

2. J4 - FOUR PIN MALE CONNECTOR

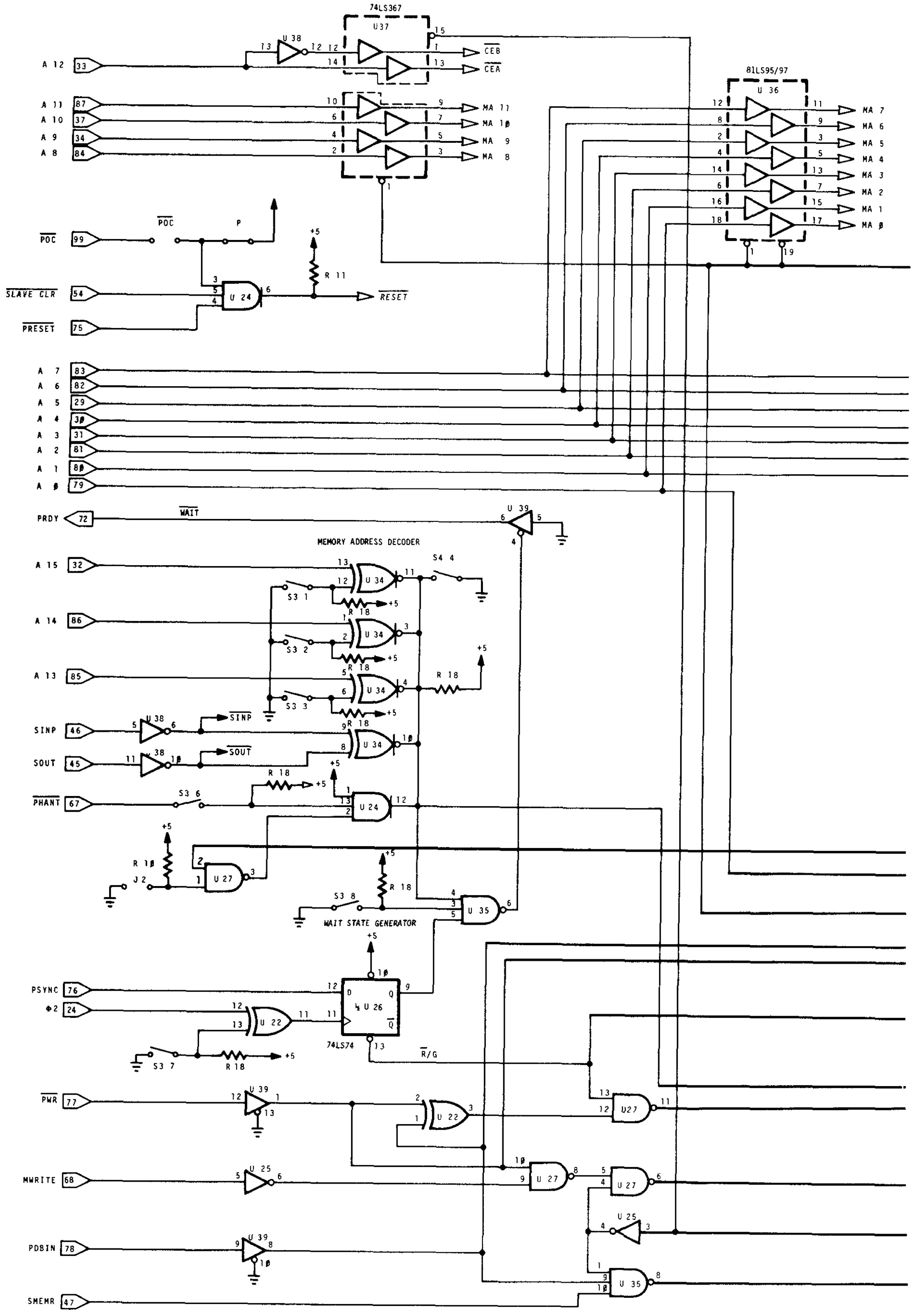
The four pin connector at J4 is provided for interfacing to F.C.C approved R.F. type modulators. The pin connections on the SPECTRUM board are listed below, and will mate directly with some commercially available modulators.

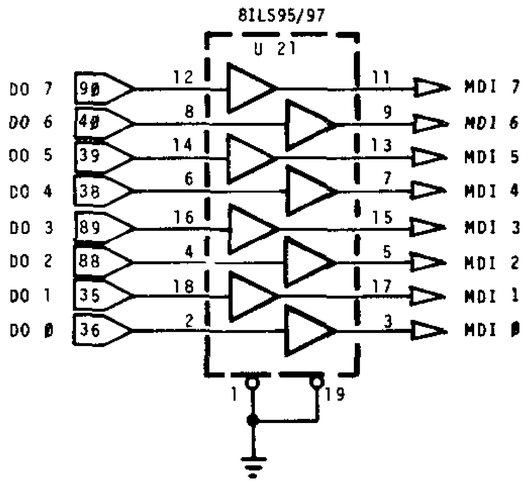
PIN NUMBER	SIGNAL
1	GROUND
2	75 ohm VIDEO
3	NO CONNECTION
4	+ 12 VOLTS

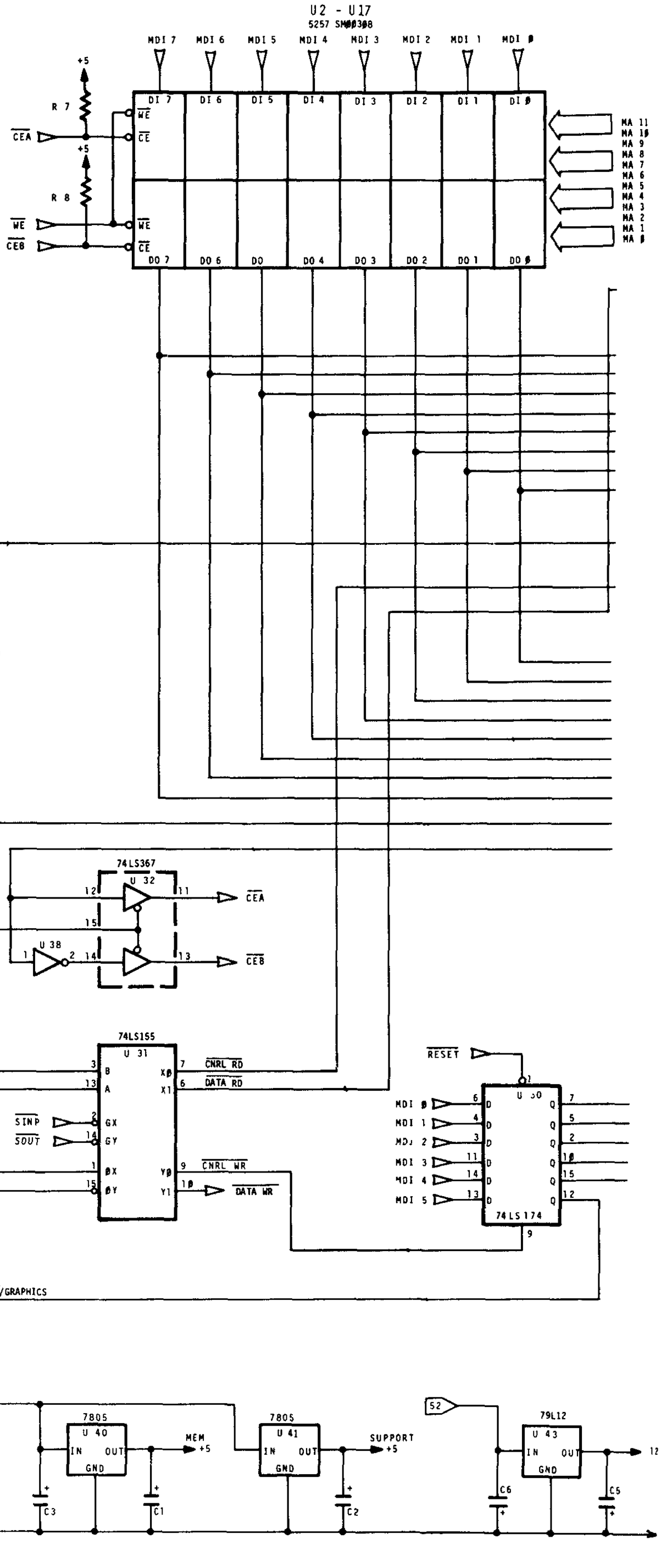
NOTE: Always insure that if using an R.F. modulator, that you use an F.C.C. approved type with an isolation switch. If not using an isolation switch, make sure that you completely remove your antenna lead in from the terminals on your television.

FOR BEST RESULTS. . . .

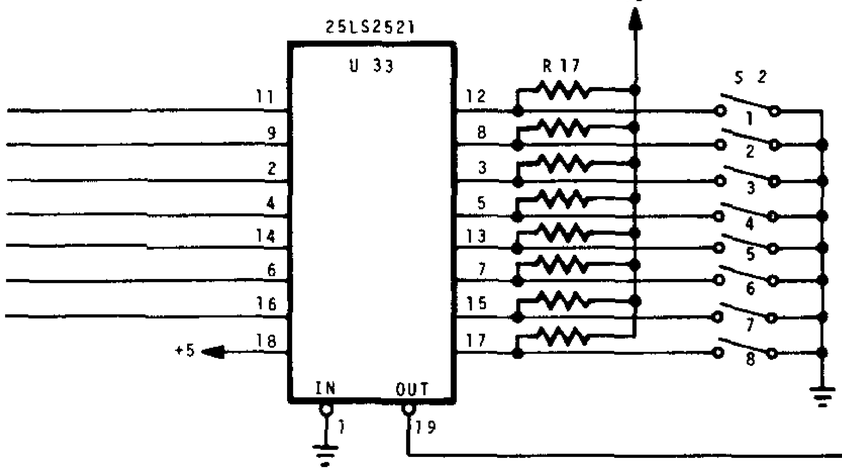
If not using a computer grade color monitor for displaying the output of your SPECTRUM board, a good quality television is a must. The old clunker that nobody wanted and the $149 wonder at the discount store probably won't give you the quality picture that you want to see. So, if your going to buy a television, new or used, get a good quality one that is 100% solid state, has good high voltage regulation, has a transformer (for safety's sake!), and has D.C. restored video. Look for one that has a sharpness control and a control called Black Level (this is a good indication that the set has D.C. video restoration). Zenith, RCA, and SONY make excellent small color televisions that are a great addition to any home when not used for color graphics.


74LS367
U37
U 38
A 12
33
CEB
CEA
A 11
87
A 10
37
A 9
34
A 8
84
MA 11
MA 10
MA 9
MA 8
81LS95/97
U 36
MA 7
MA 6
MA 5
MA 4
MA 3
MA 2
MA 1
MA 0
POC
99
P
+5
R 11
SLAVE CLR
54
U 24
RESET
PRESET
75
A 7
83
A 6
82
A 5
29
A 4
30
A 3
31
A 2
81
A 1
80
A 0
79
PRDY
72
WAIT
U 39
MEMORY ADDRESS DECODER
A 15
32
A 14
86
A 13
85
S4 4
S3 1
S3 2
S3 3
U 34
R 18
SINP
46
SINP
SOUT
45
SOUT
PHANT
67
S3 6
U 24
R 10
J 2
U 27
S3 8
R 18
U 35
WAIT STATE GENERATOR
PSYNC
76
Φ2
24
U 22
74LS74
½ U 26
S3 7
R/G
PWR
77
MWRITE
68
U 25
PDBIN
78
SMEMR
47

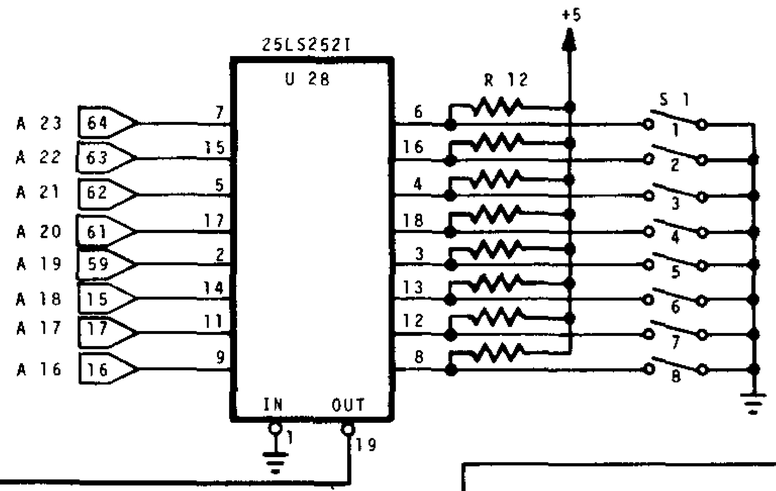


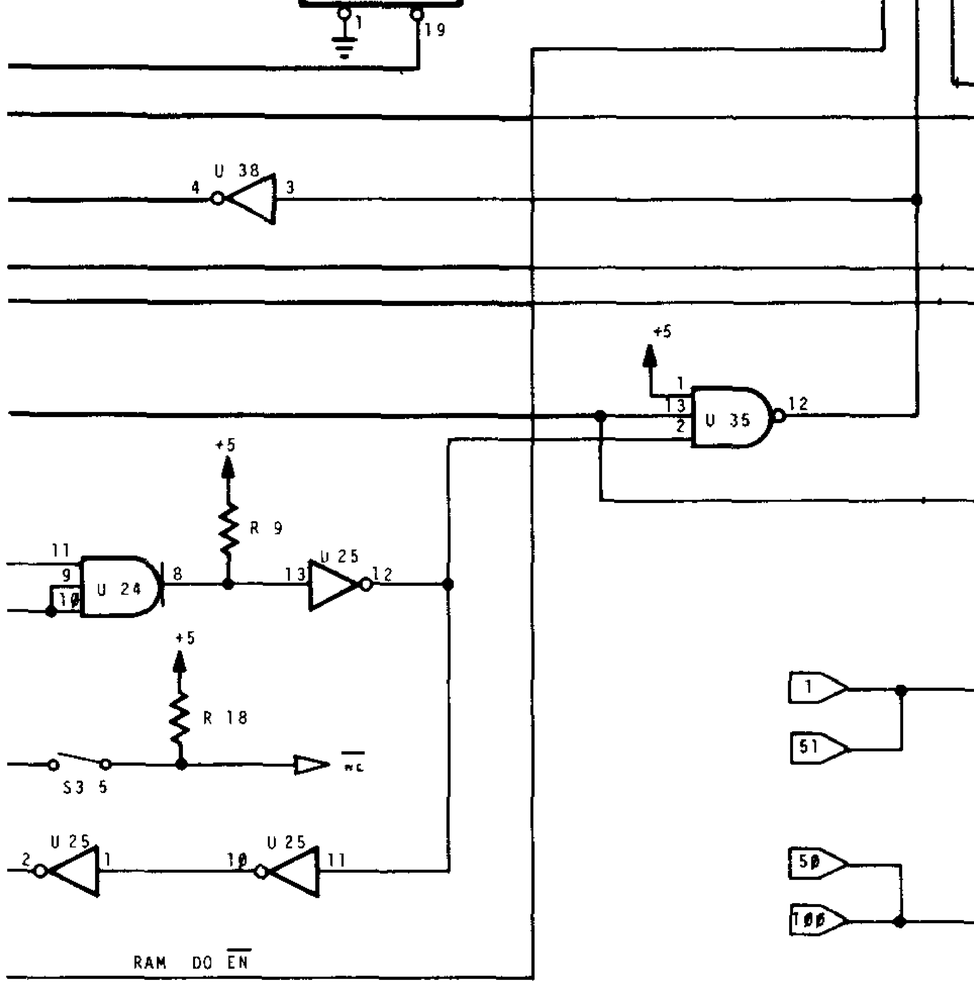


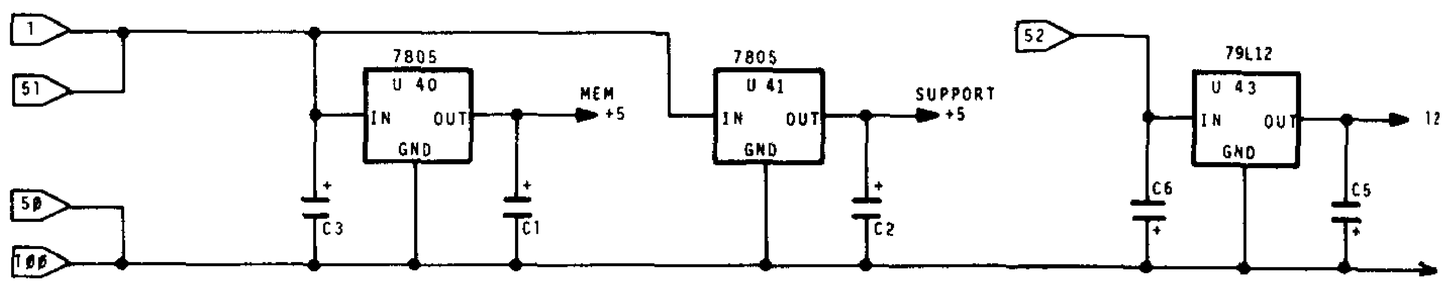
PORT ADDRESS DECODER



EXTENDED 24 BIT ADDRESS DECODER







STANDARD I/O PARALLE

U 18 74LS374

U 19 74LS374

J 3

74LS241 U 20

U 36

U 32 74LS367

U 29 6847

74LS74 ½ U 23

U 22

U 25

U 1 1372

78L12 U 42

R 13 R 5 R 3 S 4 R 14 R 16 S 5

MDI Ø MDI 1 MDI 2 MDI 3 MDI 4 MDI 5 MDI 6 MDI 7

DI 7 DI 6 DI 5 DI 4 DI 3 DI 2 DI 1 DI Ø

DATA WR

C 8 C 13 C 9 R 1 C 6 C 5 X 1 C 4 R 5 (OPTIONAL) R 4 D 1 R 2 R 19 C12 C11 Q 1 Q 2 R 20 R 22 R 21 J 1 J 4 J 5 C7

SPECTRUM

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CIRCUIT DESCRIPTION

The heart of the SPECTRUM board consists of a MOS LSI color video display generator. This display generator performs the scanning of the refresh display RAM and processes the fetched data into NTSC compatable color video signals for display on standard televisions and monitors. For an understanding of the operation of SPECTRUM, it can be roughly broken down into five separate subsections: the INTERNAL DATA BUS, the MEMORY DECODE LOGIC, the INTERNAL ADDRESS BUS, the PARALLEL I/O PORTS AND LOGIC, and the GRAPHICS GENERATOR AND VIDEO CIRCUITRY.

INTERNAL DATA BUS

The INTERNAL INPUT DATA BUS consists of octal input buffer IC21, which provides buffered data to the RAM, the PARALLEL I/O PORT and the GRAPHICS CONTROL PORT. This bus is active at all times, and data is latched from it only when the RAM or I/O ports are selected.

The INTERNAL OUTPUT DATA BUS is directly connected to the S-100 DI bus, and is driven by three separate output buffers. The RAM output is driven through octal buffer IC20, the parallel data is driven through octal latch IC18, and the board status through hex buffer IC32. All three of these buffers remains in the TRI-STATE condition until selected, and all are capable of 24ma. drive current.

MEMORY DECODE LOGIC

The MEMORY DECODE LOGIC consists of circuitry that detects a board select, and circuitry that decodes valid RAM strobe signals.

The board select logic consists primarily of IC34 and IC24, which decode A13-A15 for the RAM address, sINP and sOUT for memory reference, ADDRESS EXTEND for 24 bit addressing and PHANT* for PHANTOM decode. This signal is further gated with pWR*, pDBIN, and R*/G to decode a Valid Board Select (VBS) signal when in GRAPHICS mode. In RAM mode, pWR* and pDBIN are ignored when generating VBS.

Valid RAM strobe signals are generated by gating VBS with pDBIN and sMEMR for RAM Data Output Enable (RAM DOEN*) and pWR* and MWRT for WRITE ENABLE (WE*). These are used to enable the RAM data output buffer and write data into the RAM respectively.

VBS is also used with R*/G and IC26 to generate a wait state when in GRAGHICS mode and directly with IC37 to enable the chip select logic for the RAM.

INTERNAL ADDRESS BUS

The INTERNAL ADDRESS BUS is a dual bus that can be controlled by the 6847 GRAPHICS GENERATOR or by the S-100 bus. In normal operation, the 6847 has control of the address lines since it is constantly scanning the memory for display information, and the S-100 address drivers, IC36 and IC37, are TRI-STATED. When the RAM is accessed by the host computer, the 6847 address bus is TRI-STATED and the S-100 address drivers are given control to perform a memory read or write. As soon as this action is completed, the 6847 regains control of the address bus. (NOTE: since the 6847 depends on a constant stream of picture data from the RAM, accessing the display RAM during active display time will cause disruption of the display as incorrect data is forced onto the data bus. It is best to access the RAM during inactive display time as no picture disruption will occur.)

PARALLEL I/O PORTS AND DECODE LOGIC

The I/O ports are enabled when octal comparator IC33 decodes the proper address on the S-100 bus and decoder IC31 determines that an I/O read or write is occuring. The four decoded signals select whether a data or status read or a data or control write is to occur. In the read case, this signal is used to gate the data onto the S-100 bus, and in the write case, this signal is used to latch the data into the appropriate register.

The external data input register, IC18, is a positive edge triggered octal latch fed by the X-OR gate (IC22) acting as a programmable inverter. As data is latched into the register by a transition on the STROBE LINE, the DAV flag bit is set (IC23) to inform the processor that new data has been entered. The flag is cleared and data gated onto the bus when an I/O data read occurs.

The external data output register, IC19, is a positive edge triggered octal latch that accepts data when an I/O data write occurs. At the same time, the ATTENTION flag is set to inform an external device that that new data is available. The OUTPUT ENABLE line is fed through an X-OR (IC22) acting as a programmable inverter to enable the output data and reset the ATTENTION flag.

The graphics control data ia latched into hex latch (IC30) by a transition on the I/O control write line (CNRL WR*) and the status is gated onto the data bus through IC32 with the I/O status read signal (STAT RD*).

GRAPHICS GENERATOR AND VIDEO CIRCUITRY

The 6847 graphics generator (IC29), scans the address bus and fetches the data made available on the data bus. The outputs provided include several status/timing signals in addition to the composite video and color vector voltages used by chroma encoder IC1 (1372). The chroma encoder provides the main timing clock for the graphics generator and encodes the composite video and color vectors into a NTSC color encoded signal that is buffered to provide a low impedence video output. Crystal X1 forms the basis for a precise 3.579545 Mhz oscillator and Q1 and Q2 buffer the video output of the 1372 to provide a 75 ohm output impedence for connection to a monitor or an F.C.C approved R.F. modulator.

MEMORY TESTING ROUTINE

Figure 1.

```
3000 21 00 40            0010 STRT LXI  H,4000H
3003 3E A0               0020 END  MVI  A,0A0H
3005 32 6E 30            0030      STA  FIN
3008 3E 10               0040      MVI  A,10H
300A 84                  0050      ADD  H
300B 4F                  0060      MOV  C,A
300C 16 00               0070      MVI  D,0
300E 1E FF               0080      MVI  E,0FFH
3010 22 65 30            0090 DONE SHLD STAD
3013 AF                  0100      XRA  A
3014 47                  0110      MOV  B,A
3015 7B                  0120 SCND MOV  A,E
3016 5A                  0130      MOV  E,D
3017 57                  0140      MOV  D,A
3018 79                  0150      MOV  A,C
3019 2A 65 30            0160      LHLD STAD
301C 72                  0170 FILL MOV  M,D
301D 23                  0180      INX  H
301E BC                  0190      CMP  H
301F C2 1C 30            0200      JNZ  FILL
3022 2A 65 30            0210      LHLD STAD
3025 73                  0220 NEXT MOV  M,E
3026 7B                  0230      MOV  A,E
3027 BE                  0240      CMP  M
3028 C2 6F 30            0250      JNZ  FAIL
302B 79                  0260      MOV  A,C
302C 23                  0270      INX  H
302D 94                  0280      SUB  H
302E C2 4D 30            0290      JNZ  NDON
3031 B8                  0300      CMP  B
3032 4A                  0310      MOV  B,H
3033 CA 15 30            0320      JZ   SCND
3036 3A 66 30            0325      LDA  STAD+1
3039 00                  0330 MARK NOP
303A 00                  0331      NOP
303B 00                  0332      NOP
303C 3A 6E 30            0340      LDA  FIN
303F B9                  0350      CMP  C
3040 CA 00 30            0360      JZ   STRT
3043 79                  0370      MOV  A,C
3044 67                  0380      MOV  H,A
3045 2E 00               0390      MVI  L,0
3047 C6 10               0400      ADI  10H
3049 4F                  0410      MOV  C,A
304A C3 10 30            0420      JMP   DONE
304D 22 67 30            0430 NDON SHLD NXAD
3050 7A                  0440 LOPB MOV  A,D
3051 BE                  0450 LOPA CMP  M
3052 C2 6F 30            0460      JNZ  FAIL
3055 2C                  0470      INR  L
3056 C2 51 30            0480      JNZ  LOPA
3059 79                  0490      MOV  A,C
305A 24                  0500      INR  H
305B BC                  0510      CMP  H
305C C2 50 30            0520      JNZ  LOPB
305F 2A 67 30            0530      LHLD NXAD
3062 C3 25 30            0540      JMP  NEXT
3065                     0550 STAD DS   2
3067                     0560 NXAD DS   2
3069                     0570 FDE  DS   2
306B                     0580 FHL  DS   2
306D                     0590 FOUT DS   1
306E                     0600 FIN  DS   1
306F 22 6B 30            0610 FAIL SHLD FHL
3072 32 6D 30            0620      STA  FOUT
3075 7E                  0630      MOV  A,M
3076 32 6E 30            0640      STA  FIN
3079 EB                  0650      XCHG
307A 22 69 30            0660      SHLD FDE
307D C3 7D 30            0670 SHLT JMP SHLT
3080                     0680 *
```

Parts List

- ☐ (1) Circuit board

INTEGRATED CIRCUITS (NOTE: the following parts may have letter suffixes and prefixes along with the key numbers given below).

☐	(1)	74LS00 quad 2 input NAND	(U27)
☐	(2)	74LS04 hex inverter	(U25,U38)
☐	(1)	74LS10 triple 3 input NAND	(U35)
☐	(1)	74LS15 triple 3 in. OC NAND	(U24)
☐	(2)	74LS74 dual D flip flop	(U23,U26)
☐	(1)	74LS86 quad X-OR	(U22)
☐	(1)	74LS125 quad TS buffer	(U39)
☐	(1)	74LS155 decoder	(U31)
☐	(1)	74LS174 hex register	(U30)
☐	(1)	74LS241 octal bus driver	(U20)
☐	(2)	74LS367 hex TS buffer	(U32,U37)
☐	(2)	81LS95 octal bus driver	(U21,U36)
☐	(1)	25LS2521 octal comparator	(U33)
☐	(16)	5257 4K x 1 static RAM	(U2-U17)
☐	(1)	6847 color graphics gen.	(U29)
☐	(1)	1372 color video encoder	(U1)
☐	(2)	7805 5 volt regulator	(U40,U41)
☐	(1)	78L12 12 volt regulator	(U42)

OTHER ELECTRICAL COMPONENTS

☐	(1)	2N3906 transistor	(Q1)
☐	(1)	2N3904 transistor	(Q2)
☐	(1)	1N4148 or similar diode	(D1)
☐	(1)	crystal, 3975.545 Khz	(X1)
☐	(1)	trimmer capacitor	(C15)
☐	(3)	39uf, 10v tant. cap.	(C1-3)
☐	(2)	3.3uf, 15v tant. cap.	(C4,C13)
☐	(1)	1.8uf, 35v tant. cap.	(C7)
☐	(1)	.1uf disc cap.	(C9)
☐	(3)	.01uf disc cap.	(C8,C10,C14)
☐	(1)	100pf disc cap.	(C12)
☐	(1)	47pf disc cap.	(C16)
☐	(26)	disc caps.	
☐	(1)	56 ohm res.	(R21)
☐	(1)	360 ohm res.	(R4)
☐	(2)	750 ohm res.	(R1,R19)
☐	(1)	1K ohm res.	(R22)
☐	(1)	1.8K ohm res.	(R2)
☐	(7)	2.7K ohm res.	(R7-11,R15-16)
☐	(1)	3.3K ohm res.	(R20)
☐	(1)	5.6K ohm res.	(R6)
☐	(2)	SIP res. packs	(R17,18)

MECHANICAL COMPONENTS

☐	(36)	low profile sockets	
☐	(2)	dipswitches	(S1,S3)
☐	(2)	heat sinks	
☐	(2)	sets 6-32 hardware	
☐	(1)	RCA connector	(J1)
☐	(1)	4 pin male connector	(J4)
☐	(1)	instuction booklet	

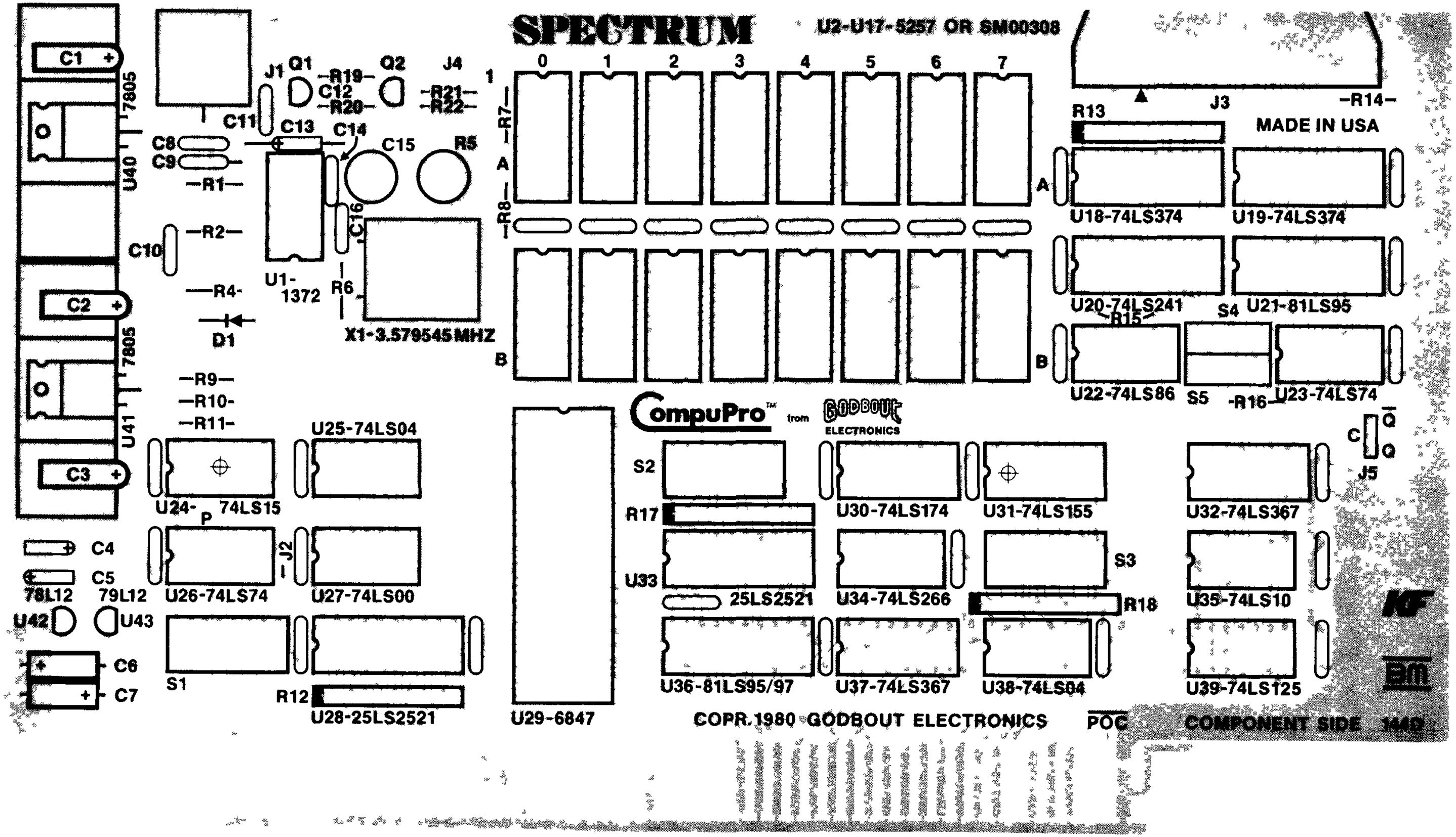
OPTIONAL COMPONENTS

PARALLEL OPTION:

☐	(2)	74LS374 octal latch	(U18,U19)
☐	(1)	79L12 minus 12 volt reg.	(U43)
☐	(1)	SIP res. pack	(R13)
☐	(1)	2.7K ohm res.	(R14)
☐	(1)	3.3uf 15v tant cap.	(C5)
☐	(1)	1.8uf 35v tant cap.	(C6)
☐	(1)	disc cap.	
☐	(2)	slide switches	(S4,S5)
☐	(1)	26 pin I/O connector	(J3)
☐	(2)	low profile socket	

EXTENDED ADDRESSING OPTION

☐	(1)	25LS2521 octal comparator	(U28)
☐	(1)	dip switch	(S1)
☐	(1)	disc cap.	
☐	(1)	SIP res. pack	(R12)
☐	(1)	low profile socket	



Component Layout

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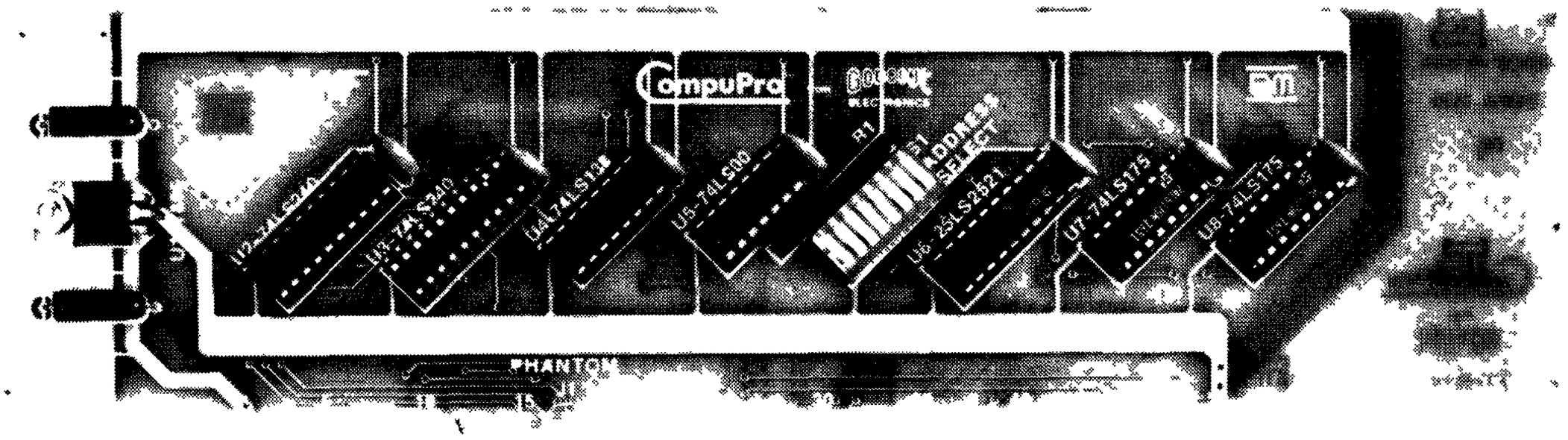
MEMORYMANAGER
USER'S MANUAL



Dual Mode • S-100

151 mac CompuPro™ from GODBOUT

ABOUT MEMORY MANAGER

Congratulations on your decision to purchase the Memory Manager, a dual mode S-100 addressing expander S-100 systems are professional level machines used in commercial industrial and scientific applications Because of bus oriented architecture, S-100 machines provide superior performance without the built in obsolescence of other systems The Memory Manager is fully compatible with the IEEE S-100 bus standard Thank you for choosing a CompuPro Product

TECHNICAL OVERVIEW

This board consists of a single latched parallel output port (dipswitch selectable to any I/O port) whose 8 bits can operate in one of two distinct modes The first mode of operation uses these 8 lines to drive the proposed IEEE S-100 address lines A16 thru A23 The second mode uses the three least significant bits to drive a three line to eight line decoder which drive the eight Godbout Econoram Qualifier lines These modes will extend addressing capabilities of S-100 systems from 64K to 16 megabytes and 512K I/O bytes respectively Other features standard to all CompuPro boards include thorough by-passing of all supply lines to suppress transients, on board regulators and low power Schottky TTL integrated circuits for reliably cool operation All this and sockets for all IC's go on to a double-sided solder-masked printed circuit board with a complete component layout legend

DUAL MODE MEMORY/MANAGEMENT

I/O PORT ADDRESS ASSIGNMENT

The single output port on this board can be addressed to any single port block in the 256 I/O port address space Dipswitch S-1 is used to select the port address as shown below

SWITCH POSITION	FUNCTION		
1	ADDRESS	A0	
2	ADDRESS	A1	
3	ADDRESS	A2	ON = "0"
4	ADDRESS	A3	
5	ADDRESS	A4	OFF = "1"
6	ADDRESS	A5	
7	ADDRESS	A6	
8	ADDRESS	A7	

EXAMPLE To address this board at port 40H, switch positions 1-6, and 8 should be *on*, and position 7 should be *off*

MODE SELECTION

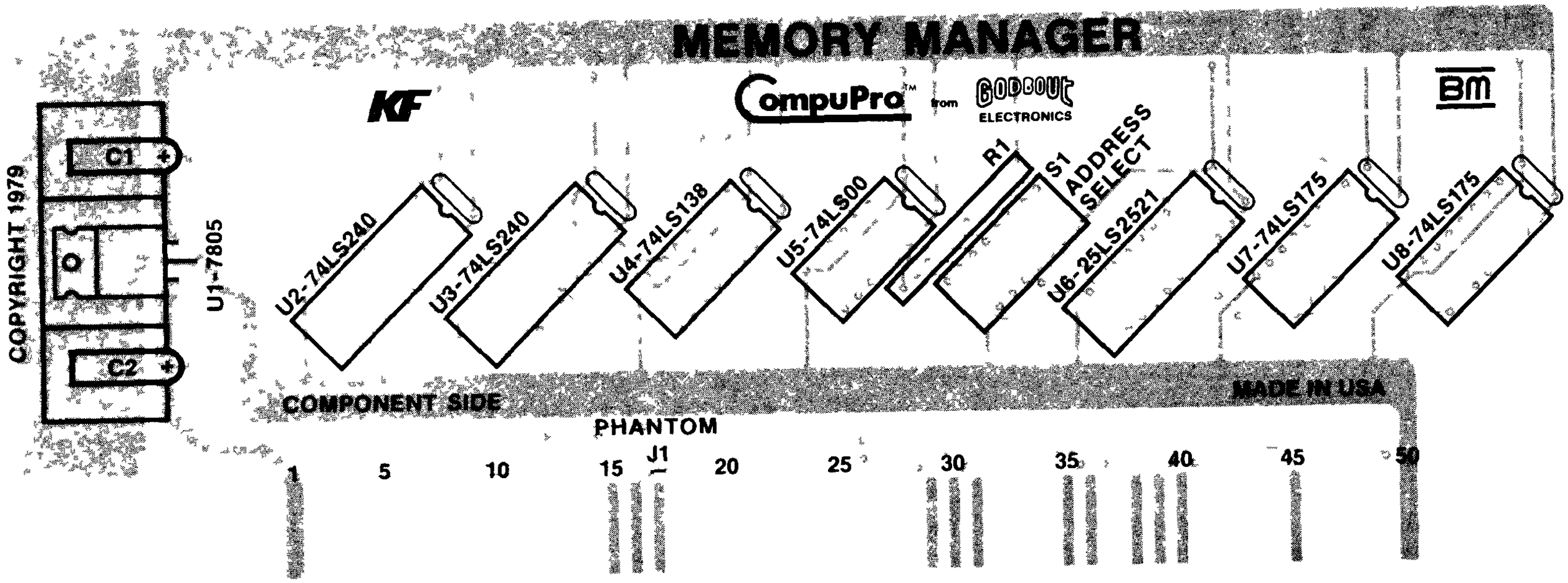
This board is designed to operate in two different modes Mode I operation uses the 8 bit output port to drive the proposed IEEE S-100 extended addressing lines A16 thru A23 for full 24 bit addressing In this mode, the 74LS240 should be installed in position U2 with U3 empty A full 16 megabytes can be accessed in this mode Econorams XA and XIV, are examples of RAMS with full 24 bit IEEE addressing Mode II operation uses the three least significant data bits (D0, D1 and D2) of the output port to drive a 3 line to 8 line decoder and 74LS240 in position U3 to drive high one of the 8 qualifier lines These eight qualifier lines correspond to 8 qualifier inputs on Econorams IIA, VII (16 and 24K), XIII and Econorom 2708 NOTE U2 should be empty in this mode

USING MODE II WITH ECONORAM MEMORY

Econorams IIA, VII, X, XII, XIII, and Econorom 2708 memory boards can all be used in Mode II to extend addressable memory up to 512K bytes By simply jumpering the qualifying line (Q0-Q7 pins 59-66) to the qualifier input pad (see your particular board manual), you have extended the amount of memory your machine can address

CIRCUIT DESCRIPTION

The memory manager consists of three basic sections, the port decoder, the data latch and the buss drivers When the proper I/O address is presented to octal comparator U6 and $\overline{PWR}$ and SOUT indicate and I/O write EOUT strobes low and the data on the data buss is latched at the end of $\overline{PWR}$ Quad latches with complimentary outputs (U7 and U8) feed the output drive U2 and decoder U4 The contents of these latches are cleared with either $\overline{POC}$ or $\overline{PRESET}$ The 8 Q outputs of U7 and U8 feed the inverting buss driver U2 for MODE I operation NOTE Address lines A16 thru A23 are tristated on $\overline{POC}$ or $\overline{PRESET}$ For Mode II operation the Q outputs from DO0 thru DO2 are fed to the three line to eight line decoder U4, which feeds the inverting buss driver U3 All qualifier outputs go low on $\overline{POC}$ or $\overline{PRESET}$

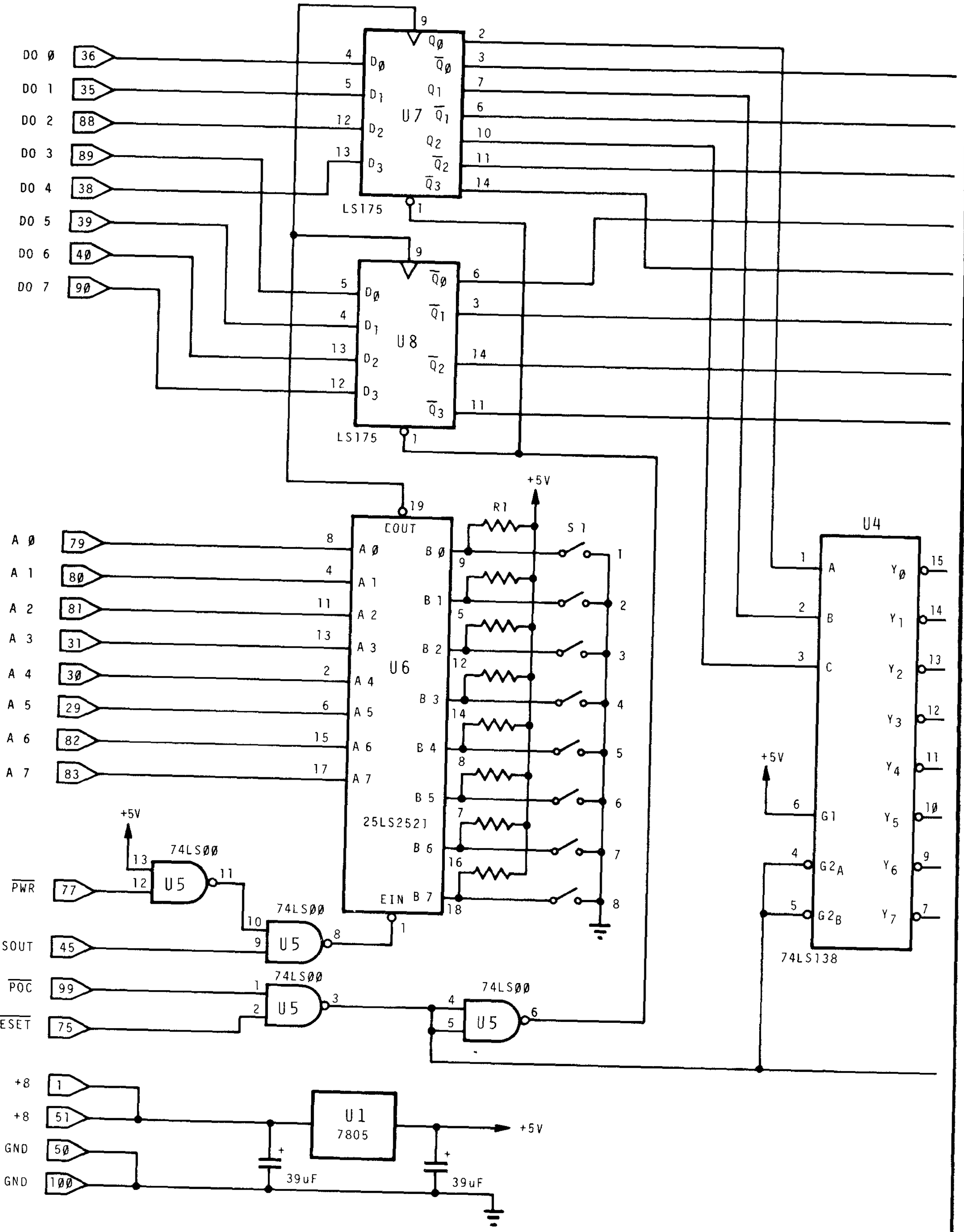


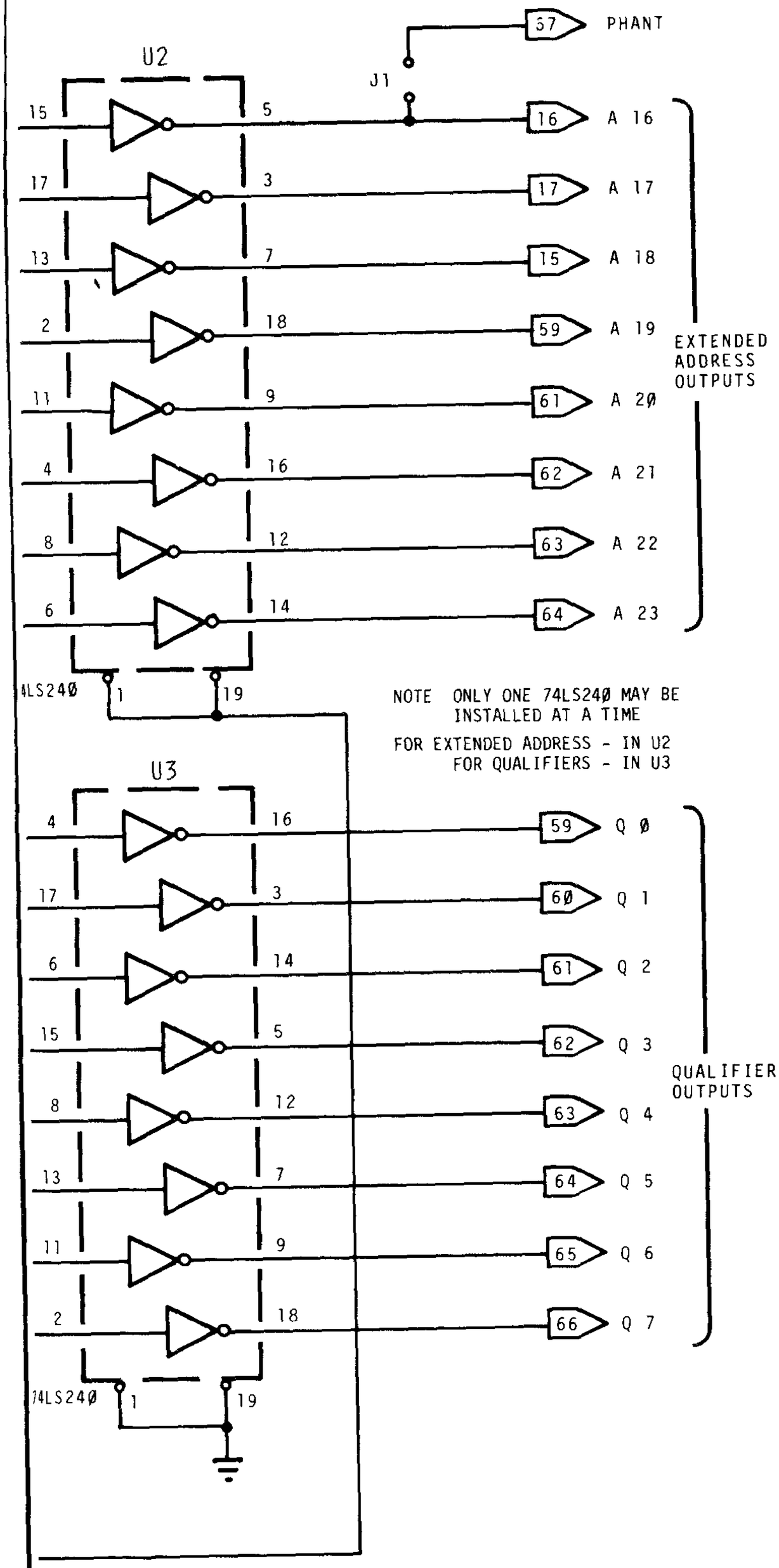
151A

COMPONENT SIDE

Component Layout

UP


DO Ø
DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
36
35
88
89
38
39
4Ø
9Ø
U7
U8
LS175
A Ø
A 1
A 2
A 3
A 4
A 5
A 6
A 7
79
8Ø
81
31
3Ø
29
82
83
U6
25LS2521
COUT
EIN
+5V
R1
S1
74LSØØ
U5
PWR
77
SOUT
45
POC
99
PRESET
75
U4
74LS138
74LS240
74LS244
+8
1
51
GND
5Ø
1ØØ
U1
7805
39uF



Parts List

- ☐ 1 - Circuit board

INTEGRATED CIRCUITS (NOTE the following parts may have letter suffixes & prefixes along with the key numbers given below)

- ☐ 1 - 7805 5V regulator (U1)
- ☐ 1 - 74LS240 octal buss driver (U2 or U3)
- ☐ 1 - 74LS138 3 to 8 line decoder (U4)
- ☐ 1 - 74LS00 quad dual input nand gates (U5)
- ☐ 1 - 25LS2521 octal comparitor (U6)
- ☐ 2 - 74LS175 quad D latches (U7 & U8)

OTHER ELECTRONIC COMPONENTS

- ☐ 2 - 39 uF 10V tantalum capacitors (C1, C2)
- ☐ 1 - single inline resistor packs (R1)
- ☐ 7 - ceramic disc bypass capacitors

MECHANICAL COMPONENTS

- ☐ 1 - 8 pole DIP switch (S1)
- ☐ 7 - low profile sockets
- ☐ 1 - set of 6-32 hardware

151 **MEMORYMANAGER**

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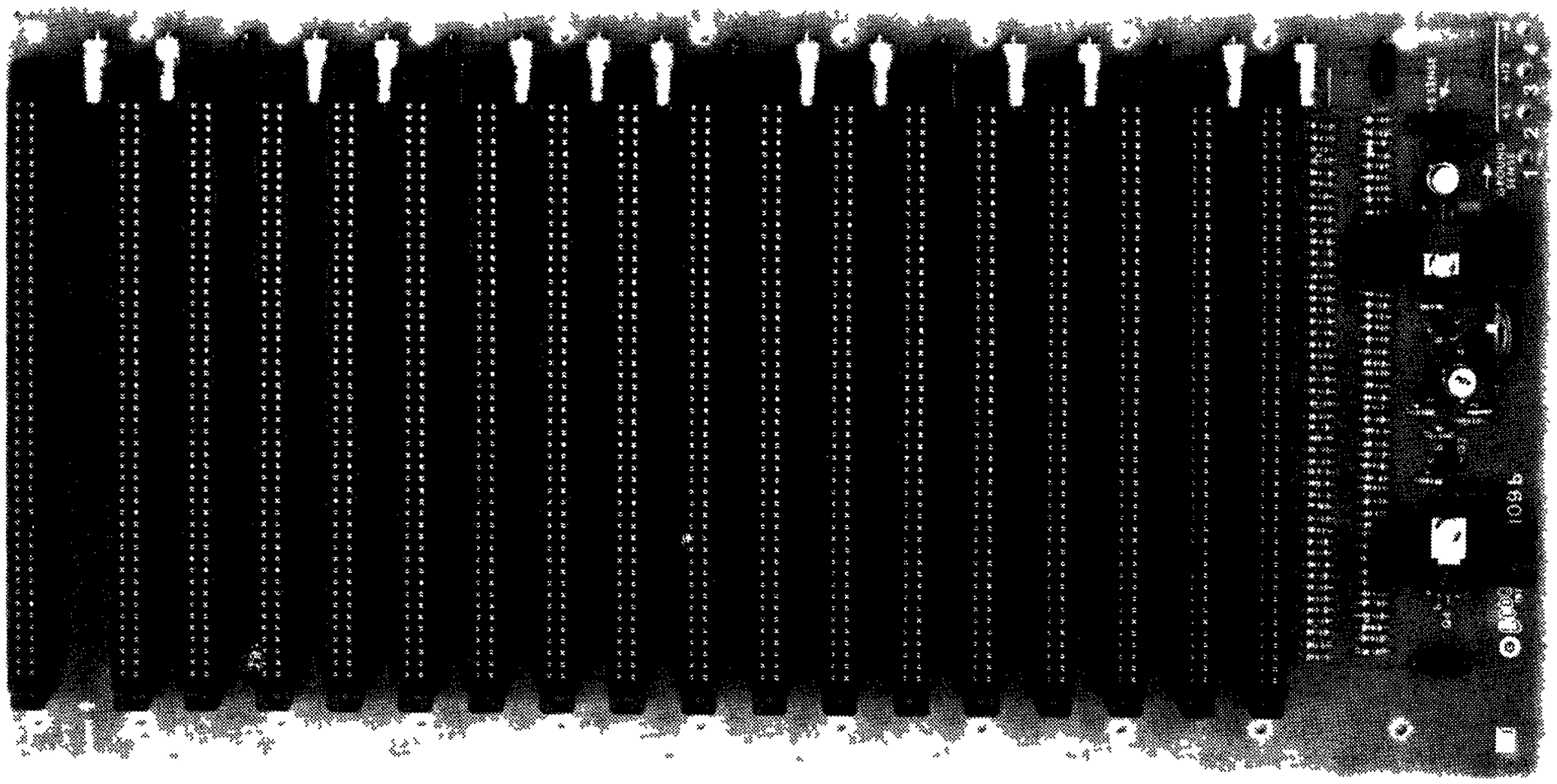
CK-105
CK-109

Motherboard Instructions

For both the 10/11 slot and 18 slot versions



GODBOUT

BILL GODBOUT ELECTRONICS
BOX 2355, OAKLAND AIRPORT, CA 94614

ORDER OF ASSEMBLY Read these instructions carefully before beginning construction, take your time and do not rush; after about 3½ hours you will end up with a high quality Motherboard. When completed, the Motherboard makes an ideal stand-alone unit to form the nucleus of a custom computer system, or, use it to add more peripheral cards to an existing machine.

(1) Check parts against the parts list for completeness and accuracy.

(2) This board uses a solder mask that virtually makes solder bridges a thing of the past. However, solder masked boards require a specific style of soldering, so read the section on soldering techniques before proceeding.

(3) Bend the leads of resistors R9 through R55, then mount in place as shown on the component layout diagram. Flip the board over as shown under soldering techniques, then solder all leads and clip off excess lead lengths.

(4) Bend leads and mount resistors R56-R102 in a manner similar to the previous step; then flip the board over, solder all leads, and clip off all excess lead lengths.

(5) Mount and solder all other resistors except the 10K trimpot in a manner similar to the previous 2 steps.

(6) There are 7 jumpers on the 10 slot board and 10 jumpers on the 18 slot board. Locate these jumpers, then install and solder jumper wires. Use #22 or heavier gauge wire.

(7) Install all capacitors on the board, carefully observing polarity. The positive end of each capacitor is marked with a (+) on the part, which corresponds to the (+) mark screened on the board at each capacitor location. Please note that on the 10 slot board, the positive end of C18 faces towards the inside of the board; on the 18 slot version, C18's positive end faces away from the board. We recommend mounting the capacitors so that the values face upwards and are easily readable.

(8) There are 10 edge connectors supplied with the 10 slot board and 18 connectors supplied with the 18 slot board. Mount and solder the edge connectors in place, noting that with the 10 slot board, there are 11 possible places to mount the edge connectors. The 11th position is for jumpering over to an existing computer motherboard if so desired.

(9) Straighten the leads of the 10K trimpot, then mount and solder in place.

(10) Install IC1, the three terminal regulator. Solder carefully in this and the next step to prevent possible heat damage to the ICs.

(11) Spread the leads of IC2 in accordance with figure 5; note that the lead associated with the flange would be pin 8 of a mini dip package. When viewed from the top, the lead to the immediate left of the flange inserts into the hole marked "1" on the circuit board.

(12) Install and solder transistors Q1 and Q2, orienting the leads as shown in figures 1 and 2. PLEASE NOTE· Transistors Q1-Q4 must be oriented correctly for proper operation of your kit. Also, solder quickly and carefully as semiconductors may be damaged by excessive heat.

(13) Referring to figure 3, mount Q3 and its associated heat sink on the board. The heat sink goes between Q3 and the circuit board as shown. Before screwing the transistor/heat sink combination into place with the hardware provided, first bend the leads of Q3 so that they fit into the holes marked E, B, and C. Next, bolt into place and then solder Q3's leads on the foil side of the board.

(14) Referring to figure 4, mount Q4 in place in a manner similar to the last step.

(15) Attach the 4 solder lugs provided, using the remaining hardware, to the 4 power connections located near the lower right hand corner of the board.

(16) Examine your work carefully (magnifying glasses are a big help in checking over solder connections) When you are satisfied that all is well, proceed to the calibration procedure step.

CALIBRATION AND BRING-UP To bring up the board, remove any peripheral cards and attach either +8V filtered but unregulated or +5V regulated to the power supply lug marked +5 (lug 2). If you are using a regulated +5V supply, leave IC1 out of the circuit and short its I and O pads together so that R103 connects directly to the +5V regulated supply. Then, measure the voltage across C5 with a Voltmeter or DC reading oscilloscope, set trimpot R1 so that your meter reads 2.6V The active terminator circuitry is now properly calibrated.

Read the remainder of this booklet to acquaint yourself with the theory behind your motherboard and the available options to accomodate specific systems.

ERRATUM

On some boards, C5 (lower left hand corner of the board) may be marked C3

PARTS LIST

(Those items marked with an asterisk (*) are included with the 18 slot version, but not with the 10 slot version)

RESISTORS

R1	10K trimpot
R2	150K resistor (brown/green/yellow)
R3, R5	560 ohm (green/blue/brown)
R4, R8	1K resistor (brown/black/red)
R6, R7	910 ohm resistor (white/brown/brown)
R9-R102	270 ohm resistor (red/violet/brown)
R103, R104	1.8K resistor (brown/gray/red)

CAPACITORS

C1, 3, 4, 5, 6, 7, 10, 13, 16, 20*, 23*	39 uF tantalum capacitor
C2	0 47 tantalum capacitor
C8, 9, 11, 12, 14, 15, 17, 18, 19*, 21*, 22*, 24*, 25*	20 uF aluminum electrolytic

SEMICONDUCTORS

Q1	PNP transistor F137 (2N2907A)
Q2	NPN transistor 3560-2/PT134 (2N3904)
Q3	NPN power transistor (GE red)
Q4	PNP power transistor D41D1
IC1	Three terminal regulator (G309H)
IC2	Micropower op amp (G4250H)

MECHANICAL PARTS

(2)	THM6070 heat sinks
(1)	Circuit board
(10)	S-100 edge connectors (note: 18 edge connectors supplied with 18 slot kit)
(4)	Solder lugs
(6)	Nuts and bolts
(1)	Data booklet

FIGURE 1

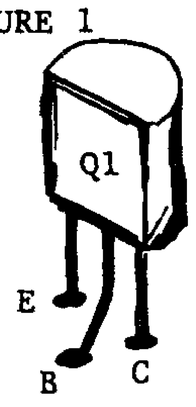
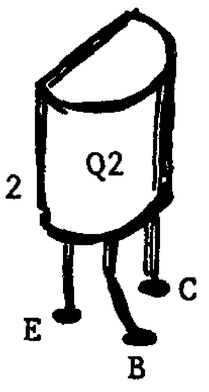


FIGURE 2



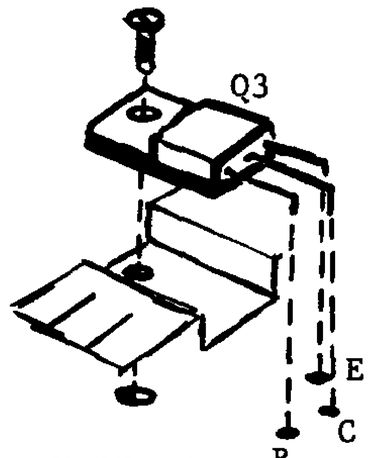


FIGURE 3

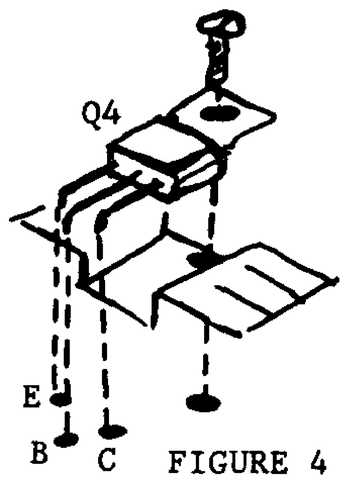


FIGURE 4

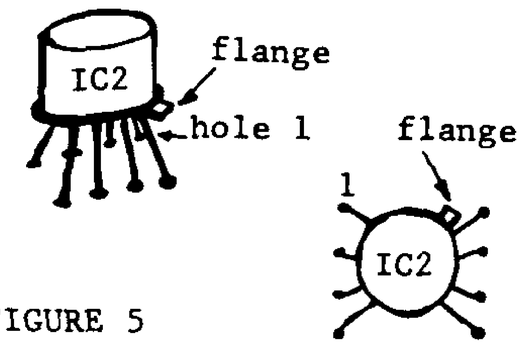
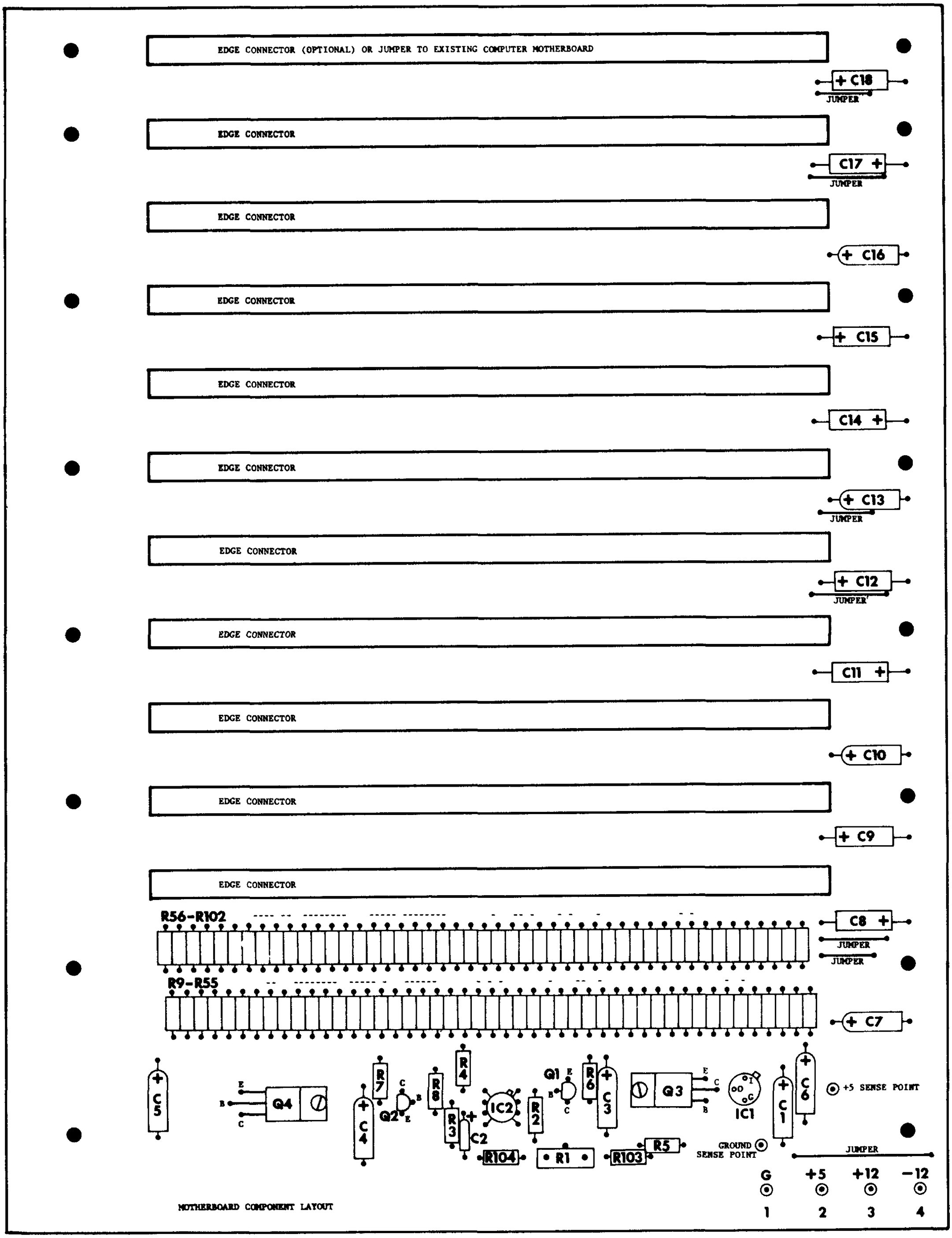


FIGURE 5



MOTHERBOARD COMPONENT LAYOUT

SOLDERING TECHNIQUES In case you are not familiar with solder masked boards they are similar to standard PC boards but are screened with a solder resistant coating on the foil side This mask is screened over the entire board except where there are solder connections to be made Thus, solder does not run down a trace but adheres to the junction of exposed board and exposed lead Because of this, soldering requires a bit of care, trying to force lots of solder on to this type of joint will make it ball up around the lead On the other hand, since solder does not comfortably hold to or flow over the resist, the chances of getting a bridge between tight, adjacent traces are decidedly minimized

When soldering with a solder masked board, we recommend keeping the component leads straight up at all times, not bent over as with other types of boards (see figure 6) To prevent components from falling out when you flip the board over to solder, flip the board over on to a table, book or other flat surface which pushes the parts against the component side of the board

To solder, bring the iron tip in at an angle, against the board pad and component lead then feed in a tiny bit of solder at opposite ends of the lead (see figure 7) This makes for a good joint with no excess solder Use of any type of solder other than rosin core solder invalidates the warranty

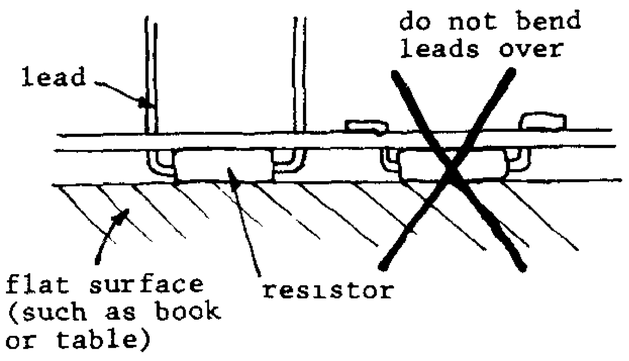
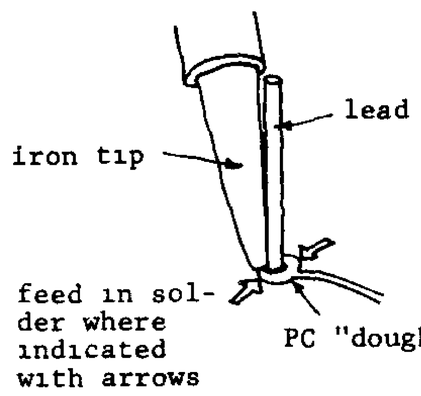


Figure 6

Figure 7



MOUNTING HOLES There are several mounting holes towards the outside vertical borders of the motherboard With the 10 slot motherboard, these are spaced in such a manner that the board may bolt directly into an IMSAI size frame, and some of the Vector-Pak enclosures also

SENSE HOLES Many power supplies incorporate sense lines that provide voltage reference feedback to the power supply However, in systems with heavy current demands, there can be a voltage drop between the output of the supply and the peripherals connected to the motherboard, therefore the sense information does not take into account the aforementioned voltage drop On the board, there are sense points for both +5V and ground If you want your power supply to read the voltage present at the motherboard, connect sense lines up to these points

POWER SUPPLY TRACES When many current-hungry cards are loaded into a motherboard the current strain on the power supply traces (especially the +12 and -12 Volt lines) becomes quite large To overcome this unbalanced current demand, the Godbout motherboard uses extra wide traces that run off to the side of the edge connectors, then connect over to the buss power lines through wire jumpers This contributes to a more reliable design Also, note that all power supply lines, as well as the active termination output, are liberally bypassed with bypass capacitors

ACTIVE TERMINATION THEORY The standard TTL termination is a 2 6V reference, comprising a 360 ohm and a 390 ohm resistor in series across the power supply, the TTL line terminates at the junction of these two resistors This type of passive termination allows for proper sourcing and sinking of the TTL line, and keeps the impedance of the line to a minimum to minimize pickup of noise and crosstalk Each one of these terminations, however also draws about 6 7 mA from the power supply So, terminating 94 lines in this manner means a standby current drain through the terminators of well over half an amp! These passive terminations don't just put a strain on your power supply, they waste energy and create heat inside your computer's cabinet I don't think we have to go much further to realize that passive termination is not such a good way to do things, although it's better than no termination at all

The active termination in the Godbout motherboard takes advantage of the fact that there is an equivalent active structure, based around a voltage source and isolating resistor, that can accomplish the same results (see figure 8) Current can either source or sink through the 270 ohm resistor, either dumping into or drawing from the voltage source Terminating more lines simply means adding more 270 ohm resistors between the line and voltage source As a result, the standby current is slashed to the standby current of the voltage source circuitry---about 15 or 20 mA, which is quite a savings in energy

The current requirement goes up as lines require more sourcing or sinking, but here we are somewhat fortunate At any given moment, on 94 lines there will be a fairly random mix of 1s and 0s from instant to instant---these tend to cancel out and thus reduce the current drive requirements of the voltage source Nonetheless, although this keeps average current consumption down, there are instances when you might have an extreme momentary need for current As a result, the voltage source has enough capacity built-in to take care of the most adverse cases

The structure of the voltage source is fairly simple (see schematic), IC1 sets up a stable voltage reference independent of master supply variations IC2, a micropower op amp, hooks up as a simple voltage divider with Q1-Q4 set up as current boosting devices to cover any large current demands R1, the trimpot, adjusts the output voltage of the op amp---hence the terminator voltage---to 2 6V Since the op amp is forced to run from +5V when the motherboard is powered from a regulated +5V supply, you might expect some problems since that low a supply voltage range is marginal for most op amp types However, the 4250 micropower op amp chosen for this application can work satisfactorily down to +3V, so it's working well within spec

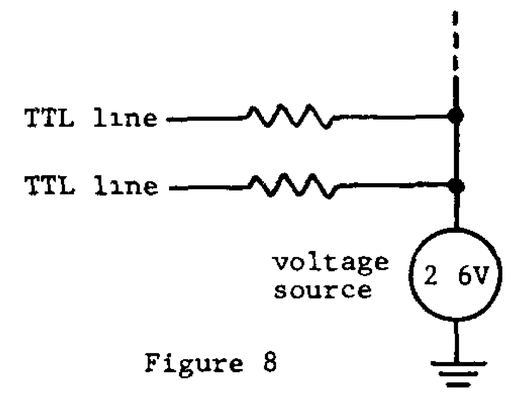
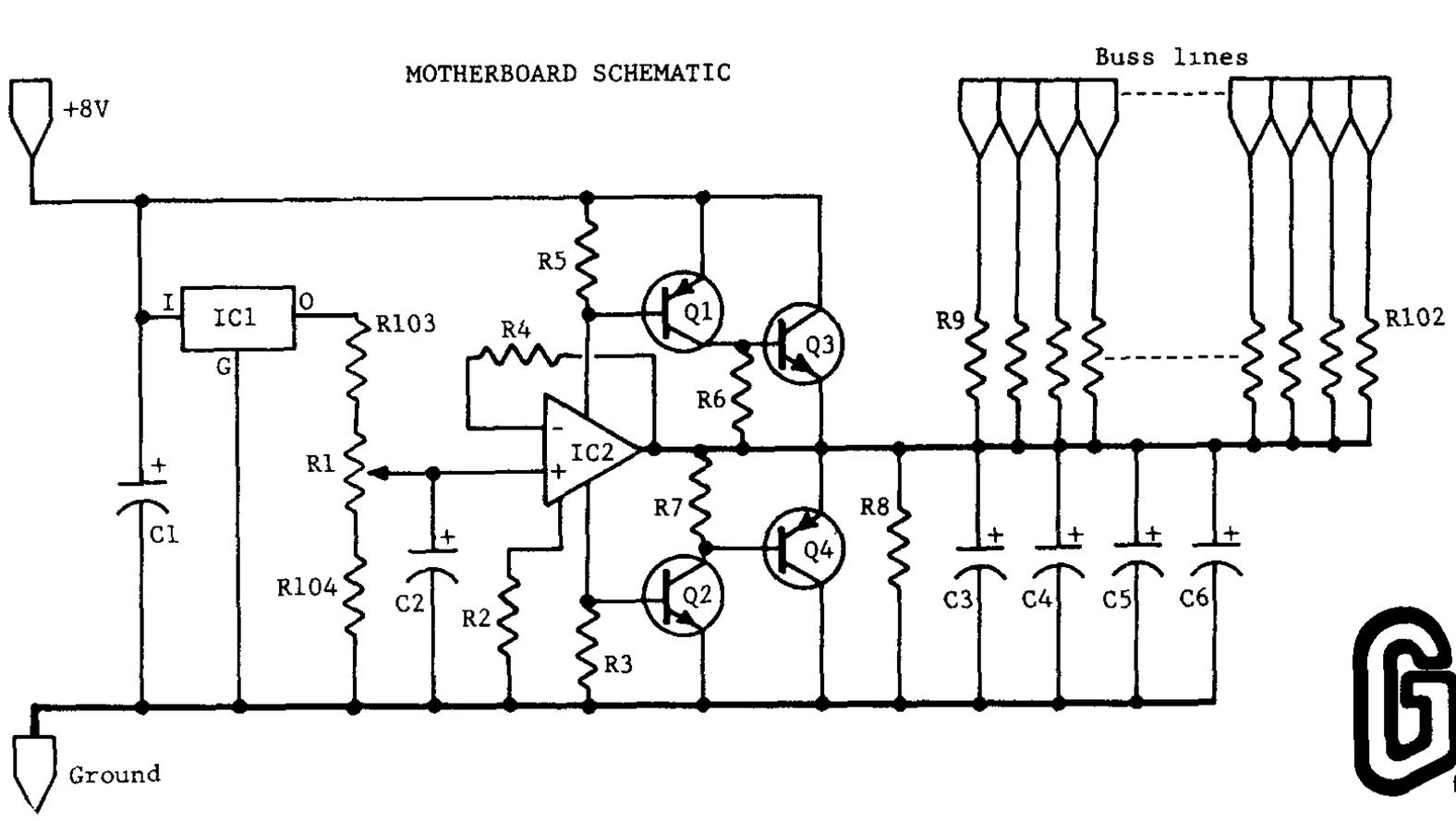


Figure 8

MOTHERBOARD SCHEMATIC



In the 10 slot version, the following bypass capacitors tie across the following supply lines

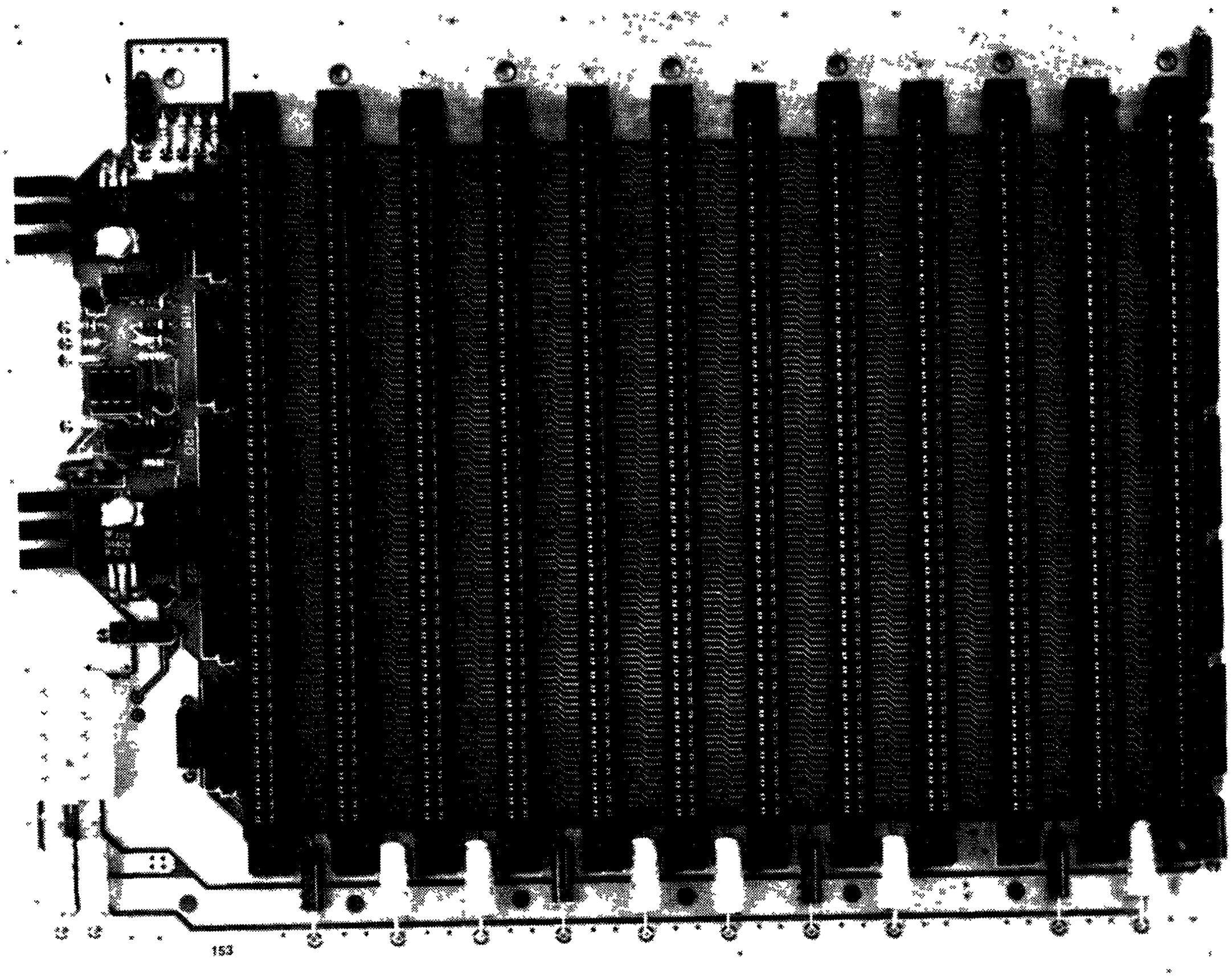
+5 C7, C10, C13, C16
+12 C9, C12, C15, C18
-12 C8, C11, C14, C17

In the 18 slot version, the following bypass capacitors tie across the following supply lines

+5 C7, C10, C13, C16, C20, C23
+12 C9, C12, C15, C19, C22, C25
-12 C8, C11, C14, C17, C18, C21, C24

GODBOUT
BILL GODBOUT ELECTRONICS
BOX 2355 OAKLAND AIRPORT CA 94614

MOTHERBOARD User's Manual



IEEE·696/S-100 Shielded/Terminated 6·12·20 Slot with Reset

155

CompuPro™ from GODBOUT

8/80

COMPUPRO MOTHERBOARDS

Thank you for choosing a **CompuPro Product.** We are sure you will find this to be a very high quality product that will give you years and years of dependable service.

The termination circuitry has evolved over the last few years and is a tried and proven method of reducing noise in your system. As shipped the termination circuitry is adjusted to maintain a voltage of +2.7 VDC on all bus pins (other than power distribution). This should be checked by measuring between any bus pin and ground with no boards in the motherboard and readjusted if needed with trimpot R6. This is the only calibration necessary.

The connector on the left edge of the board is connected to ground and bus pin 75. This can be used for connecting a RESET pushbutton to a system which has no other means of generating RESET. The power socket makes for a convenient method of distributing the system power to the motherboard, and is rated for more than 30 AMPS on the +8 volt line. There are four pins for ground, four pins for +8 volts, and one each for the +15 and -15 volts. The connector is keyed to prevent connecting errors, and the power wires are color coded as follows:

COLOR	VOLTAGE
BLACK	GROUND
RED	+8 V
GREY	+15 V
PURPLE	-15 V

TOP VIEW

P1	GND	GND	+8	+8	-15
	GND	GND	+8	+8	+15

NOTE: On all but the 6 slot motherboard there are provisions for using a fast-tab connector to distribute the +8 volts to the bus with very little loss due to board trace resistance. These fast-tabs should be connected to one of the +8 volt distribution wires coming from the power supply.

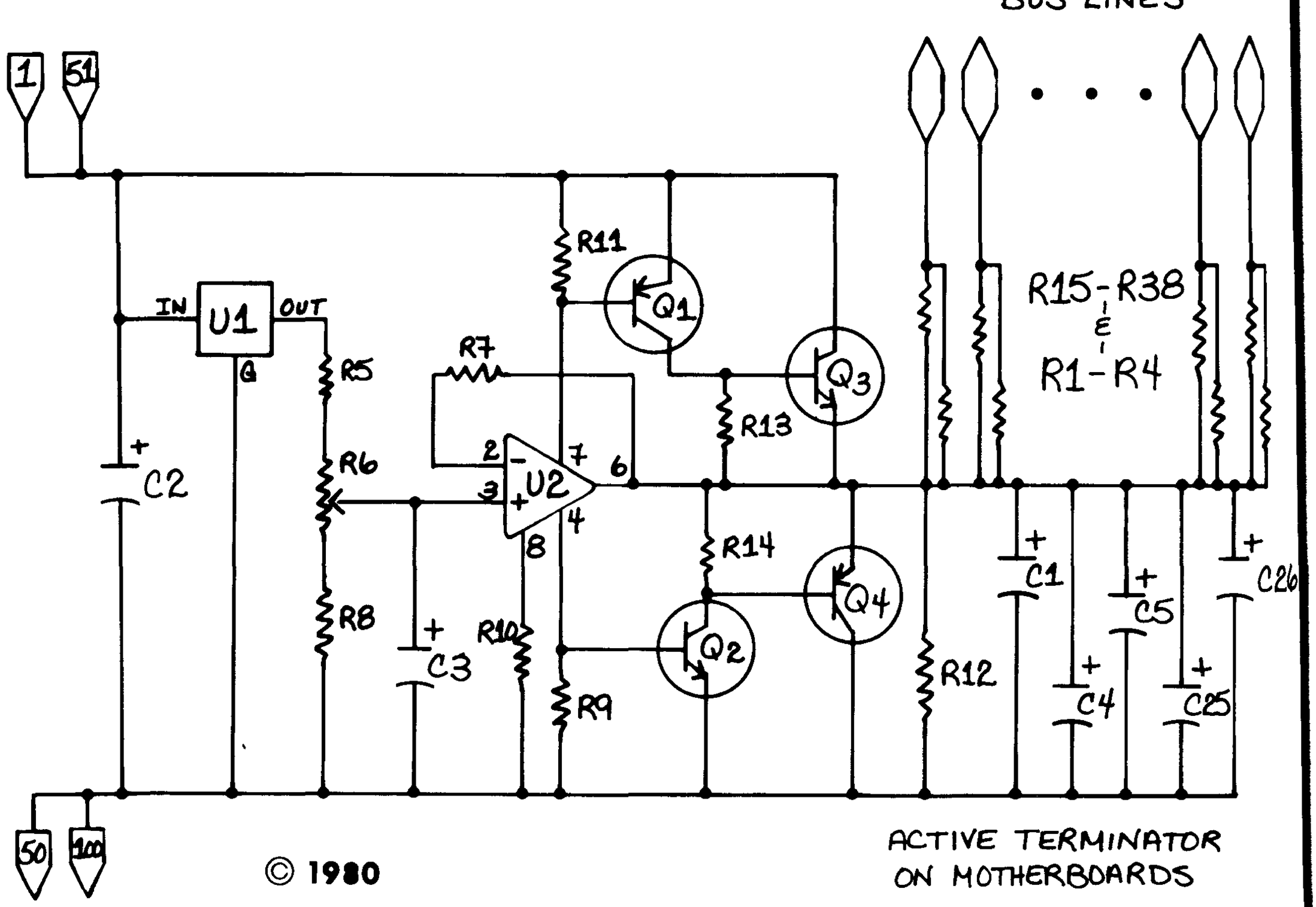
ACTIVE TERMINATION THEORY

The standard TTL termination is a 2.7V reference, comprising a 360 ohm and a 390 ohm resistor in series across the power supply; the TTL line terminates at the junction of these two resistors. This type of passive termination allows for proper sourcing and sinking of the TTL line, and keeps the impedance of the line to a minimum to minimize pickup of noise and crosstalk. Each one of these terminations, however, also draws about 6.7 mA from the power supply. So, terminating 94 lines in this manner means a standby current drain through the terminators of well over half an amp! These passive terminations don't just put a strain on your power supply, they waste energy and create heat inside your computer's cabinet. We don't have to go much further to realize that passive termination is not such a good way to do things, although it's better than no termination at all.

The active termination in the **CompuPro Motherboard** takes advantage of the fact that there is an equivalent **ACTIVE** structure, based around a voltage source and isolating resistor, that can accomplish the same results (see figure below). Current can either source or sink through the 280 ohm resistance (two 560 ohm resistors in parallel), either dumping into or drawing from the voltage source. Terminating more lines simply means adding more 280 ohm resistors between the line and voltage source. As a result, the standby current is slashed to the standby current of the voltage source circuitry---about 15 or 20 mA, which is quite a savings in energy.

The current requirement goes up as lines require more sourcing or sinking, but here we also are somewhat fortunate. At any given moment, on 94 lines there will be a fairly random mix of 1's and 0's from instant to instant---these tend to cancel out and thus reduce the current drive requirements of the voltage source. Nonetheless, although this keeps average current consumption down, there are instances when you might have an extreme momentary need for current. As a result, the voltage source has enough capacity built-in to take care of the most adverse cases.

The structure of the voltage source is fairly simple (see schematic); IC-1 sets up a stable voltage reference independent of master supply variations. IC-2, a micropower op amp, hooks up as a simple voltage divider with Q1-Q4 set up as current boosting devices to cover any large current demands. R6, the trimpot, adjusts the output voltage of the op amp---hence the terminator voltage---to 2.7V. Since the op amp is forced to run from +5V when the motherboard is powered from a regulated +5V supply, you might expect some problems since that low a supply voltage range is marginal for most op amp types. However, the 4250 micropower op amp chosen for this application can work quite well down to +3V, so it's working well within spec.



MOTHERBOARD PARTS LIST

MECHANICAL PARTS

*S-100 edge connectors (6,12, or 20)
*Nylon nuts and screws
*I.C. socket 8 pin
*Mounting hardware for transistors
 Nylon power connector and plug
*Reset connector and plug
 circuit board

RESISTORS

* SIP Resistors 560 Ohm	R15-R34
10K trimpot	R6
* 150K ohm resistor	R10
* 560 ohm resistor	R1-R4,R9, R11,R35-R38
*1K ohm resistor	R7,R12
*910 ohm resistor	R13,R14
*1.8K ohm resistor	R5,R8

CAPACITORS

* 39 uF tantalum capacitor
  C1,C2,C4,C5,C8,C11,C25,C26 (all)
  C19,C22 (on 20 slot only)
  C14 (on 12 & 20 slot only)
  C3
  C6,C7,C9,C10,C12 (all)
  C13,C15-C17 (on 12 & 20 slot only)
  C18,C20,C21,C23,C24 (on 20 only)
* 0.47 uF tantalum capacitor
* 20 uF electrolytic

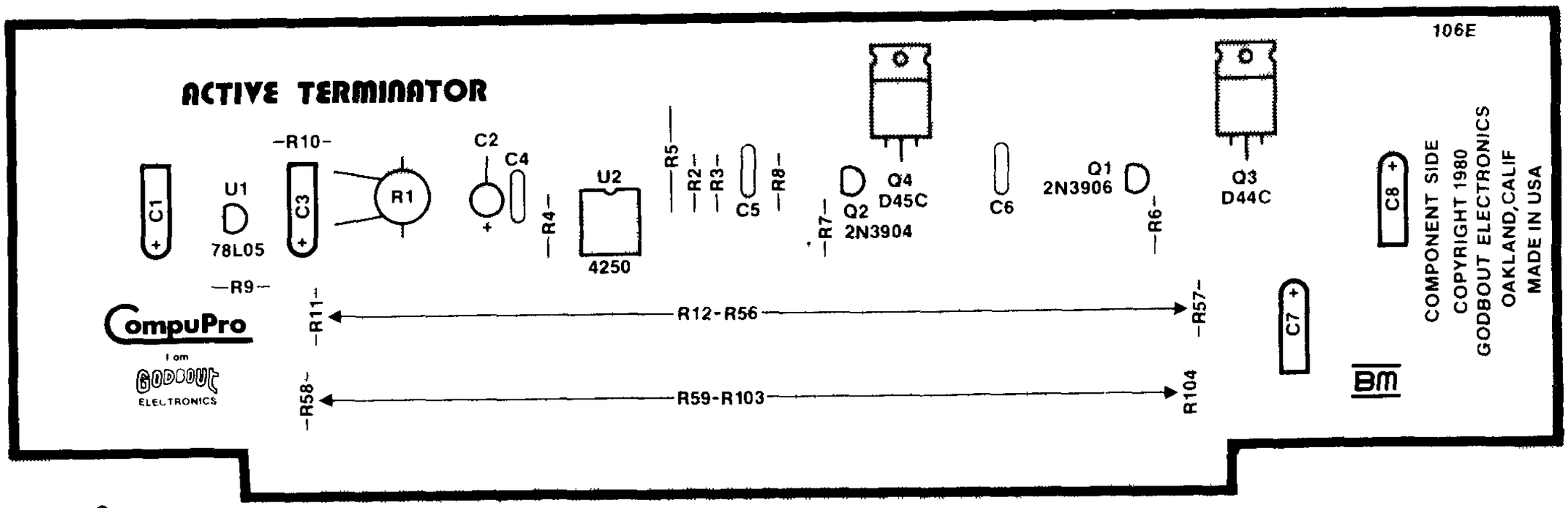
SEMICONDUCTORS

* PNP transistor 2N3906	Q1
* NPN transistor 2N3904	Q2
* NPN power transistor D44C	Q3
* PNP power transistor D45C	Q4
* +5 Volt regulator 78L05	U1
Micropower op amp 4250	U2

* means parts are wave soldered to motherboard.

Active Terminator no. 106

COMPONENT SIDE



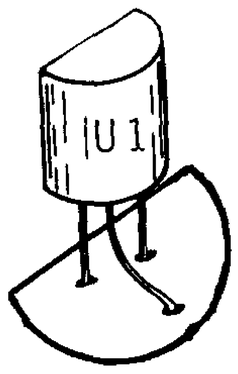
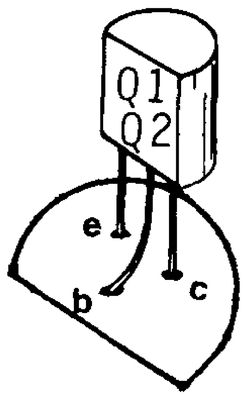


FIGURE 3



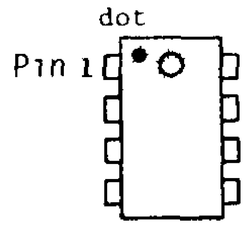
ORDER OF ASSEMBLY READ THESE INSTRUCTIONS CAREFULLY AND TAKE YOUR TIME

(1) CHECK ALL PARTS AGAINST THE PARTS LIST (2) THIS BOARD USES A SOLDER MASK THAT VIRTUALLY MAKES SOLDER BRIDGES A THING OF THE PAST HOWEVER, SOLDER MASKED BOARDS REQUIRE A SPECIFIC STYLE OF SOLDERING, SO FLIP THIS SHEET OVER AND READ THE SECTION OF SOLDERING TECHNIQUES BEFORE PROCEEDING (3) MOUNT RESISTORS R11-R57, FLIP THE BOARD OVER AS SHOWN UNDER SOLDERING TECHNIQUES, THEN SOLDER ALL LEADS AND CLIP OFF EXCESS LEAD LENGTH (4) MOUNT RESISTORS R58 R104, FLIP THE BOARD OVER THEN SOLDER ALL LEADS AND CLIP EXCESS LENGTH AS IN PREVIOUS STEP (5) MOUNT AND SOLDER ALL OTHER RESISTORS EXCEPT THE TRIMPOT IN A MANNER SIMILAR TO THE LAST TWO STEPS (6) INSTALL THE CAPACITORS ON THE BOARD, CAREFULLY OBSERVING POLARITY WE RECOMMEND MOUNTING THE CAPACITORS SO THAT THEIR VALUES FACE UPWARD AND ARE EASILY READABLE AFTER CHECKING POLARITY, SOLDER IN PLACE (7) MOUNT AND SOLDER THE TRIMPOT, R1, IN PLACE (8) INSERT U1, THE 78L05 (SEE FIGURE 1), THREE TERMINAL REGULATOR TO PREVENT POSSIBLE HEAT DAMAGE, SOLDER IT QUICKLY AND CAREFULLY (9) INSTALL THE 8-PIN MINIDIP SOCKET FOR U2, SOLDER MAKE SURE PIN 1 IS CORRECTLY IDENTIFIED AND THE IC CORRECTLY ORIENTED, INSERT IC2 (SEE FIGURE 2) (10) INSTALL AND SOLDER TRANSISTORS, Q1 AND Q2, ORIENTING THE LEADS AS SHOWN IN FIGURE 3 (11) INSTALL AND SOLDER Q3 AND Q4 IN PLACE AS SHOWN IN FIGURE 4

PLEASE NOTE TRANSISTORS Q1-Q4 MUST BE PROPERLY ORIENTED FOR YOUR KIT TO WORK PROPERLY (12) FINALLY, EXAMINE YOUR WORK CAREFULLY WHEN YOU ARE COMPLETELY SATISFIED THAT ALL IS WELL TURN TO THE OTHER SIDE OF THIS SHEET FOR CORRECT CALIBRATION PROCEDURE

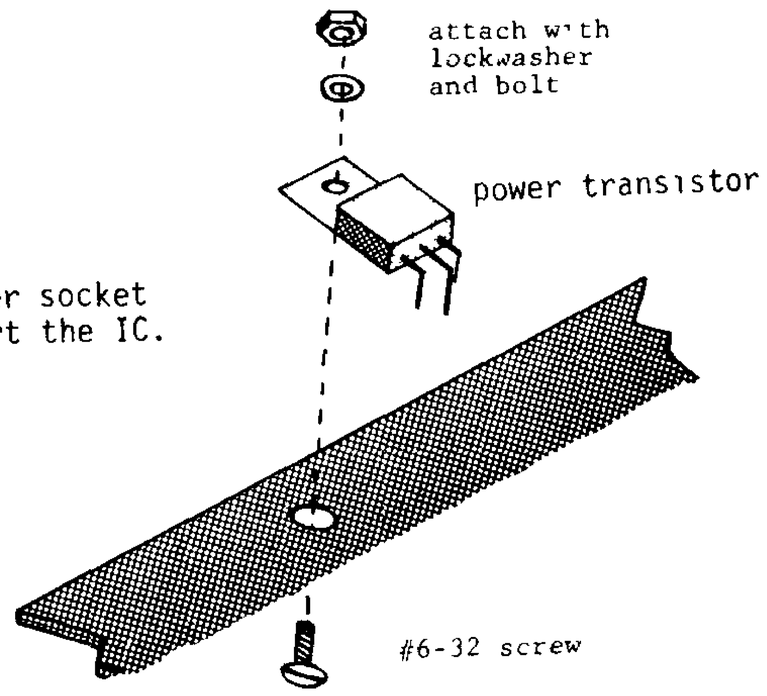
FIGURE 2

IC2



NOTE Insert and solder socket before you insert the IC.

FIGURE 4



PARTS LIST - ACTIVE TERMINATOR BOARD

R1	Trimpot
R2	150K resistor (brn/gr/yel)
R3, R5	560 ohm resistor (gr/blu/brn)
R4, R8	1K resistor (brn/blk/red)
R6, R7	910 ohm resistor (wh/brn/brn)
R9, R10	1.8K resistor (brn/gry/red)
R11-R104	270 ohm resistor (red/viol/brn)
C1,3,7,8	39 uF tantalum capacitor
C2	0.47 uF tantalum capacitor
C4,5,6	01 uF disc capacitor
Q1	PNP transistor (2N3906)
Q2	NPN transistor (2N3904)
Q3	NPN transistor (D44CX)
Q4	PNP transistor (D45CX)
U1	3 terminal regulator (78L05)
U2	micropower op amp (LM4250CN)
(1)	Circuit board
(2)	6-32 nuts, bolts & lockwashers
(1)	8-pin socket

CompuPro™ from GODBOUT ELECTRONICS

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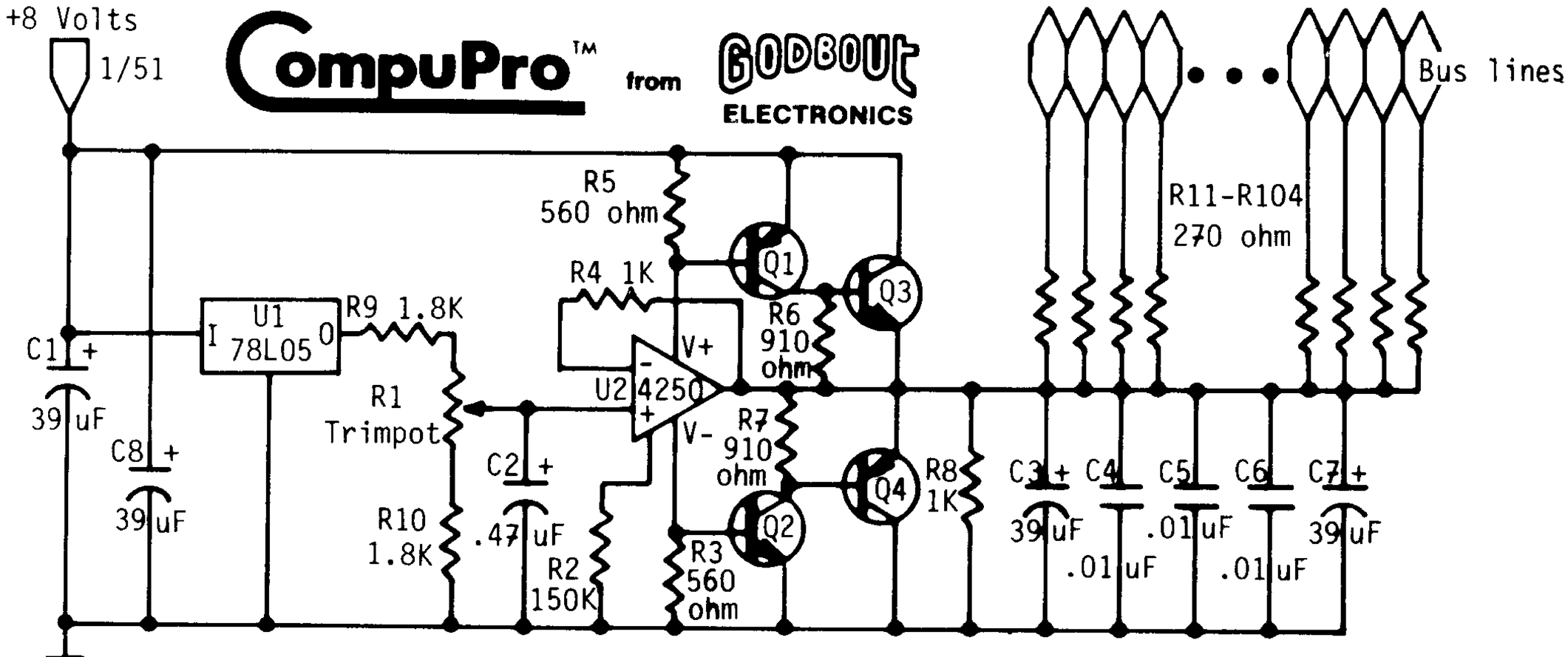


FIGURE 1

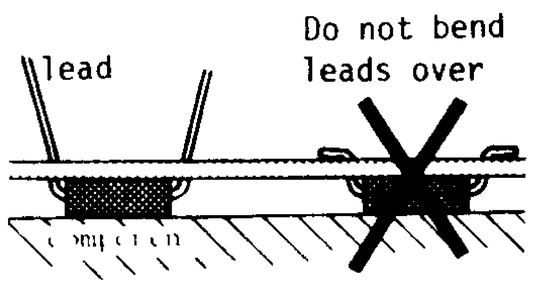


FIGURE 2

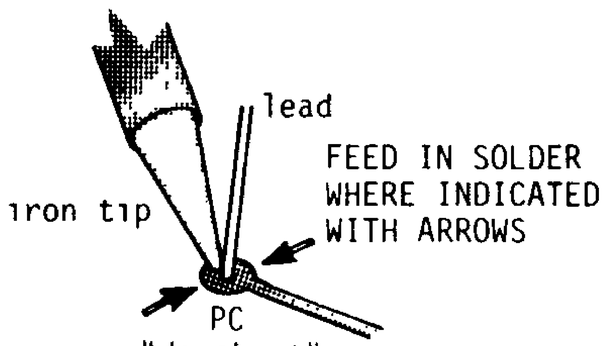
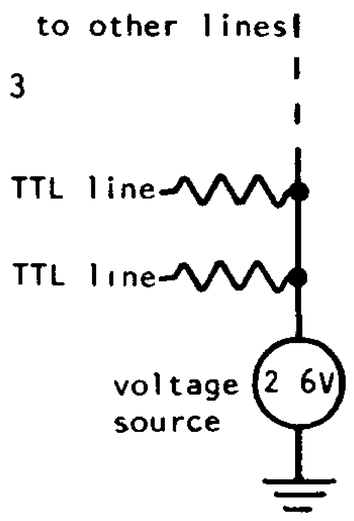


FIGURE 3



SOLDERING TECHNIQUES Solder masked boards are similar to standard PC boards but are screened with a solder resistant coating on the foil side This mask is screened over the entire board, except where there are solder connections to be made Thus, solder does not run down a trace but adheres to the junction of the exposed board and exposed lead Because of this, soldering requires a bit of care, trying to force lots of solder on to this type of joint will make it ball up around the lead On the other hand, since solder does not comfortably hold to or flow over the resist, the chances of getting a bridge between tight, adjacent traces are decidedly minimized

When soldering with a solder masked board, we recommend keeping the component leads straight up at all times, not bent over as with other types of boards (see Figure 1) To prevent components from falling out when you flip the board over to solder, flip the board over on to a table, book, or other flat surface, which pushes the parts against the component side of the board

When soldering, bring the iron tip in at an angle, against the board pad and component lead, then feed in a tiny bit of solder at opposite ends of the lead (see Figure 2) This makes for a good joint with no excess solder Use of any type of solder other than rosin core solder invalidates the warranty

CALIBRATION To bring up the board, remove any peripheral cards and attach either +8V filtered but unregulated or +5V regulated to the positive supply terminal of the active terminator board If you are using a regulated +5V supply, leave U1 out of the circuit and short the input and output pads together so that R9 connects directly to the +5V regulated supply Then measure the voltage across C3 of C7 with a voltmeter of DC reading scope, set trimpot R1 so that your meter reads 2 7V The active terminator circuitry is now properly calibrated

ACTIVE TERMINATION THEORY The standard TTL termination is a 2 7V reference, composed of a 360 and 390 ohm resistor in series across the power supply, the TTL line terminates at the junction of these two resistors This type of passive termination allows for proper sourcing and sinking of the TTL line, and keeps the impedance of the line to a minimum to minimize pickup of noise and crosstalk Each one of these passive terminations, however, also draws about 6 7mA from the power supply So, terminating 94 lines in this manner means a standby current drain through the terminators of well over half an Amp! These passive terminations don t just put a strain on your power supply, they waste energy and create heat inside your computer's cabinet We don't have to go much further to realize that passive termination is not the best way to do things, although it is better than no termination at all

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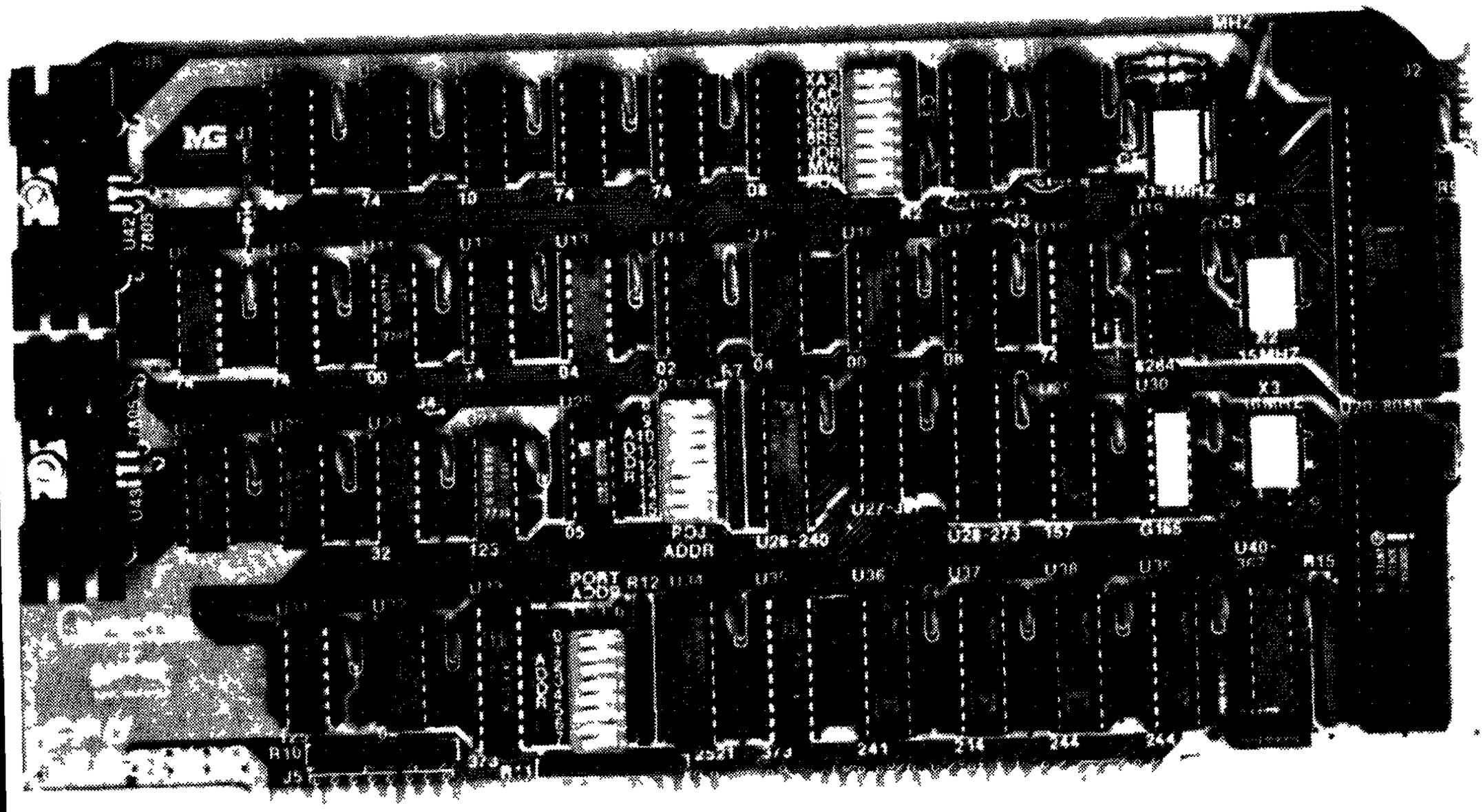
Rev. 9/80

CPU 8085/88
USER'S MANUAL



IEEE · S-100
DUAL CPU
5MHz - 8 bit 8085
5MHz - 16 bit 8088

161 mac
CompuPro™ from GODBOUT
7/80

HOW TO GET YOUR CPU 8085/88 TO RUN IN UNDER 5 MINUTES WITHOUT READING THE MANUAL

This section is for those of you who are so anxious to see if your new CPU board works that you can't wait long enough to read the manual. This section will tell you how to set the switches up so that the **CPU 8085/88** will look most like your older CPU board.

WE STRONGLY RECCOMEND THAT YOU RELAX, AND READ THE MANUAL!! If, after reading and following the directions in this section, your system doesn't work, DON'T CALL!!! READ THE MANUAL FIRST!!!

8085 ONLY

If your CPU 8085/88 was factory assembled, or you are using a version that contains both CPUs, don't read this section. Skip to the next section. This section is for those of you who purchased an 8085 only version, UNKIT.

You will need to install two jumpers, J3 and J4. (If you followed the assembly instructions carefully, you should have already installed them.) J3 is located above and to the right of U17 and J4 is located above and to the right of U23.

Use a piece of component lead for the jumpers and leave about a 1/4 inch loop above the board so that they may be easily cut when you want to add an 8088.

SWITCH SETTINGS

Dip switch 1 is located between U6 and U7. It is used to select various operational modes of the **CPU 8085/88.**

DIP SWITCH 1

SWITCH POSITION	LABELED	HOW TO SET IT
1	XA3	**OFF.**
2	XAC	**OFF.**
3	IOW	**OFF.**
4	5RS	**ON.**
5	8RS	**ON.**
6	JOR	**ON.**
7	MW	**OFF** if you have a front panel, **ON** otherwise.
8	POJ	**ON** if you need power-on-jump, **OFF** otherwise.

Dip switch 2 is located between U25 and U26 and is used to set the power-on-jump address. If you don't need power-on-jump, you should have set Dip Switch 1, position 8 to OFF, and you can skip this section.

DIP SWITCH 2

SWITCH POSITION	LABELED	HOW TO SET IT
1	ADDR 8	**ON** to match addr. bit 8.
2	ADDR 9	**ON** to match addr. bit 9.
3	ADDR 10	**ON** to match addr. bit 10.
4	ADDR 11	**ON** to match addr. bit 11.
5	ADDR 12	**ON** to match addr. bit 12.
6	ADDR 13	**ON** to match addr. bit 13.
7	ADDR 14	**ON** to match addr. bit 14.
8	ADDR 15	**ON** to match addr. bit 15.

Dip switch 3 is used to set the I/O port that is used by the Memory Manager and swapping processors. The Compupro 'standard' is port address FD hex, and here's how to set it:

DIP SWITCH 3

SWITCH POSITION	LABELED	HOW TO SET IT
1	ADDR 0	OFF
2	ADDR 1	ON
3	ADDR 2	OFF
4	ADDR 3	OFF
5	ADDR 4	OFF
6	ADDR 5	OFF
7	ADDR 6	OFF
8	ADDR 7	OFF

Switch 4 is located in the upper right hand corner of the board and is the large switch with the red paddle. It is used to select either 2 or 5 Mhz operation for the 8085.

TURN THIS SWITCH SO THAT THE PADDLE IS IN THE LEFT-MOST POSITION. This will select 2 Mhz operation, which is a good place to start.

If you have a IMSAI-type front panel, plug the cable into J2. J2 is a 16 pin socket located in the upper right hand corner of the board. You will also want to turn position 7 of Dip Switch 1 (MW), OFF.

ABOUT THE CPU 8085/88

Congratulations on your purchase of the **CPU 8085/88** - an advanced processor board designed specifically for full electrical and mechanical compatibility with the IEEE S-100 bus standard. The S-100 bus is the professional level choice for commercial, industrial and scientific applications. This bus provides for ready expansion and modification as the state of the art improves. We believe that this board, with the rest of the **CompuPro** family, is one of the best boards available for that bus.

Features such as 5 Mhz operation, 24 bits of extended addressing, power-on jump, and the ability to have 16 bit power in an S-100 system at a reasonable price, make the **CPU 8085/88** another proud member of the **CompuPro** family.

Thank you for choosing a **CompuPro** product.... welcome to the club!

TECHNICAL OVERVIEW

The **CPU 8085/88** Dual Processor board was specifically designed to make it easy for the S-100 Bus user to get into the world of 16 bit micros, while at the same time preserving compatiblity with existing hardware and software.

We accomplished this goal by choosing the Intel 8088 16 bit CPU, (an 8 bit bus version of the 8086), and the 8085A 8 bit CPU. The 8085 provides both hardware and software compatibility with the current crop of S-100 peripherals, and the 8088 provides for greatly enhanced software capability while maintaining an 8 bit external bus for hardware compatibility.

The user may switch back and forth between the two processors with a simple software command. For example, this allows the user to let the 8085 run his currently available (and familiar) disk operating system while letting the 8088 run the more advanced applications software. One processor would then "call" the other to handle the task most suited to it.

This environment is also extremely effective when trying to develop new software for the 8088. One may use tools available that run under the 8085 (such as CP/M and Microsoft's 8086/88 Macro Cross-Assembler that runs under CP/M) to write the new code and then simply switch over to the 8088 to try it out. PROM's need not be burned and erased and systems pulled apart to transfer the code to the 8088 system.

Both processors currently run at 5 Mhz which maximizes bus throughput. A switch is provided to slow the 8085 down to 2 Mhz for software dependent timing loops that want to run at that speed and are not easily changed. Intel says that an 8 Mhz 8088 and faster 8085's are on the way, and this board was designed with the faster chips in mind. By merely changing a crystal you may upgrade the board to use a faster processor when they become available. Current state of the art in UART's (used in serial I/O boards) is barely able to cope with this 5 Mhz bus rate, so a switch is provided on the **CPU 8085/88** to add one wait state to every I/O cycle.

Power-on-jump circuitry is provided that allows the CPU to begin it's execution at any 256 byte boundary (within the lower 64K). A switch is provided to disable this feature. A switch is also provided to allow the power-on-jump circuitry to be active at power-on only, or to work at power-on and every time a RESET occurs (jump-on-reset).

The 8085 can directly address 64K bytes of memory, but our built-in Memory Manager scheme allows access to the full 16 megabytes available per the IEEE S-100 standard. The 8088 can directly address 1 megabyte, but our Memory Manager is smart enough to know which processor is in control. Thus the 8088 uses only the upper four bits of the Memory Manager so it too can access the 16 megabyte address space. This will be described in greater detail later.

The **CPU 8085/88** rigidly adheres to the IEEE S-100 standard to insure compatibility with future S-100 components, but should also work quite well with most well designed pre-IEEE hardware. For example, provision is made to use the IMSAI front panel even though it doesn't exactly fit into the new standard.

Many long hours of thought and revision went into this product and we at Compupro are confident that it will provide years of solid service. We sincerely hope that you will enjoy it.

8085 Only OPERATION

If you purchased the 8085-only version of this board you will need to install two jumpers. If you have the assembled and tested or CSC versions, these jumpers are installed for you already.

One is labeled J3 and is located above and slightly to the right of U17. The other is labeled J4 and is located above and slightly to the right of U23.

Use a small piece of wire, such as that left over from a component lead. Be sure and leave enough of a loop (about 1/4 inch) so that it may be easily cut when upgrading to the 8088. Solder the jumpers on the solder side of the board and trim off the excess leads.

If you are providing your own 8088 and 8284, do not install J3 and J4!

SWITCH S1

Switch S1 is located between U6 and U7 and is used to select the various options and operational modes of the **CPU 8085/88.**

EXTENDED ADDRESS OPTIONS

The first two positions of S1 are used to control how the upper 8 address bits (A16-23) respond to certain system operations.

Switch position 1 is labeled **XA3** and is used to control whether or not A16-23 will be tri-stated when ADSBL* is asserted on the S-100 Bus. ADSBL* is used to tri-state the system address bus, usually during a DMA.

Newer DMA devices that meet the IEEE S-100 specs are required to provide the full 24 bit address to the bus during a DMA, but most of the older devices do not.

If you have a device that provides all 24 address bits then turn switch position 1 ON. Otherwise turn switch position 1 OFF.

Switch position 2 is labeled **XAC** and is used to control whether or not the extended address bits (A16-23) are cleared when RESET* is asserted on the S-100 Bus.

The extended address register will always be cleared on a power-up, but after your program sets it's value you may not want it to be cleared (set to 0) each time a RESET occurs.

If you desire the bits to be cleared on RESET* then turn switch position 2 ON. If you want to leave the register unchanged after a RESET* then turn switch position 2 OFF.

I/O WAIT STATE SELECTION

Switch position S3 is labeled **IOW** and is used to control whether or not a wait state will be inserted into every I/O cycle.

This is particularly useful when running at 5 Mhz and beyond. Older design I/O boards may have trouble running at 5 Mhz, especially those with UARTs. To deal with this problem the **CPU 8085/88** allows automatic insertion of one wait state to each I/O cycle.

To allow wait state generation turn switch position 3 ON. To inhibit automatic wait state generation turn switch position 3 OFF.

PROCESSOR INITIALIZATION AFTER SWAP OPTIONS

The **CPU 8085/88** contains circuitry that handles orderly change-overs between the 8085 and the 8088. Part of this circuitry determines what state the respective processor will be in when it comes "on line".

One mode of operation will cause a RESET to be issued to the processor as it comes on line. This will cause the 8085 to go through a power-on-jump sequence (if enabled) or to begin execution at address 0000 hex. The 8088 will begin execution at FFFF0 hex.

Otherwise, when each processor comes on line it will begin it's execution at the place where it went off line. In other words, it just picks up where it left off.

If you desire the 8085 to always be reset when it comes on line then turn switch position 4 ON (labeled **5RS** for 8085-Reset-On-Swap). If you want the 8085 to resume operations in place when coming on line, then turn switch position 4 OFF.

If you desire the 8088 to always be reset when it comes on line then turn switch position 5 ON (labeled **8RS** for 8088-Reset-On-Swap). If you want the 8088 to resume operations in place when coming on line, then turn switch position 5 OFF.

NOTE: When both processors come on line the first time they will go through their normal power-up sequence regardless of the settings of these two switches.

JUMP-ON-RESET

The **CPU 8085/88** contains a "power-on-jump" circuit that allows the 8085 to begin it's execution at any 256 byte page boundary. In the strictest sense of the definition, a power-on-jump circuit should only be active at power on. But sometimes it is convenient to perform the jump each time a RESET* occurs. We have provided this option for you.

Switch position 6 is labeled **JOR** and is used to determine whether or not the 8085 will jump on reset or only on power on. If you desire a jump sequence to occur for resets then turn switch position 6 ON. If you want the jump to occur at power on only then turn switch position 6 OFF.

MWRITE ENABLE

Switch position 7 is labeled **MW** and is used to determine if the **CPU 8085/88** will generate the S-100 signal MWRITE.

The IEEE S-100 standard states that MWRITE shall be generated only in one place in a given system. Some systems, notably those with front panels (ie:IMSAI 8080), have circuitry that generate MWRITE. This circuitry is not easily disabled. Some systems do not have an MWRITE generator, so it is up to the CPU to provide MWRITE to the bus.

The important point here is that you only want one MWRITE generator in your system. If your current system has an MWRITE generator in it, you will want to turn switch position 7 OFF. If your current system has no MWRITE generator in it (or if you are about to remove your old CPU card that generated it) you will want to turn switch position 7 ON.

To sumarize, turning switch position 7 ON will allow the **CPU 8085/88** to generate MWRITE and turning switch position 7 OFF will inhibit generation of MWRITE by the **CPU 8085/88.**

POWER-ON-JUMP ENABLE

Switch position 8 is labeled **POJ** and is used to enable or disable the power-on-jump feature of the **CPU 8085/88.**

If you desire to have the power-on-jump feature active then turn switch position 8 ON. If you don't want the power-on-jump feature to be active then turn switch position 8 OFF.

If the power-on-jump feature is not utilised then the 8085 will begin it's execution at 0000 hex, which is it's normal mode of operation.

DIP SWITCH 2

POWER-ON-JUMP ADDRESS

Dip switch 2 is located between U25 and U26 and it is used to set the address that the **CPU 8085/88** will jump to on power-on if enabled.

The **CPU 8085/88** can jump to any 256 byte page boundary in the lower 64K of address space. Switch 2 is set to correspond to the bit pattern of A8-15 of the page you want to jump to. When a switch is ON it represents a "one" and conversly when a switch is OFF it represents a "zero".

SWITCH 2

Switch Position	Address Bit	
1	A8	
2	A9	
3	A10	ON = "1"
4	A11	
5	A12	
6	A13	OFF = "0"
7	A14	
8	A15	

For example, if you want to jump to E000 you would turn switch positions 1 through 5 OFF and switch positions 6 through 8 ON.

DIP SWITCH 3

MEMORY MANAGER/PROCESSOR SWAP PORT ADDRESS

Dip switch 3 is located between U33 and U34 and is used to set the address of the I/O port that is used to control the memory manager (output) and to swap processors back and forth (input).

One port address is used by the **CPU 8085/88** and it is determined by setting the positions of dip switch 3 to correspond to the lower 8 address bits (A0-7) of the desired port address.

When a switch is turned ON it represents a "zero" and conversly when a switch is turned OFF it represents a "one". Note that this is the opposite of switch 2.

SWITCH 3

Switch Position	Address Bit	
1	A0	
2	A1	
3	A2	ON = "0"
4	A3	
5	A4	
6	A5	OFF = "1"
7	A6	
8	A7	

The "standard" port address is FD hex. Any software that is provided by Compupro will assume that this switch is set for port FD. To set the switch for port FD turn switch position 2 ON and all other switch positions OFF.

2 OR 5 MHz OPERATION

SWITCH 4

Switch 4 is used to select whether the 8085 will run at 2 Mhz or 5 Mhz. In some older systems, with slower memory, it may be necessary to run at 2 Mhz. Some older generation hardware will not operate correctly or reliably at 5 Mhz (such as the IMSAI front panel). Also some software has timing loops that depend on a 2 Mhz processor. If possible these loops should be modified, but some are undocumented making them hard to find and therefore change. If this is the case, you will probably want to run at 2 Mhz.

Switch 4 is located at the upper right hand corner of the board and is the large paddle switch with the red handle.

Putting the switch in the left-most postion will cause the 8085 to run at 2 Mhz. Putting Switch 4 in the right-most position will cause the 8085 to run at 5 Mhz.

This switch is not designed to be changed while running. It may work while running, but your program may also bomb. We make no guarantees!

Note that this switch affects the 8085 only. The 8088 always runs at 5 Mhz.

USING THE MEMORY MANAGER

The Compupro Memory Manager scheme works as follows:

A standard 8 bit microprocessor (such as the 8085) can only directly address 64K bytes of memory. That takes a 16 bit address bus. But the new IEEE S-100 standard provides for 24 bits of address bus which allows addressing of 16 megabytes. The problem is how to allow a processor with only 16 bits of address to appear to have 24 bits.

What we have done is to take an eight bit output port and latch any data byte that is written to it. This latched information is then bufferred and placed on the upper 8 address lines on the S-100 bus (A16-23). Now an 8 bit processor has access to 16 megabytes instead of it's usual 64K bytes.

Those that are familiar with bank select schemes will appreciate that this is quite similar, but instead of having the port duplicated on every memory board, it appears in only one place in the system. The biggest advantage that this has over bank select schemes is that the physical memory boards are standardized because of the IEEE defined address lines.

So when using the 8085 one just writes an 8 bit word out to the output port that is selected by the setting of Dip Switch 3 and then by the begining of the next cycle that address will appear on A16-23.

But things are a bit different when using the 8088. The 8088 has 20 address bits so it can directly address 1 megabyte of memory. The Memory Manager is smart enough to know if the 8088 is in control of the bus. If the 8088 is in control, only the upper four bits of the memory manager port are used and the lower four come direct from the 8088. In other terms, A0-19 come from the 8088 and A20-23 come from the Memory Manager latch.

As with the 8085, the 8088 will write a full byte to the port, but only the upper four bits will ever see the bus. The full byte is latched, however, and all eight bits will appear on the bus when the 8085 comes back on line.

All eight bits will always be cleared (set to 0) on power up. See the Option Selection section of this manual for more options concerning the Memory Manager. (Dip Switch 1, positions 1 and 2, and Dip Switch 3.)

SWAPPING PROCESSORS

On power-up, the 8085 will always be in control of the bus and the 8088 will be asleep, just as if it was never turned on. To change over to the 8088, and to subsequently change back and forth, all that need be done is a simple INPUT instruction from the Processor Swap Port.

This port is shared with the memory manager port in that they share the same address space. Hence they are both set with dip switch 3. The memory manager uses the output side, and the swap function uses the input side. The "standard" port address is FD hex. See the Option Selection section of this manual to find out how to set this address.

When the 8088 comes on line for the first time, it will go through it's normal initialization sequence, which is that it will begin to execute code at address FFFF0 (0FFFF0 if you take the Memory Manager into account). After that first time it comes on line there are two optional ways for it to come on line thereafter.

One is just like the first, in that a RESET will be issued to the 8088 before any execution can ensue. This will cause it to again begin to execute code at FFFF0.

The other mode is one where the 8088 just "sleeps" in place until it is reawakened, when it picks up where it left off as if nothing had happenned.

Either mode can be useful depending on the application. The RESET mode may be useful in a developement atmosphere, but the sleep mode may be more practical in a real-time environment.

The 8085 can work in just the same way as the 8088. It will either do a normal power-on sequence (where it executes at 0000) or it can do a power-on-jump if enabled, when the system is powered up.

Ater the 8088 gains control, by the 8085 doing an IN to the processor swap port, you have the same options for when it comes back on line as you do with the 8088.

You may have the 8088 in one mode and the 8085 in the other or both the same. See the Option Selection section of this manual (Dip Switch 1, locations 4 and 5) to determine how to select the modes you desire.

Note that if you elect the RESET mode for the 8085 and the power-on-jump is enabled, the 8085 will do a power-on-jump sequence each time it comes on line.

Since the command to swap processors is an IN instruction, and the purpose is not really to read any information from the input port, FF hex will be returned in the A register. This means that any previous contents will be lost. So if the contents of the A register are important to you, be sure to store it somewhere first (a PUSH instruction would be the most likely).

The following is an example of a typical program flow using both processors, assume sleep mode for both:

Computer Powers Up
8085 does a power-on-jump
Program begins to execute
Time to swap processors
Load in object module for 8088
Set up jump to 8088 code at FFFF0 hex
Push A register
Do an IN from port FD hex
(on board hardware puts 8085 to sleep
and wakes up 8088)
8088 now on line
8088 begins execution at FFFF0 hex
Jump to object module
Perform task
Time to swap processors
(ie: need something from disk)
Put info to be passed in RAM
(ie: task info: drive number, sector etc.)
Push A register
Do an IN from port FD hex
8085 back on line
Pop A register
Perform task
Push A register
Do an IN from port FD hex
8088 back on line
etc.

The last obvious consideration is that one processor should generally not modify the execution or stack areas of the other processor. This requires careful planning on the part of the programmer.

The complete software picture would require an entire book in itself and maybe someone out there would like to write one, but this manual will not attempt to delve into it any further.

The **CPU 8085/88** contains four basic sections of circuitry. They are: The Processor and Bus Interface Circuitry, the Processor Swap Circuitry, the Memory Manager Circuitry and the Power-on-Jump Circuitry. We will discuss each section individually.

The processor and S-100 Bus interface circuitry performs the necessary primitive functions such as providing clocks to the CPUs, signal buffering and timing conversion to fit the S-100 IEEE standard. Some signals are "synthesized" for the S-100 bus since neither CPU generates those signals directly.

The 8085 has a built-in clock generator which the **CPU 8085/88** takes advantage of when running at 5 Mhz. A crystal that is two times the desired frequency is hooked across the appropriate pins. In this case the crystal is X3 and is 10 Mhz which gives us the desired 5 Mhz operating frequency.

But in-between the crystal and the 8085 is a SPDT switch, S4. S4 allows either the crystal to be hooked up directly to the CPU or allows insertion of a 4 Mhz clock signal (more about that signal later). This causes the CPU to run at 2 Mhz.

The 8088 requires a completely different clock circuit. It requires a clock frequency three times the desired operating frequency and it must have a 67/33 % duty cycle. For this we use the Intel 8284 IC, a clock generator designed specifically for the 8088/86. The 15 Mhz crystal, X2 is hooked up to the 8284 which then provides the necessary division by three and the proper duty cycle. No provision has been made, other than by changing the crystal, to alter the 8088's operating frequency.

The S-100 bus requires a 2 Mhz clock signal on pin 49 regardless of the operating frequency of the processor. This is provided by an oscillator comprised of three sections of U8 and X1, a 4 Mhz crystal. The 4 Mhz output of the oscillator is used above to run the 8085 at 2 Mhz. The 4 Mhz signal is also divided by a flip-flop to 2 Mhz, is buffered and goes out to the bus.

Both processors have a bi-directional data bus. Both are tied together (one is always tri-stated). The resultant data bus is buffered by U37 and then goes out onto the DO bus. U37 can be tri-stated by the DODSB* signal on the S-100 Bus. The DI bus is buffered by U38 and U38's outputs are tied to the internal data bus. Those outputs are enabled by the DBIN signal, but will be disabled by the POJ* signal or the RUN line on the S-100 bus. RUN is used by IMSAI-type front panels to force data into the CPU over the 16 pin cable (J2) so the DI buffer should be turned off. A pull-up resistor is provided on the RUN line so that systems not utilising this line will still work. Note that RUN is no longer a specified signal on the S-100 Bus. [7]

Both the 8085 and the 8088 put the lower 8 address bits on the data bus during the first part of the cycle. The ALE signal from both processors is used to latch this information. Both ALE signals are ORed by a section of U23 to generate the SYSALE signal. We now have a common ALE signal for the whole card that will represent the 8085 ALE when it is in control and the 8088 ALE when it is in control.

The data bus is tied to the inputs of of U35, a 74LS373 transparent latch. The latch control is hooked to the SYSALE signal. This latches the address information from the data bus. The outputs of U35 become A0-A7 on the S-100 Bus.

A8-15 from both processors are tied together (one is always tri-stated) and are buffered by U36 and go out onto the S-100 bus. Both U35 and U36 may be tri-stated by the ADSB* signal.

The 8085 has three lines; S0, S1, and IO/M* from which all of the possible states of operation (status) may be decoded. The 8088 has three similar lines; SSO, IO/M* and DT/R*. The code on the two sets of lines is completely different. All the lines from the 8088 are tri-stated during a HOLD, but S0 and S1 from the 8085 are not. Two sections of U40 allow these two signals to be tri-stated, being contolled by the HLDA signal from the 8085.

The two sets of three lines may now be tied together. These are fed into a bipolar PROM, U30, that decodes the signals into the S-100 status signals. But the codes on the two lines are different. The **CPU 8085/88** has a signal called 8/5* that is high when the 8088 is in control and low when the 8085 is in control. This signal is used to select between two sets of data inside the PROM so that the three lines are decoded differently depending on which processor is driving the lines.

The status signals are buffered by U39 and then go out to the S-100 bus. The outputs of U39 may be tri-stated by the SDSB* signal.

The processor control signals on the S-100 Bus, pSYNC and the like, are the most difficult to synthesize, so we will discuss each signal seperately.

The signal pSYNC is used to signify the begining of each machine cycle. The SYSALE signal occurs at the begining of each machine cycle so it makes sense to use that for pSYNC.

It cannot be used directly because it does not have the proper relationship to the bus clock.

SYSALE sets a flip-flop by clocking in a "1" as it rises. The output of the flip-flop is connected to the D input of another flip-flop. The second flip-flop is clocked by the system clock so that after the next rising edge of the clock it's output will go high. This is the pSYNC signal.

When the inverting output of the second flop goes low it clears the first flip-flop which makes the D input to flop 2 go low. On the next rising edge of the system clock this low will be clocked out ending the pSYNC signal.

The first flip-flop is needed because ALE is not guaranteed to be stable during that first rising edge of the clock.

The signal pSTVAL* goes low to signify that the address and status bus are stable and contain valid information. This signal is generated by NANDing pSYNC with inverted system clock.

The signal pDBIN is used to signify that the CPU wants to read data on the DI bus. It is the read strobe for the S-100 bus. The S-100 bus specification states that pDBIN should go high during a memory read, input or interrupt acknowledge cycle.

The RD* signals from the CPUs will go low for a memory or I/O cycle, but not for an interrupt acknowledge cycle. The INTA* signal goes low for interrupt acknowledge cycles.

So to synthesize the pDBIN signal the INTA* signals from both CPUs are tied together, as are the RD* signals. (As with the data bus, only one is ever active). The composite RD* and INTA* signals go into the inputs of a NAND gate which provides inversion and an OR function at the same time. So either RD* or INTA* can cause pDBIN.

The output of this gate is the DBIN signal used on-board, but occurs too early to meet the S-100 Bus spec. Therefore the DBIN signal is gated by the inversion of pSYNC so that pDBIN cannot start until pSYNC is low. The resultant signal is inverted and becomes pDBIN.

The signal pWR* is used to signify that valid data is on the DO bus to be written into a memory or I/O device. It is the generalized write strobe for the S-100 bus.

Both WR* lines from the CPUs are tied together (one is always tri-stated). The signal direction is OK for the S-100 bus, but the timing is not. The S-100 Bus spec states that data must be valid before the leading edge of the write strobe and after the trailing edge of the write strobe.

The 8085 and 8088 guarantee data to be valid after the trailing edge, but not before the leading edge. Therefore we must delay the leading edge of pWR*. Delaying pWR* until the next positive clock edge will meet the timing requirements nicely, so we do just that.

The write strobe is presented simultaneously to one input of an OR gate and the D input of a flip-flop. The clock input to the flip-flop is the system clock which has been clocking in a high from the inactive write strobe, so the output of the flop will be high. The output of the flop is connected to the other input of the OR gate.

So when the write strobe is inactive (high), both inputs to the OR gate will be high making the output high. When the write strobe goes low, one input to the OR gate will go low but the output will remain high. After the next rising edge of the clock the output of the flip-flop will go low making the other input to the OR gate low. The two lows will cause the output of the OR gate to go low making our pWR* signal. When the write strobe returns high, so will the output of the OR gate ending pWR* at the right time.

The pHLDA signal is used to signify that the processor has relinqushed the bus to another temporary master, usually a DMA device. The generation of this signal will be covered under the section concerning the processor swap circuitry.

All of these signals are buffered by U27 and go out to the S-100 Bus. U27 may be tri-stated by assertion of the CDSB* signal.

The two RDY signals on the S-100 Bus are used to extend the current bus cycle for slow memory, single stepping etc. They are ANDed together along with the on-board I/O wait state generator. The resultant output is then connected directly to the 8085 RDY input, but is synchronized to the clock by a flip-flop for the 8088. The output of the flip-flop goes to the ready input of the 8284 and then to the 8088 itself. The flip-flop is necessary because of a timing idiosyncracy in the 8284.

The on-board wait state generator is a flip-flop whose D input is an extended ALE derived from the pSYNC generator. This is clocked in and out by the system clock, causing one wait state to be generated. The CLR input to the flip-flop is tied to the IO/M line from both processors which is low during memory cycles. This will cause the flip-flop to be inactive during memory cycles so that wait states will only be generated during I/O cycles.

The output of the flip-flop is connected/disconnected from the RDY circuits by a dip switch.

The interrupt lines, NMI* and pINT* are inverted and then gated by some AND gates that are turned on and off by the 8/5* line and it's inversion. This logic is used to steer the interrupt inputs to the processor currently on line.

The MWRT signal is the memory write strobe for the S-100 bus and is generated by NORing pWR* and the status line sOUT. MWRT may be disconnected from the bus by a dip switch. MWRT is buffered by a section of U31.

The power-on-clear circuitry is used to initialize on board logic and also to generate the POC* signal for the S-100 Bus. Tri-state buffers are enabled by the POC* signal to also drive RESET* and SLVCLR* low at power-on, per the S-100 bus spec.

A simple RC time constant is formed by R15 and C9 which is buffered by a section of U40 acting as a schmitt trigger.

This completes the description of the Processor and Bus Interface Circuitry. Next we will describe how the Processor Swap Circuitry operates.

PROCESSOR SWAP CIRCUITRY

It is the job of the processor swap circuitry to handle the orderly change-over between the two CPUs on the **CPU 8085/88.**

The basic theory is this: One processor is "put to sleep" by pulling it's HOLD line high. This line is normally used for DMA. We are told by the CPU that it has gone to sleep (relinquished the bus by tri-stating it's outputs and suspending all internal operations) by the HLDA line that is active high.

What the processor swap circuitry does is to alternatively make the HOLD line to each processor high and low to control which one is on line. Since the HOLD line is also normally used for DMA, some logic must be provided to steer the pHOLD* line from the S-100 bus to the processor on line, and to arbitrate between a hold from the bus and an internal hold.

There must also be a "command" signal that tells the circuitry to change processors. This is done by decoding an I/O port and making a command pulse each time an access is done. This port address is shared with the Memory Manager circuitry (described later).

At power-on, the signal 85HOLD from the output of flip-flop U10 will be low, and the signal 88HOLD from the output of filp-flop U9 will be high. This means that the 8085 will come up running and the 8088 will be held. Also a signal named 8/5* will be low signifying that the 8085 is in control. This signal originates from flip-flop U5.

The I/O port is decoded by the 25LS2521 eight bit comparator, U34. The output of U34 is inverted and applied to one input of U3, a three input NAND gate. The other two inputs are tied to pDBIN and sINP. When all three signals are high the output of U3 will go low. This is inverted and used to clock a flip-flop, U2. The flip-flop's D input is tied high making the non-inverting output of the flop go high. The non-inverting output is tied, through two inverters for delay, to the clear input of the flop. So after two gate delays the flip-flop will be cleared. This produces a short pulse at it's outputs. This signal is called PORTPULSE*, and is the swap command pulse we need.

When PORTPULSE* occurs, it sets the output of U10a to a one. Assuming there is no DMA request from the bus PHOLD (an internal board inversion of the bus pHOLD*) will be low. This allows the high from U10a to pass through the OR gate U23, presenting a high to the D input of U10b. On the next positive transition of the 8085 clock, the output of U10b (85HOLD) will go high. This causes a hold request to be issued to the 8085.

When the 8085 is done with the current cycle or cycles it will raise it's HLDA line, 5HLDA. This indicates that the 8085 outputs are tri-stated and internal operations have been suspended. When 5HLDA rises it will clock a low out of flip-flop U9a. This low will pass through OR gate U23 and appear at the D input to U9b. After the next rising edge of the 8088 clock, the output of U9b (88HOLD) will go low. This will allow the 8088 to begin operations.

On the next occurence of PORTPULSE* the whole process will be reversed.

PORTPULSE* will also clock U4b which is set up as a divide by two toggle. U4b's output will be low at power-on. This output is tied to the D input of U5a. The output of U5a (8/5*) will also be low at power-on. The clock input of U5a will be clocked by either 5HLDA or 8HLDA going low, signifying a processor coming on line.

So when PORTPULSE* occurs U4b will change states, and when a processor comes on line the state of U4b will be clocked through U5a, changing the state of the 8/5* line. This lets the on-board circuitry know which processor is in control.

The signal that clocks U5a (signifying a CPU coming out of a hold state) also clocks U4a. U4a then produces a pulse called HOLDOVER*. The signal that clocks U5a and U4a is inverted (which means it now signifies a CPU going into the hold state) and used to clock U12b. The D input of U12b is the PHOLD signal which will be low if there is no bus DMA request.

The output of U12b is BHLDA, which after being buffered becomes pHLDA on the S-100 Bus. So if there is no bus hold request (PHOLD low), when U12b is clocked, BHLDA will remain low. This is exactly what we want- we don't want the bus to see the internal hold operations.

But if PHOLD is high, BHLDA will go high. When the HOLDOVER* pulse occurs, at the end of the DMA, U12b will be reset causing BHLDA to return low.

Some arbitration is needed to hold off a hold request from the S-100 Bus during a processor swap. This is accomplished with flip-flop U2b and a NOR gate U14.

The pHOLD* signal from the S-100 Bus goes to one input of the NOR gate. The other input comes from the output of U2b. This output is normally low, allowing the pHOLD* signal through the gate (with inversion). The output of the gate becomes PHOLD. When PORTPULSE* occurs, a high will appear at the output of U2b which will inhibit pHOLD* from going through the NOR gate. The HOLDOVER* pulse will clear U2b allowing pHOLD* through the gate again.

PHOLD is allowed to ripple through the sections of U9 and U10 because of OR gate U23. This allows the hold request to get to the processors, unless it is held off by the previously discussed circuitry.

When the processor changes, so must the system clock. This is accomplished with a flip-flop, U12a, and some tri-state buffers from U24.

The flip-flop is constantly being clocked by the current system clock. The non-inverting output is hooked to the tri-state control of one section of U24 (U24b) and the inverting output is hooked to the tri-state control of another section of U24, U24a. The D input to the flop is hooked to the 8/5* line.

The input to U24b is the clock from the 8085 and the input to U24a is the clock from the 8088. Since the tri-state inputs are connected to opposite outputs of U12a, only one section of U24 will be turned on at a time.

When 8/5* changes, the change will be reflected in the outputs of U12a which will turn on the appropriate section of U24 allowing the correct clock to become the system clock.

The last section of the processor swap circuitry concerns the Reset-On-Swap option. This circuit allows a RESET to be issued to the processor that is just coming on line.

U7 is a 74LS221 dual one-shot. A one-shot produces a pulse of a fixed duration in response to an edge-triggered input. The duration of the pulse is set by a resistor and capacitor.

The resistors and capacitors in this case are R3 and 4, and C5 and C6. Their values will produce a pulse of about two microseconds.

The trigger inputs are the HLDA signals from the CPUs. The trigger inputs of U7 are set up to trigger on the negative going edge. So, for example, when 5HLDA falls (signifying that the 8085 is about to come on line) a 2 microsecond pulse will be issued from U7. This pulse goes to the 8085 reset input which causes the processor to reset.

The outputs of U7 may be connected/disconnected from operation by means of a dip switch.

This completes the section on the processor swap circuitry. Next we will explain the Memory Manager.

MEMORY MANAGER CIRCUITRY

The function of the memory manager is more clearly defined in the section entitled USING THE MEMORY MANAGER. Please refer to that section for an explanation of what the memory manager's functions are. Here we will only explain how the circuitry works.

As explained in the previous section, the memory manager's port address decoder is shared with the processor swap port. The processor swap port uses the 'input' side, while the memory manager uses the 'output' side.

The output is decoded by the signal from U34, sOUT and the inversion of pWR*. These three signals are connected to the inputs of a three input NAND gate, U3. The output of U3 will go low when all three inputs are high, signifying an output to the selected port. The output will return high at the end of the output cycle, but data will still be valid.

This positive going edge is used to latch data from the data bus into U28, a 74LS273 octal latch. The upper four outputs of the latch go to U33, a 74LS373 octal transparent latch. The lower four outputs of U28 go to half the inputs of U29, a 74LS157 quad two input multiplexer.

The control input to the multiplexer is the 8/5* line. When 8/5* is low, signifying that the 8085 is in control, the four outputs of U28 pass through the multiplexer to the other four inputs of U33. But when the 8088 is in control (8/5* high), the four outputs of the multiplexer no longer represent the outputs of U28, but instead represent A16-19 from the 8088.

SYSALE is used to latch the outputs from U28 and U29 into U33. The outputs of U33 become the S-100 extended address bits A16-23. SYSALE is needed because the 8088 only puts address info on the A16-19 lines during the first part of the cycle (as it does with the data/address lines). It also ensures that the address on the bus changes at the first part of the next cycle, instead of the last part of the current cycle.

U28 will be cleared at power-on. It may also be cleared by each succesive bus RESET* depending on the position of a dip switch.

The outputs of U33 will be tri-stated by a POC*, RESET* or ADSB*. ADSB* can be ignored by the memory manager by setting a dip-switch.

This completes the description of the memory manager circuit. Next we will discuss the operation of the power-on-jump circuit.

POWER-ON-JUMP CIRCUITRY

The power-on-jump circuitry used in the **CPU 8085/88** is designed to allow the 8085 to begin execution of a program at some address other than 0000. It does this by forcing a jump op-code (C3 hex, followed by a byte of zeroes and then an eight bit value that contains the starting address of the page you want to jump to.

At power-on, flip-flop U5b is cleared, setting it's non-inverting output high. This output is connected to one input of NAND gate U16. The other input to U16 is connected to DBIN. When both signals are high, the output (POJ*) will go low. This will enable the octal buffer U26 and disable the normal DI driver, U38.

At address 0, a C3 hex will be presented to the inputs of U26 and thus to the 8085. C3 is the 'jump' op-code. At address 1, a byte of zeroes will be presented to the inputs of U26. At address 2, the setting of dip switch 2 will be presented to the inputs of U26. The setting of dip switch 2 should correspond to the upper byte of the desired memory address.

Finally, at the next address, U5 will clock it's non-inverting output low, causing U26 to be tri-stated and the normal DI buffer to be re-enabled. This allows the next byte to be read from the bus, and normal execution ensues.

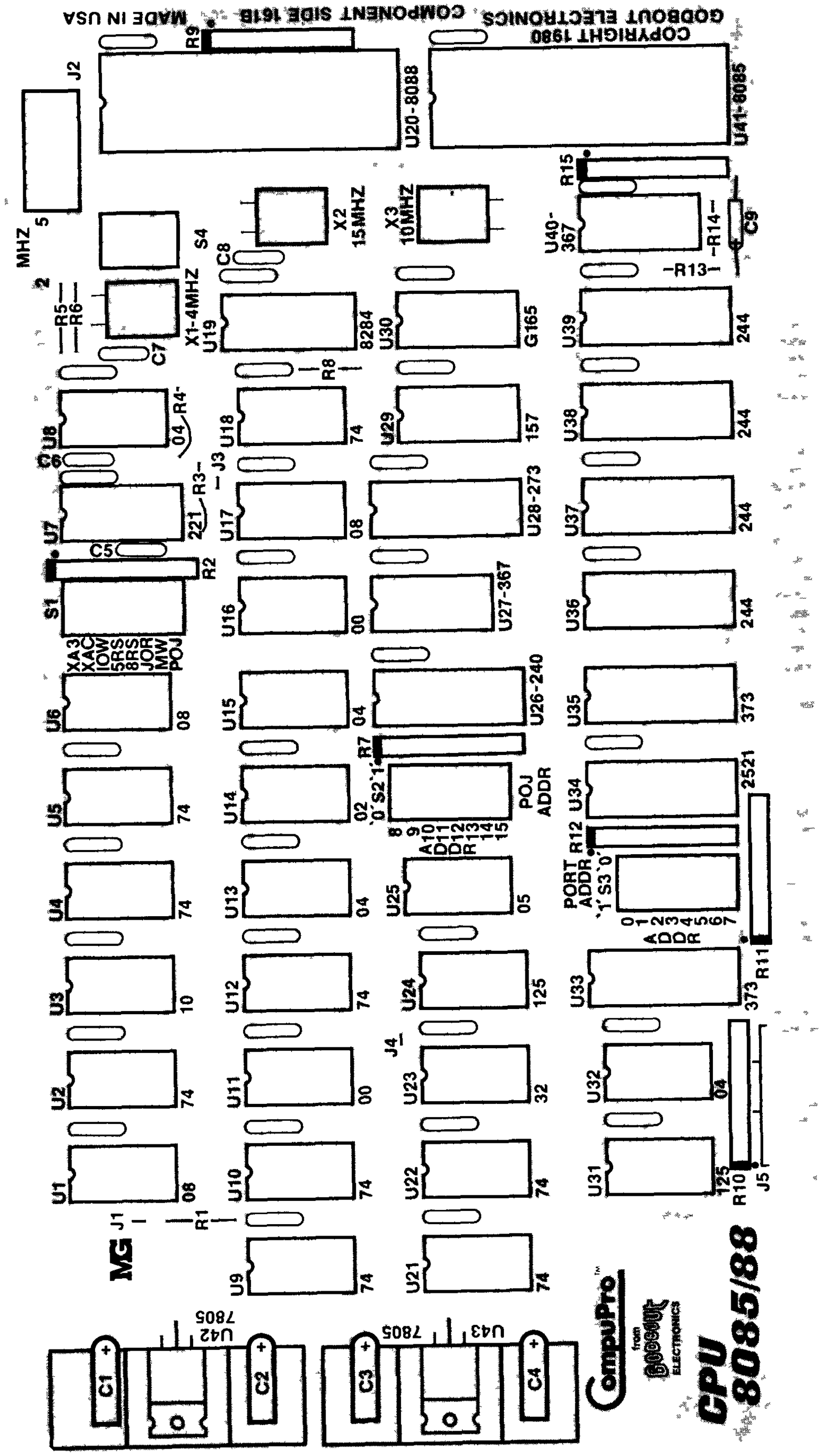
The output of U16 (POJ*), can be disabled by a dip switch, which will cause the power-on-jump circuitry to be inactive.

The power-on-jump circuitry will activate after a POC*, and if desired, after each RESET*. This option is also set with a dip switch.

This completes the circuit description of the **CPU 8085/88.**

Parts List

☐	(1)	Circuit Board		
		INTEGRATED CIRCUITS (NOTE. the following parts may have letter suffixes and prefixes along with the key numbers given below.		
☐	(2)	74LS00	quad 2 input NAND	(U11,16)
☐	(1)	74LS02	quad 2 input NOR	(U14)
☐	(4)	74LS04	hex inverter	(U8,13,15,32)
☐	(1)	74LS05	hex inverter O.C.	(U25)
☐	(3)	74LS08	quad 2 input AND	(U1,6,17)
☐	(1)	74LS10	triple 3 input NAND	(U3)
☐	(1)	74LS32	quad 2 input OR	(U23)
☐	(9)	74LS74	dual D flip-flop	(U2,4,5,9,10 12,18,21,22)
☐	(2)	74LS125	quad tri-state driver	(U24,31)
☐	(1)	74LS157	quad 2 input MUX	(U29)
☐	(1)	74LS221	dual one shot	(U7)
☐	(1)	74LS240	octal inv. bus driver	(U26)
☐	(4)	74LS244	octal bus driver	(U36-39)
☐	(1)	74LS273	octal latch	(U28)
☐	(2)	74LS367	hex bus driver	(U27,40)
☐	(2)	74LS373	octal trnsprnt latch	(U33,35)
☐	(1)	25LS2521	octal comparator	(U34)
☐	(1)	G165	32x8 bipolar PROM	(U30)
☐	(1)	8085A-2	5 Mhz microprocessor	(U41)
☐	(2)	7805	5 volt regulator	(U42,43)
		OTHER ELECTRICAL COMPONENTS		
☐	(1)	crystal, 4 Mhz		(X1)
☐	(1)	crystal, 10 Mhz		(X3)
☐	(5)	39mfd, 10v tantalum capacitor		(C1-4,9)
☐	(2)	.001mfd disc capacitor		(C5,6)
☐	(1)	.01mfd disc capacitor		(C7)
☐	(36)	bypass, disc capacitor		
☐	(1)	270 ohm resistor		(R13)
☐	(2)	390 ohm resistor		(R5,6)
☐	(2)	1K ohm resistor		(R8,14)
☐	(3)	4.7K ohm resistor		(R1,3,4)
☐	(7)	SIP resistor networks		(R2,7,9-12,15)
		MECHANICAL COMPONENTS		
☐	(42)	low profile sockets		
☐	(3)	8 position DIP switches		(S1-3)
☐	(1)	paddle switch		(S4)
☐	(2)	heat sinks		
☐	(2)	sets 6-32 hardware		
☐	(2)	card ejectors		
☐	(1)	set user's manuals		
		ADDITIONAL COMPONENTS FOR 8088 OPTION		
☐	(1)	8088	5 Mhz 16 bit MPU	(U20)
☐	(1)	8284	clock generator	(U19)
☐	(1)	crystal, 15 Mhz		(X2)
☐	(1)	10pfd disc capacitor		(C8)

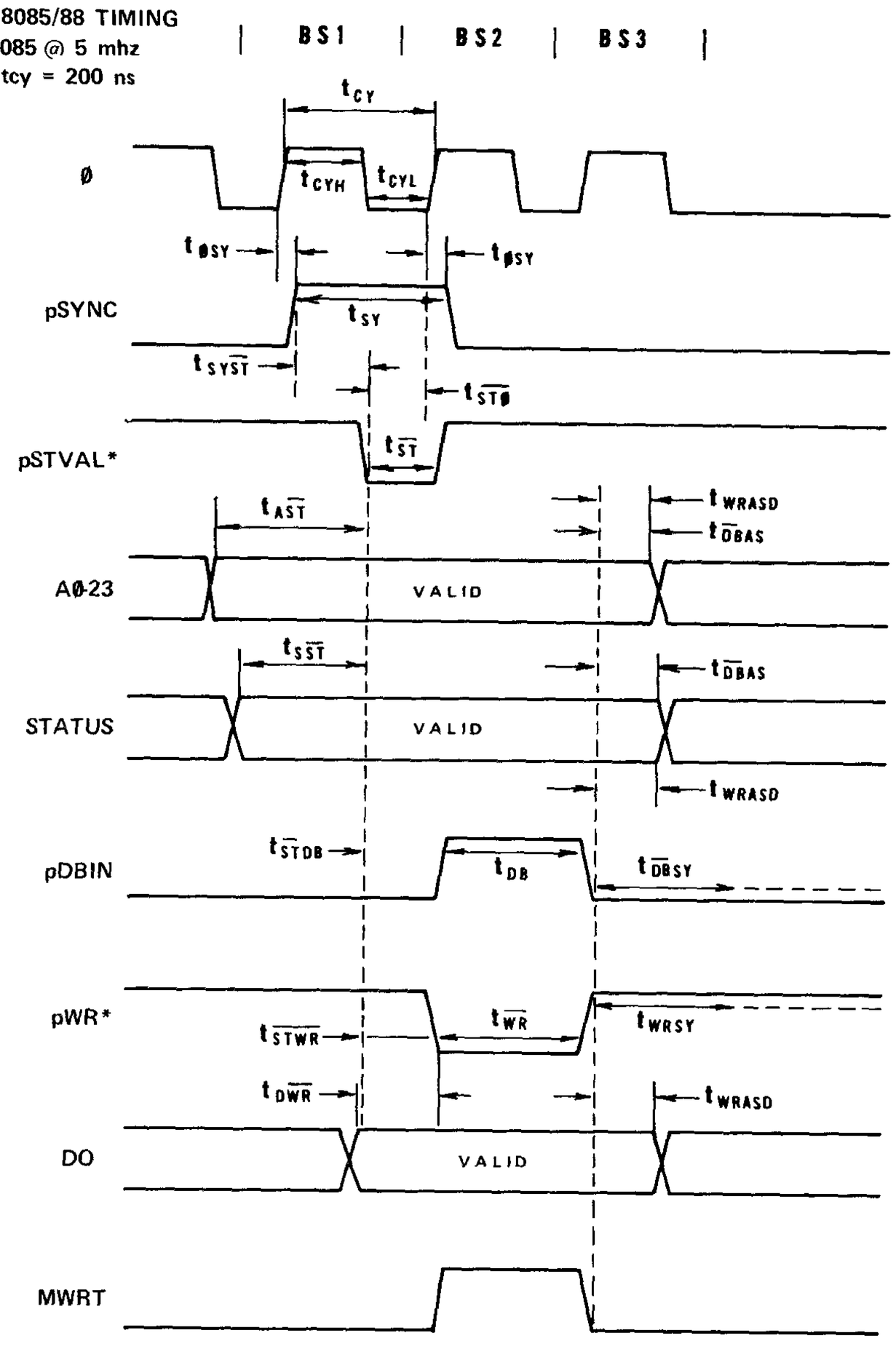


Component Layout

8085 READ/WRITE CYCLE TIMING
BASED ON IEEE S-100 TIMING PARAMETERS
(see timing diagram for meaning of signal mnemonics)

		IN NSECS 8085 2MHZ	8085 5MHZ	IEEE SPEC MIN	IEEE SPEC MAX
tCY	Ø PERIOD	500	200	166	2000
tCYH	Ø PULSE WIDTH HIGH	245	100	0.4tCY	-
tCYL	Ø PULSE WIDTH LOW	225	80	0.4tCY	-
tØSY	DELAY Ø HIGH TO pSYNC HIGH: DELAY Ø HIGH TO pSYNC LOW	18	18	10	-
tSY	pSYNC PULSE WIDTH HIGH	500	200	0.7tCY	-
tSTØ	pSTVAL* LOW PRIOR TO Ø HIGH DURING pSYNC	215	83	0	-
tST	pSTVAL* PULSE WIDTH LOW	225	90	50	-
tSYST	DELAY pSYNC HIGH TO pSTVAL* LOW	240	100	20	-
tAST	ADDRESSES STABLE PRIOR TO pSTVAL* LOW DURING pSYNC HIGH	500	200	70	-
tSST	STATUS STABLE PRIOR TO pSTVAL* LOW DURING pSYNC HIGH	400	160	40	-
tDB	pDBIN PULSE WIDTH HIGH	465	180	0.9tCY	-
tSTDB	DELAY pSTVAL* LOW TO pDBIN HIGH	240	90	20	-
tDBSY	DELAY pDBIN LOW TO pSYNC HIGH	500	200	0	-
tDBAS	HOLD TIME FOR ADDRESSES AND STATUS AFTER pDBIN LOW	240	80	50	-
tACC	DELAY pSTVAL* LOW TO DATA VALID	600	150	minimum	-
tWR	pWR* PULSE WIDTH LOW	500	190	0.9tCY	-
tSTWR	DELAY pSTVAL* LOW TO pWR* LOW	240	98	30	-
tWRSY	DELAY pWR* HIGH TO pSYNC HIGH	480	200	0	-
tDWR	SETUP TIME DO VALID TO pWR* LOW	250	100	0.1tCY	-
tWRASD	HOLD TIME ADDRESSES FROM pWR* HIGH	220	75	0.2tCY	-
tWRASD	HOLD TIME STATUS FROM pWR* HIGH	245	100	0.2tCY	-
tWRASD	HOLD TIME DO FROM pWR* HIGH	225	100	0.2tCY	-
tWRMR	DELAY pWR* LOW TO MWRT HIGH; pWR* HIGH TO MWRT LOW	5	5	-	30

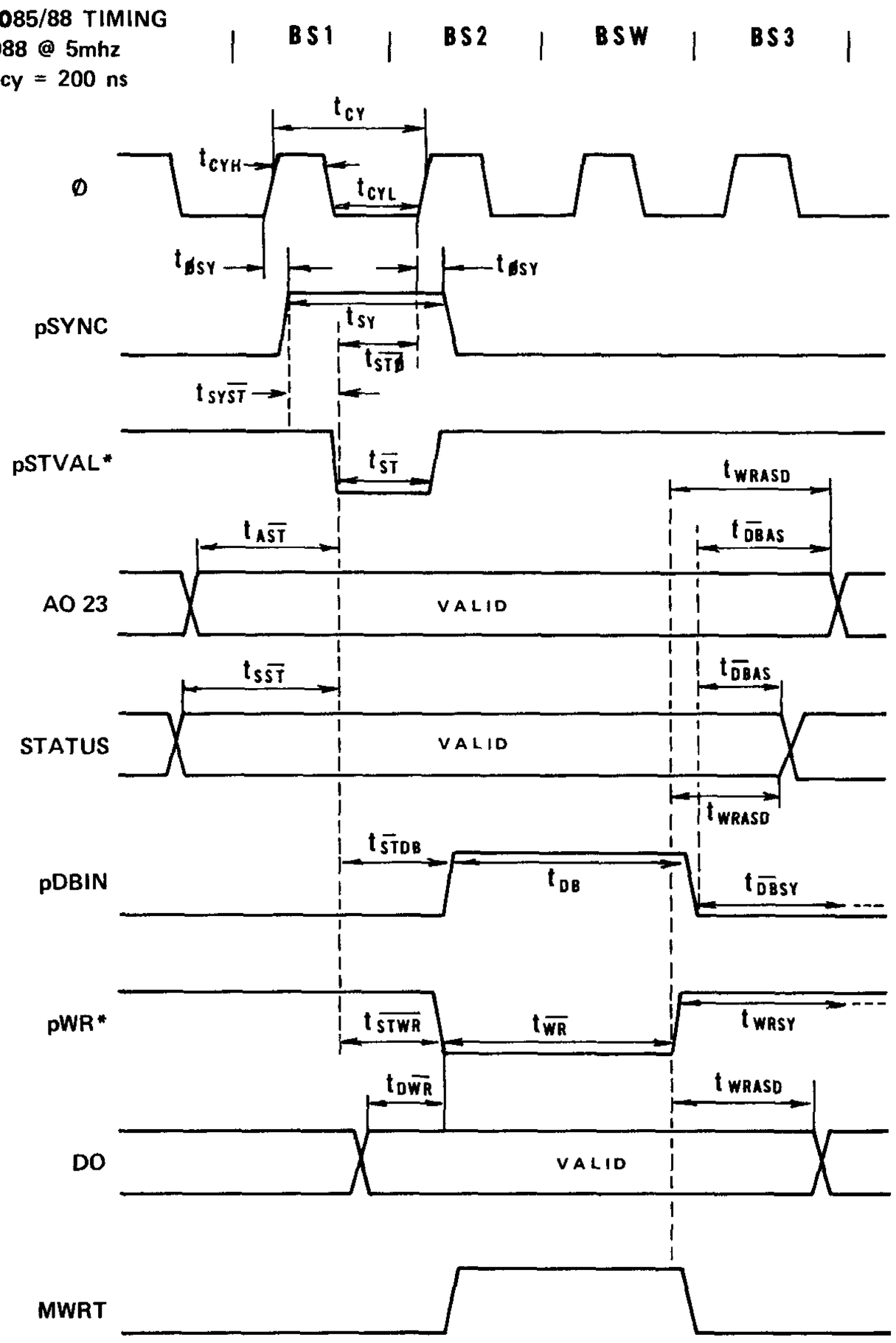
CPU 8085/88 TIMING
8085 @ 5 mhz
tcy = 200 ns

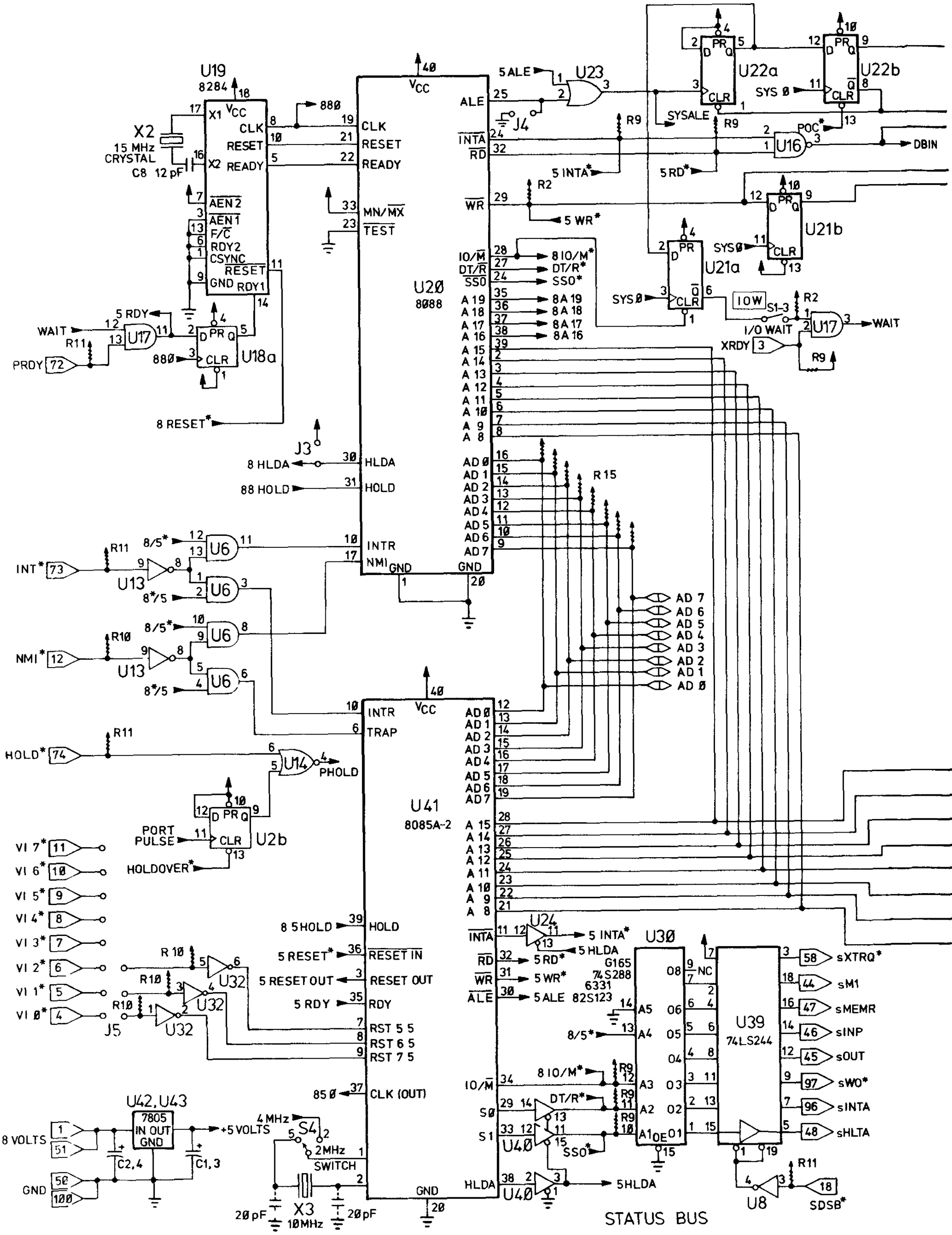


8088 READ/WRITE CYCLE TIMING
BASED ON IEEE S-100 TIMING PARAMETERS
(see timing diagram for meaning of signal mnemonics)

		IN NSECS		
		8088	IEEE SPEC	
		5MHZ	MIN	MAX
tCY	Ø PERIOD	200	166	2000
tCYH	Ø PULSE WIDTH HIGH	65	0.4tcy	-
tCYL	Ø PULSE WIDTH LOW	110	0.4tCY	-
tØSY	DELAY Ø HIGH TO pSYNC HIGH: DELAY Ø HIGH TO pSYNC LOW	20	10	-
tSY	pSYNC PULSE WIDTH HIGH	180	0.7tCY	-
tSTØ	pSTVAL* LOW PRIOR TØ O HIGH DURING pSYNC	120	0	-
tST	pSTVAL* PULSE WIDTH LOW	120	50	-
tSYST	DELAY pSYNC HIGH TO pSTVAL* LOW	50	20	-
tAST	ADDRESSES STABLE PRIOR TO pSTVAL* LOW DURING pSYNC HIGH	180	70	-
tSST	STATUS STABLE PRIOR TO pSTVAL* LOW DURING pSYNC HIGH	200	40	-
tDB	pDBIN PULSE WIDTH HIGH	280	0.9tCY	-
tSTDB	DELAY pSTVAL* LOW TO pDBIN HIGH	150	20	-
tDBSY	DELAY pDBIN LOW TO pSYNC HIGH	280	0	-
tDBAS	HOLD TIME FOR ADDRESSES AND STATUS AFTER pDBIN LOW	180,120	50	-
tACC	DELAY pSTVAL* LOW TO DATA VALID	400	minimum	
tWR	pWR* PULSE WIDTH LOW	260	0.9tCY	-
tSTWR	DELAY pSTVAL* LOW TO pWR* LOW	140	30	-
tWRSY	DELAY pWR* HIGH TO pSYNC HIGH	320	0	-
tDWR	SETUP TIME DO VALID TO pWR* LOW	100	0.1tCY	-
tWRASD	HOLD TIME ADDRESSES FROM pWR* HIGH	180	0.2tCY	-
tWRASD	HOLD TIME STATUS FROM pWR* HIGH	140	0.2tCY	-
tWRASD	HOLD TIME DO FROM pWR* HIGH	180	0.2tCY	-
tWRMR	DELAY pWR* LOW TO MWRT HIGH; pWR* HIGH TO MWRT LOW	10	-	30

CPU 8085/88 TIMING
8088 @ 5mhz
tcy = 200 ns





CPU 8085/88

234 EARLY

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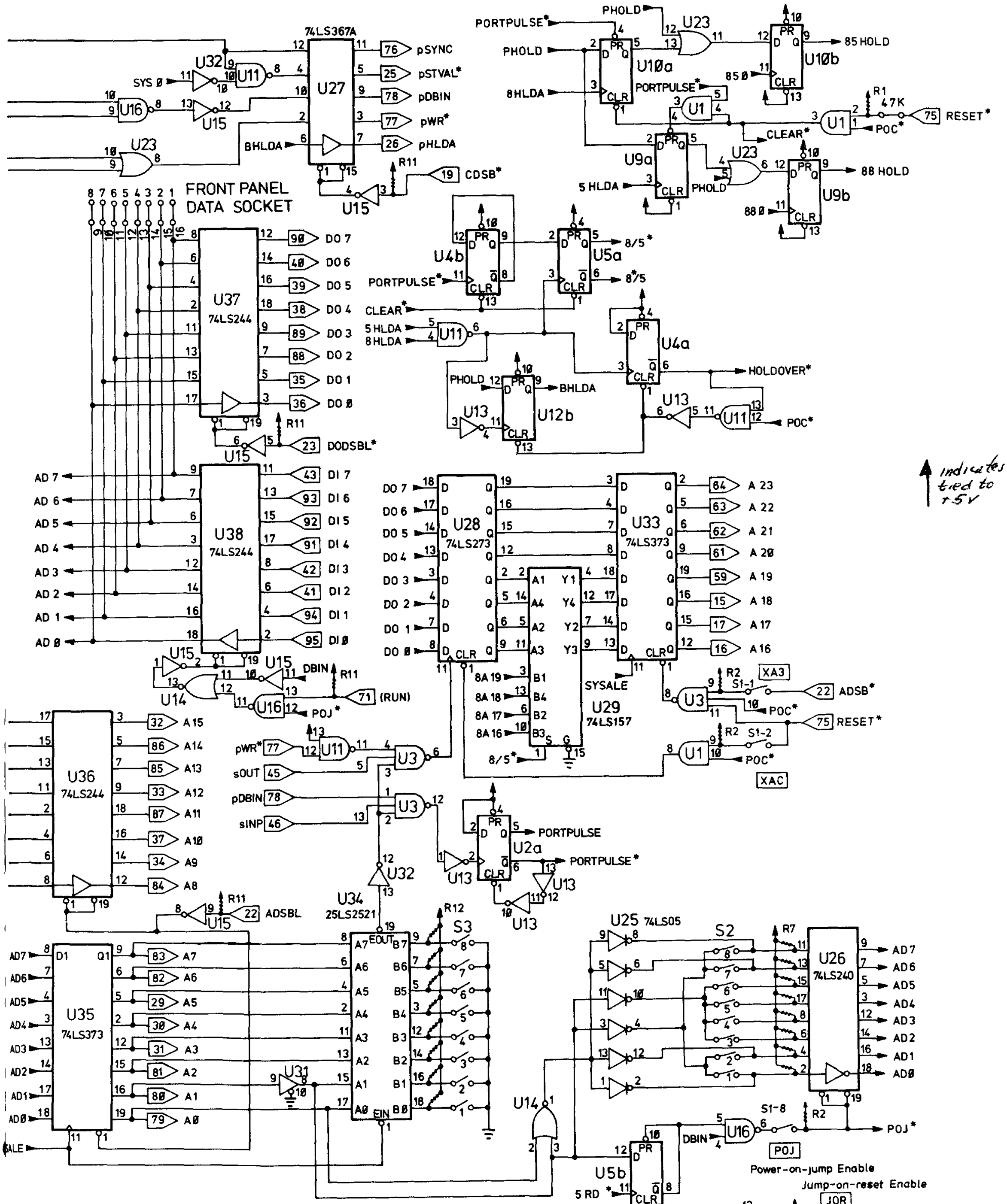

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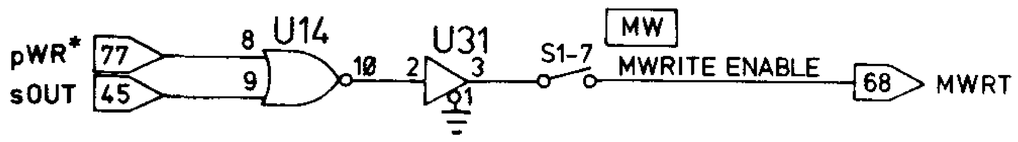
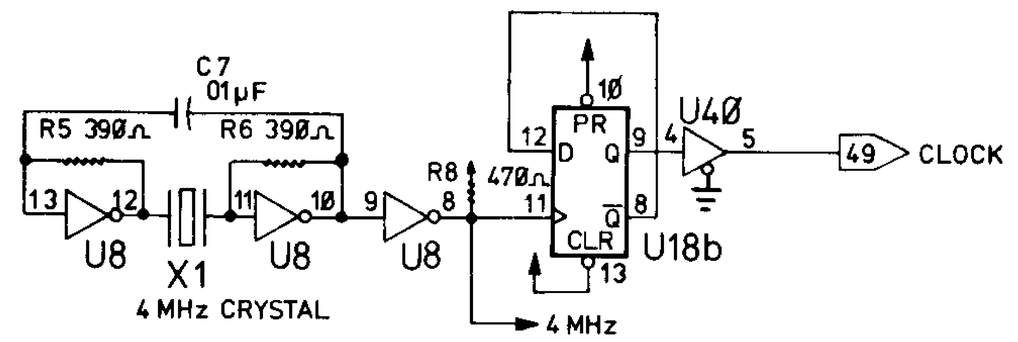
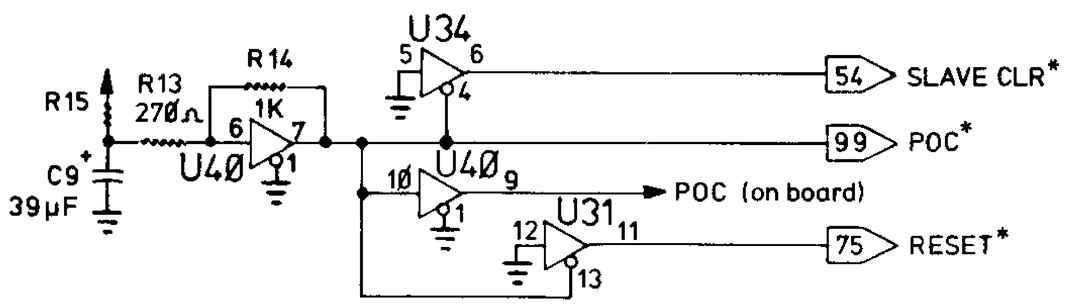
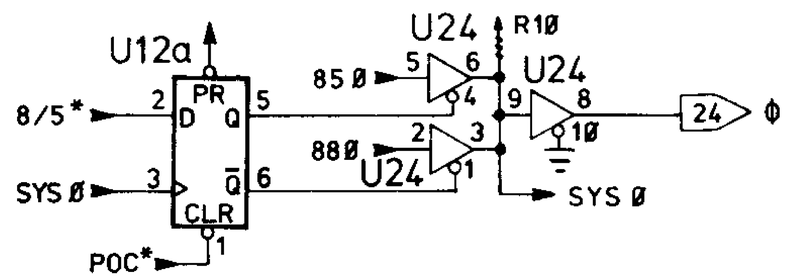
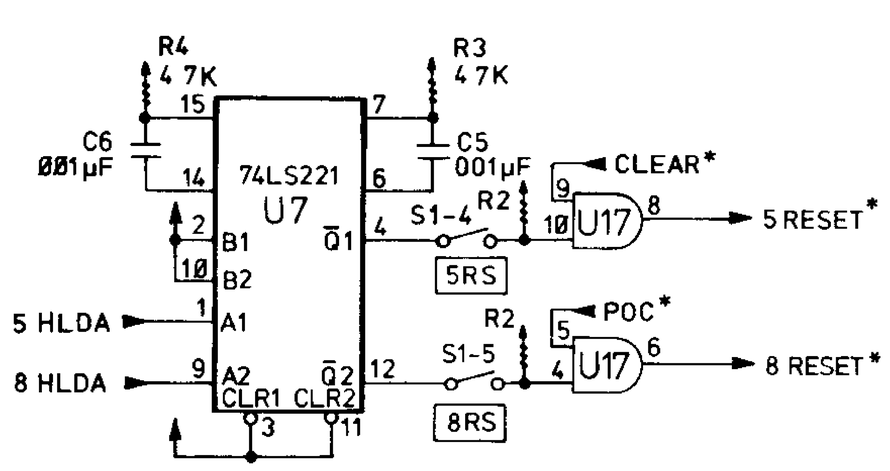
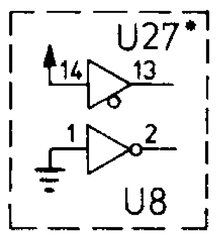












Unused Gates

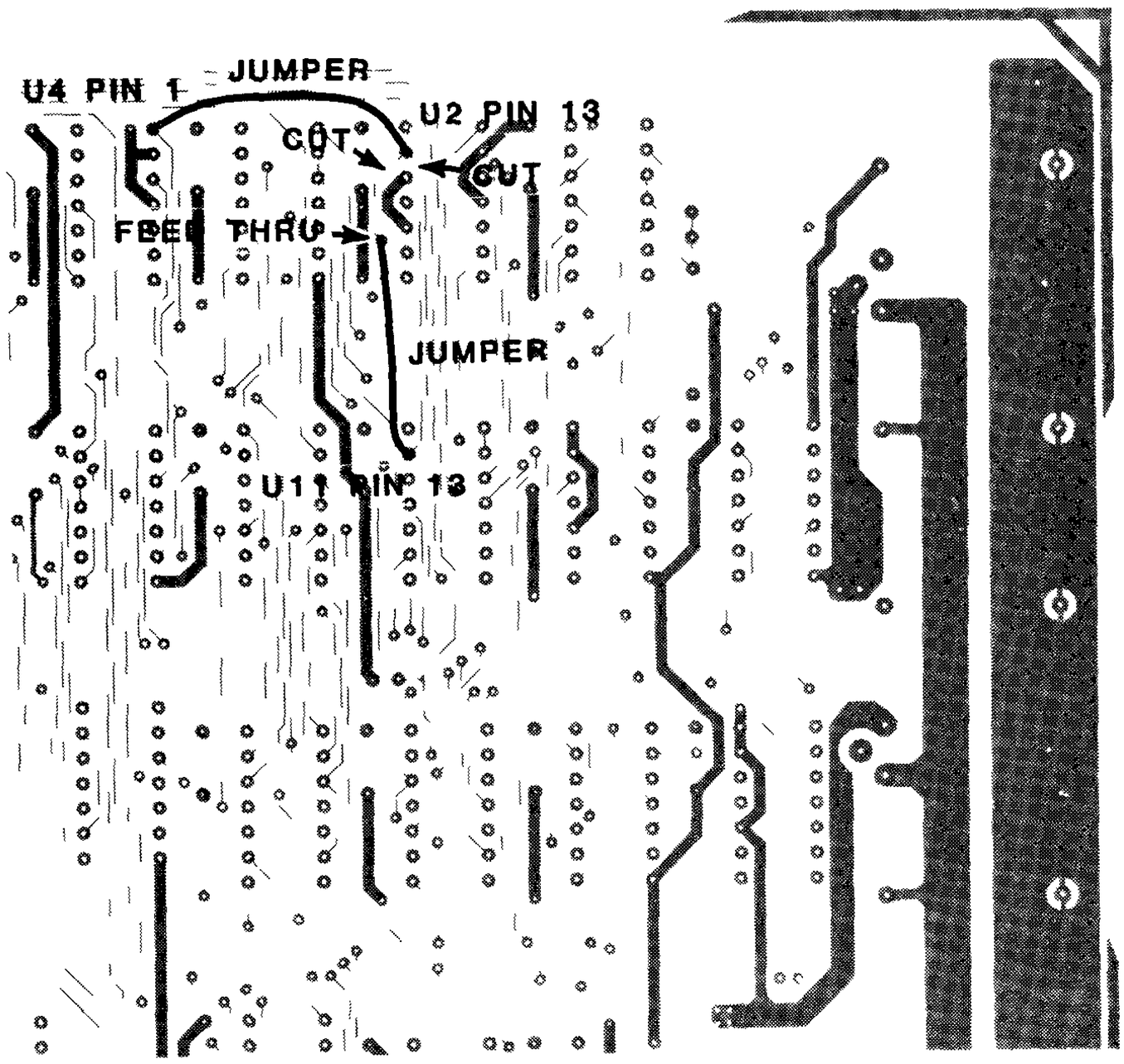
MODS TO CPU 8085/88 FOR DMA OPERATION

If you have a CPU 8085/88 "B" revision (161B) and are using DMA in your system you should make the following mods to your board:

1. Using an Xacto knife, carefully cut the two traces that connect to U2, pin 13, on the solder side (back) of the board. Take care not to damage any other traces on the board.

2. Using wire-wrap or similar insulated wire, connect a jumper from U2, pin 13, to U4 pin 1, on the solder side (back) of the board. Also connect a jumper from the feed-through closest to U2, pin 9, to U11, pin 13. Be careful not to create shorts between any other traces, and be sure to use only high grade rosin core solder.

SEE ILLUSTRATION



ADDED OPTION JUMPERS FOR "D" REVISION CPU 8085/88

We have added two "option jumpers" to the "D" revision of the CPU 8085/88. The first concerns the use of IMSAI type front panels and the second determines how the 8088 responds to a RESET.

JUMPER J6

J6 is located at the lower left hand corner of the circuit board, just below U31.

1. If you are using and IMSAI or similar front panel, you will probably want to install J6.

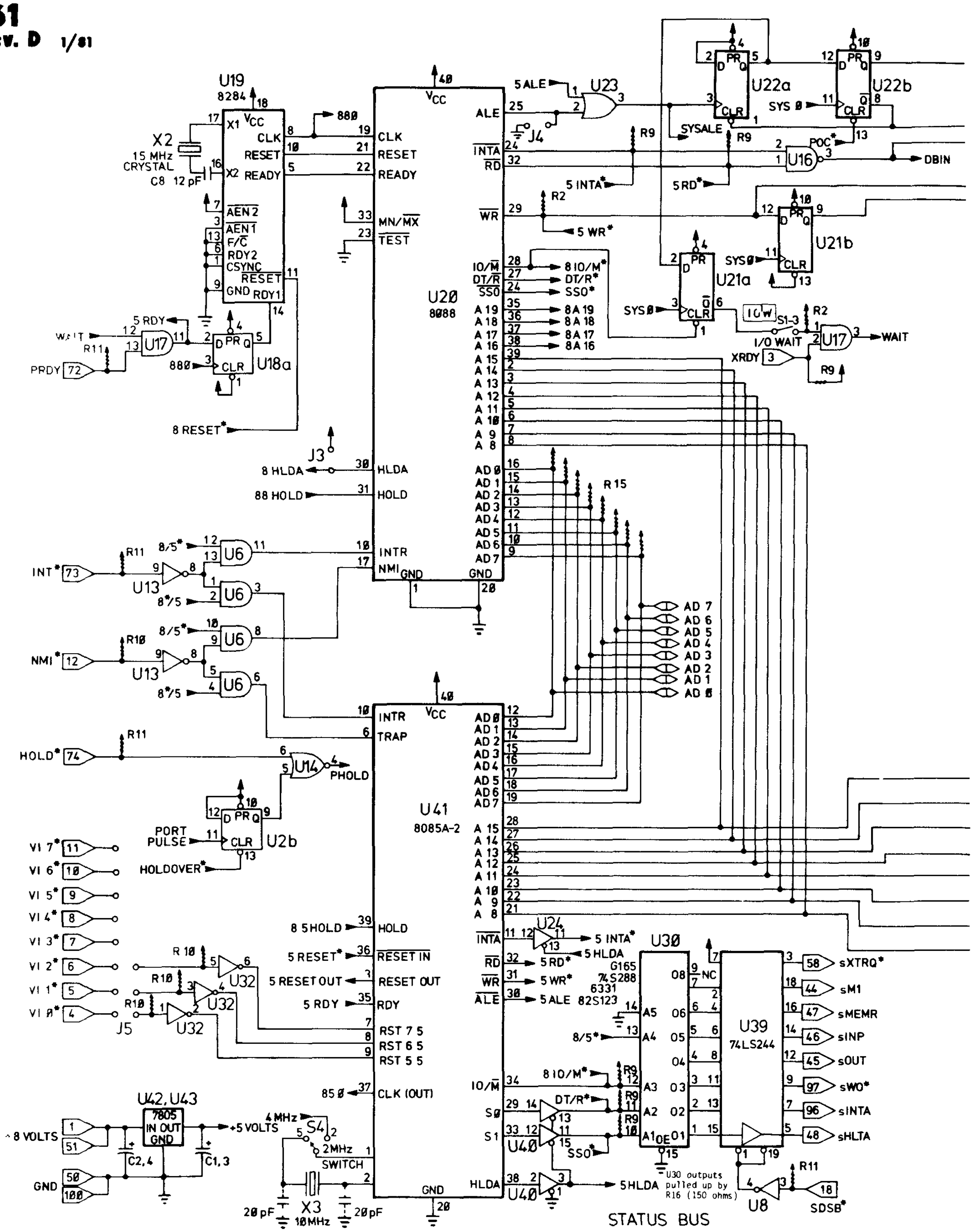
ONE WORD OF CAUTION: In older S-100 systems, Bus pin 53 was used for a signal called SSWDSB (sense switch disable). The new IEEE S-100 standard has redefined pin 53 as GND. If you install J6 (which brings pin 53 into the board) and a new board happens to ground pin 53, your CPU will cease to function (along with your front panel).

JUMPER J7

J7 is located between U16 and U17 and has three pads labeled A, B and C. J7 determines whether the 8088 is reset only at power-on or at both power-on and every time the system is reset (usually by pushing the RESET button).

1. If you want the 8088 to reset only at power-on, then you need do nothing with J7, (we have connected pads C and B for you).

2. If you want the 8088 to always be reset along with the 8085, then you should carefully cut the trace connecting pads C and B. Use an Xacto knife and be careful not to damage any other traces. Then solder in a jumper between pads A and B.



CPU 8085/88

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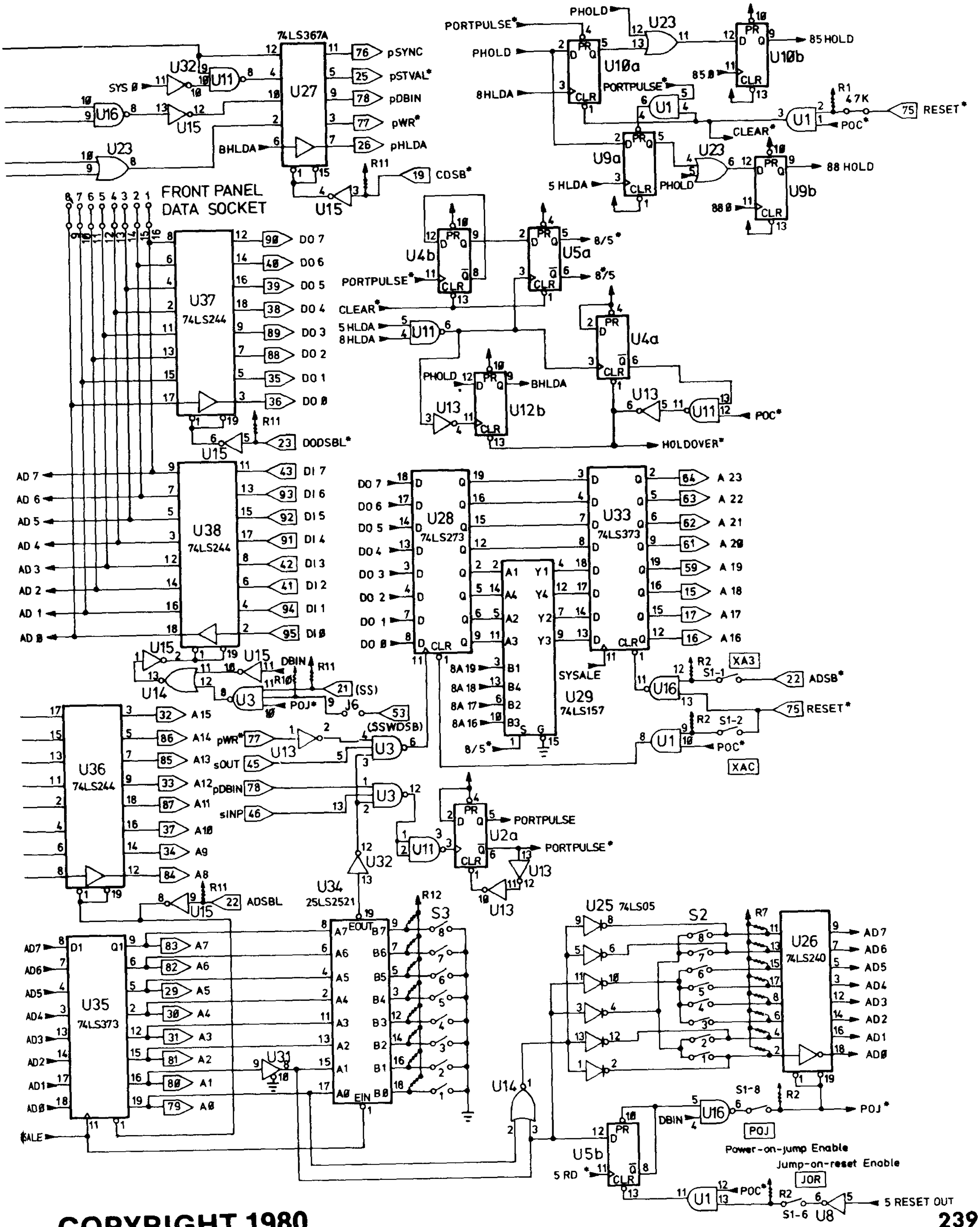

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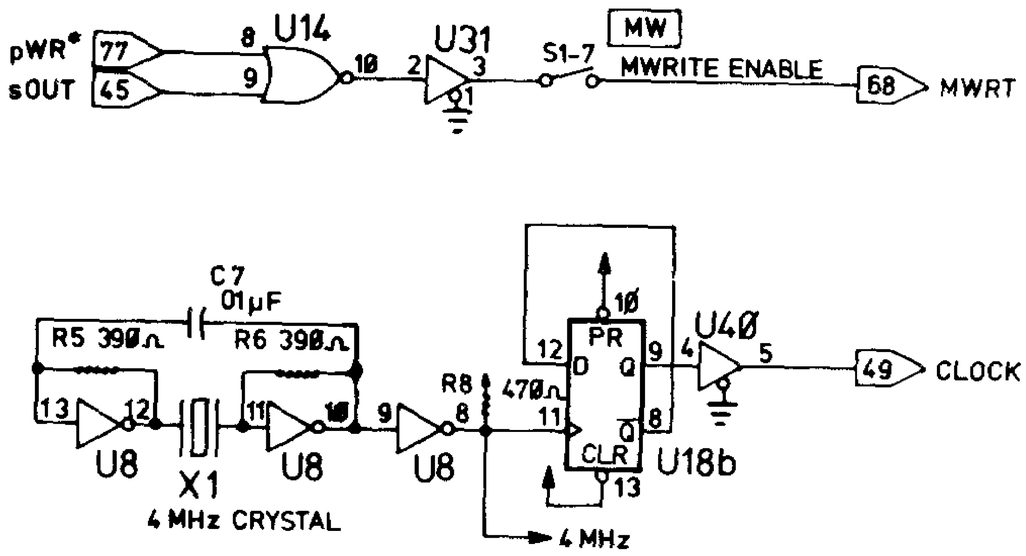
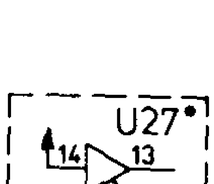
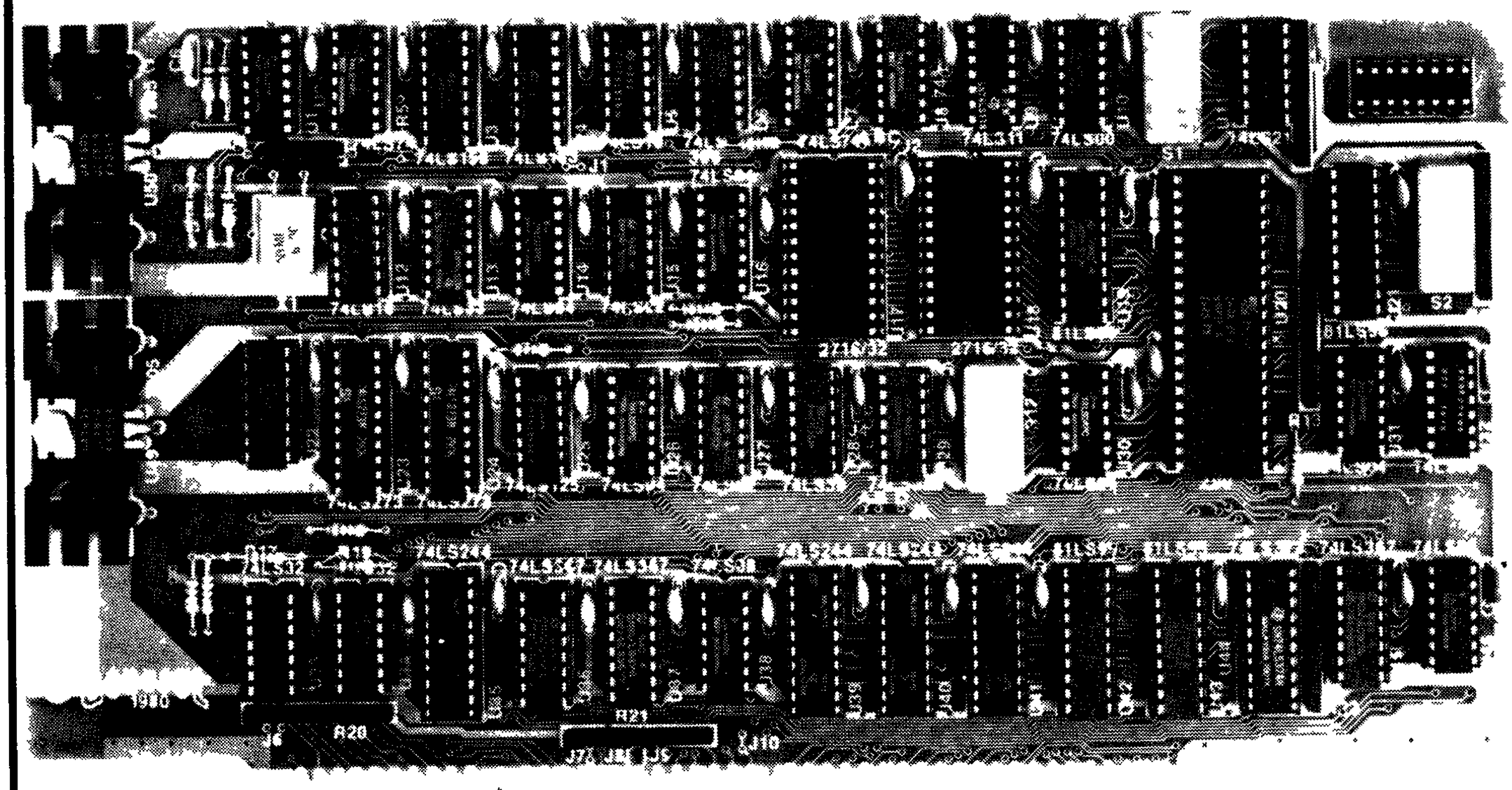




Unused Gates

CPU-Z
USER'S MANUAL



IEEE S-100
4-6 MHz CPU
with onboard RAM/ROM & interrupt control

160 mac

CompuPro™ from GODBOUT

10/80

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ABOUT CPU-Z

Congratulations on your decision to purchase the **CPU Z** board, specifically designed for electrical and mechanical compatibility with the IEEE S-100 bus standard. The S-100 bus is the professional level choice for commercial, industrial, and scientific applications. This bus provides for ready expansion and modification as the state of the computing art improves. We believe this board, along with the rest of the S-100 portion of the **CompuPro** family, is one of the best boards available for that bus.

As amateur radio operators have contributed greatly to communication technology, so too the computer hobbyist has provided the microcomputer industry with many significant developments. In recognition of this fact, we also make this board available in **"UNKIT"** form for those who enjoy the challenge of assembling and testing a fine computer board.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing a **CompuPro CPU Z** board...welcome to the club!

TECHNICAL OVERVIEW

The **CPU Z** was specifically designed to give the user one of the best Z80 CPU boards for the S-100 bus. The board features on-board PROM sockets, a power-on-jump circuit to any 256 byte boundary, a Memory Manager to extend the addressing range of the system from 64K-bytes to a maximum of 16M-bytes of system RAM, fully maskable vectored interrupts to speed up system throughput by eliminating polling loops, and wait state generation circuitry for all machine cycles.

Other features standard to all CompuPro boards include thorough bypassing of all supply lines to suppress transients, on board regulators, and low power Schottky TTL and MOS technology integrated circuits for reliable, cool operation. All this and sockets for all IC's go into a double sided, solder masked printed circuit board with a complete component legend.

USING THE VECTORED INTERRUPTS

The CPU chip recognizes 8 instructions as Restart0 - Restart7. These instructions will cause the program counter to jump to one of eight locations depending on the Restart instruction.

RESTART	Program Counter(HEX)
0	0
1	8
2	10
3	18
4	20
5	28
6	30
7	38

At these locations, jumps to interrupt driver routines can be placed into either RAM or PROM. Then when one of the VI0 - VI7 lines goes low, the specific routine can instantly be started to service the interrupting device. Upon Power-on-Clear or reset (RESET*) the interrupt mask is cleared, enabling all eight interrupt lines (NOTE: This does NOT mean that the Z80 has interrupts enabled.). Then (with the VI switch (SW3-8) turned ON) when any of the VI inputs goes low the Restart will be generated if the CPU has previously received an Enable Interrupts (FB(H)) command. To disable an individual interrupt line, or a group of lines, the mask must be set up by an output to Port FE(H) with the desired mask in the Accumulator. A "1" in the mask will disable the interrupt line, and a "0" will enable the interrupt line.

If it is desired to use this **CPU Z** board with the Z80 mode 2 interrupts, the on-board vector generation circuitry must be disabled. To do this switch SW3-8 should be turned OFF, and all 1's should be output to the interrupt mask port (Port FE(H)). This will prevent the **CPU Z** from responding to the V.I. lines, but it will still respond to the bus interrupt signal (bus pin 73).

EXAMPLE	(HEX)	(BINARY)
to disable VI5-VI7	07	(00000111)
to disable VI2	20	(00100000)
to disable all	FF	(11111111)

Note that the VI lines are all open collector and more than one device can be connected to each VI line by using open collector gates.

It is recommended to put a "DEAD MEMORY" error recovery routine at location 38 (H), since this location will be jumped to in case the CPU encounters an FF (H) instruction, which corresponds to a restart 7. This is the instruction that will be read from a memory location for which there is no system memory. Location 38 is the most common launching pad for CPU flights into never-never land.

USING THE NONMASKABLE INTERRUPT

The S-100 BUS has a NMI* pin (bus pin 12) which is implemented on the CPU card for any function that the user desires. NMI* is primarily used for a catastrophic system failure, such as loss of primary power. This interrupt enables the processor to execute a short program to save current system parameters on either a disc or some other nonvolatile memory before total power is lost (which usually takes milliseconds, lots of time for a computer). The NMI* causes the CPU to jump to address 66(H), which should be initialized with a routine to control the interrupt.

EXTENDED ADDRESSING

Address lines A16-A23 are driven through output port FD(H) and can be changed with a simple output instruction. Upon Power-on-Clear or reset (RESET*) the extended address lines will be reset to 0, bringing the system up in base page. To access memory in other than base page requires an output to Port FD(H) with the desired page address in the Accumulator in order to set the extended address lines A16-A23. These address lines are pin numbers 16, 17,15, 59, 61, 62, 63, & 64, for address lines A16-A23 respectively.

Example shown below:

ACCUMULATOR DATA		TO ACCESS PAGE
(HEX)	(BINARY)	(HEX)
40	01000000	40
2	00000010	2
F0	11110000	F0

Of course, to take advantage of this extended addressing feature requires memory boards which respond to extended address lines. If a board does not monitor the S-100 extended address lines, then only the normal 16 address lines will be decoded.

WAIT STATES

A single wait state may be added to any processor cycle by closing the corresponding dip switch on SW1. A wait may be added to:

CYCLE	SWITCH POSITION
PROM	1
I/O	2
MEMORY	3
INSTRUCTION	4

Due to critical timing requirements of the Z80 during an instruction fetch (M1), extra time may be required for marginally slow memory chips. When running at 4 MHZ some RAM chips may also need more time for each memory operation than is normally allowed. The on board PROM sockets may be used for many different speed PROM's, and when running at 4 MHZ a wait state may be needed for a fetch there also. The I/O wait should rarely be needed because of the fact that few I/O boards run slow and the Z80 automatically generates one I/O wait state, but the provision is made to the user.

ON-BOARD-MEMORY SOCKETS

The MEMORY sockets on this board are set up to take INTEL 2716, T.I. 2516 2Kx8 EPROMS, or any of the new 2Kx8 RAM chips which are pin compatible (Hitachi HM6116 or equivalent). By cutting J2(A-B) on the solder side above U17, J4 on the solder side to the left of U29, an J5(A-C) on the solder side beside U29 and installing jumpers J2(A-C) and J5(A-B) the sockets can now be used for 2732 4Kx8 EPROMS. (NOTE: Extreme care must be used when soldering in the jumpers so as not to damage the board or any of the traces. A soldering iron of no more than 25 watts should be used.) With 2732's SW3-4 is no longer used to address the sockets. The on-board sockets will be totally disabled when switch SW3-5 is ON. With SW3-6 ON, the sockets are addressable anywhere in base page (A16-A23 are all 0) on a 4K boundry (8K for the 2732's). This feature allows the user to have MEMORY in base page only. With SW3-6 OFF, the sockets ignores address lines A16 - A23 and occupies every page of memory. A prime example of how to use the sockets in this "shadow" mode would be to use them with SW3-6 turned ON and the Power-on-jump set to the start of the PROM address, then when the system is initially turned on the program in the PROM will start and either initialize the system by booting in a disk program, or some other type of routine. Then the last thing the PROM will do is jump to the RAM address where the initialization routine was loaded. The first thing that program will do is an output to port FD(H) of anything except 0. This will set the extended page address to the page that was in the Accumulator, and the sockets will be disabled. RAM which was overlapped with the PROM can now be used and a complete memory map is available to the user. SW3 positions 1-4 are used for address lines A15-A12. The socket closest to the Z80 chip is the low address half PROM and the right socket the high half.

Example:

SWITCH S3				DESIRED START ADDRESS (HEX)	
1	2	3	4	2716	2732
0	0	0	0	0000-0FFF	0000-1FFF
0	0	0	1	1000-1FFF	
0	0	1	0	2000-2FFF	2000-3FFF
0	0	1	1	3000-3FFF	
:	:	:	.	: :	:
:	:	:	.	. :	. :
1	0	1	0	A000-AFFF	A000-BFFF
:	:	.	.	:	
1	1	1	1	F000-FFFF	

ON = "0" OFF = "1"

To disable ROM completely, turn ON SW3-5

CLOCK

The clock for this system can be set to allow the CPU to run at either 2MHZ or 4MHZ. SW1-5 is used to select between these two speeds. When SW1-5 is ON the CPU will run at 2MHZ and bus pin 24 (ϕ) will have a 2MHZ square wave on it. When SW1-5 is OFF, the system will run at 4MHZ and bus pin 24 will have a 4MHZ square wave on it. With a 24MHZ crystal used for X1 the speed switch SW1-5 will select between processor speeds of 6MHZ (when ON) and 3MHZ (when OFF). Bus pin 49 (CLK) will always have a 2MHZ signal on it.

POWER-ON-JUMP/JUMP-ON-RESET

Provisions have been made on this board to allow the processor to jump to any memory location on a 256 byte boundary on either a power-on only, or every reset also. To enable this feature, JMP ENABLE (SW1-8) should be turned ON and the jump address should be set on switch S2 according to the table below. To enable the jump on every reset also, SW3-7 should also be turned ON.

SWITCH POSITION		FUNCTION	
1	..... "	A15	
2	..... "	A14	
3	..... "	A13	
4	..... "	A12	ON = "1"
5	..... "	A11	OFF = "0"
6	..... "	A10	
7	..... "	A9	
8	..... "	A8	

EXAMPLE: To jump to E900 for a North Star floppy disc system, S2 positions 1-3,5, and 8 should be ON and S2 positions 4,6,and 7 should be OFF. JMP ENABLE (SW1-8) should be ON to enable this feature.

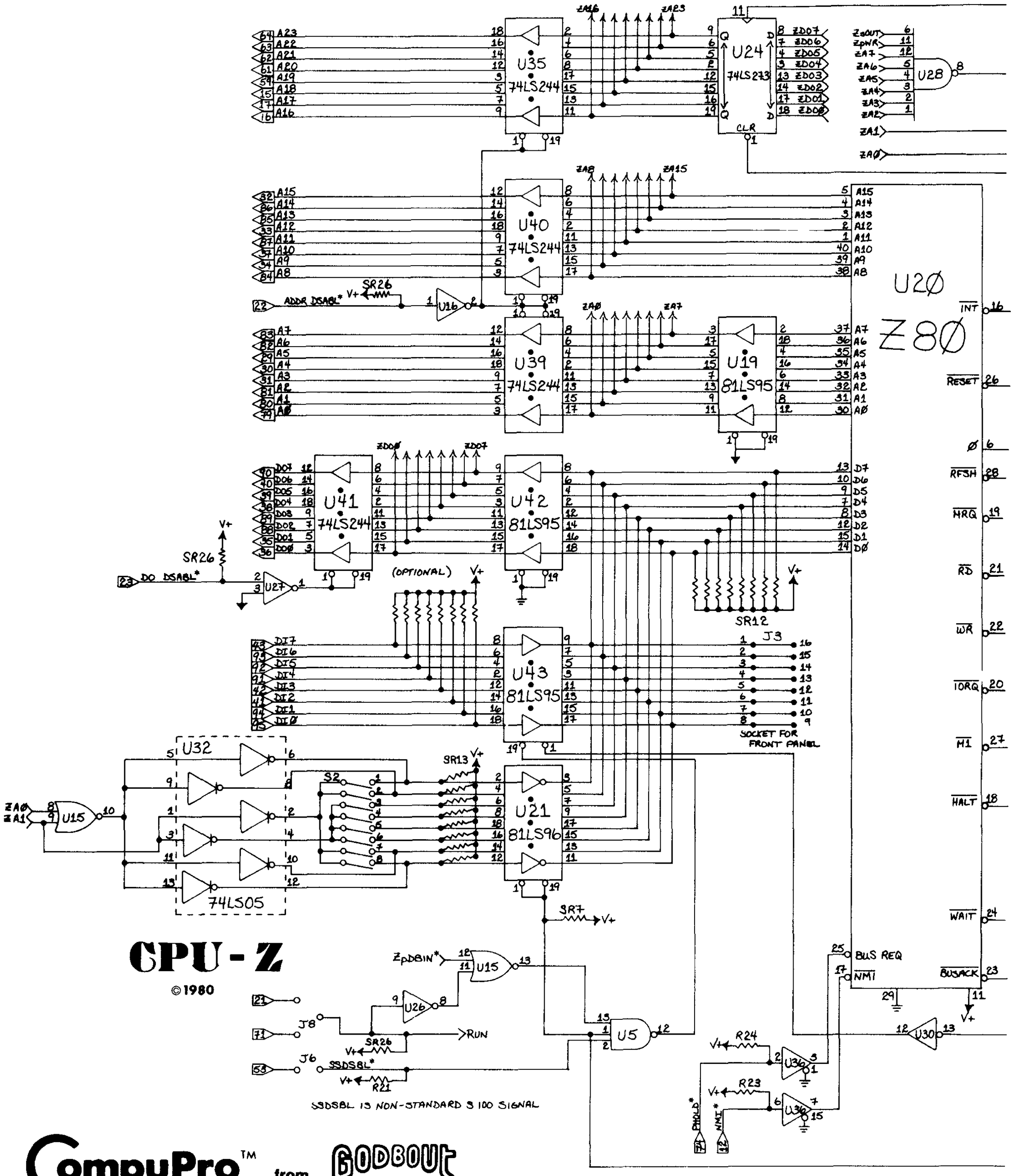
NOTE: Since the jump circuitry disables the input buffer, it is unnecessary to use the phantom line (S-100 pin 67) for proper operation.

MWRITE GENERATION

The **CPU Z** has circuitry on board for generating the MWRITE signal (bus pin 68) and a positive going strobe will be generated for each memory write operation. This circuitry looks at the bus and whenever the sOUT signal is low, and the pWR* signal strobes low, a MWRITE strobe will be generated. This signal must be generated at only one source in each system. If there is a front panel in your system it also may be generating the MWRITE signal, and the signal from the **CPU Z** must be disabled. There are two ways to disable this signal: A) Cut jumper J7 on the solder side below U36 and R26; or B) Remove pin 9 of U36 from its socket and let the pin hang out, this makes it easier to reconnect the pin should you ever want MWRITE to be generated from the **CPU Z** board in the future. If MWRITE is generated in more than one place, memory boards that rely on MWRITE as their write strobe may not work properly.

IMSAI FRONT PANEL USAGE

Although we will soon be manufacturing a front panel that will be fully compatible with the IEEE standard, if you have an IMSAI type front panel this CPU will require minor modifications to work properly. The problems arise from the fact that the IMSAI front panel (which does not conform to the IEEE standard) requires some signals that are not on the S-100 bus. Jumper pads are provided to allow these lines to be used. J6, and J8 should be installed to connect bus pins 53, and 71 respectively to control the CPU from the front panel. When the system is set to run at 4MHZ, the front panel will force the CPU to run at 2MHZ when the RUN/STOP signal is in the STOP mode. This will allow for proper front panel operation which is speed dependent. Socket J3 in the upper right corner is for the front panel connector. The CPU MWRITE circuitry will also have to be disabled if the front panel is going to generate MWRITE (bus pin 68). Jumper J9 can be installed to have the CPU drive bus pin 27 (which was the WAIT line), but this is not necessary for proper system operation.



SSDSBL IS NON-STANDARD S 100 SIGNAL

CPU-Z

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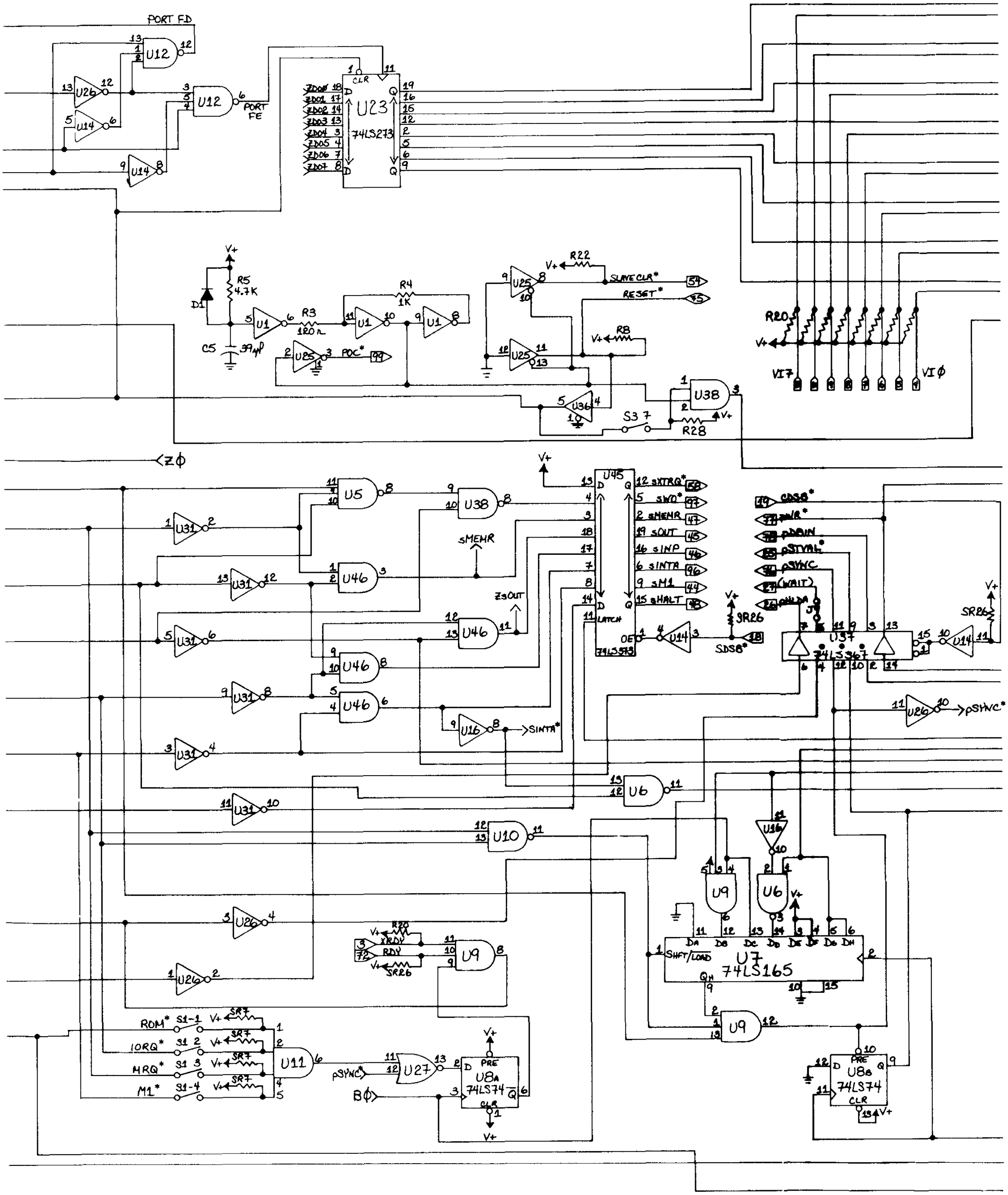
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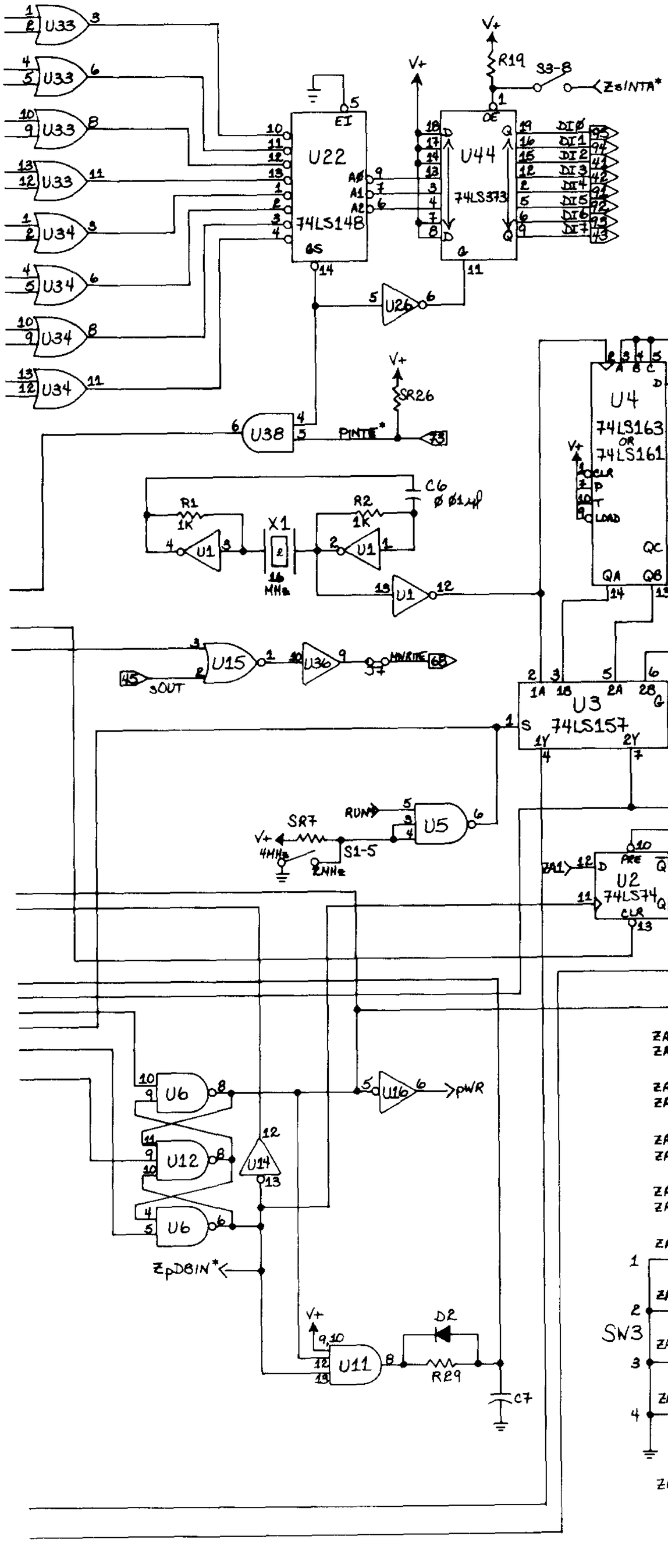
U12
U26
U14
U12
PORT FE
CLR
U23
74LS273
ZD00
ZD01
ZD02
ZD03
ZD04
ZD05
ZD06
ZD07
D
Q
V+
R5
4.7K
D1
U1
R3
120 Ω
R4
1K
C5
39μF
U25
POC*
99
R22
SLAVE CLR*
54
RESET*
55
R8
R20
VI7
VIØ
U38
S3 7
R28
ZØ
U5
U31
U46
sMEMR
ZsOUT
U45
12 sXTRQ*
5 sWO*
2 sMEMR
19 sOUT
16 sINP
6 sINTA
9 sM1
15 sHALT
LATCH
OE
U14
SDS0*
SR26
CDS0*
pWR*
pDBIN
pSTVAL*
pSYNC
(WAIT)
pWAIT
U37
74LS367
U26
pSYNC*
SINTA*
U16
U6
U10
U9
R20
XRDY
RDY
SR26
U7
74LS165
SHIFT/LOAD
U11
ROM*
IORQ*
MRQ*
M1*
S1-1
S1 2
S1 3
S1-4
SR7
U27
BØ
U8A
74LS74
PRE
CLR
U8B


U33
U34
U22
74LS148
EI
GS
U44
74LS373
R19
S3-8
Z≤INTA*
U26
U38
PINTE*
SR26
U4
74LS163
OR
74LS161
CLR
P
T
LOAD
R1
1K
R2
1K
C6
Ø.01μf
X1
16 MHz
U1
U15
SOUT
MWRITE
U3
74LS157
U36
2/4 MHz
SR7
RUN
S1-5
4MHz
2MHz
U5
U2
74LS74
PRE
CLR
S1-8
POJ
ENABL
ZA1
U27
R15
X2
4MHz
R14
C8
0.01μf
C9
R10
R6
Q1
R11
R18
BØ
ZØ
U6
U12
U14
U16
pWR
ZpDBIN*
U11
D2
R29
C7
U13
ZA23
ZA22
ZA21
ZA20
ZA19
ZA18
ZA17
ZA16
ZA15
ZA14
ZA13
ZA12
ZA11
U29
R17
R16
R9
R27
SW3
S3-6
S3-5
J4
J5
U10
CEB*
CEA*
Jumpers J2, J4 & J5 are to use 2732's
J2
U18
2716
U17
2716
sMEMR
+8
GND
C4
C3
C2
C1
U47
7805
U48
7805
IN
OUT
GND
C1-C4 = 99μf
Ø Ø1μf

VECTORED INTERRUPTS AND MASK

Upon reset (RESET*) U23 is cleared, and will output all lows to the Or-gates (U33 & U34). The VI0 - VI7 inputs normally sit at a high level, and hence all inputs on U22 are high. This resting state makes the GS output high. Upon receiving a vectored interrupt when one of the VI0 - VI7 inputs goes low, U22 will output a value corresponding to the highest priority interrupt on the lines. This value will go to U44 and when the CPU acknowledges the interrupt, the proper Restart command will go to the CPU. When a 1 has been written into the mask port FE(H), U23 will output a high to the associated Or-gate (U33 & U34). Then when an interrupt pulls the input low, U22 will still have a high input and will never detect interrupts that are being masked out.

EXTENDED ADDRESSING

When an OUT FD(H) instruction is executed, the data bits in the Accumulator are latched into U24 and output on bus lines A16-A23. These address lines will be tri-stated along with the other 16 address lines when ADDR-DSABL (Bus pin 22) is driven low by an external device requesting control of the bus.

CPU STATUS LINES

The S-100 bus has eight status signals that all bus masters must provide, these signals come from U45. During either a read cycle or a write cycle these status signals are latched on the bus. A short time after the read or write signal goes away the status signals are allowed to toggle. The S-100 status signals are shown below, along with their associated bus pins. (A * suffix means active low signal.)

SIGNAL	BUS PIN
sWO*	97
sMEMR	47
sINTA	96
sM1	44
sINP	46
sOUT	45
sHLTA	48
sXTRQ*	58

These status bits are decoded from the seven control signals coming from the Z80 as shown below:

STATUS SIGNALS

CONTROL SIGNAL	sWO* (a) or (b)	sMEMR	sINTA	sM1	sINP	sOUT	sHLTA
RFSH*	1 X	X	X	X	X	X	X
MRQ*	0 X	0	X	X	X	X	X
RD*	1 X	0	X	X	0	X	X
WR*	X 0	X	X	X	X	0	X
IORQ*	X X	X	0	X	0	0	X
M1*	X X	X	0	0	X	X	X
HALT*	X X	X	X	X	X	X	0

(A* suffix means active low signal)
An X means a don't care condition.
The SXTRQ* signal is permanently high since this is an 8 bit processor.

SYSTEM CLOCK

The system clock circuitry consists mainly of U1, U3, and U4. The 16 MHZ square wave is fed into U4 which divides it down to the desired system clock speed. The multiplexer U3 will feed either 16 MHZ or 8 MHZ to the pSYNC and pSTVAL* generation circuitry and 2MHZ or 4MHZ to the Z80 and bus for the system clock. The Z80 clock has inverters from U30 along with some discrete devices for providing the required clock rise and fall time. If jumper J8 is used, then when the RUN LINE (bus pin 71) is low the input to U5 will be low and cause the system to run at 2 MHZ. This is the same circuitry that switch SW1-5 uses to determine the system speed. The 2MHZ clock for bus pin 49 is generated with crystal X2, inverters in U27, and a flip-flop in U2 which is then fed through a buffer to bus pin 49.

POWER-ON-JUMP(POJ)/JUMP-ON-RESET(JOR)

The jump circuitry consists of octal inverter U21 (81LS96), DIP switch SW2, SIP resistor R23, hex o.c. inverter U32 (74LS05), a "D" flip flop U2, the POJ enable switch SW1-8, and JOR enable switch SW3-7. With the POJ enable switch ON, upon receiving a power-on-clear, the "D" flip flop is cleared which disables input buffer U43, and enables jump buffer U21. This action starts a three byte sequence which will cause the CPU to jump to the proper starting location. The CPU is reset to address 0, and from the jump buffer a jump (C3H) instruction is put on the data bus. At address 1 the low order address of zero is then put on the data bus, then at address 2 the high order address coming from the jump switch setting is placed on the data bus. When address 2 is in the address buffer the "D" flip flop will then be clocked to the set state and disable the jump buffer while enabling the data input buffer. The "D" flip flop will not get cleared again until the next POC. This complete sequence also occurs for every RESET*, if switch SW3-7 is turned ON. This option will allow the CPU to come up with a known jump on power-on and then later when a reset is recognized the CPU can either start again at 0(H) or jump to the address in switch SW2.

WAIT STATES

The CPU wait line (Z80 pin 24) is driven by three main sources, causing the processor to give more time for certain devices or system states. The three sources are; a) The RDY (pin 72) bus signal, which will be driven by an external device which must have more time to respond to the CPU, b) The XRDY (pin 3) bus signal which is driven by the front panel (if the system has one), and c) On board selector to generate a wait state for four different states. The on-board wait state will come from the settings of SW1 positions 1-4. M1 (SW1-4) will generate a wait state for every instruction cycle. The MRQ (SW1-3) will generate a wait state for every memory fetch cycle. The IORQ (SW1-2) will generate a wait state during every I/O operation. Finally, the ROM switch (SW1-1) will generate a wait state for every access of the on-board MEMORY. U8 will remain in the clear mode with Q* high unless one of these switches (SW1 positions 1-4) is turned ON. Then when one of the selected inputs go low, U8 will be set and cause the wait input (on the CPU) to go low. These wait states can only start when pSYNC is high. When pSYNC goes low U8 will be clocked low with the next negative edge of the system clock.

SWITCH SUMMARY

S1 POSITION	FUNCTION
1	WAIT STATE FOR ROM
2	WAIT STATE FOR I/O
3	WAIT STATE FOR MEMORY FETCH
4	WAIT STATE FOR INSTRUCTION FETCH
5	SPEED SWITCH (OFF = 4 MHZ.)
6	NOT USED
7	NOT USED
8	POWER-ON-JUMP ENABLE

S2 POSITION	FUNCTION	
1	JUMP ADDRESS BIT A15	
2	JUMP ADDRESS BIT A14	
3	JUMP ADDRESS BIT A13	ON = "1"
4	JUMP ADDRESS BIT A12	OFF = "0"
5	JUMP ADDRESS BIT A11	
6	JUMP ADDRESS BIT A10	
7	JUMP ADDRESS BIT A9	
8	JUMP ADDRESS BIT A8	

S3 POSITION	FUNCTION	
1	SOCKET ADDRESS BIT A15	
2	SOCKET ADDRESS BIT A14	ON = "0"
3	SOCKET ADDRESS BIT A13	OFF = "1"
4	SOCKET ADDRESS BIT A12	
5	SOCKET DISABLE (WHEN ON)	
6	SOCKET BASE PAGE ONLY (WHEN ON)	
7	JUMP-ON-RESET ENABLE	
8	INTERRUPT ENABLE FOR VECTORED INTERRUPTS	

JUMPER SUMMARY

J2 - Used with J4, J5, to convert memory sockets for 2732 use

J3 - Front panel data socket

J4 - See J2

J5 - See J2

J6 - SSDSBL for IMSAI type systems

J7 - MWRITE brought to Bus pin 68

J8 - Run or single step for IMSAI type systems

J9 - WAIT brought to Bus pin 27

Parts List

(1) **CPU Z** circuit board

INTERGRATED CIRCUITS (NOTE: the following parts may have letters, suffixes and prefixes along with the key numbers given below.)

(2)	74LS00	quad 2 input NAND	(U6, U10)
(2)	74LS02	quad 2 input NOR	(U15, U27)
(6)	74LS04	hex inverter	(U1, U14, U16, U26, U30, U31)
(1)	74LS05	hex inverter o.c.	(U32)
(2)	74LS08	quad 2 input AND	(U38, U46)
(2)	74LS10	triple 3 input NAND	(U5, U12)
(1)	74LS11	triple 3 input AND	(U9)
(1)	74LS21	dual 4 input AND	(U11)
(1)	74LS30	8 input NAND	(U28)
(2)	74LS32	quad 2 input OR	(U33, U34)
(1)	74LS33	quad 2 input NOR o.c.	(U13)
(2)	74LS74	dual "D" flip flop	(U2, U8)
(1)	74LS125	quad buffers	(U25)
(1)	74LS148	octal encoder	(U22)
(1)	74LS158	quad 2-to-1 mux.	(U3)
(1)	74LS161/3	4 bit counter	(U4)
(1)	74LS165	8 bit shift register	(U7)
(4)	74LS244	octal bus driver	(U35, U39-41)
(1)	74LS266	quad 2 input XNOR	(U29)
(2)	74LS273	octal latches	(U23, U24)
(2)	74LS367	hex bus driver	(U36, U37)
(2)	74LS373	octal latches	(U44, U45)
(3)	81LS95	octal bus driver	(U19, U42, U43)
(1)	81LS96/98	octal bus inverter	(U21)
(1)	Z80A	Z80 microprocessor	(U20)
(2)	7805	5 volt regulator	(U47, U48)
(1)	2N3906	PNP transistor	(Q1)

OTHER ELECTRONIC COMPONENTS

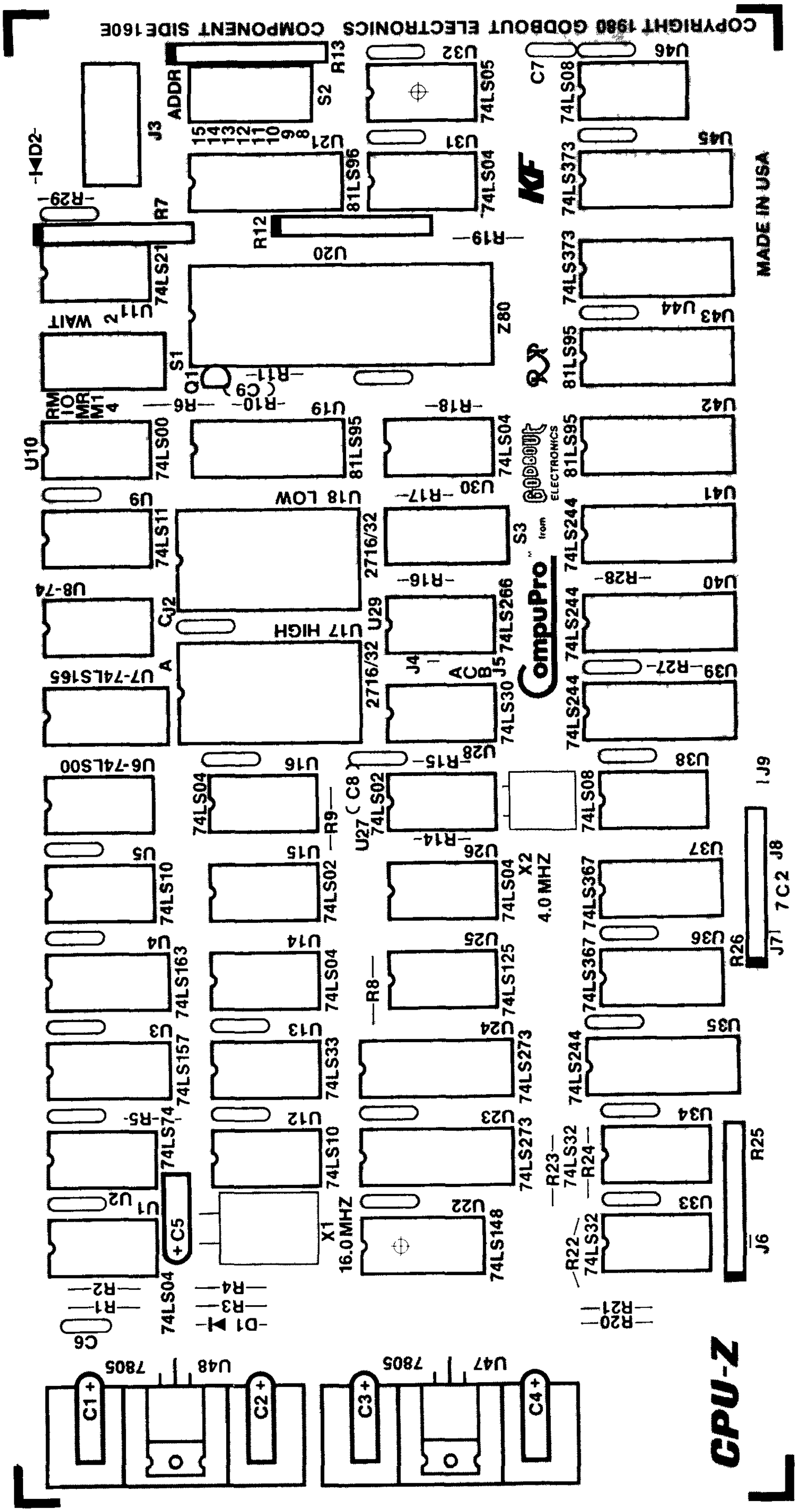
(5)	SIP resistor packs	(SR7, SR12, SR13, SR25, SR26)*
(5)	39uf Tantalum capacitors	(C1 - C5)
(1)	390 - 430 pF capacitor	(C7)*
(1)	43pf capacitor	(C9)*
(27)	Ceramic Bypass capacitors	All OTHER*
(2)	33 ohm resistors c.f.	(R11, R18)*
(1)	120 ohm resistor c.f.	(R3)*
(1)	150 ohm resistor c.f.	(R6)*
(1)	390 ohm resistor c.f.	(R29)*
(1)	910 ohm resistor c.f.	(R10)*
(5)	1K ohm resistors c.f.	(R1, R2, R4, R14, R15)*
(6)	1.5K ohm resistors c.f	(R8, R20 - R24)*
(7)	4.7K ohm resistors c.f	(R5, R9, R16, R17, R19, R27, R28)*
(1)	16MHz crystal	(X1)
(1)	4MHz crystal	(X2)
(2)	Glass signal diodes	(D1, D2)*

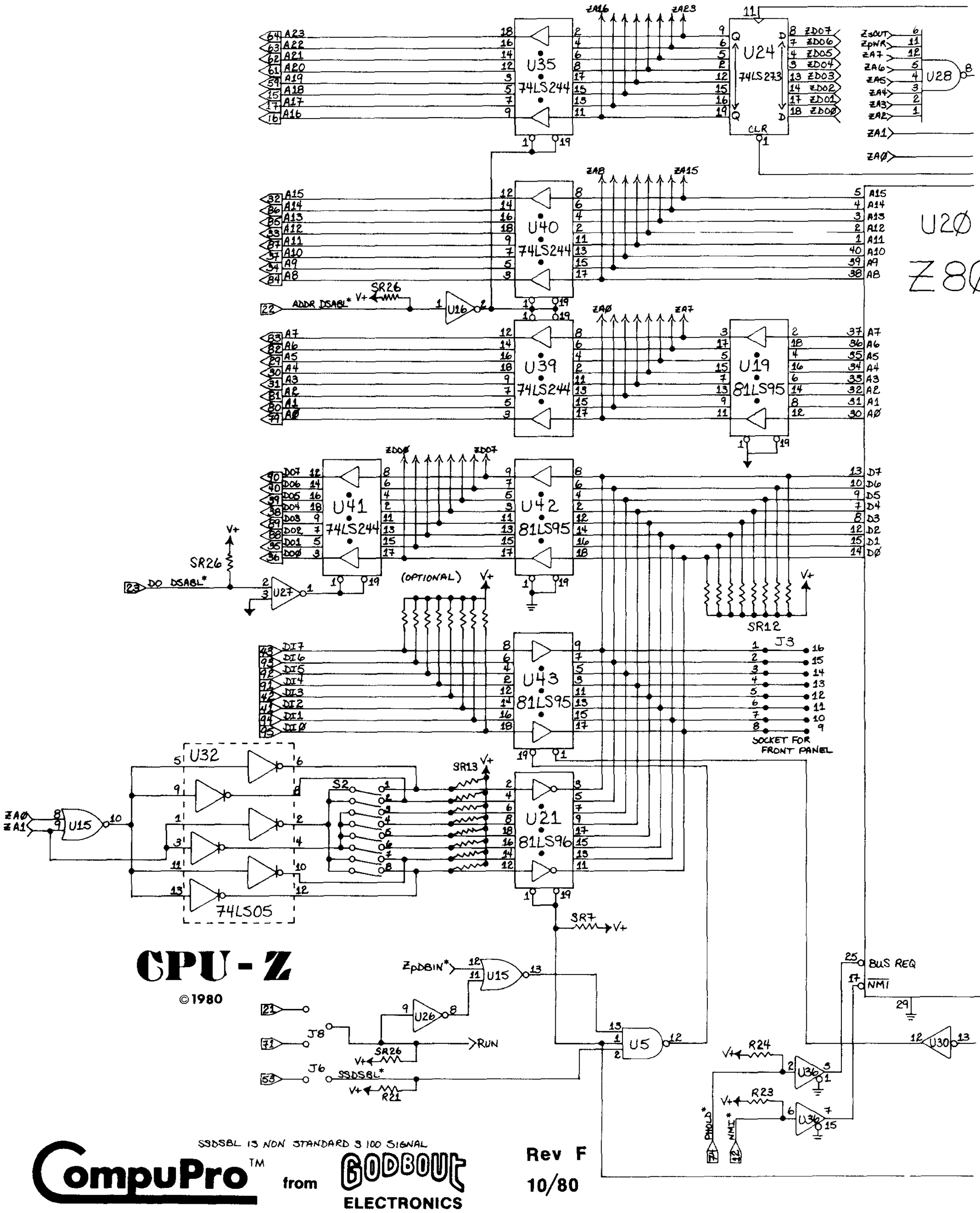
MECHANICAL COMPONENTS

(46)	Low profile sockets*	
(3)	Dip switch, 8 position	(S1-S3)*
(2)	TO-220 heat sinks	
(2)	Sets 6-32 hardware	
(2)	Card extractors	

* supplied already soldered on the board

Component Layout





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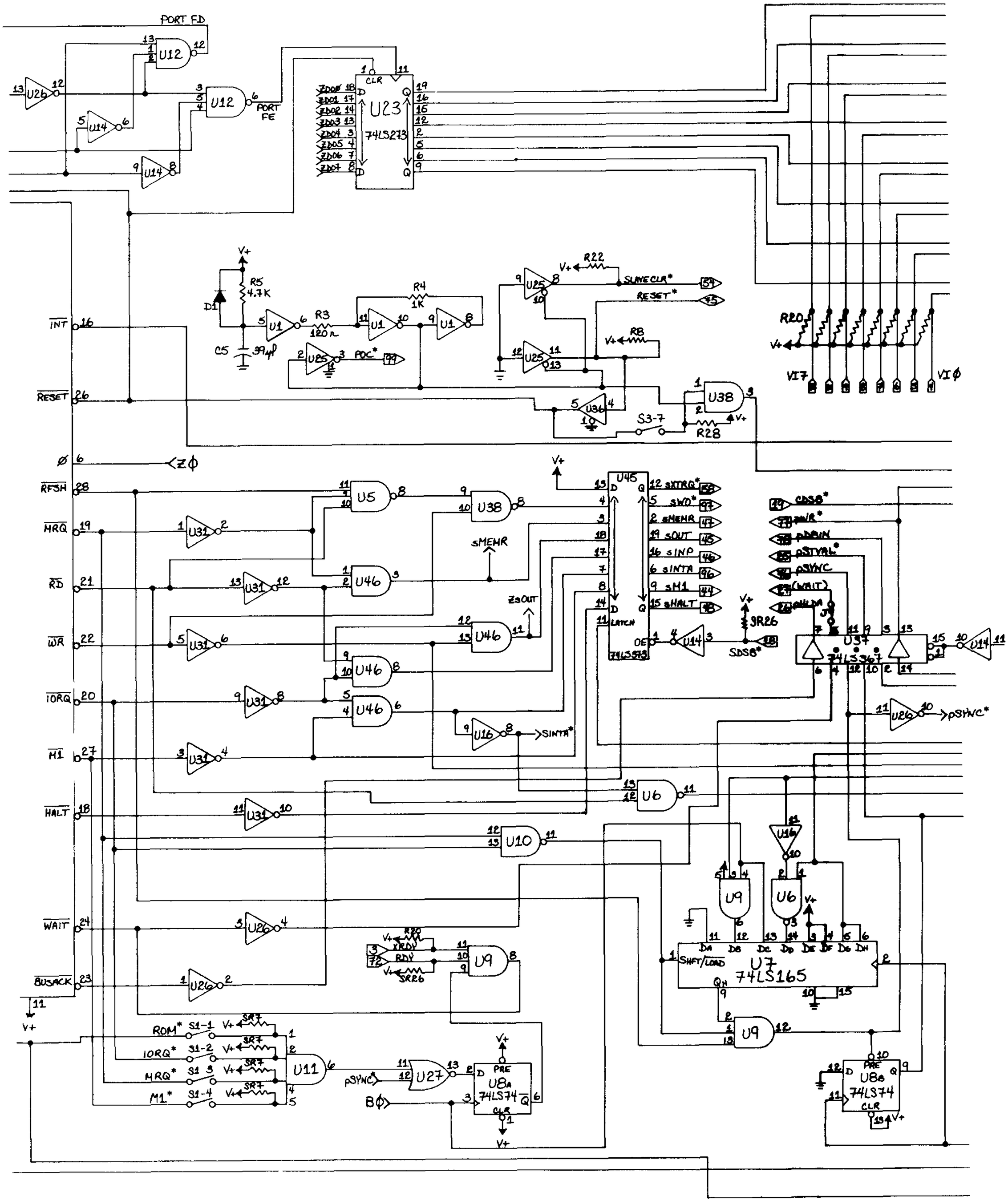
Rev F

10/80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U26
U14
PORT FE
U23
74LS273
CLR
ZD00
ZD01
ZD02
ZD03
ZD04
ZD05
ZD06
ZD07
V+
R5 4.7K
D1
C5 .39µF
R3 120R
R4 1K
U1
U25
PDC*
R22
SLAVECLR*
RESET*
R8
R20
VI7
VIØ
U38
U36
S3-7
R28
INT
RESET
Ø
ZØ
RFSH
HRQ
RD
WR
IORQ
M1
HALT
WAIT
BUSACK
U31
U5
U46
sMEHR
ZsOUT
U45
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pHLDA
U14
U26
pSYNC*
U16
SINTA*
U6
U10
U9
XRDY
RDY
SR6
U11
ROM*
IORQ*
MRQ*
M1*
S1-1
S1-2
S1-3
S1-4
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Q
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SHIFT/LOAD
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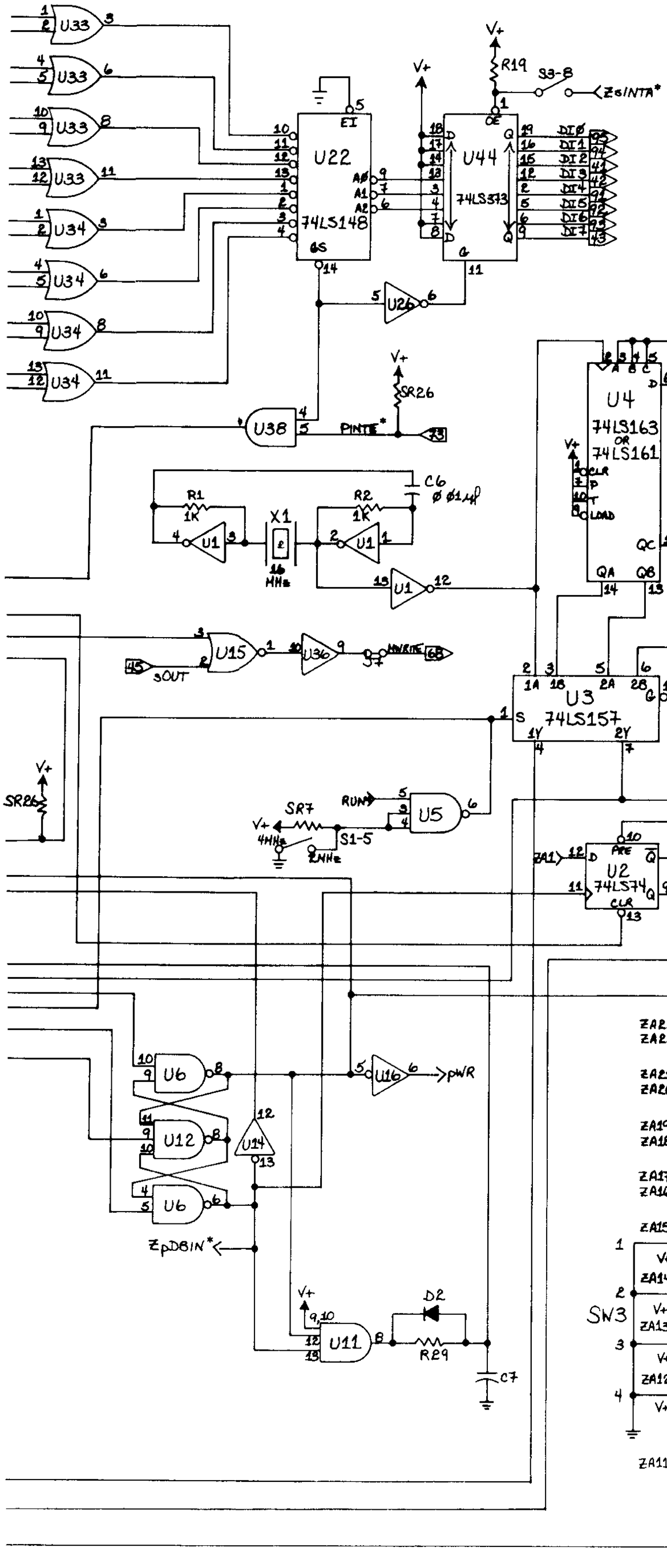
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D
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S3-8
ZesINTA*
V+
U26
SR26
PINTE*
U38
C6
Ø.01μf
R1
1K
R2
1K
X1
16 MHz
U1
U15
SOUT
U36
MWRITE
U4
74LS163
OR
74LS161
CLR
P
T
LOAD
QA
QB
QC
U3
74LS157
U2
74LS74
PRE
CLR
S1-8
POJ
ENABL
SR7
RUN
S1-5
4MHz
2MHz
U5
U6
U12
U14
U16
U11
pWR
ZpDBIN*
D2
R29
C7
U13
U29
U10
U30
SW3
S3-6
S3-5
R17
R16
R9
R27
R15
R14
CB
0.01μf
X2
4MHz
U27
2/4 MHz
C9
R6
R10
R11
R18
Q1
BØ
ZØ
CLK
2MHz
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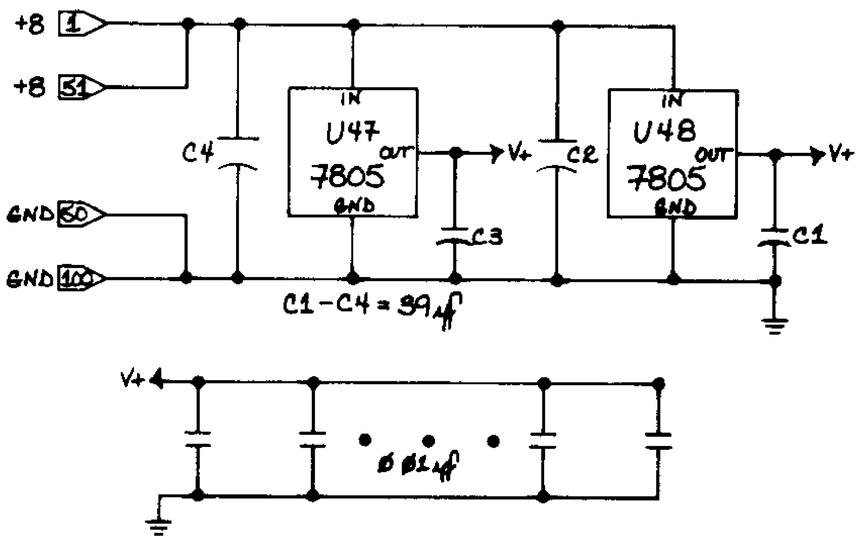
J4
J5
U18
2716
U17
2716
SMEMR
CEB*
CEA*


+8
GND
C4
C1-C4 = 39μf
U47
7805
U48
7805
IN
OUT
GND
C3
C2
C1
V+
Ø Ø1μf