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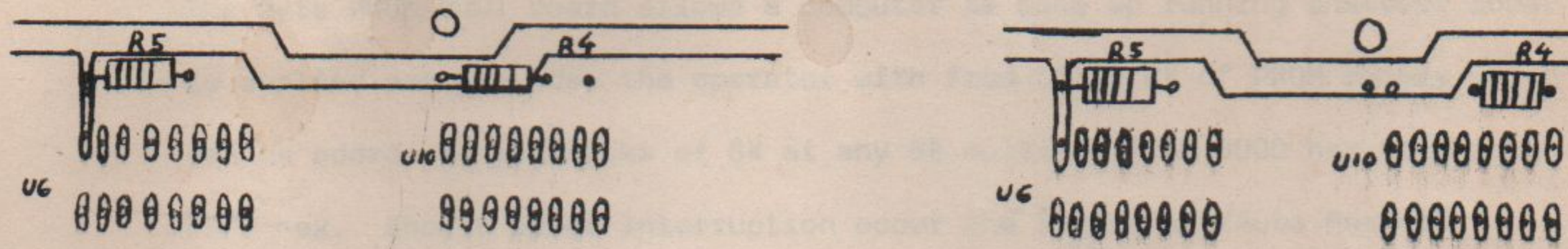
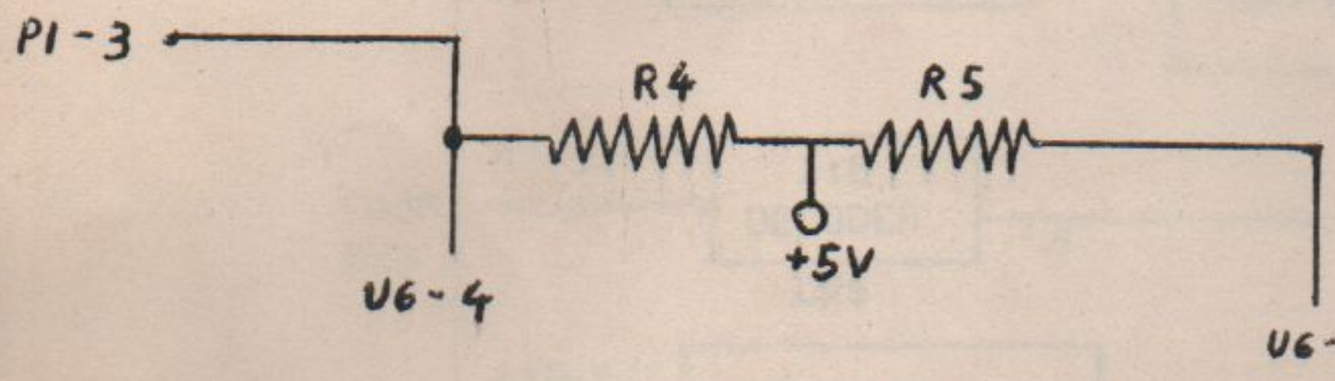
ADDENDUM TO BYTE PROM/BOOT DOCUMENTATION

Resistor R4, part #00085-004 (1K ohm - ¼w - 5%), as shown located above U10 on the resistor placement photograph (photo 1 page 9).... should be relocated as shown below.

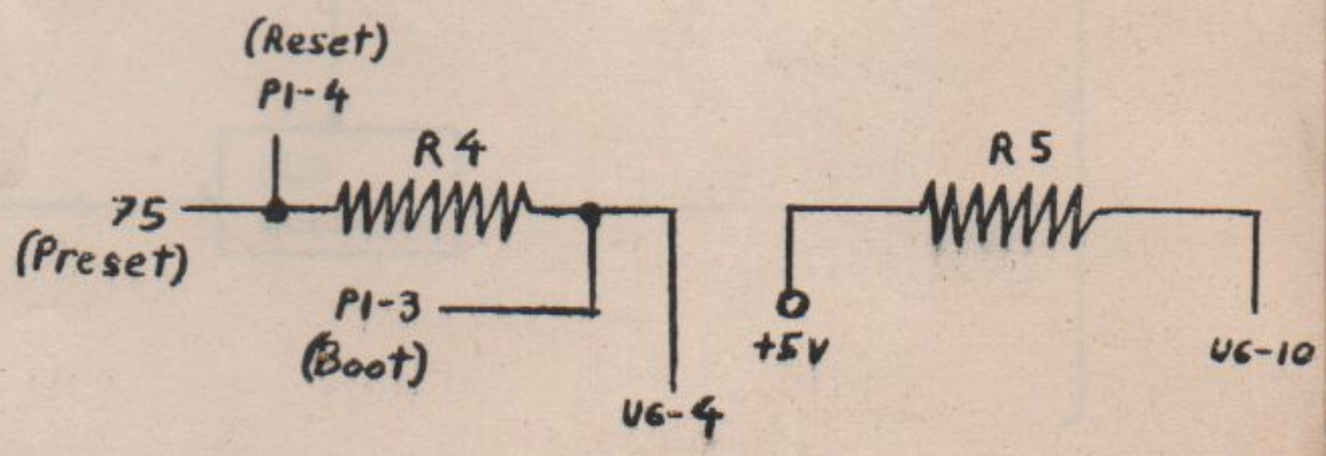


The Schematic should be changed as follows:

FROM:



TO:



NOTE: P1-6 to ground shown on schematic in two (2) places should be P1-7.

BYTE incorporated

BYTE PROM/BOOT BOARD

FUNCTIONAL DESCRIPTION

The Byte PROM/BOOT board allows a computer to come up running whenever power is applied and provides the operator with from 1K to 8K of PROM memory which can be addressed in blocks of 8K at any 8K multiple from 0000 hex up through FFFF hex. Should power interruption occur the Power Fail/Auto Restart feature (available only on the Byte board) allows for an orderly shutdown procedure. Functional block diagrams for the PROM and Power Fail/Auto Restart board sections are shown in Figures 1 and 2 respectively.

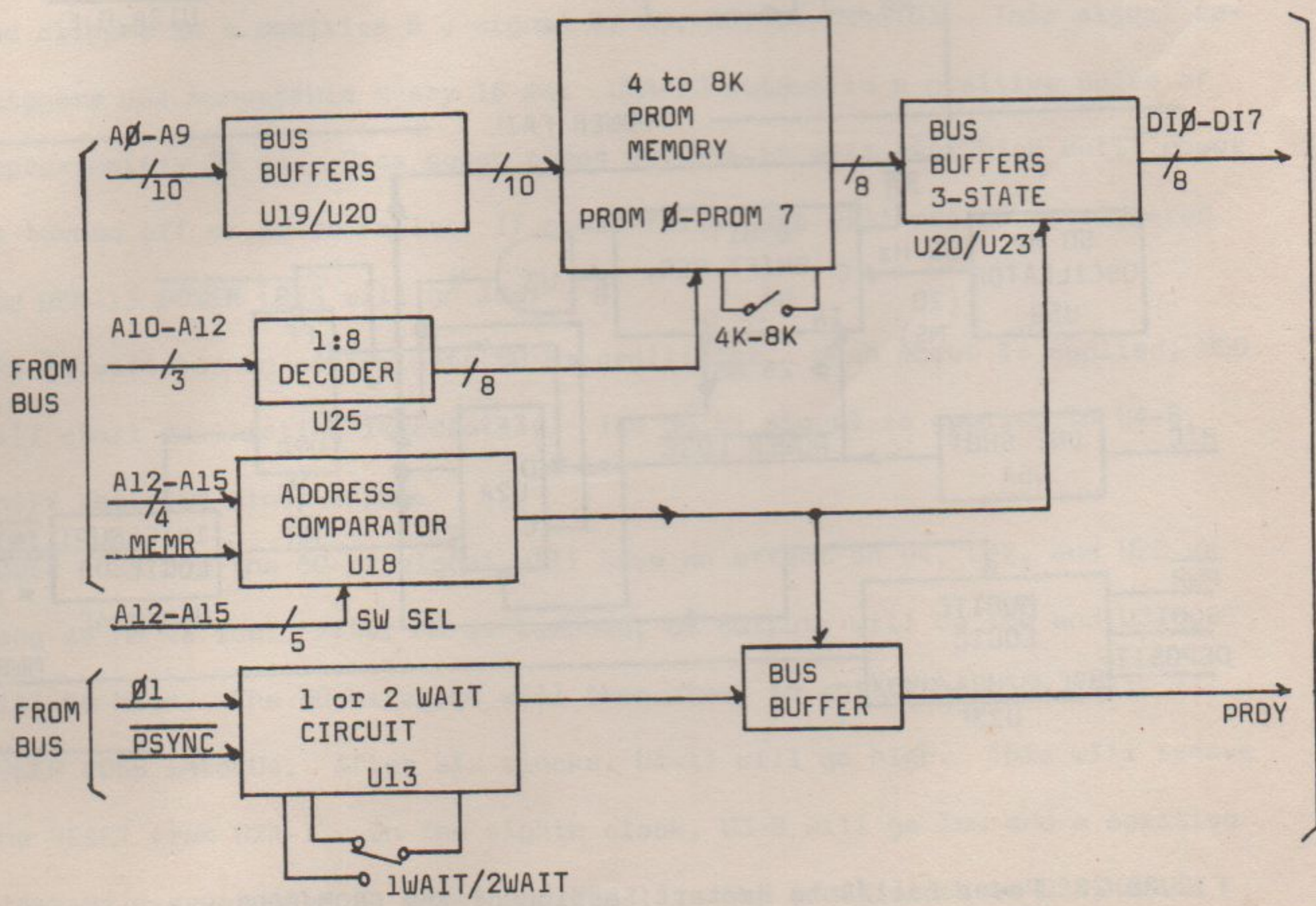


FIGURE 1. PROM Section of the PROM/BOOT Board Functional Block Diagram

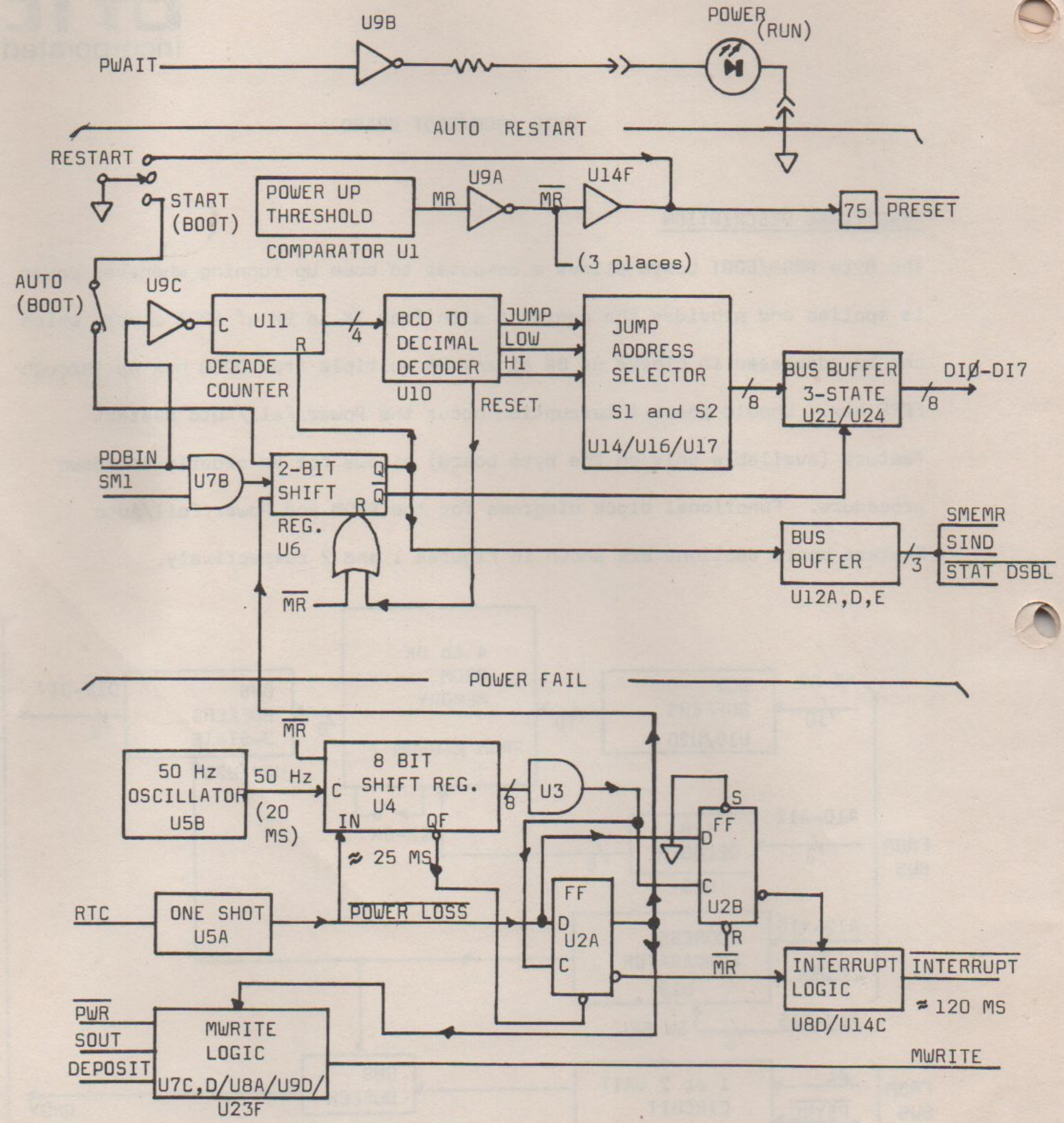


FIGURE 2. Power Fail/Auto Restart Section of the PROM/BOOT Board Functional Block Diagram

THEORY OF OPERATION

Power On

When power is first applied to the computer, the CPU registers and all other logic will assume some random state. U1 is wired as a 555 monostable oscillator. A low on U1-2 immediately triggers the 555, making U1-3 high for approximately 300 ms. U1-3 is inverted to produce master reset ($\overline{MR}$). $\overline{MR}$ is used to hold U4 outputs low and U2-8, U6-6, 8 high for as long as $\overline{MR}$ is low. $\overline{MR}$ is buffered and applied to bus pin 75 $\overline{PRESET}$. The program counter in the CPU chip will be held at address 0000H for as long as $\overline{PRESET}$ is low.

The program counter can also be set to address 0000H by momentarily placing BOOT/RESET (START/RESTART on the BYT-8) switch in the RESET position.

Power Up

A 60 Hz signal is on bus pin 55. The 60 Hz signal is rectified, filtered, and clipped to a positive 5 v signal by R8, R9, C6, and D3. This signal retriggers U5A monostable every 16 ms. U5A-13 output is a positive pulse of approximately 25 ms. Once power comes up, U5A-13 will stay high until power is turned off or power fails. If power fails, U5A will not be retriggered and U5A-13 $\overline{POWER\ LOSS}$ will go low.

U5B is wired as an approximate 50 Hz oscillator. When power is applied, U5B will start oscillating immediately. The 50 Hz signal is applied to U4-8, shift register clock input.

$\overline{POWER\ LOSS}$ and the 50 Hz signal will have no effect on U4, U2A, and U2B as long as $\overline{MR}$ is low. After $\overline{MR}$ is removed, U4 outputs will be low and U2-6, 8 will be high. The 50 Hz clock will then start to shift the high U4-1, 2 $\overline{POWER\ LOSS}$ into U4. After six clocks, U4-11 will go high. This will remove the RESET from U2A-1. On the eighth clock, U3-8 will go low and a positive clock will be applied to U2A-3 and U2B-11. The input clock to U2B has no effect as the D input is grounded. U2A-5 will go high and U2A-6 will go low

as the D input to U2A is high ($\overline{\text{POWER LOSS}}$). U2A-6 going low will not generate an interrupt request because U8D-13 is high. When U2A-5 goes high, MWRITE circuit is enabled and a clock is applied to U6A-3, AUTO BOOT circuit. This clock is used to start the power-on AUTO BOOT if S3/AUTO BOOT switch is open.

AUTO BOOT can also be started at any time by momentarily placing BOOT/RESET switch in the BOOT position.

Power Down

When power is turned off or if power fails, the 60 Hz signal applied to U5A monostable will stop. $\overline{\text{POWER LOSS}}$ will go low when U5A is not retriggered. $\overline{\text{POWER LOSS}}$ going low will set U28-8 low. With U8D-12, 13 low, U8D-11 and U14C-6 ($\overline{\text{INTERRUPT}}$) will go low. This will generate an interrupt request to the CPU chip. Your software could then do whatever clean-up was possible before power failed completely. Six 50 Hz clocks later, U4-11 will go low, setting U2A-6 high. This will remove the interrupt request and disable the MWRITE circuit.

Preset

When power is applied or P1-4 is grounded with the front panel switch, the CPU chip will set the program counter to address 0000H. When the switch is released, the CPU will start executing any program that is at that address.

AUTO BOOT

AUTO BOOT is an automatic jump to a two byte address, initiated by either turning power on or by momentarily placing BOOT/RESET (START/RESTART on the BYT-8) switch in the BOOT position. The address to be jumped to is placed in switches S1 and S2. S1 is the lower address byte and S2 is the upper address byte. When power is turned on, U2-5 will go high and clock U6-3. If S3/AUTO BOOT switch is open, U6-5 will go high and AUTO BOOT will start.

If the AUTO BOOT is started by momentarily placing BOOT/RESET switch in the BOOT position, U6-5 will be forced high.

When bus pin 44 (SM1) and bus pin 78 (PDBIN) go high, the CPU is in an instruction fetch mode. U7B-6 will go high and clock U6-11. If U6-12 was high, U6-9 will be clocked high and bus pin 18 ($\overline{\text{STAT DSBL}}$) will go low. This will tri-state the CPU status latch information. U6-9 will also force SMEMR, SINP, and SM1 low, and remove the reset from counter U11. Disabling the status latch and forcing SMEMR and SINP low will inhibit any memory or any input device from placing data onto the data input bus. U6-8 going low will untri-state the gates between the data input bus and switches S1 and S2.

U10 is a BCD to one of ten decoders. The input to the decoder is counter U11 output. With counter U11 at zero, U10-1 will be low. The jump command and the jump address in switch S1/AØ through S2/A15 are only allowed onto the data input bus when a boot has started. If a boot has started, a jump instruction will be forced onto the data bus. This will happen just after U7B-6 clocks U6B-9 high. The CPU will input the jump command and PDBIN will go low. When PDBIN goes low, counter U11 will up count by one and U10-2 will go low. U10-2 going low will force the low address byte in S1 onto the data input bus. The CPU will input this byte when PDBIN goes high again. PDBIN going low will set U10-3 low and the high byte in S2 will be forced onto the data input bus. The CPU will input this byte when PDBIN goes high. When PDBIN goes low, U10-4 will go low and will reset U6-5, 9 low. SM1, SMEMR, and SINP are allowed to float and the CPU status latch information is applied to the bus. At the same time, gates U21 and U24 are tri-stated. The CPU program counter will now contain the address that was set into switches S1 and S2. The CPU will then start executing the instructions stored there.

PROM

Bus address AØ through A9 are buffered and connected to PROMØ through PROM7. The outputs of all eight PROMs are paralleled and connected to the data input bus through tri-state gates U20 and U23. Data from the PROMs will only be applied to the data input bus if comparator output U18-9 is low. The output of only one PROM is allowed to be connected to the inputs of the tri-state gates at any time. Addresses AØ-A9 will address the 1024 paralleled bytes of each PROM. Addresses A1Ø-A12 are decoded by U25 into eight 1024 blocks. This enables only one of the eight PROMs at any one time. The $\overline{\text{CHIP SELECT}}$ on the PROMs are active low. If addresses A10, A11, and A12 were low, then U25-1 would be low and PROMØ would be enabled.

For 2708 PROMs, close 4K/8K contacts of dip socket connector S3. Contacts A12 of switch S3 must be open or address bus A12 will be shorted to ground. Contacts A13 through A15 of switch S3 select which one of the eight 8192 byte blocks the board will respond to.

Below are the switch positions for addressing 2708 PROMs. 0 = closed contacts, 1 = open contacts.

START ADDRESS	S3 4K/8K	S3 A12	S3 A13	S3 A14	S3 A15
0000	0	1	0	0	0
8192	0	1	1	0	0
16384	0	1	0	1	0
24576	0	1	1	1	0
32768	0	1	0	0	1
40960	0	1	1	0	1
48128	0	1	0	1	1
56320	0	1	1	1	1

Comparator output U18-9 will go low when address bus A13 through A15 equals A13 through A15 of switch S3, SMEMR is high, and B1 and T1 of U18 are equal. The data in the addressed byte of the selected PROM will then be placed onto the data input bus.

WAIT

At the beginning of each MEMORY READ, the CPU will reset U13-5, 9 by placing PSYNC (bus pin 76) high. The contents of one of the memory addressing registers is placed onto the address bus. The status information is also placed onto the data bus. On the low going edge of the next phase 1 (Ø1) clock, the status information is latched into the status latch. SMEMR will then go high. PSYNC will go low, removing the reset from U13-1, 13.

Each PROM will decode the same byte as determined by the address bus AØ through A9. Address bus A10, A11, A13 will select which of the eight PROMs can output to the tri-state gates. Address A13 through A15 will have stabilized and if the same as selected by S3/A13, S3/A14, S3/A15 will cause U18-9 to go low, enabling the tri-state gates to place the data from the selected PROM onto the data input bus.

WAIT states are used to make the CPU wait until the PROMs have had time to respond to address changes. The slower the PROMs used, the more WAIT states needed. The following are the settings for the different PROM speeds.

PROM SPEED	S3/1WAIT	S3/2WAIT
450 ns	Open	Open
1.0 us	Closed	Open
1.5 us	Open	Closed

If no WAIT states are selected, PRDY (bus pin 72) is high and the CPU keeps going. If one WAIT is selected, then Ø1 clock will have to clock once. If two WAITs are selected, then two Ø1 clocks are needed. Once PRDY goes high, the CPU can input the byte on the data input bus.

MWRITE

After power is applied and the power up circuitry has set U7C-9 high, the MEMORY WRITE (MWRITE) circuit is enabled. Memory can be written into by either $\overline{\text{DEPOSIT}}$ going low or by the CPU setting $\overline{\text{PWR}}$ (bus pin 77) low with SOUT (bus pin 45) low.

Power LED

The BYT-8 front panel power LED can be used as either a power on indicator or as a WAIT LED. To use the LED as a power LED, insert R13. For a WAIT LED, just insert R12.

ASSEMBLY NOTES

Before proceeding, verify that all parts called out in the parts list are in the kit. Sockets are only supplied for the eight PROMs. It is advisable that sockets be used in all IC locations. These may be purchased at the local BYTE SHOP.

Use only a fine tipped 25-35 watt solder iron. Do not overheat the traces.

Use only a high quality resin core solder.

After each component is inserted into the board, solder it in place. Clip the leads and verify that there are no solder bridges.

Do not remove or install board with power applied.

When inserting and removing PROMs from conductive foam or from sockets, always touch foam or ground trace before touching PROMs. This will remove any static charge that you might have. PROMs should be stored in conductive foam, foil, or on the board, and not just sitting on the work bench.

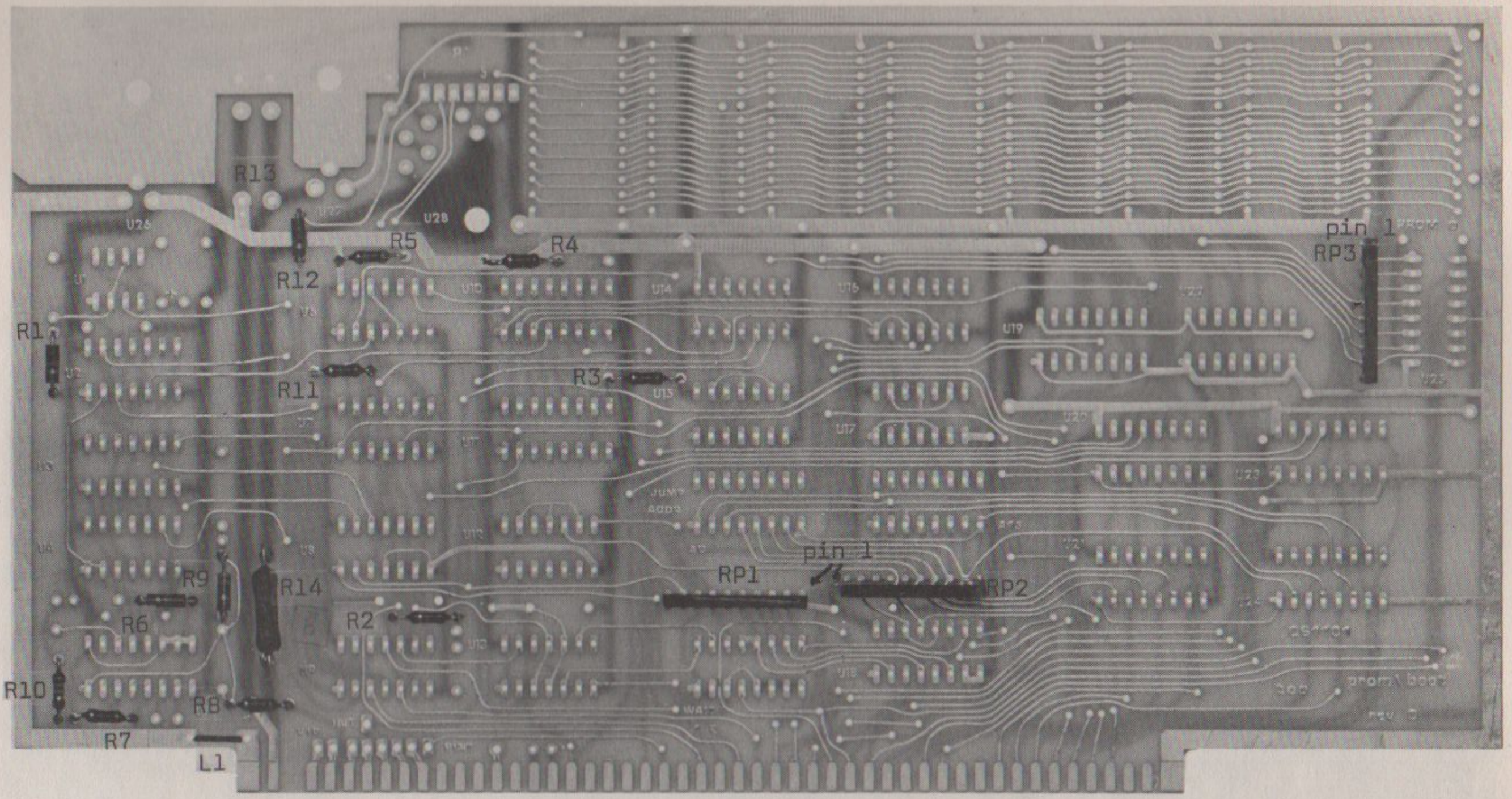


PHOTO 1

Install resistors, resistor packs, and jumper L1. Refer to Parts List for proper values.

NOTE: 1) Install R12 if BYT-8 front panel LED is to be used as a WAIT LED. If the LED is to be used as a power LED, install R13.

2) Observe pin 1 orientation for the resistor packs.

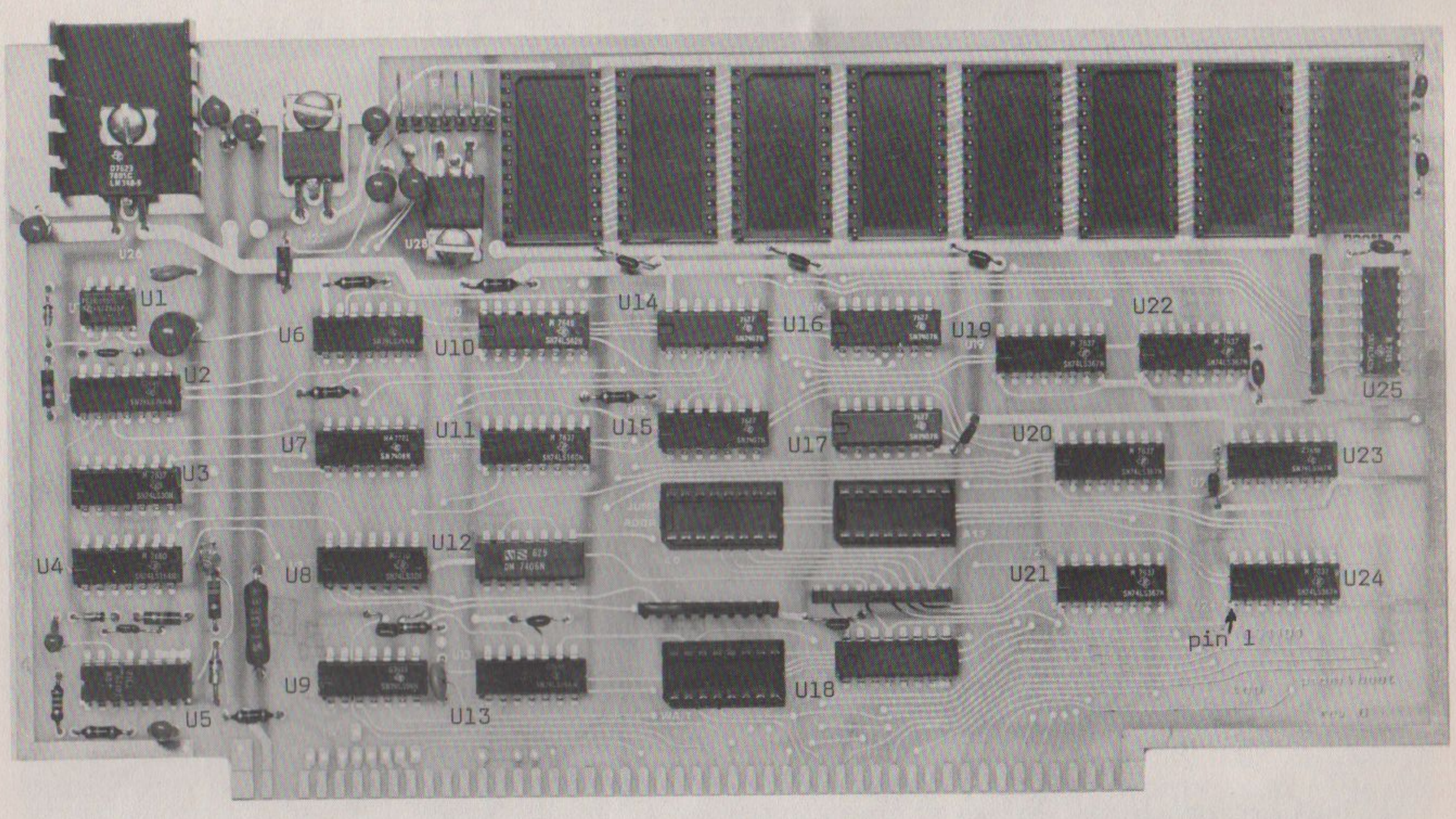


PHOTO 4

Observe pin 1 orientation and install the remaining IC's. See Parts List for type.

To Finish Assembly

1. Install 2708 PROMs into the sockets. Set the board address and jump address as per PROM and BOOT theory. (See Figure 3. below.)
2. Set S3/1WAIT and S3/2WAIT dip socket connectors as per WAIT theory.
3. Open S3/AUTO BOOT dip socket connector if power on AUTO BOOT is desired.

Wiring Instructions for BYT-8 Front Panel LED

Connector J1 called out below is the female half of P1.

1. Remove wires from LED and START/RESTART switch to mother board.
2. Wire anode end of LED to J1-1.
3. Wire cathode end of LED to center of START/RESTART switch.
4. Wire center terminal of switch to J1-6.
5. Wire upper terminal of switch to J1-3.
6. Wire lower terminal of switch to J1-4.
7. Install front panel to computer main frame.
8. Apply power. If AUTO BOOT is enabled, the CPU should start running the program at switch S1 and S2 address. Try MANUAL BOOT; the CPU should start over at the same address.

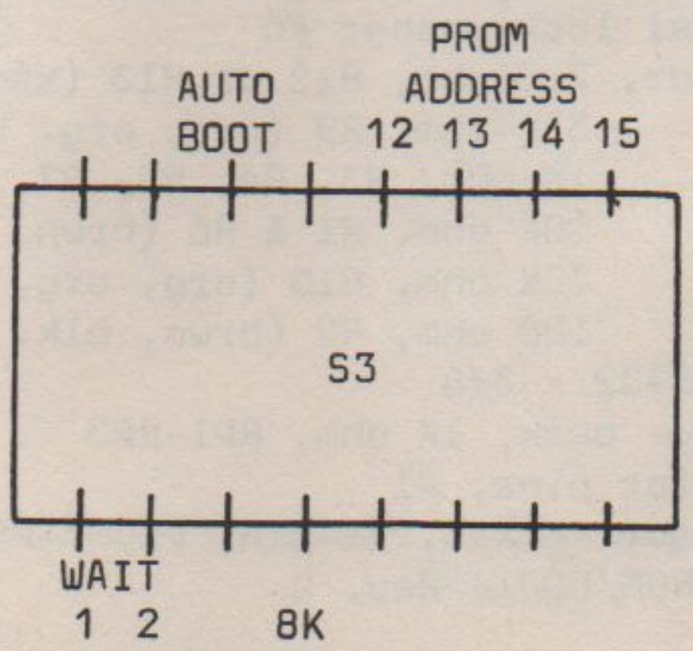


FIGURE 3. S3 Dip Plug Diagram

PROM/BOOT PCB Assembly Parts List

PART NUMBER	QTY	PART DESCRIPTION
00011-005	13	Capacitor, .1 ufd, 15 v, mica dipped, SC1-SC13
00015-003	1	dipped tantalum, 47 ufd, 10 v, C1
00015-004	2	dipped tantalum, 4.7 ufd, 25 v, C4, C5
00015-006	1	dipped tantalum, 1 ufd, 35 v, C6
00011-003	1	ceramic, .01 ufd, 15 v, C2
00011-004	1	ceramic, 100 pfd, 15 v, C3
00015-005	6	dipped tantalum, 10 ufd, 25 v, C7-C12
00025-002	2	Diode, silicon, 1N914, D1 & D2
00025-001	1	Diode, Zener, 1N4732, D3
00045-001	1	IC, Digital, 7406N, U12
00045-003	6	74LS367N, U19-U24 (74367, 8097)
00045-005	1	74LS04N, U9
00045-006	1	74LS30N, U3
00045-007	3	74LS74N, U2, U6, & U13
00045-012	1	74LS08N, U7
00045-015	1	74LS123N, U5
00045-022	1	555CN, U1
00045-023	1	74LS164N, U4
00045-024	1	74LS32N, U8
00045-025	2	74LS42N, U10 & U25
00045-026	1	74LS160N, U11
00045-027	4	7407N, U14-U17
00045-028	1	8131N, U18
00033-001	1	Linear IC, 7805C, +5 v regulator, U26
00033-002	1	LM340T-12, -12 v regulator, U27
00033-004	1	LM320T-5.2, -5 v regulator, U28
00048-002	3	Hex Nut, 6-32
00021-001	1	Connector, male plug, P1
00021-002	3	Connector, male plug, S1-S3
00022-001	1	Connector, female receptacle, P1
00027-001	1	Heat Sink, 1.2" x 1", U26
00059-001	1	Resistor, wire wound, 33 ohm, 3w, R14
00076-002	3	Internal lock washer #6
00085-001	1	Resistor, 220 ohm, R12 or R13 (red, red, brwn)
00085-003	1	330 ohm, R9 (org, org, brwn)
00085-004	6	1K ohm, R3, R4, R5, R7, R8, & R11 (brwn, blk, red)
00085-006	2	10K ohm, R1 & R6 (brwn, blk, org)
00085-008	1	33K ohm, R10 (org, org, org)
00085-007	1	100 ohm, R2 (brwn, blk, brwn)
00153-004	3	BHMS, 6-32 x 3/8
00172-003	3	Resistor pack, 1K ohm, RP1-RP3
00183-001	7	Connector pins, P1
00184-004	8	Connector socket, 24-pin, PROMØ-PROM7
61101-001	1	PCB, PROM/BOOT, Rev. 0

Rev. 0, 6/77