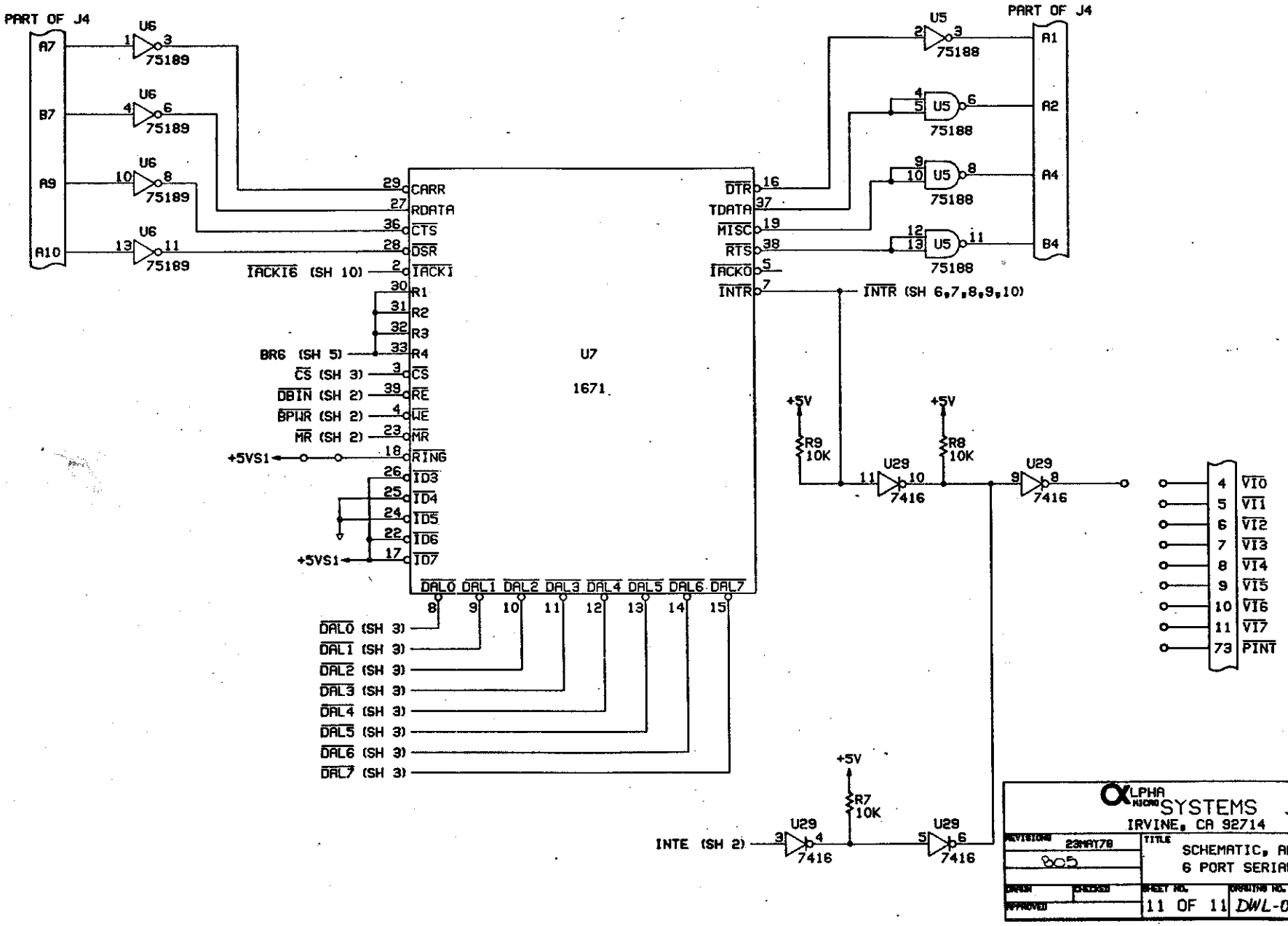
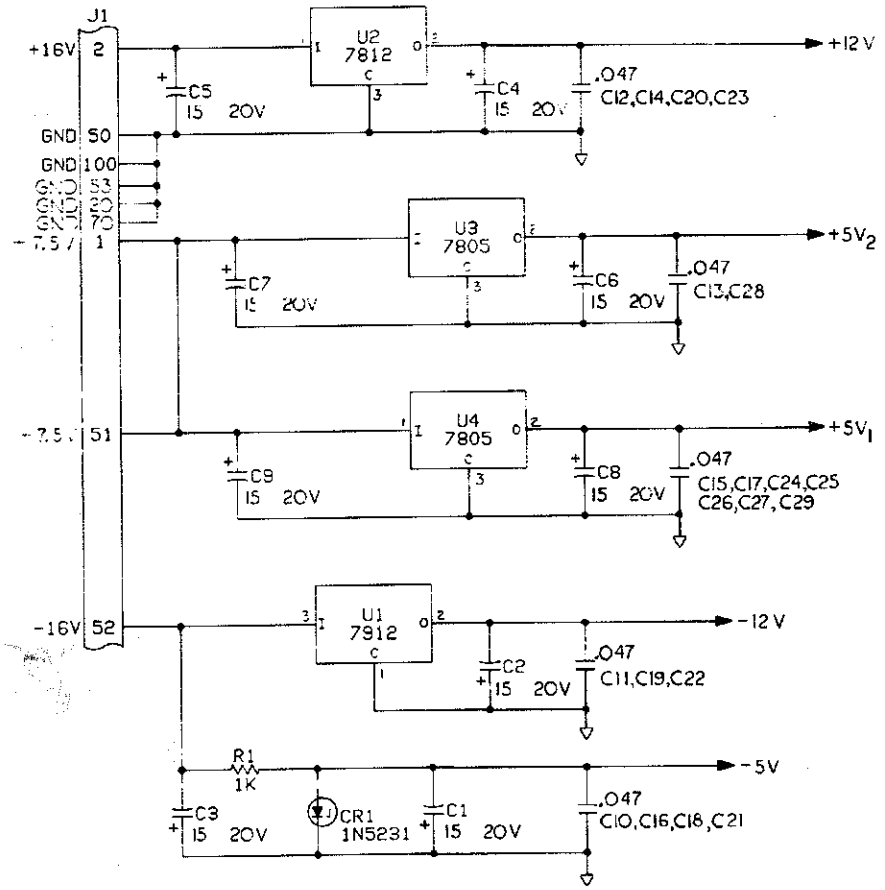

PART OF J4
A7
B7
A9
A10
U6
75189
U5
75188
PART OF J4
A1
A2
A4
B4
U7
1671
CARR
RDATA
CTS
DSR
IACKI
R1
R2
R3
R4
CS
RE
WE
MR
RING
ID3
ID4
ID5
ID6
ID7
DTR
TDATA
MISC
RTS
IACKO
INTR
IACKI6 (SH 10)
BR6 (SH 5)
CS (SH 3)
DBIN (SH 2)
BPWR (SH 2)
MR (SH 2)
+5VS1
INTR (SH 6,7,8,9,10)
DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7
DAL0 (SH 3)
DAL1 (SH 3)
DAL2 (SH 3)
DAL3 (SH 3)
DAL4 (SH 3)
DAL5 (SH 3)
DAL6 (SH 3)
DAL7 (SH 3)
+5V
R9
10K
R8
10K
R7
10K
U29
7416
INTE (SH 2)
VI0
VI1
VI2
VI3
VI4
VI5
VI6
VI7
PINT
ALPHA MICRO SYSTEMS
IRVINE, CA 92714
REVISIONS
23MAY78
805
TITLE
SCHEMATIC, AM-300
6 PORT SERIAL I/O
DRAWN
CHECKED
APPROVED
SHEET NO.
11 OF 11
DRAWING NO.
DWL-00300-00

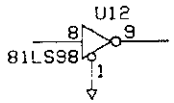


REVISIONS				
REV.	COMP. REV.	DESCRIPTION	DATE	APPROVED
B02		REVISE PER EN00212	9-13-79	
B02		DEVIATION EN00112	9-21-79	
B03		REVISE PER EN00117	9-13-79	
B05		REVISE PER EN00263	6-19-80	G. MANSON
B06		REWORK PER EN00328		
B07		REVISE PER EN00397		
B08		REVISE PER EN00406		

2. CAPACITORS ARE IN MICROFARADS.
1. RESISTORS ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

SPARES



VCC AND GND TABLE

VCC PIN NO. +5V1	VCC PIN NO. +5V2	VCC PIN NO. +12V	VCC PIN NO. -5V	VCC PIN NO. -12V	GND	I.C. NO.
14					7	U10,16,26,29,30,31,35
16					8	U20,28,34,36,38
20					10	U12,32,37,39,40
	14				7	U6,14,22
2		9			11	U11,19,27
		14		1	7	U5,9,13,17,21,25
		40	1		20	U7,8,15,16,23,24

LAST REF. DESIG. USED	REF. DESIG. NOT USED
C29 CR1 R15 U40 Y3 J14	U33, R10

ALPHA MICRO SYSTEMS
IRVINE, CA 92714

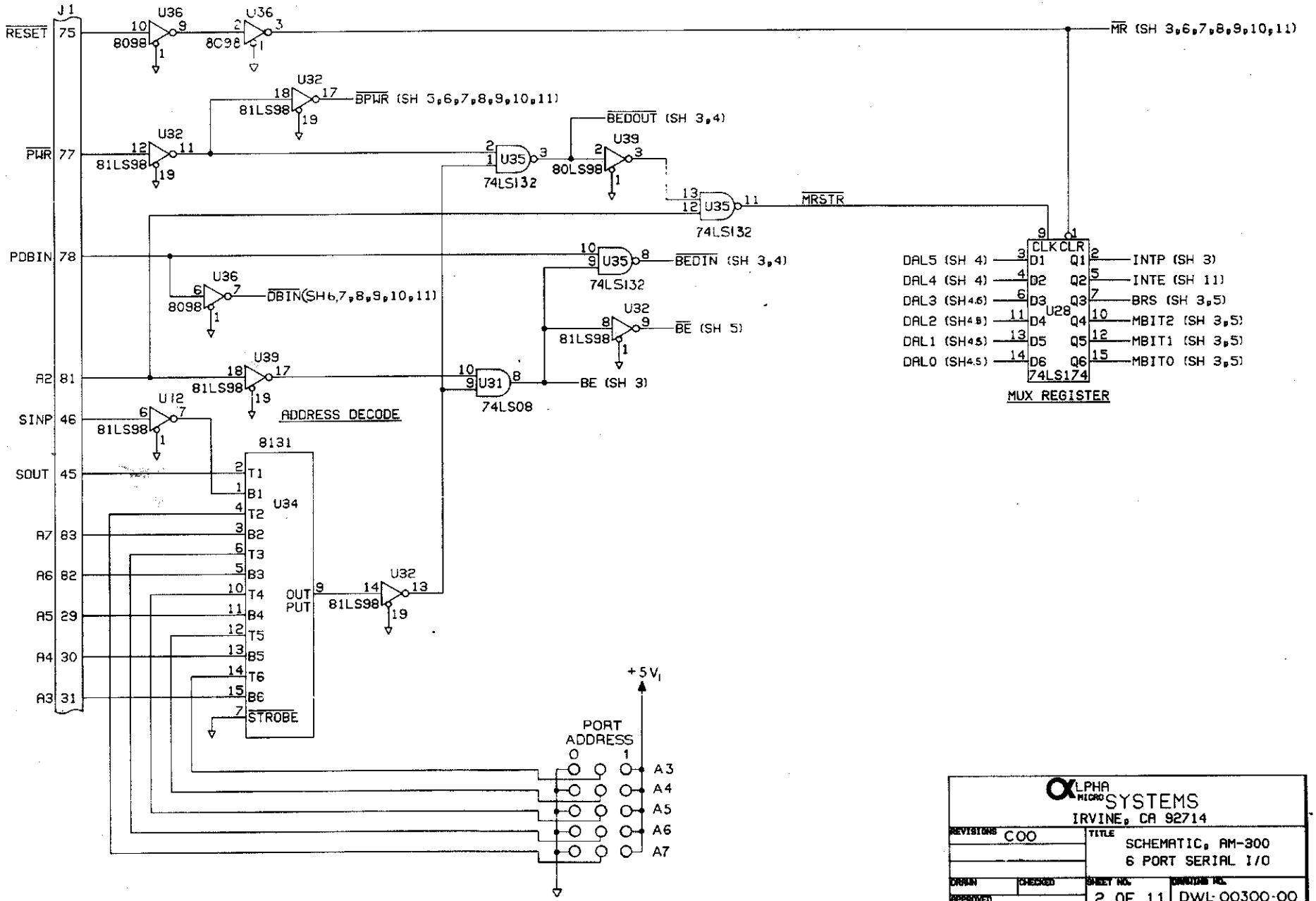
REVISIONS COO

TITLE: SCHEMATIC, AM-300 6 PORT SERIAL I/C

DRAWN | CHECKED | APPROVED

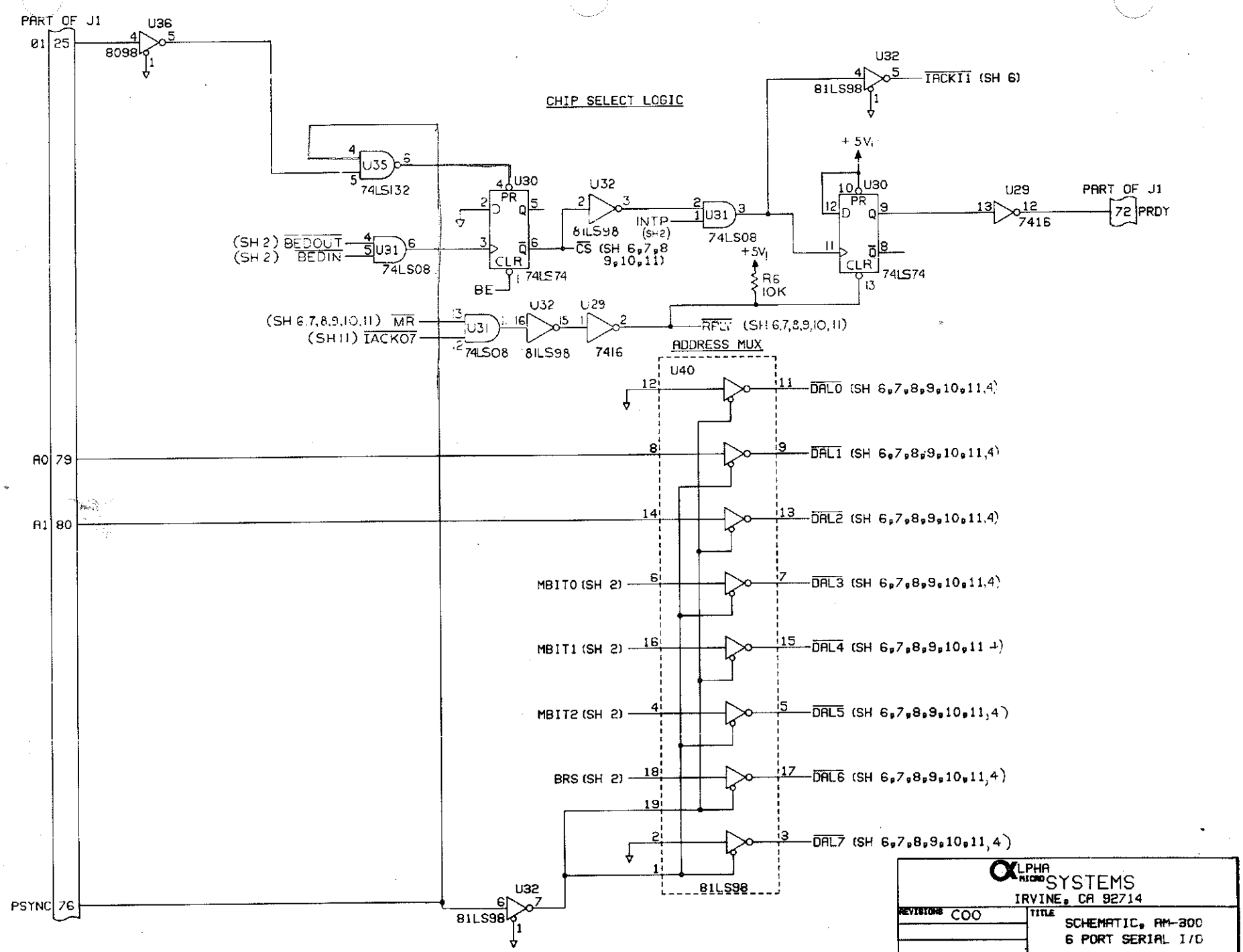
SHEET NO. 1 OF 11

DRAWING NO. DWL-00300-00



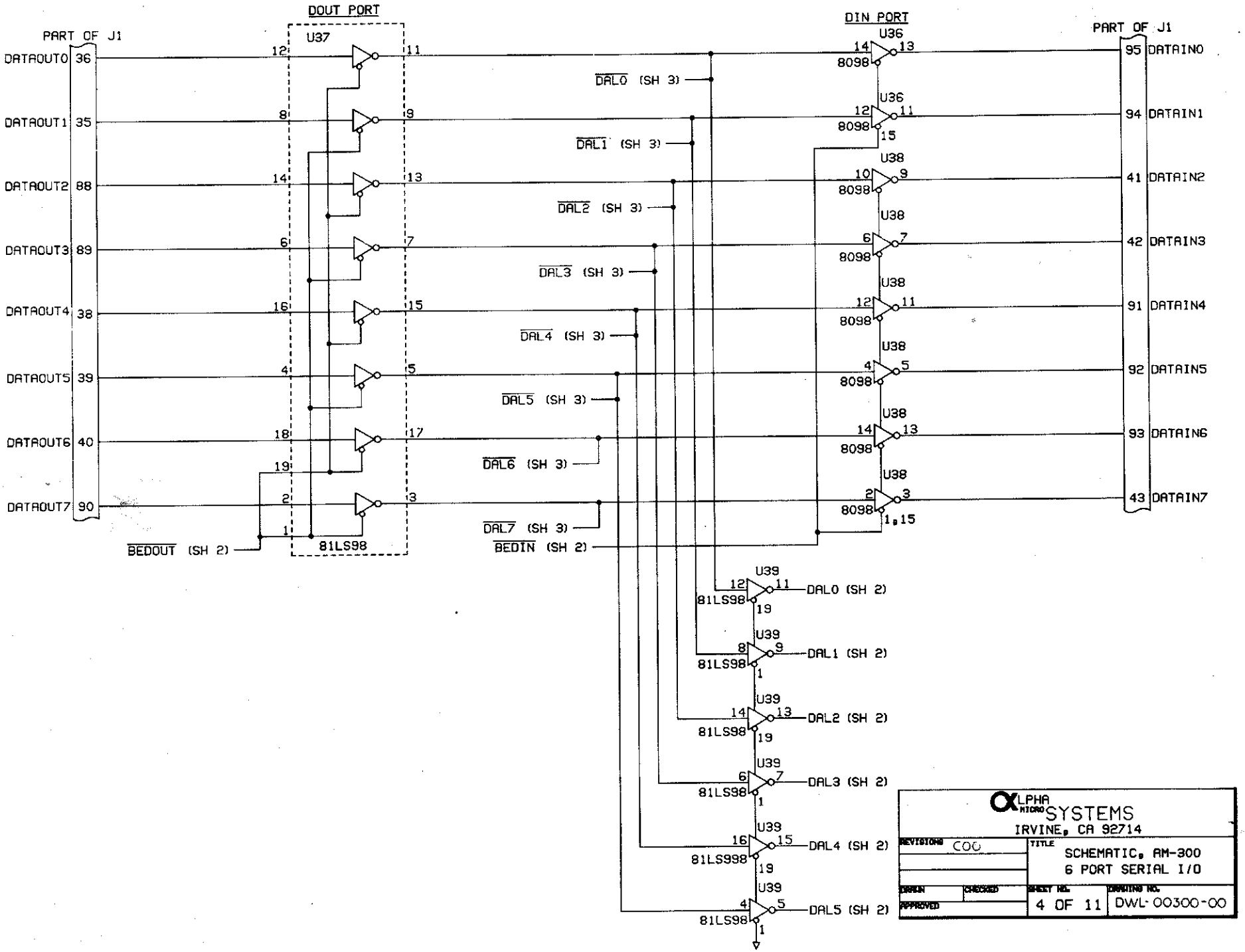
ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS: COO	TITLE: SCHEMATIC, AM-300 6 PORT SERIAL I/O	
DRAWN / CHECKED / APPROVED	SHEET NO.: 2 OF 11	DRAWING NO.: DWG-00300-00



ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS COO	TITLE SCHEMATIC, AM-300 6 PORT SERIAL I/O
DRAWN / CHECKED / APPROVED	SHEET NO. 3 OF 11
	DRAWING NO. DWL-00300-00



ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS	TITLE
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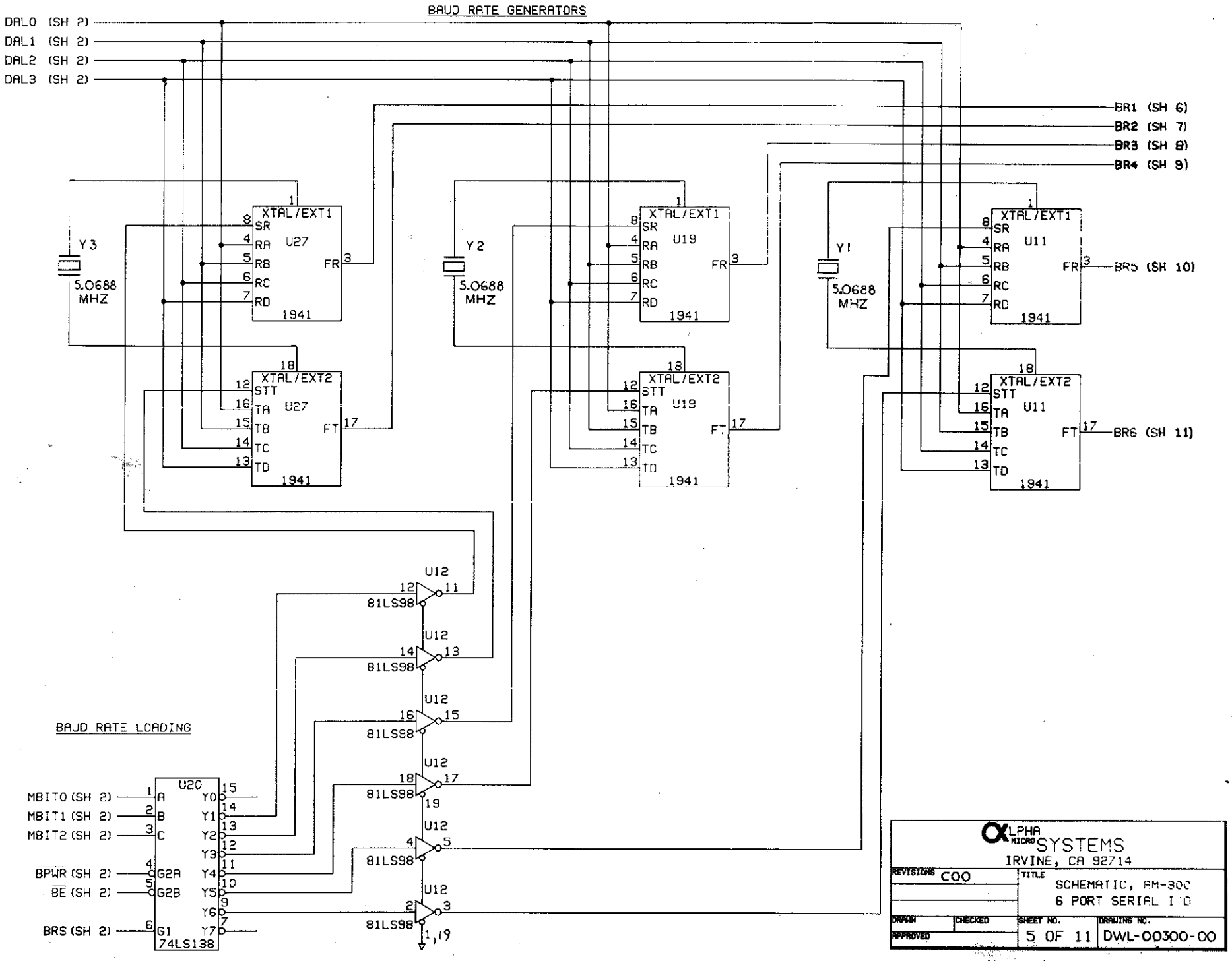
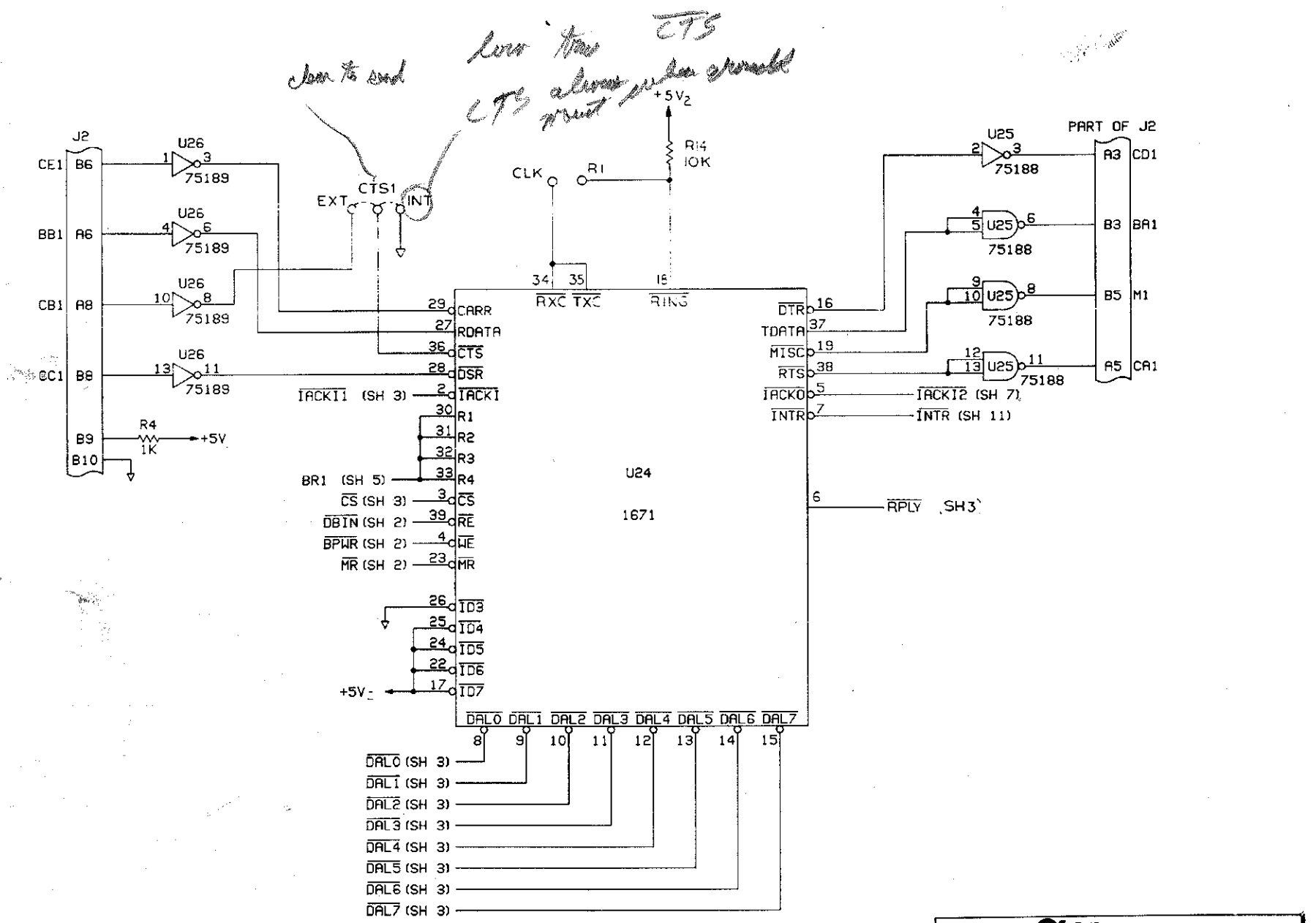
DRAWN / CHECKED / APPROVED	SHEET NO. 4 OF 11
	DRAWING NO. DWL-00300-00


BAUD RATE GENERATORS
DAL0 (SH 2)
DAL1 (SH 2)
DAL2 (SH 2)
DAL3 (SH 2)
BR1 (SH 6)
BR2 (SH 7)
BR3 (SH 8)
BR4 (SH 9)
BR5 (SH 10)
BR6 (SH 11)
Y3
Y2
Y1
5.0688 MHZ
XTAL/EXT1
XTAL/EXT2
U27
U19
U11
1941
SR
RA
RB
RC
RD
FR
STT
TA
TB
TC
TD
FT
U12
81LS98
BAUD RATE LOADING
U20
74LS138
MBIT0 (SH 2)
MBIT1 (SH 2)
MBIT2 (SH 2)
BPWR (SH 2)
BE (SH 2)
BRS (SH 2)
G2A
G2B
G1
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
ALPHA MICRO SYSTEMS
IRVINE, CA 92714
REVISIONS COO
TITLE
SCHEMATIC, AM-300
6 PORT SERIAL I O
DRAWN
CHECKED
APPROVED
SHEET NO.
5 OF 11
DRAWING NO.
DWL-00300-00



ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS	TITLE
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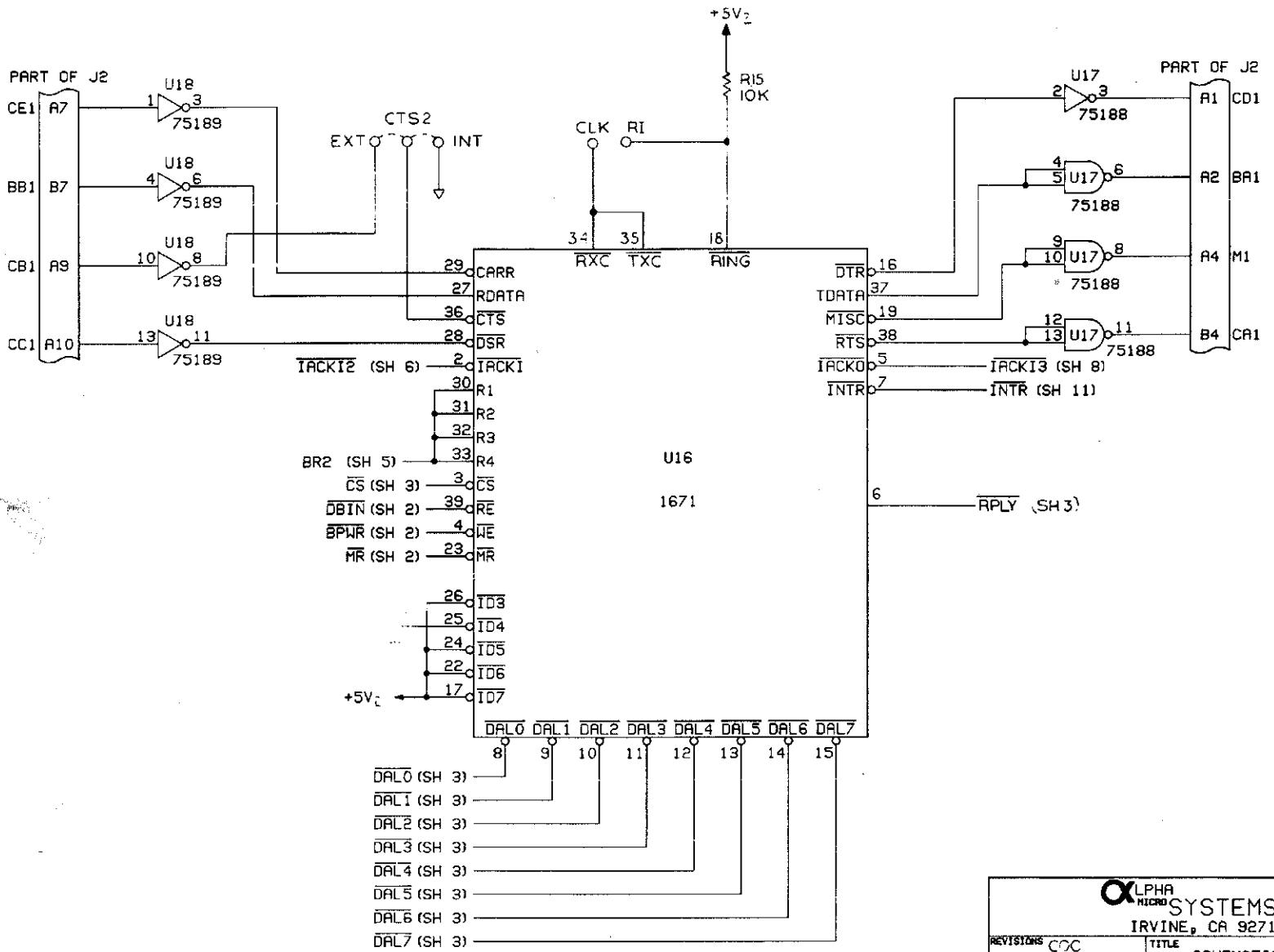
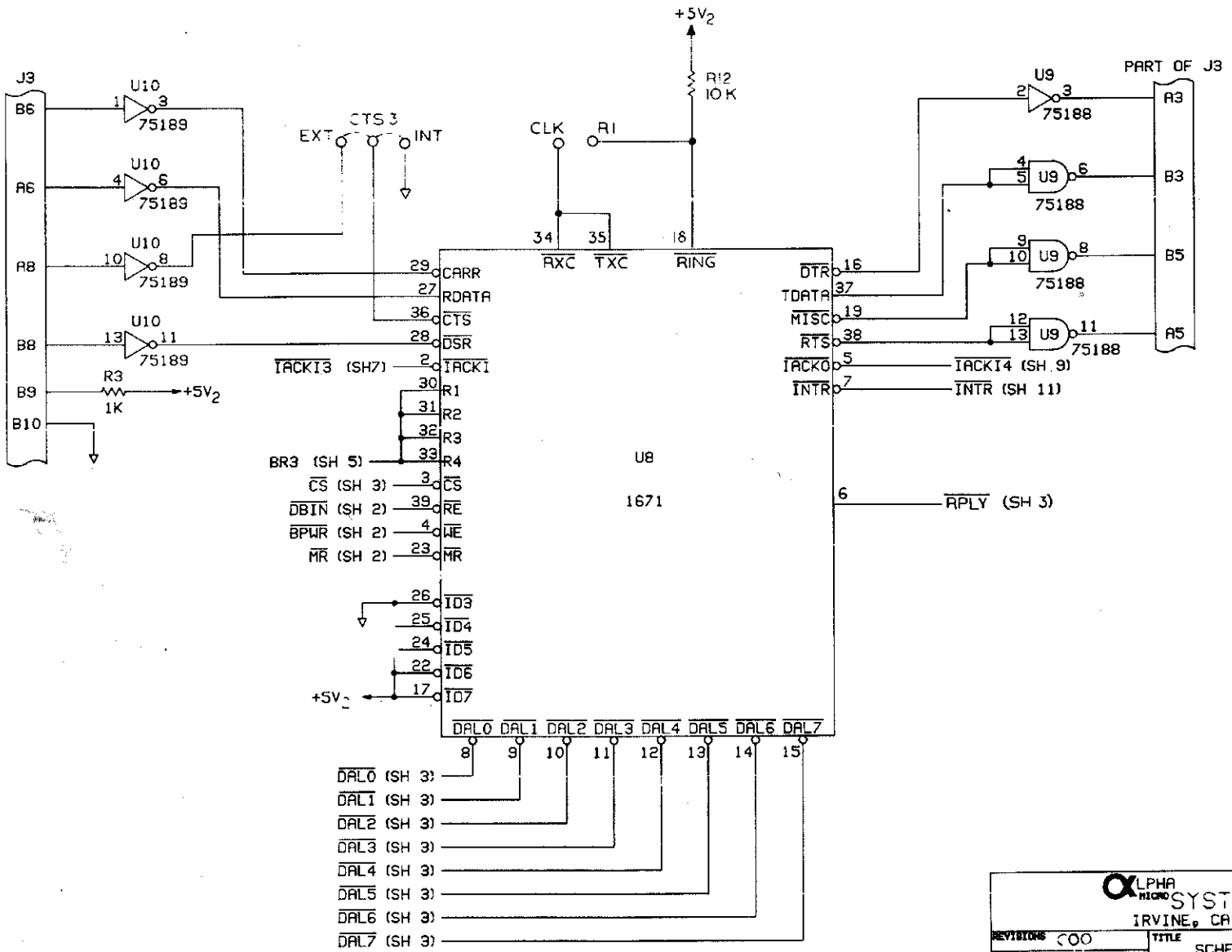
DRAWN / CHECKED / APPROVED	SHEET NO. 6 OF 11 DWL-00300-00

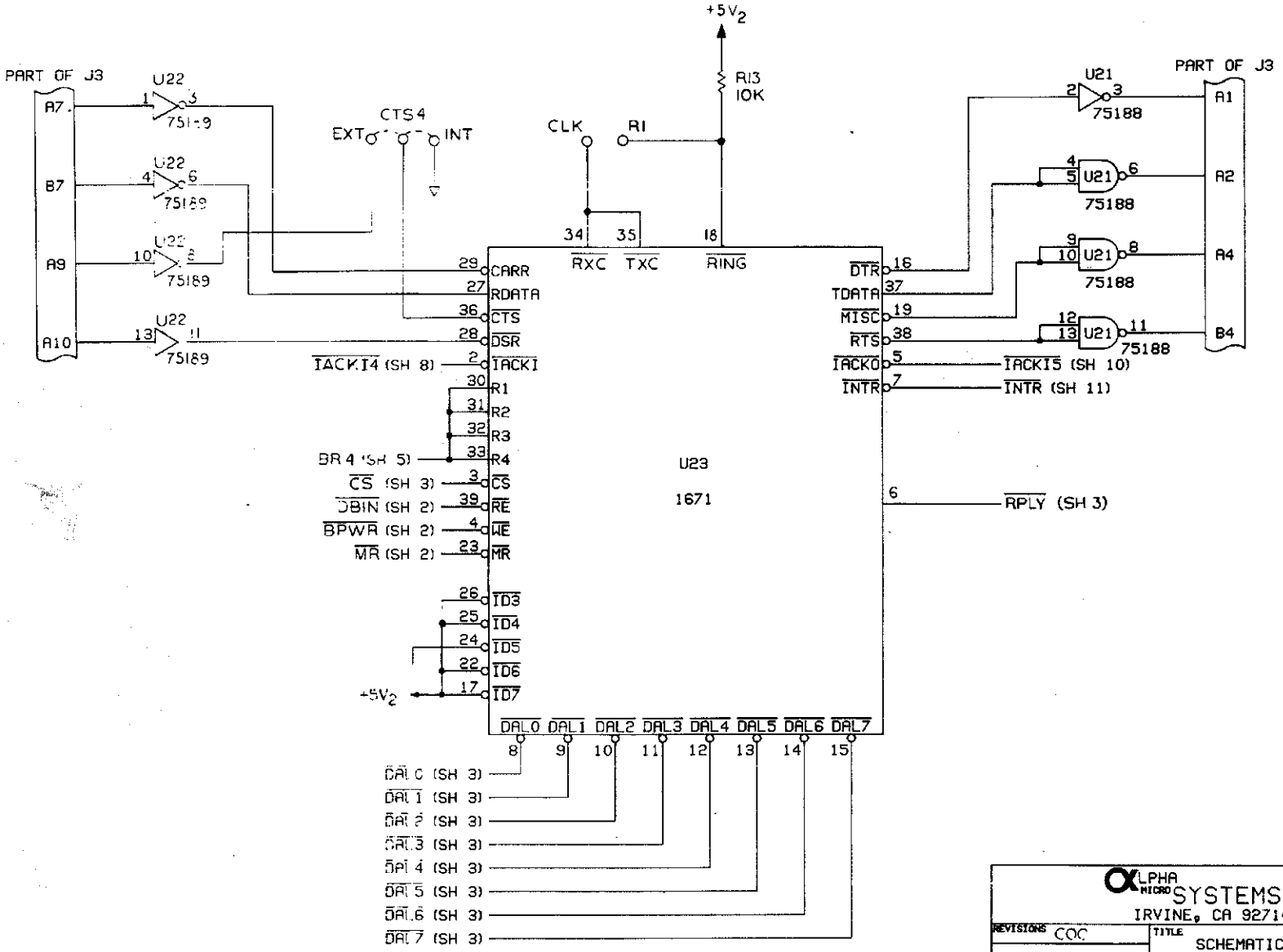


ALPHA MICRO SYSTEMS IRVINE, CA 92714	
REVISIONS COC	TITLE SCHEMATIC, AM-300 6 PORT SERIAL I/O
DRAWN / CHECKED / APPROVED	SHEET NO. 7 OF 11
	DRAWING NO. DWG-00300-

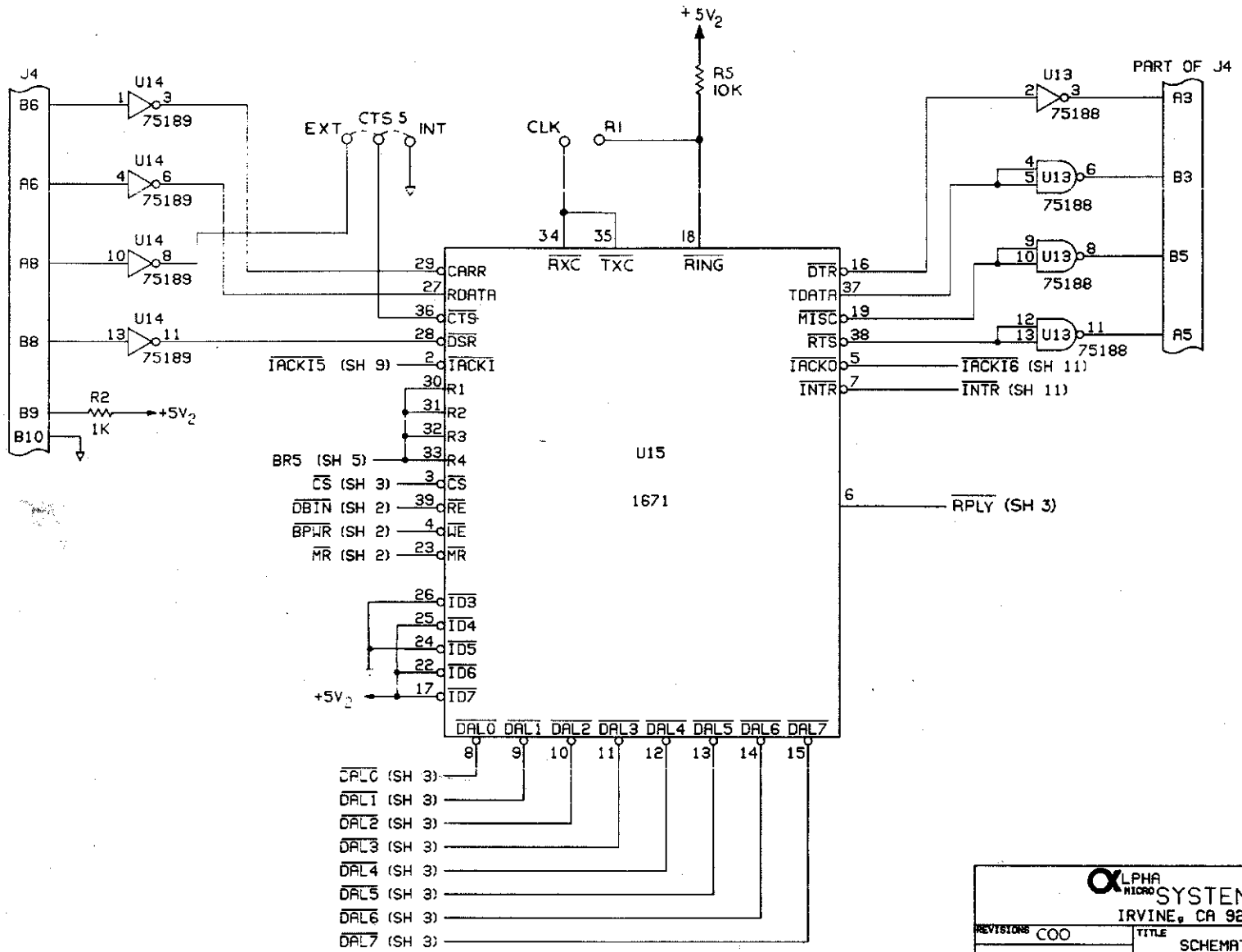


ALPHA MICRO SYSTEMS
IRVINE, CA 92714

REVISIONS 000	TITLE SCHEMATIC, AM-300 6 PORT SERIAL I/O
DRAWN / CHECKED / APPROVED	SHEET NO. 8 OF 11 DWG NO. DWL-00300-00



ALPHA MICRO SYSTEMS IRVINE, CA 92714	
REVISIONS COC	TITLE SCHEMATIC, AM-300 6 PORT SERIAL I/O
DRAWN / CHECKED / APPROVED	SHEET NO. 9 OF 11
	DRAWING NO. DWL-003[illegible]-00



ALPHA MICRO SYSTEMS IRVINE, CA 92714	
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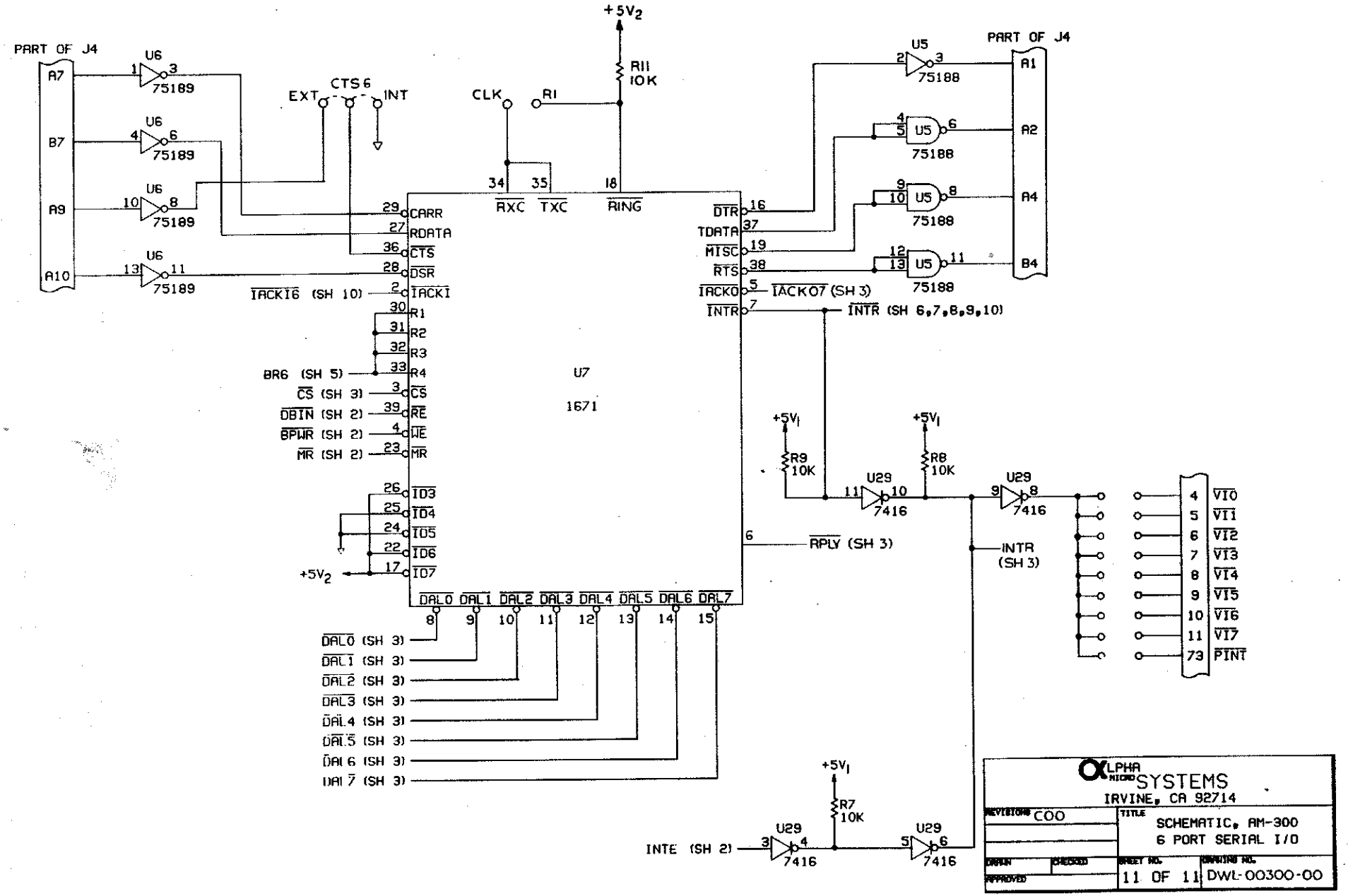
DRAWN / CHECKED / APPROVED	SHEET NO. 10 OF 11
	DRAWING NO. DWG-00300-00


PART OF J4
A7
B7
A9
A10
U6
75189
EXT
CTS 6
INT
CLK
RI
+5V2
RII
10K
34
35
18
RXC
TXC
RING
U7
1671
29 CARR
27 RDATA
36 CTS
28 DSR
2 IACKI
IACK16 (SH 10)
30 R1
31 R2
32 R3
33 R4
BR6 (SH 5)
3 CS
CS (SH 3)
39 RE
DBIN (SH 2)
4 WE
BPWR (SH 2)
23 MR
MR (SH 2)
26 ID3
25 ID4
24 ID5
22 ID6
17 ID7
+5V2
DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7
8 9 10 11 12 13 14 15
DAL0 (SH 3)
DAL1 (SH 3)
DAL2 (SH 3)
DAL3 (SH 3)
DAL4 (SH 3)
DAL5 (SH 3)
DAL6 (SH 3)
DAL7 (SH 3)
16 DTR
37 TDATA
19 MISC
38 RTS
5 IACKO
IACK07 (SH 3)
7 INTR
INTR (SH 6,7,8,9,10)
6 RPLY (SH 3)
U5
75188
PART OF J4
A1
A2
A4
B4
+5V1
R9
10K
R8
10K
U29
7416
INTR
(SH 3)
4 VI0
5 VI1
6 VI2
7 VI3
8 VI4
9 VI5
10 VI6
11 VI7
73 PINT
INTE (SH 2)
R7
10K
ALPHA MICRO SYSTEMS
IRVINE, CA 92714
REVISIONS COO
TITLE
SCHEMATIC, AM-300
6 PORT SERIAL I/O
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DRAWING NO.
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RUNNING MORE THAN ONE AM-300 I/O CONTROLLER

The AM-300 Serial I/O Controller in an AM-100 system is applicable to Alpha Microsystems' AM-300 Rev.A&B and is fairly straightforward. But,it is important that each step be followed exactly in order for the procedure to work properly.

The hardware and software portions will be covered separately with examples given in each area.

HARDWARE CHANGES

Two hardware items must be changed. First the board I/O address must be changed, and second, the board interrupt level must be changed.

	Suggested I/O Address	Interrupt Level
1st AM-300 board	F8(normal)	3
2nd AM-300 board	E8	6
3rd AM-300 board	D8	7

The suggested interrupt levels are only a guide. The interrupt level you use must not be used by any other board on the system If you have an AM-100 based system, be sure to enable the same interrupt level on the AM-100 board.

As an example, a second AM-300 board will be set up using I/O address E8 and interrupt level 6. See Figure 1 below. On the AM-300 board, find the ADDRESS HEADER and the INTERRUPT lines.

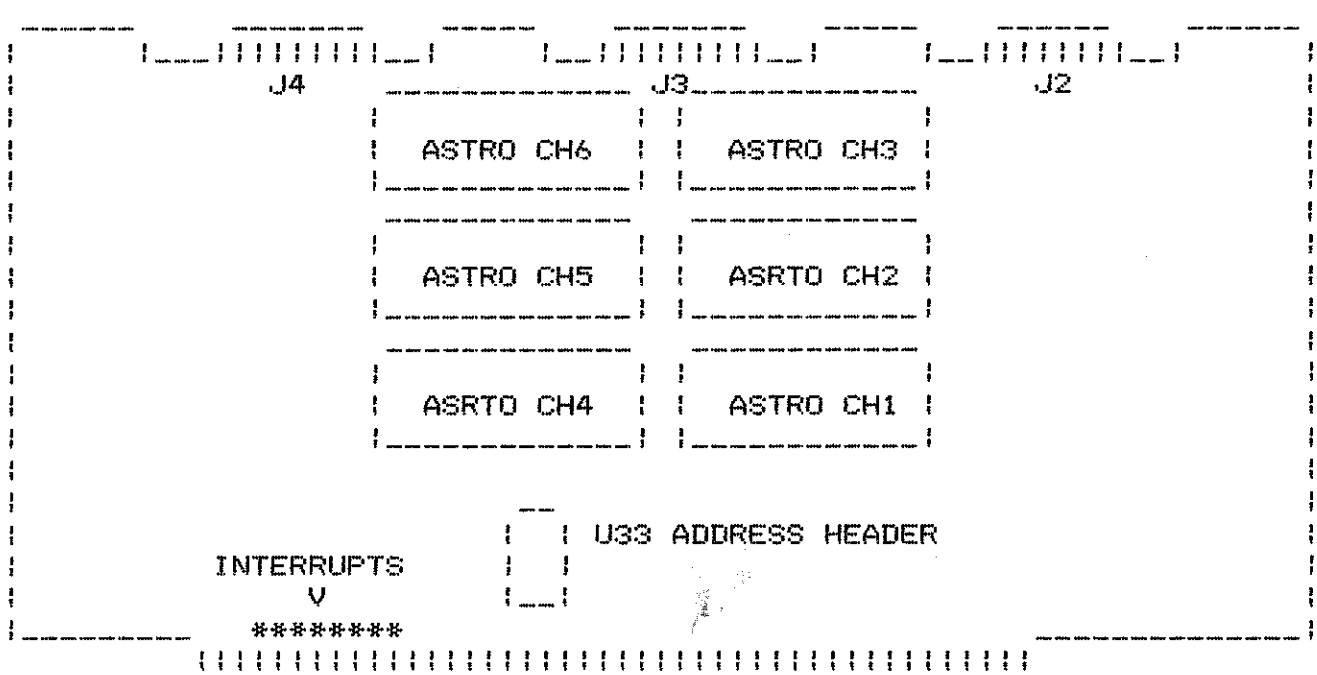
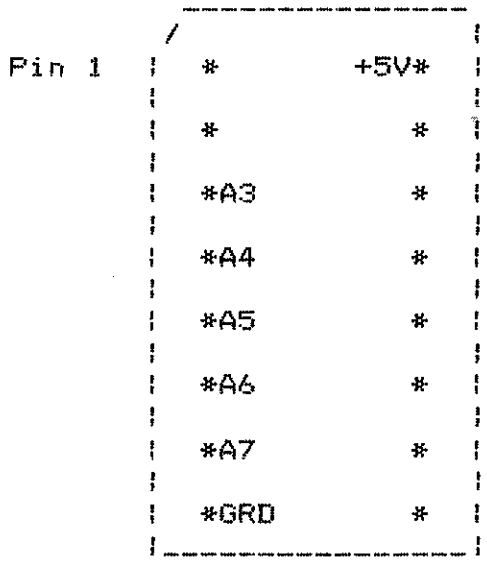


FIGURE 1 AM-300 BOARD

The address header is normally set up for address F8. This header will be changed to E8. Figure 2 shows the address header and the pin identification. Pins 3 thru 7 are the address lines A3 thru A7. Pin 16 is + 5 volts and pin 8 is ground. The address lines are tied to +5 volts to make the address lines "1" level or to ground for a "0" level.



An address of F8 will have A3,A4,A5,A6 and A7 jumpered to +5 volts.

An address of E8 will have A3,A5,A6 and A7 jumpered to +5 volts and A4 jumpered to ground.

An address of D8 will have A3,A4,A6 and A7 jumpered to +5 volts and A5 jumpered to ground.

FIGURE 2
ADDRESS HEADER

After the address has been changed to E8, the interrupt level must be changed to "6" for this example. See Figure 3 for interrupt identification.

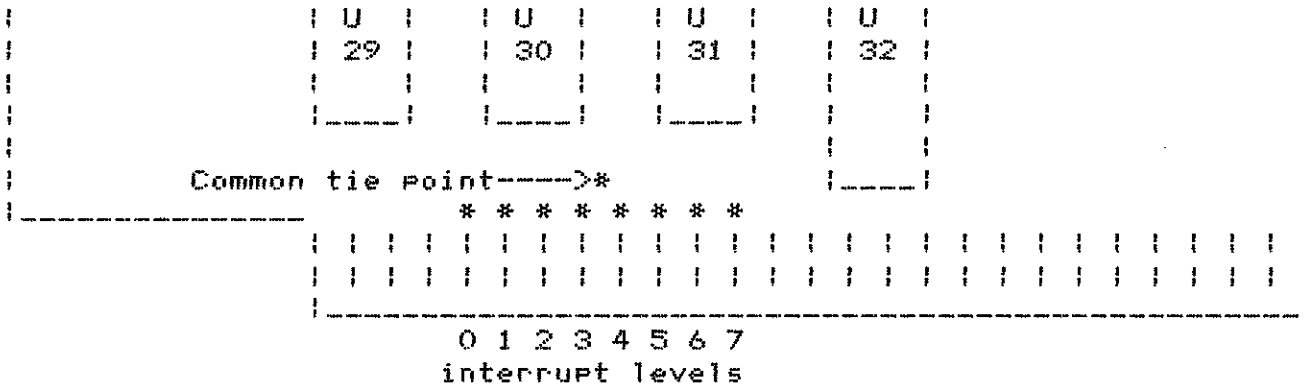


FIGURE 3 AM-300 BOARD (Lower left corner)

To change the interrupt, level the jumper (foil etch on older boards) must be installed from the common tie point to the correct interrupt pad. In this example to the pad labeled "VI 6".

Note: The interrupts are labeled on the board. The labeling may look like "V10 to V17". Should be "VI0 to VI7".

SOFTWARE CHANGES

Now, a new driver must be generated for the second AM-300 board. The source for the AM-300 driver is located in PPN [10,2], file "AM300.MAC". Copy this file to "AM301.MAC". Using the "VUE" or "EDIT" program change two lines in the AM301.MAC file. In the beginning of the file are the two lines which must be changed to reflect the hardware changes.

The first; find the line that reads:

```
AMX=177770              ;BOARD ADDRESS
```

If the board address has been changed to "E8" on the header; change this line to read:

```
AMX=177750              ;BOARD ADDRESS
```

If the board address has been changed to "D8" on the header; change this line to read:

```
AMX=177730              ;BOARD ADDRESS
```

Note: The octal address is calculated by adding the address of the board to 177400 octal.

Second; find the line that reads:

```
AMV=3                   ;INTERRUPT VECTOR LEVEL
```

Change this line to reflect the same interruupt level that was set up on the board. For interrupt level "6" this line should read:

```
AMV=6                   ;INTERRUPT VECTOR LEVEL
```

After the two changes have been made, the file must now be reassembled using the MACRO program. To MACRO the program, type the following:

```
MACRO AM301.MAC [RETURN]
```

The MACRO program will generate two new files in PPN 10,2. They are:

```
AM301.OBJ
AM301.PRG
```

Erase the AM301.OBJ file, it is not needed. The AM301.PRG file must be renamed to AM301.IDV and transferred to area 1,6 on the system disk where the drivers must reside.

When assigning terminals to the second AM-300 through the TRMDEF statement in the SYSTEM.INI file, use the AM301.IDV in the same manner as the AM300.IDV. AM301 must be specified for the interface driver rather than AM300 in order for the system to recognize the correct driver.

Test the driver by creating a TEST.INI and then MONTST the system using the TEST.INI file.

Table 4-3. (Con't) ASTRO Signal List

SIGNAL	PIN	FUNCTION
$\overline{\text{RPLY}}$ $\overline{\text{REPLY}}$	6	This open drain output is made low when the ASTRO is responding to being selected by an address on the DAL during read or write operations or in affirming that it is the interrupting source during interrupt polling.
R1-R4 CLOCK RATES	30-33	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by the Control Register.
TDATA (BA) TRANSMITTED DATA	37	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.
RDATA (BB) RECEIVED DATA	27	This input receives serial data into the ASTRO.

Table 4-3. (Con't) ASTRO Signal List

SIGNAL	PIN	FUNCTION
$\overline{\text{RTS}}$ ($\overline{\text{CA}}$) REQUEST TO SEND	38	This output is enabled by the Control Register and remains in a low state during transmitted data from the ASTRO.
$\overline{\text{CTS}}$ ($\overline{\text{CB}}$) CLEAR TO SEND	36	This input, when low, enables the transmitter section of the ASTRO.
$\overline{\text{DSR}}$ ($\overline{\text{CC}}$) DATA SET READY	28	This input generates an interrupt when going On or Off while the Data Terminal Ready signal is On. It appears as a bit in the Status Register.
$\overline{\text{DTR}}$ ($\overline{\text{CD}}$) DATA TERMINAL READY	16	This output is generated by a bit in the Control Register and indicates Controller readiness.
$\overline{\text{RING}}$ ($\overline{\text{CE}}$) RING INDICATOR	18	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the "Off" condition.

Table 4-3. (Con't) ASTRO Signal List

SIGNAL	PIN	FUNCTION
$\overline{\text{CARR}}$ ($\overline{\text{CF}}$) CARRIER DETECTOR	29	This input from the Data Set generates an interrupt when going On or Off if Data Terminal Ready is On. It appears as a bit in the Status Register.
$\overline{\text{IXTC}}$ ($\overline{\text{DB}}$) TRANSMITTER TIMING	35	This input is the Transmitter 1X Data Rate Clock. Its use is selected by the Control Register. The transmitted data changes on the negative transition of this signal.
$\overline{\text{IXRC}}$ ($\overline{\text{DD}}$) RECEIVER TIMING	34	This input is the Receiver 1X Data Rate Clock. Its use is selected by the Control Register. The Received Data is sampled by the ASTRO on the positive transition of this signal.
$\overline{\text{MISC}}$ MISCELLANEOUS	19	This output is controlled by a bit in the Control Register and is used as an extra programmable signal.

Syn Register. This 8-bit register is loaded from the DAL lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the DAL lines. It must be loaded with logic zeroes in all unused high-order bits.

DLE Register. This 8-bit register is loaded from the DAL lines by a Write operation and holds the "DLE" character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

Transmitter Holding Register. This 8-bit parallel buffer register holds parallel transmitted data transferred from the DAL lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

Transmitter Register. This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted data output.

Control Registers. There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL lines by a Write operation or read onto the DAL lines by a Read operation. The registers are cleared by a Master Reset.

Status Register. This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL lines by a Read operation.

Data Access Lines. The DAL is an 8-bit bi-directional bus port over which all address, data, control, and status transfers occur. In addition to transferring data and control words, the DAL lines also transfer information related to addressing of the device, reading and writing requests, and interrupting information.

4.2.2.2 Asynchronous Mode Operation.

Framing of asynchronous characters is provided by a Start bit (logic low) at the beginning of a character and a Stop bit (logic high) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character bit. If this bit is a logic high, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit is a logic low, the Framing Error Status flag is set and the Receiver assumes this bit to the Start bit of the next character. Character assembly continues from this point if the input is still a logic low when sampled at the theoretical center of the assumed Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeros is assembled along with a zero in the Stop bit location, the first received logic high is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character least significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the Transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Mark (logic high) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for a 1.5-, or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

4.2.2.3 Synchronous Mode Operation.

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters is transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transport mode of operation.

4.2.2.4 Detailed Operation.

Receiver. The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X Clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the mark-to-space transition of the Received Data Start bit and defines, through clock counts, the center of each received data bit within +0 , -3 at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all mark-to-space transitions of the Received Data inputs when using 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every mark-to-space data transition by setting bit 4 of Control Register 1 to a logic high, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeros. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Register.

Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE register are not loaded into the Receiver Holding Register, and the DR interrupt is not generated, if bit 3 of Control Register 2 (CR23=SYN Strip) or bit 4 of Control Register 1 (CR14=DLE Strip) are set respectively, the SYN-DET and DLE-DET status bits are set with the next non SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received, only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter. Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request to Send bit is set to a logic one in the Control Register and the Clear To Send input is a logic low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (bits 5 = Force DLE and 6 = TX Transparent of Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the Transmitter Holding Register to insure forcing the DLE character prior to transmission of the data character.

The Transmitter Register output passes through a flip-flop which delays the output by the one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate.

This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character, the Transmitter enters an idle state. During this idle time a logic high will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16=0). In the Synchronous Transmit Transparent mode (enabled by bit 6 of Control Register 1=Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the CTS goes high, the transmitted data output will go high.

When the Transmit parity is enabled, the selected odd or even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

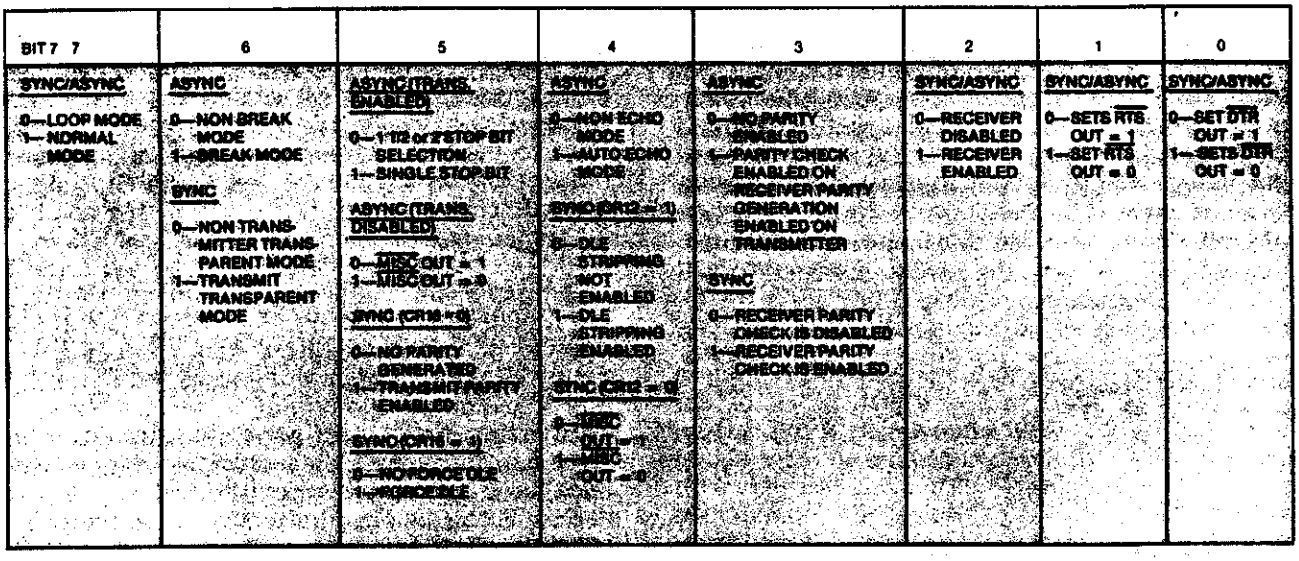


Figure 4-6. Control Register 1

4.2.2.5 Device Programming.

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip. The Control Register contents are shown in Figures 4-6 and 4-7.

Control Register 1. This is an 8-bit control register that holds device programming signals.

Bit 7. A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the TD pin held in a Mark condition and the input to the RD pin disregarded.

b. With a 1X clock selected, the Transmitter clock also becomes the Receive Clock.

c. The Data Terminal Ready (DTR) Control bit is connected to the Data Set Ready (DSR) input, with the DTR output pin held in an Off condition (logic high), and the DSR input pin is disregarded.

d. The Request to Send Control bit is connected to the Clear To Send (CTS) and Carrier Detector inputs, with the RTS output pin held in an Off condition (logic high), and the CTS and Carrier Detector input pins are disregarded.

e. The Miscellaneous pin is held in an Off (logic high) condition.

A logic 1 on bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Bit 6. In the Asynchronous mode a logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Holding Register.

In the Synchronous mode a logic 1 sets the Transmitter in a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE can be forced ahead of any character in the Transmitter Holding Register when CR15 is a logic one in the sync mode.

Bit 5. In the Asynchronous mode a logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes 2-Stop bit transmission for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

In the Synchronous mode a logic 1 combined with a logic 0 on Bit 6 of Control Register 1 enables Transmit parity; if CR15=0 or CR16=1 no parity is generated.

When set to a logic 1 with bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Holding Register as part of the Transmit Transparent mode.

Bit 4. In the Asynchronous mode a logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmit Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeros (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

In the Synchronous mode a logic 1, with the Receiver enabled, does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Holding Register; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver a logic 1 on this bit also causes the Receiver timing to synchronize on mark-to-space transitions.

Bit 3. In the Asynchronous mode a logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

In the Synchronous mode a logic 1 bit enables check of parity on received characters only. Note: Transmitter parity enable is controlled by CR15.

Bit 2. A logic 1 enables the ASTRO to receive data into the Receiver Holding Register, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 1. Controls the Request To Send output on pin 38 to control the CA circuit of the Data Set. The RTS output is inverted from the state of CR11. A logic 1 combined with a low logic Clear To Send input enables the Transmitter and allows THRE interrupts to be generated. A logic 0 disables the Transmitter and turns off the external Request To Send signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request To Send output may be used for other functions such as "Make Busy" on 103 Data Sets.

Bit 0. Controls the Data Terminal Ready output on pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The DTR output is inverted from the state of CR10.

Control Register 2. Control Register 2, unlike Control Register 1, cannot be changed at any given time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state. Control Register 2 contents are shown in Figure 4-7.

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 SYNC (CR14 = 0) 0—NO SYN STRIP 1—SYN STRIP SYNC (CR14 = 1) 0—NO DLE-SYN STRIP 1—DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - IX CLOCK 001 - RATE 1 CLOCK 010 - RATE 2 CLOCK 011 - RATE 3 CLOCK 100 - RATE 4 CLOCK 101 - RATE 4 CLOCK ÷ 2 110 - RATE 4 CLOCK ÷ 4 111 - RATE 4 CLOCK ÷ 8

Figure 4-7. Control Register 2

Bits 7-6. These bits select the character length as follows:

Bits 7-6	Character Length
00	8 bits
01	7 bits
10	6 bits
11	5 bits

When parity is enabled it must be considered as a bit when making character length selection, i.e., 5 character bits plus parity = 6 bits.

Bit 5. A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bit 4. A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 3. In the Asynchronous mode a logic 0 selects the rate 1-32X clock input (pin 30) as the Receiver Clock rate and a logic 1 selects the same clock rate for the Receiver as selected by bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by bits 2-0.

In the Synchronous mode a logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip CR14 is a logic 1, or all SYN characters in the Non-transparent mode to be stripped out and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as it is transferred to the Receiver Holding Register.

Bits 2-0. These bits select the Transmit and Receive clocks. The Input Clock to the Rate 4 pin may be divided down to form the 32X clock from a multiple clock as shown on the next page.

Bits 2-0	Clock
000	1X clock for Transmit and Receive (pins 35 and 34 respectively)
001	32X clock - Rate 1 input (pin 30)
010	32X clock - Rate 2 input (pin 31)
011	32X clock - Rate 3 input (pin 32)
100	32X clock - Rate 4 input 1 (pin 33)
101	32X clock - Rate 4 input 2 (pin 33)
110	32X clock - Rate 4 input 4 (pin 33)
111	32X clock - Rate 4 input 8 (pin 33)

Status Register. The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set. The Status word is shown in Figure 4-8, and defined below.

BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE	• DATA SET READY	• CARRIER DETECTOR	• FRAMING ERROR • SYN DETECT	• DLE DETECT • PARITY ERROR	• OVERRUN ERROR	• DATA RECEIVED	• TRANSMITTER HOLDING REGISTER EMPTY

Figure 4-8. Status Register

Bit 7. This bit is set to a logic 1 whenever there is a change in state of the Data Set Ready or Carrier Detector inputs while Data Terminal Ready (bit 0 of Control Register 1) is a logic 1 or the Ring Indicator is turned on, with DTR a logic 0. This bit is cleared when the Status Register is read onto the Data Access Lines.

Bit 6. This bit is the logic complement of the Data Set Ready input on pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 5. This bit is the logic complement of the Carrier Detector input on pin 29.

Bit 4. In the Asynchronous mode a logic 1 indicates that received data contained a log 0 bit after the last data bit of the character in the Stop bit slot, while the Receiver was enabled. This indicates a Framing error. This bit is set to a logic 0 if the proper logic 1 condition for the Stop bit was detected.

In the Synchronous mode a logic 1 indicates that the contents of the Receiver Register matched the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character. In both modes the bit is cleared when the Receiver is disabled.

Bit 3. When the DLE Strip is enabled (bit 4 of Control Register 1) the Receiver parity check is disabled and this bit is set to a logic 1 if the previous character to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled this bit is set to a logic 1 when the Receiver is enabled, and the last received character has a parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in either of the above modes when the Receiver is disabled.

Bit 2. A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Holding Register has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Holding Register. This bit is cleared when no Overrun condition is detected, i.e., the next character transfer time or when the Receiver is disabled.

Bit 1. A logic 1 indicates that the Receiver Holding Register is loaded from the Receiver Register, if the Receiver is enabled. It is cleared to a logic 0 when the Receiver Holding Register is read onto the Data Access Lines, or the Receiver is disabled.

Bit 0. A logic 1 indicates that the Transmitter Holding Register does not contain a character while the Transmitter is enabled. It is set to a logic 1 when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the Transmitter is disabled.

4.2.2.6 Input/Output Operations.

All Data, Control, and Status words are transferred over the Data Access Lines (DAL0-DAL7). Additional input lines provide controls for addressing a particular unit, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or Input takes data from the ASTRO and places it on the DAL lines, while a Write or Output places data from the DAL lines into the ASTRO.

Read. A Read operation is initiated by the placement of an eight-bit address on the DAL by the Controller. When the Chip Select signal goes to a logic low state, the ASTRO compares bits 7-3 of the DAL with its hard-wired ID code (pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its RPLY line low to acknowledge its readiness to transfer data.

Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Holding Register

When the Read Enable (RE) line is set to a logic low condition by the Controller, the ASTRO gates the contents of the addressed register onto the DAL. The Read operation terminates and the device becomes unselected when both the Chip Select and Read Enable return to a logic high condition. Reading of the Receiver Holding Register clears the DR Status bit. Bit 0 must be a logic low in read or write operations.

Write. A Write operation is initiated by the placement of an eight-bit address on the DAL by the Controller. The ASTRO compares bits 7-3 of the DAL with its ID code when the Chip Select input goes to a logic low state. If a Match condition exists the device is selected and makes its RPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Holding Register

When the Write Enable (WE) line is set to a logic low condition by the Controller, the ASTRO gates the data from the DAL into the addressed register. If data is written into the Transmitter Holding Register, the THRE Status bit is cleared to a logic zero. The 100 address loads both the SYN and DLE registers. After writing into the SYN register, the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses resets this condition such that the next 100 will address the SYN register.

Interrupts. The following conditions generate interrupts:

1. Data Received (DR) - Indicates transfer of a new character to the Receiver Holding Register while the Receiver is enabled.

2. Transmitter Holding Register Empty (THRE) - Indicates that the THR register is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty THR, or after the character is transferred to the Transmitter Register making the THR empty.

3. Carrier On - Indicates Carrier Detector input goes low when DTR is on.

4. Carrier Off - Indicates Carrier Detector input goes high when DTR is on.

5. DSR On - Indicates the Data Set Ready input goes low when DTR is on.

6. DSR Off - Indicates the Data Set Ready input goes high when DTR is on.

7. Ring On - Indicates the Ring Indicator input goes low when DTR is off.

Each time an interrupt condition exists the INTR output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the interrupt request by setting the Chip Select (CS) and the Interrupt Acknowledge Input (IACKI) to the ASTRO to a low state. On this transition all non-interrupting devices receiving the IACKI set their Interrupt Acknowledge Output (IACKO) low, enabling lower priority daisy-chained devices to respond to the interrupt request. The highest priority device that is interrupting will then set its RPLY low. This device places its ID code on bit positions 7-3 of the DAL when a low RE signal is received. In addition bit 2 is set to a logic one if any of the interrupt numbers 1 and 3-7 above occurred, and remains a logic low if the THRE has caused the interrupt.

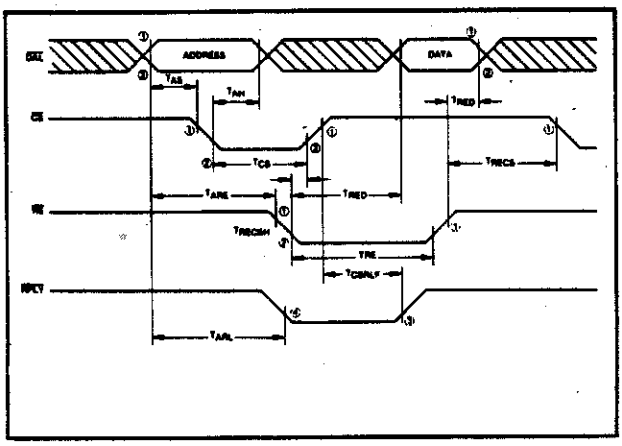
To reset the interrupt condition (INTR) Chip Select (CS) an IACKI must be received by the ASTRO. A setup time must exist between CS and the RE or WE signals to allow chip selection prior to read/write operations and deselection control through the latter signals. The data is removed from the DAL when the RE signal returns to the logic high state.

4.2.2.7 Timing.

Timing characteristics for Read cycles, Write cycles, and Interrupt cycles are shown in Table 4-4 and Figures 4-9, 4-10 and 4-11. Flow diagrams for processing are contained in Figures 4-12 and 4-13.

TABLE 4-4. Signal Timing

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{AS}	Address Set-Up Time	0			ns	
t_{ah}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Delay	0		250	ns	R_L = 2.7 KΩ



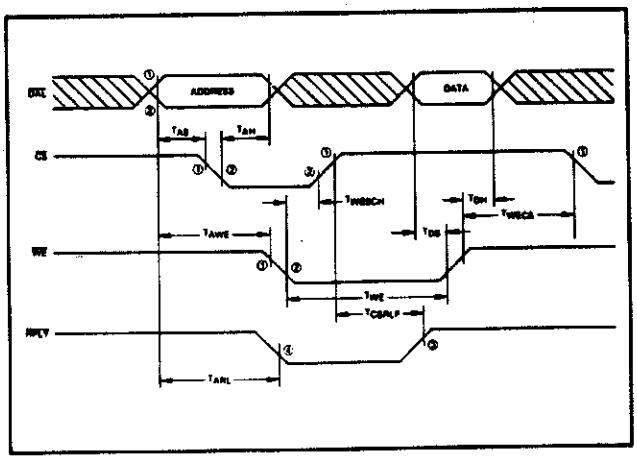
1 = VIH(min) = 2.4V
2 = VIL(max) = 0.8V
3 = VOH(min) = 2.8V
4 = VOL(max) = 0.4V

NOTE 1: ID DECODE is the major factor in TARE and TARL timing.

NOTE 2: If changing the Control Registers while processing data the WE pulse width must be contained within the Data Valid envelope to insure correct data processing.

T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{RED}	$\overline{RE}$ to Data Out Delay			180	ns	C_L = 20 pf
T_{RE}	$\overline{RE}$ Width	200		1000	ns	

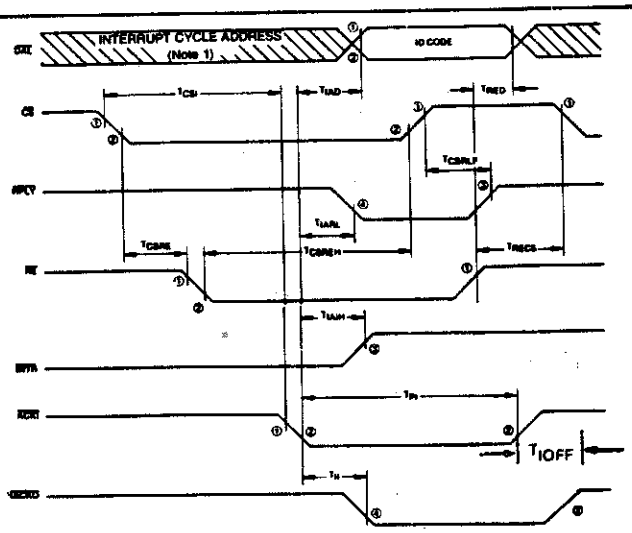
Figure 4-9. Read Timing



1 = VIH(min) = 2.4V
2 = VIL(max) = 0.8V
3 = VOH(min) = 2.8V
4 = VOL(max) = 0.4V

T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
TWECS	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	

Figure 4-10. Write Timing



Note 1: DAL0 must be a logic high during CS to form an Interrupt Cycle Address during Daisy Chain Interrupt Response.

1 = VIH(min) = 2.4V
2 = VIL(max) = 0.8V
3 = VOH(min) = 0.4V
4 = VOL(max) = 0.4V

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{RED}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay			180	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{IAIH}	$\overline{IACKI}$ ON to $\overline{INTR}$ OFF Delay			300	ns	
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{IOFF}	$\overline{IACKO}$ OFF Delay From $\overline{CS}$ OFF, RE OFF, or $\overline{IACKI}$ HIGH.			250	ns	See Note 2.

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.
Note 2: $\overline{IACKO}$ goes false after the last one of the following three signals go false: $\overline{CS}$, $\overline{RE}$ and $\overline{IACKI}$. $T_{:OFF}$ is measured from the last signal going false.

Figure 4-11. Interrupt Timing

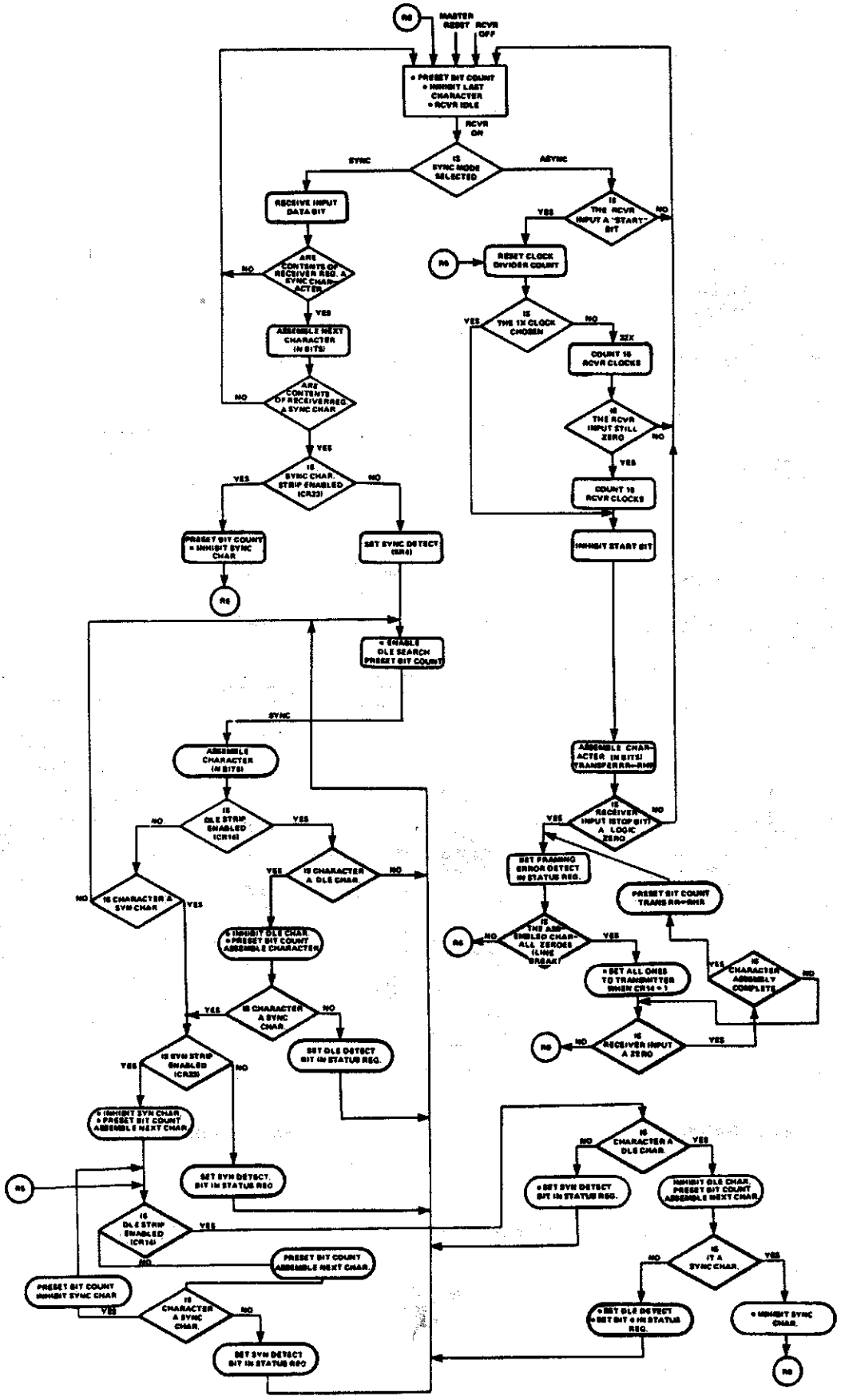


Figure 4-12. Receiver Section Flow Diagram

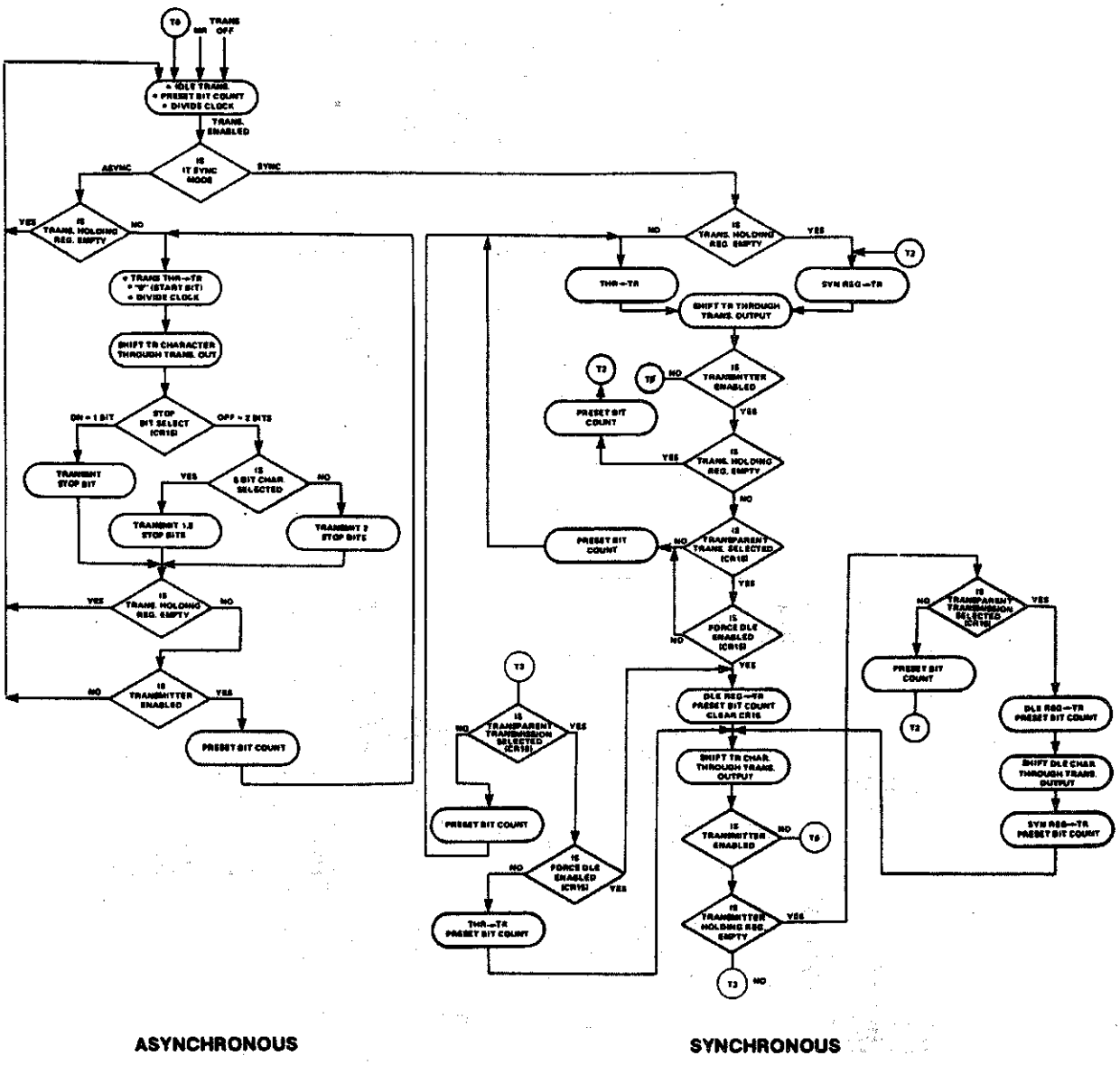
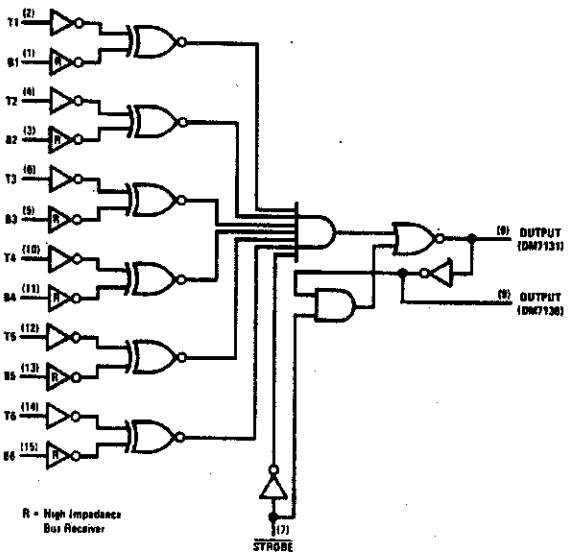


Figure 4-13. Transmitter Section Flow Diagram

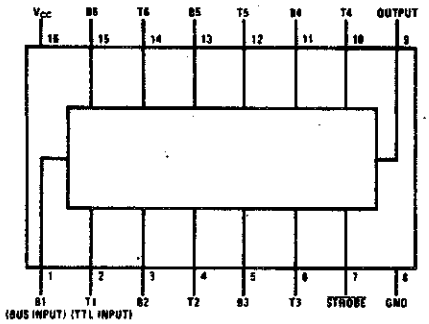
4.2.3 Bus Comparator (U34).

This device compares two binary words of two to six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are TTL inputs, whereas inputs of the second word are high impedance receivers driven by a terminated data bus. The output has a latch that is strobe controlled. The transfer of information to the output occurs when the STROBE input goes from a logical 1 to a logical 0 state. Inputs may be changed while the STROBE is at the logical 1 level, without affecting the state of the output. For logic and connections see Figure 4-14.

Logic Diagram



Connection Diagram



Truth Table

CONDITION	$\overline{\text{STROBE}}$	OUTPUT	
		DM71/8131	DM71/8136
T = B, T ≠ B	H	Q_{N-1} *	Q_{N-1} *
T = B	L	L	H
T ≠ B	L	H	L

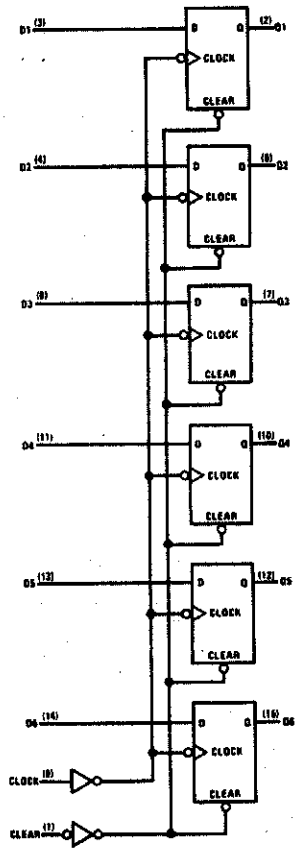
*Latched in previous state

Figure 4-14. Bus Comparator Connections

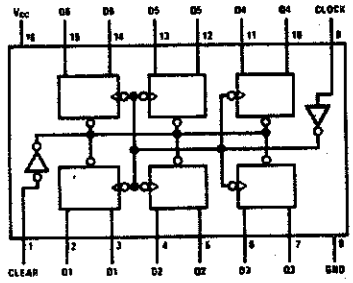
4.2.4 D Flip-Flops With Clear (U28).

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For logic and connections see Figure 4-15.

Logic Diagram



Connection Diagram



Truth Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

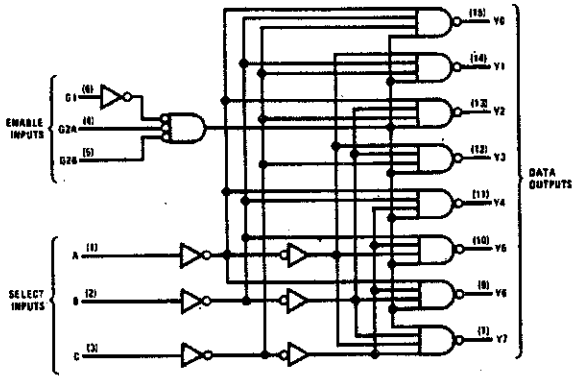
H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = 175, LS175, and S175 only

Figure 4-15. D Flip-Flop Connections

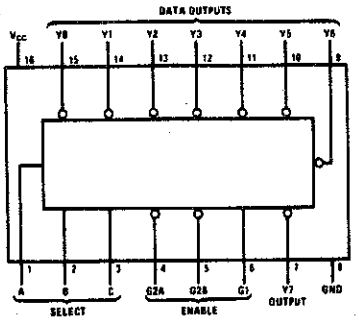
4.2.5 Decoder (U20).

These are Schottky-clamped circuits designed for memory-decoding or data-routing applications requiring very short propagation delay times. This DIP decodes one of eight lines, based on the conditions at the three binary select inputs and the three enable inputs. For logic and connections see Figure 4-16.

Logic Diagram



Connection Diagram



Truth Table

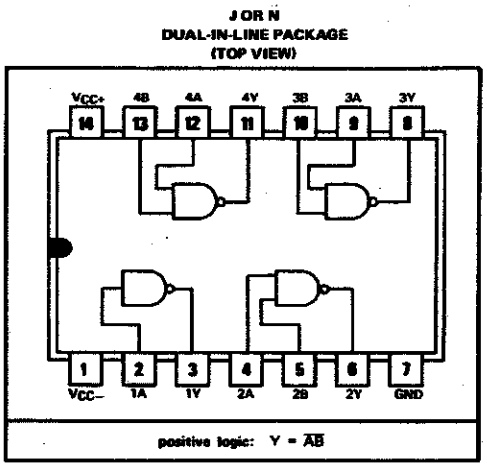
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Figure 4-16. Decoder Connections

4.2.6 Line Drivers (U5, U9, U13, U17, U21, U25).

This device is a monolithic, quadruple line driver that interfaces data terminal equipment with data communications equipment. Operation is in conformance with EIA standard RS-232C. For logic and connections see Figure 4-17.

Logic/Connection Diagram



Truth Table

FUNCTION TABLE

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

Schematic

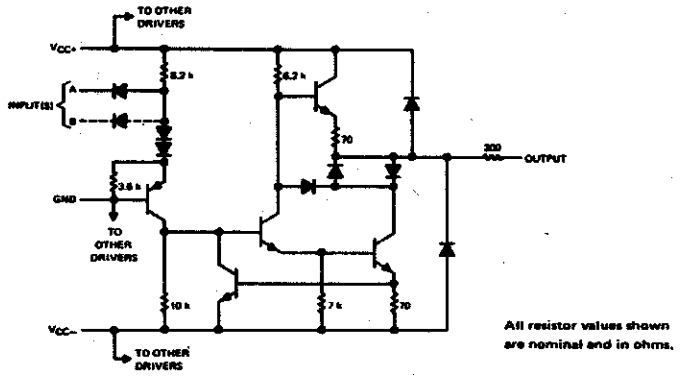
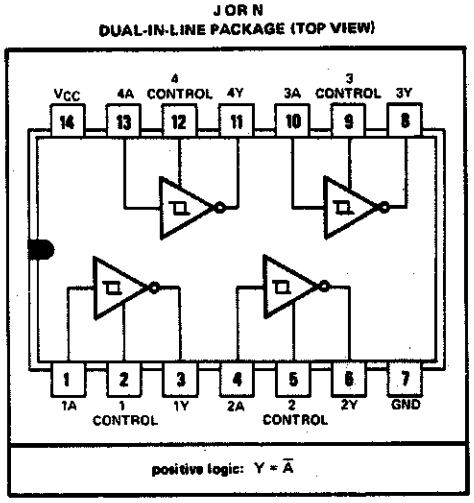


Figure 4-17. Line Driver Connections

4.2.7 Line Receivers (U6, U10, U14, U18, U22, U26).

This device is a monolithic, quadruple line receiver that satisfies the requirements of the standard interface between data terminal equipment and data communications equipment. Operation is in conformance with EIA standard RS-232C. Logic and connections are shown in Figure 4-18.

Logic/Connection Diagram



Schematic

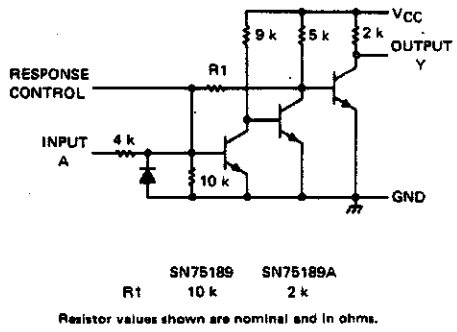
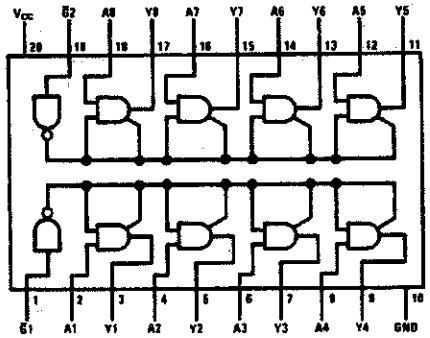


Figure 4-18. Line Receiver Connections

4.2.8 Tri-State Buffers (U12, U32, U37, U39, U40).

This device provides eight, two-input buffers in each package that employs low power Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state, while the other input passes the data through the buffer. The outputs are placed in the tri-state condition by applying a high logic level to the enable pins. For logic and connections see Figure 4-19.

Logic/Connection Diagram



Truth Table

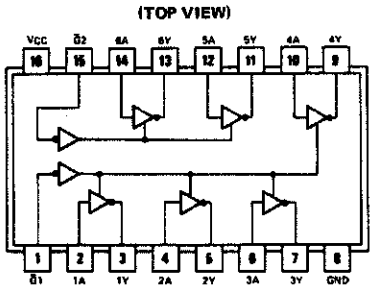
INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Figure 4-19. Tri-State Buffer Connections

4.2.9 Hex Tri-State Buffers (U36, U38).

These devices provide six, two-input buffers in each package. One of the two inputs to each buffer is used as a control line to gate the output onto the high impedance state, while the other input passes the data through the buffer. The outputs are placed in the tri-state condition by applying a high logic level to the control pins. For logic and connections see Figure 4-20.

Connection Diagram



Truth Table

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

H = high level, L = low level,
X = irrelevant, Z = high-impedance

Figure 4-20. Hex Tri-State Buffer Connections

4.2.10 Quad 2-Imput and Gate (U31).
For connection diagram see figure 4-21.

Connection Diagram

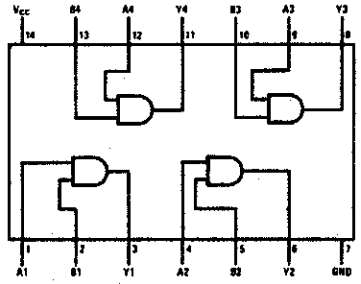
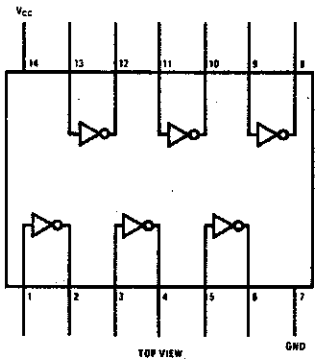


Figure 4-21. Quad 2-Input Connections

4.2.11 Hex Inverter Buffer/Driver (U29).

This device is fully compatible with TTL and DTL logic circuits. It provides high-voltage, open collector outputs and high sink current capability. See Figure 4-22 for schematic and connections.

Logic Diagram



Schematic

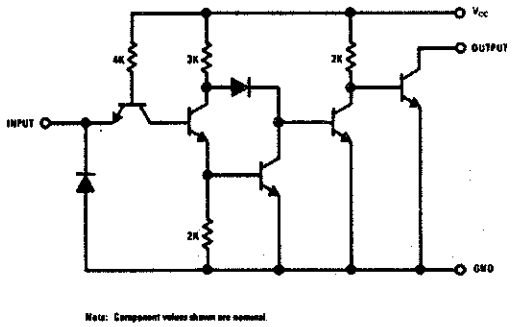
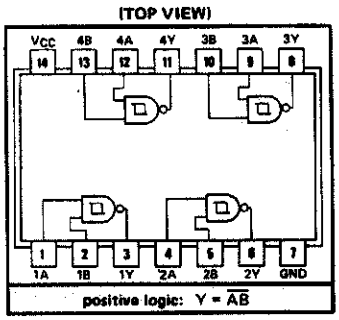


Figure 4-22. Hex Inverter Buffer/Driver Connections

4.2.12 Schmitt-Trigger Positive-NAND Gate (U35).

This device, with Schmitt action, allows both circuits to function as a NAND gate with different input threshold levels for positive and negative-going signals. Logic and connections are shown in Figure 4-23.

Logic/Connection Diagram



Schematic

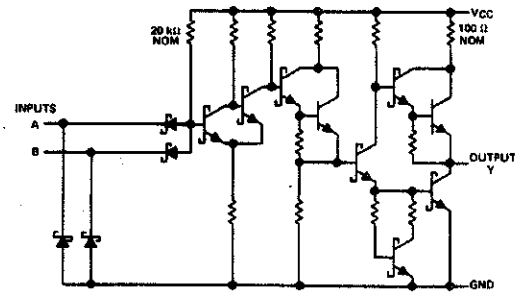
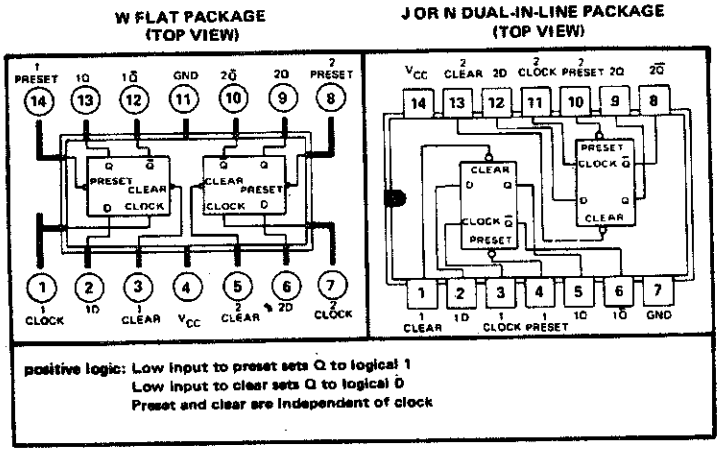


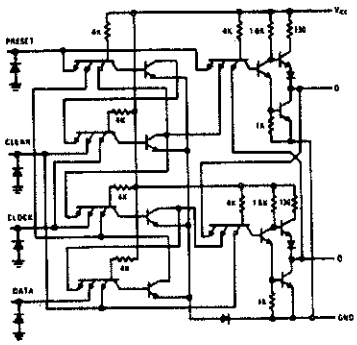
Figure 4-23. Schmitt-Trigger Positive-NAND Gate and Connections

4.2.13 Dual D-Type Edge-Triggered Flip-Flop (U30).
This monolithic, Dual, D-Type, Edge-Triggered Flip-Flop provides direct clear and preset inputs and complementary Q and Q outputs. Input information is transferred to the outputs on the positive edge of the clock pulse. For logic and connections see Figure 4-24.

Logic/Connection Diagram



Schematic



Truth Table

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

Figure 4-24. Dual, D-Type Flip-Flop and Connections

SECTION V
MAINTENANCE AND TROUBLESHOOTING

5.0 INTROCUCTION.

The AM-300 circuit board performs to full capability with a minimum of maintenance. This section describes maintenance and troubleshooting procedures and procedures for handling warranty returns.

5.1 CIRCUIT BOARD CHECKOUT.

The AM-300 circuit board was fully tested before it left Alpha Microsystems and will operate satisfactorily in the system if the hardware and software requirements of Sections Two and Three of this manual are met. Should a problem arise, use the following procedures to identify and locate the fault.

1. Check all cabling for proper seating of connectors.

2. Check the circuit board for proper seating in the slot.

3. Check all power connections for correct voltages.

4. Check jumper options to ensure correctness of application. These include interrupt jumpers on AM-100.

5. Verify that the fault is in the AM-300 and not either in the system or in the peripherals. This can best be accomplished with substitution of a known good circuit board if available.

5.2 WARRANTY PROCEDURES.

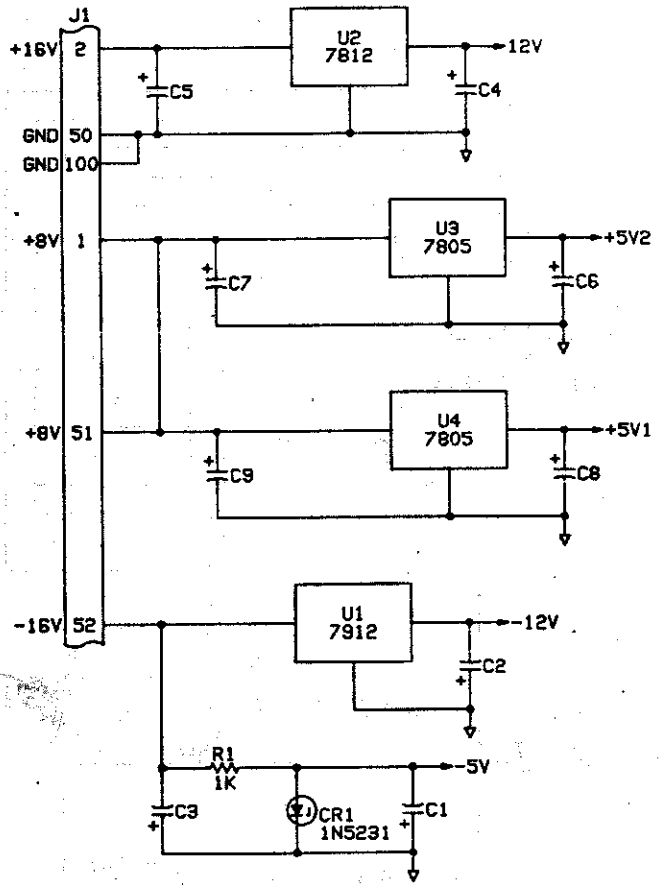
This circuit board is covered by warranty issued by Alpha Microsystems Inc., Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro International Support/Services Group for information.

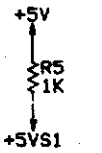
5.3 DIAGNOSTICS

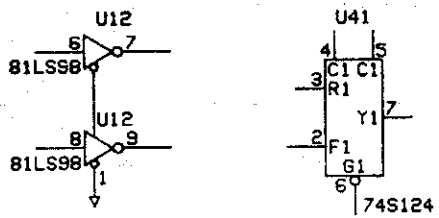
Diagnostic testing software and hardware is available from the Alpha Micro International Support Services group, along with complete documentation and operating instructions.

Table 6-1. Component Cross Reference List

REF. DESIG.	MFG. TYPE NO.	PAR. NO.	REF. DESIG.	MFG. TYPE NO.	PAR. NO.
U1	7912	-	U22	75189	4.2.7
U2	7812	-	U23	1671	4.2.2
U3	7805	-	U24	1671	4.2.2
U4	7805	-	U25	75188	4.2.6
U5	75188	4.2.6	U26	75189	4.2.7
U6	75189	4.2.7	U27	1941	4.2.1
U7	1671	4.2.2	U28	74LS174	4.2.4
U8	1671	4.2.2	U29	7416	4.2.11
U9	75188	4.2.6	U30	7474	4.2.13
U10	75189	4.2.7	U31	74LS08	4.2.10
U11	1941	4.2.1	U32	81LS98	4.2.8
U12	81LS98	4.2.8	U33	-	-
U13	75188	4.2.6	U34	8131	4.2.3
U14	75189	4.2.7	U35	74LS132	4.2.12
U15	1671	4.2.2	U36	74368	4.2.9
U16	1671	4.2.2	U37	81LS98	4.2.8
U17	75188	4.2.6	U38	74368	4.2.9
U18	75189	4.2.7	U39	81LS98	4.2.8
U19	1941	4.2.1	U40	81LS98	4.2.8
U20	74LS138	4.2.5	U41	-	
U21	75188	4.2.6			







REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
B02	INCORP PER ENGO012	9-13-79	
B03	INCORP PER ENGO017	9-13-79	
B05	INCORP PER EN 00263	6-19-80	

2. CAPACITORS ARE IN MICROFARADS.
1. RESISTORS ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

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REVISIONS	TITLE	
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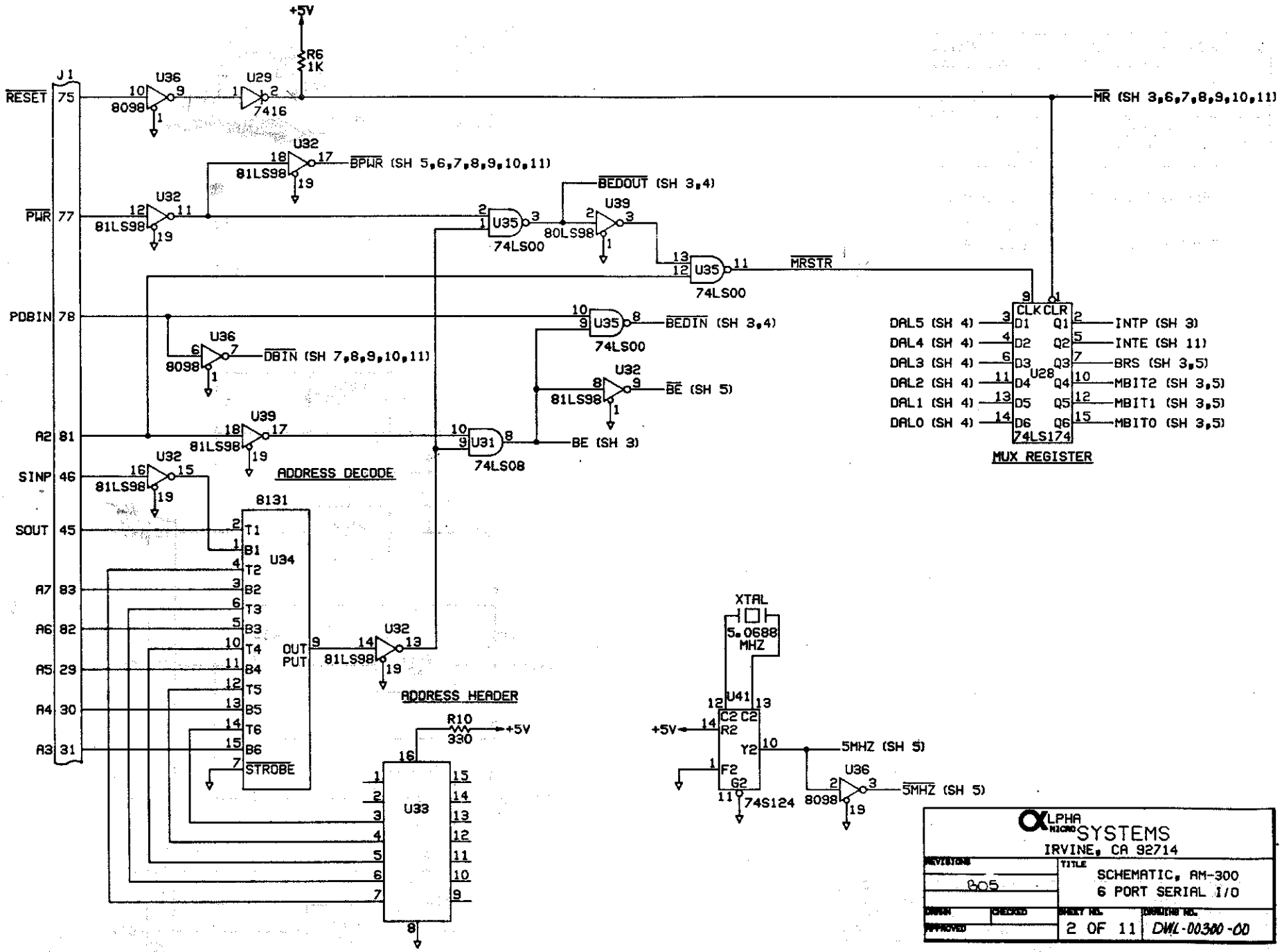

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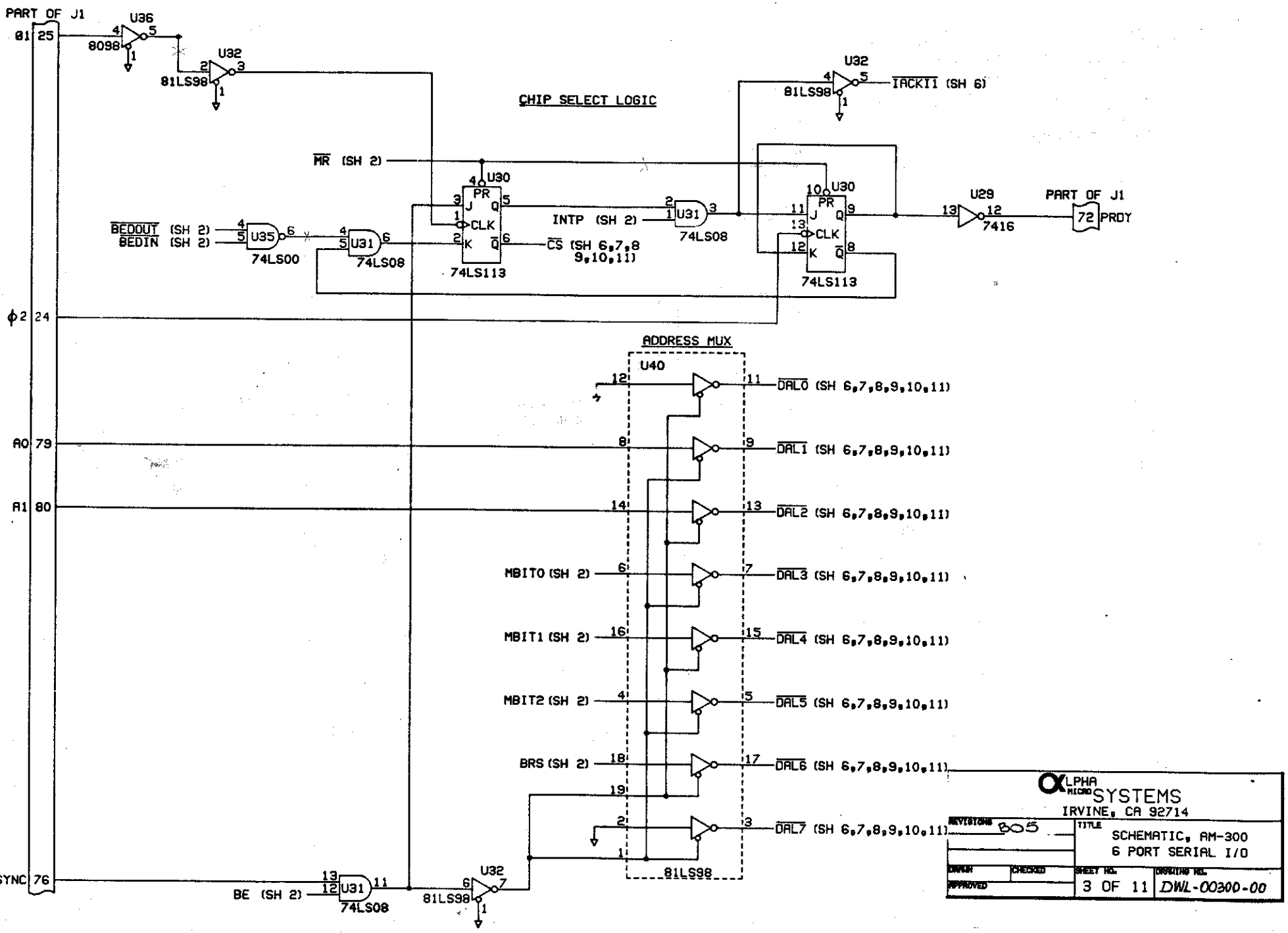
PART OF J1
81 25
U36
8098
U32
81LS98
CHIP SELECT LOGIC
U32
81LS98
IACK1I (SH 6)
MR (SH 2)
U30
PR
J Q
CLK
K Q
74LS113
BEDOUT (SH 2)
BEDIN (SH 2)
U35
74LS00
U31
74LS08
CS (SH 6,7,8 9,10,11)
INTP (SH 2)
U31
74LS08
U30
74LS113
U29
7416
PART OF J1
72 PROY
ADDRESS MUX
U40
DAL0 (SH 6,7,8,9,10,11)
DAL1 (SH 6,7,8,9,10,11)
DAL2 (SH 6,7,8,9,10,11)
DAL3 (SH 6,7,8,9,10,11)
DAL4 (SH 6,7,8,9,10,11)
DAL5 (SH 6,7,8,9,10,11)
DAL6 (SH 6,7,8,9,10,11)
DAL7 (SH 6,7,8,9,10,11)
81LS98
φ2 24
A0 79
A1 80
MBIT0 (SH 2)
MBIT1 (SH 2)
MBIT2 (SH 2)
BRS (SH 2)
PSYNC 76
BE (SH 2)
U31
74LS08
U32
81LS98
ALPHA MICRO SYSTEMS
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REVISIONS B05
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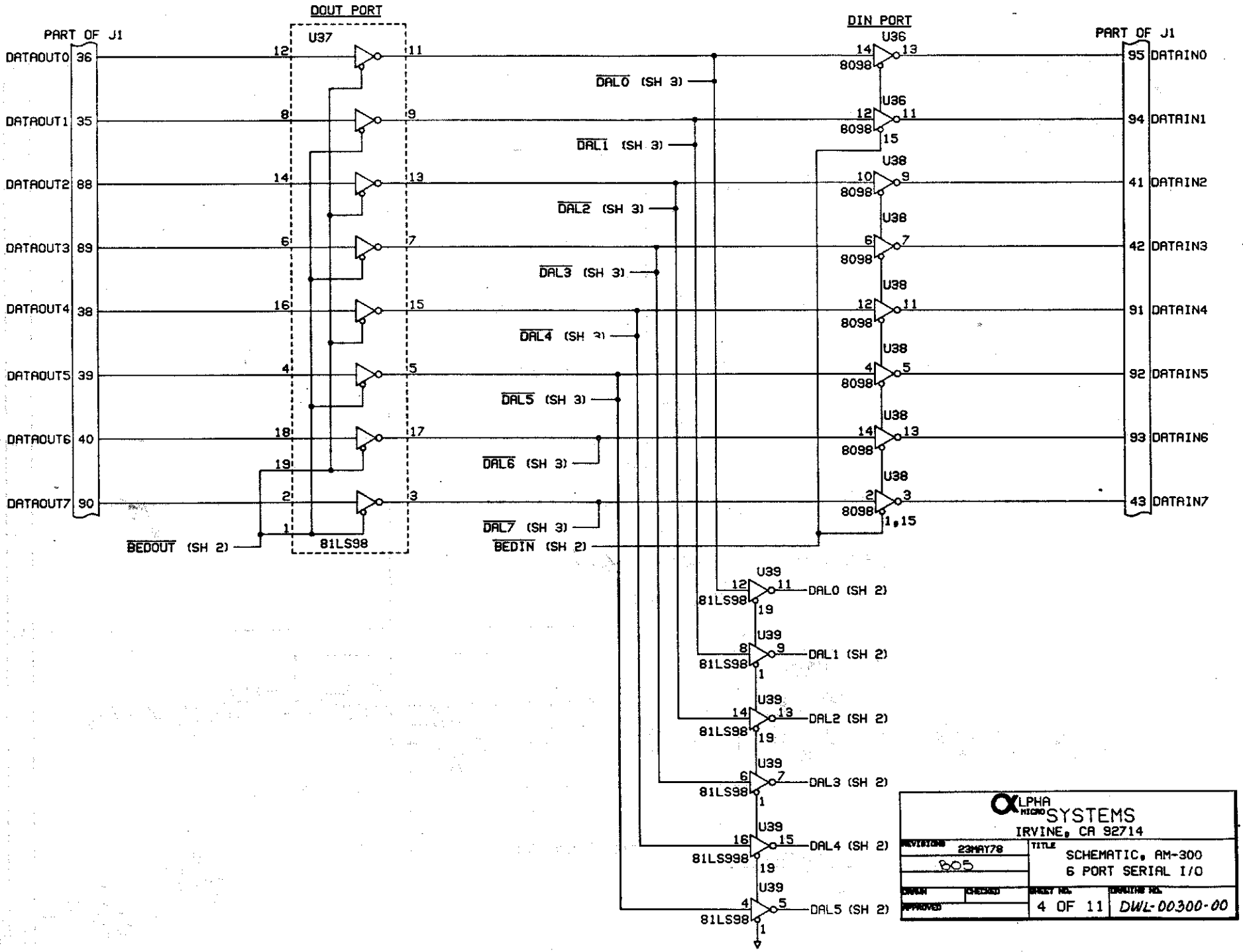
DOUT PORT
PART OF J1
U37
DATAOUT0 36
DATAOUT1 35
DATAOUT2 88
DATAOUT3 89
DATAOUT4 38
DATAOUT5 39
DATAOUT6 40
DATAOUT7 90
81LS98
BEDOUT (SH 2)
DAL0 (SH 3)
DAL1 (SH 3)
DAL2 (SH 3)
DAL3 (SH 3)
DAL4 (SH 3)
DAL5 (SH 3)
DAL6 (SH 3)
DAL7 (SH 3)
BEDIN (SH 2)
DIN PORT
U36
U38
8098
PART OF J1
95 DATAIN0
94 DATAIN1
41 DATAIN2
42 DATAIN3
91 DATAIN4
92 DATAIN5
93 DATAIN6
43 DATAIN7
U39
DAL0 (SH 2)
DAL1 (SH 2)
DAL2 (SH 2)
DAL3 (SH 2)
DAL4 (SH 2)
DAL5 (SH 2)
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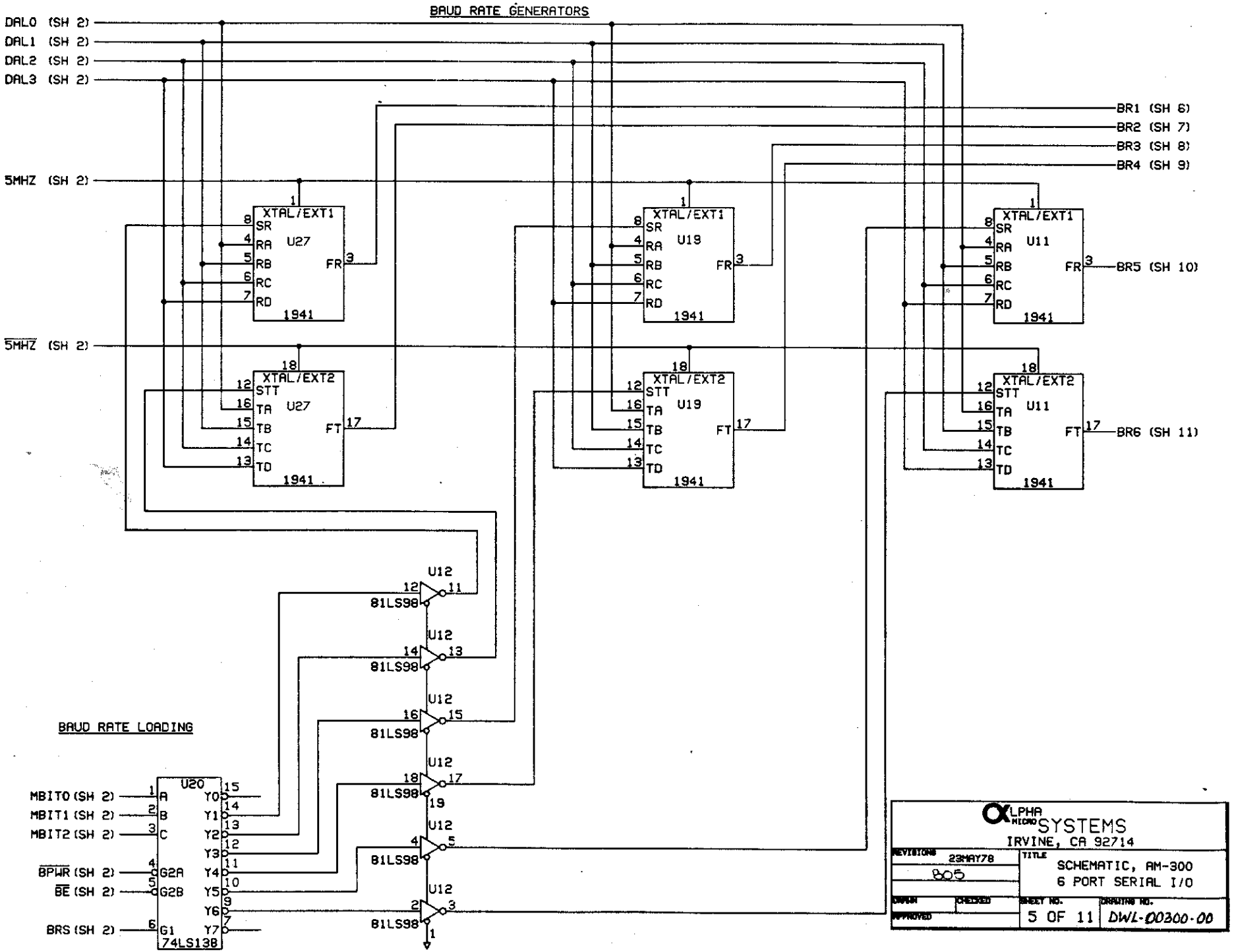
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DAL0 (SH 2)
DAL1 (SH 2)
DAL2 (SH 2)
DAL3 (SH 2)
5MHZ (SH 2)
5MHZ (SH 2)
BR1 (SH 6)
BR2 (SH 7)
BR3 (SH 8)
BR4 (SH 9)
BR5 (SH 10)
BR6 (SH 11)
XTAL/EXT1
XTAL/EXT2
U27
U19
U11
1941
SR
RA
RB
RC
RD
FR
STT
TA
TB
TC
TD
FT
U12
81LS98
BAUD RATE LOADING
U20
74LS138
MBIT0 (SH 2)
MBIT1 (SH 2)
MBIT2 (SH 2)
BPWR (SH 2)
BE (SH 2)
BRS (SH 2)
G2A
G2B
G1
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
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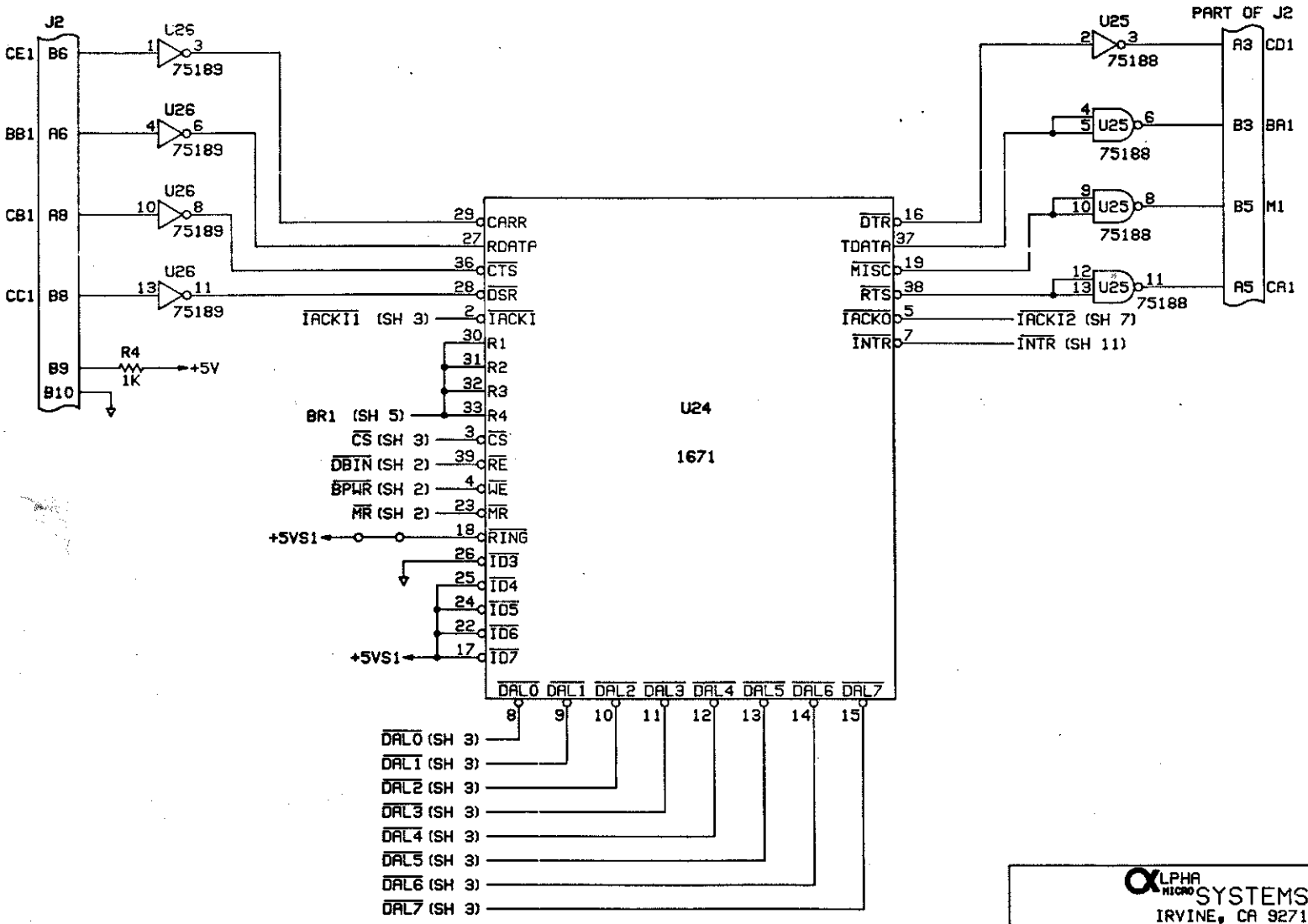

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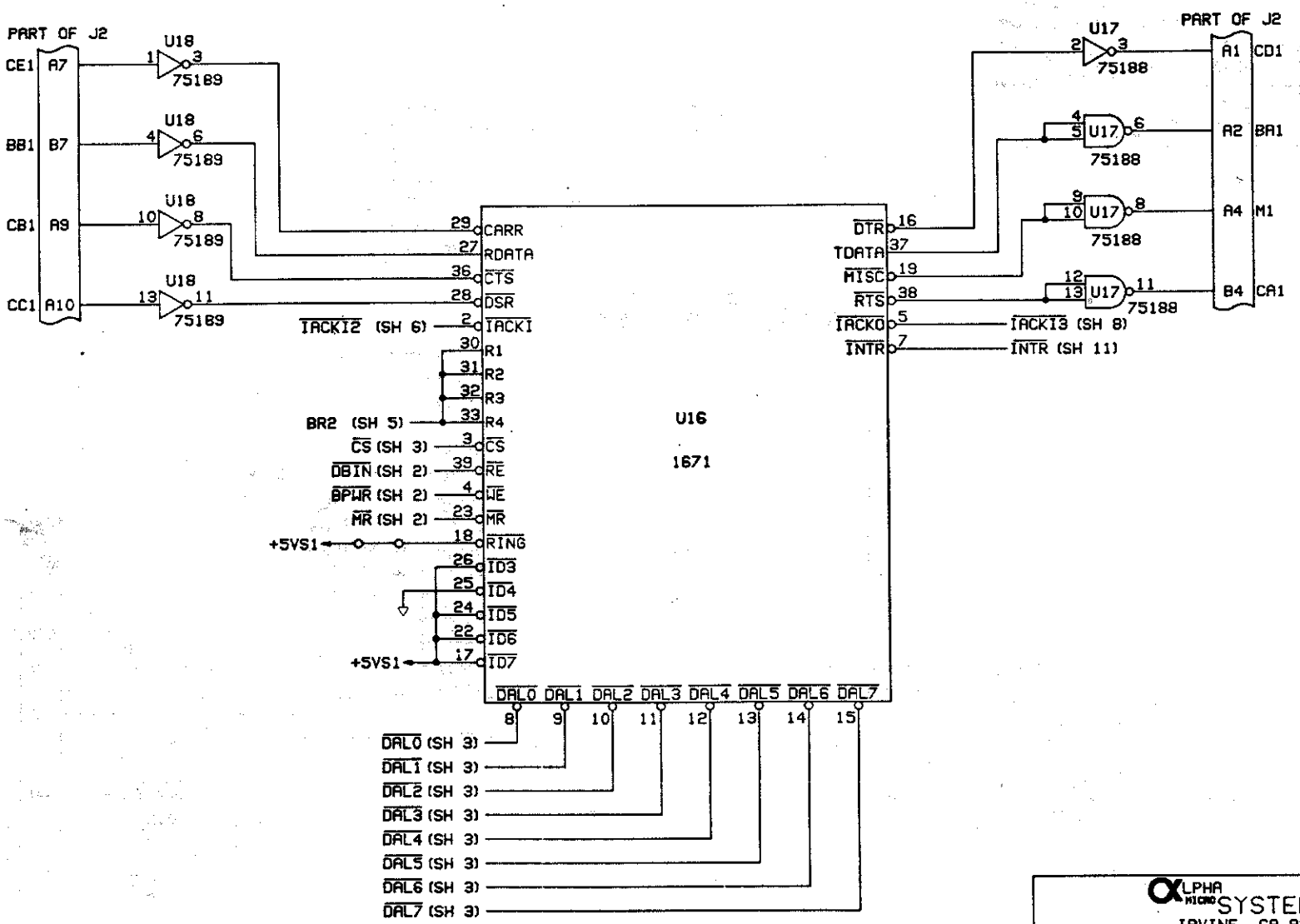

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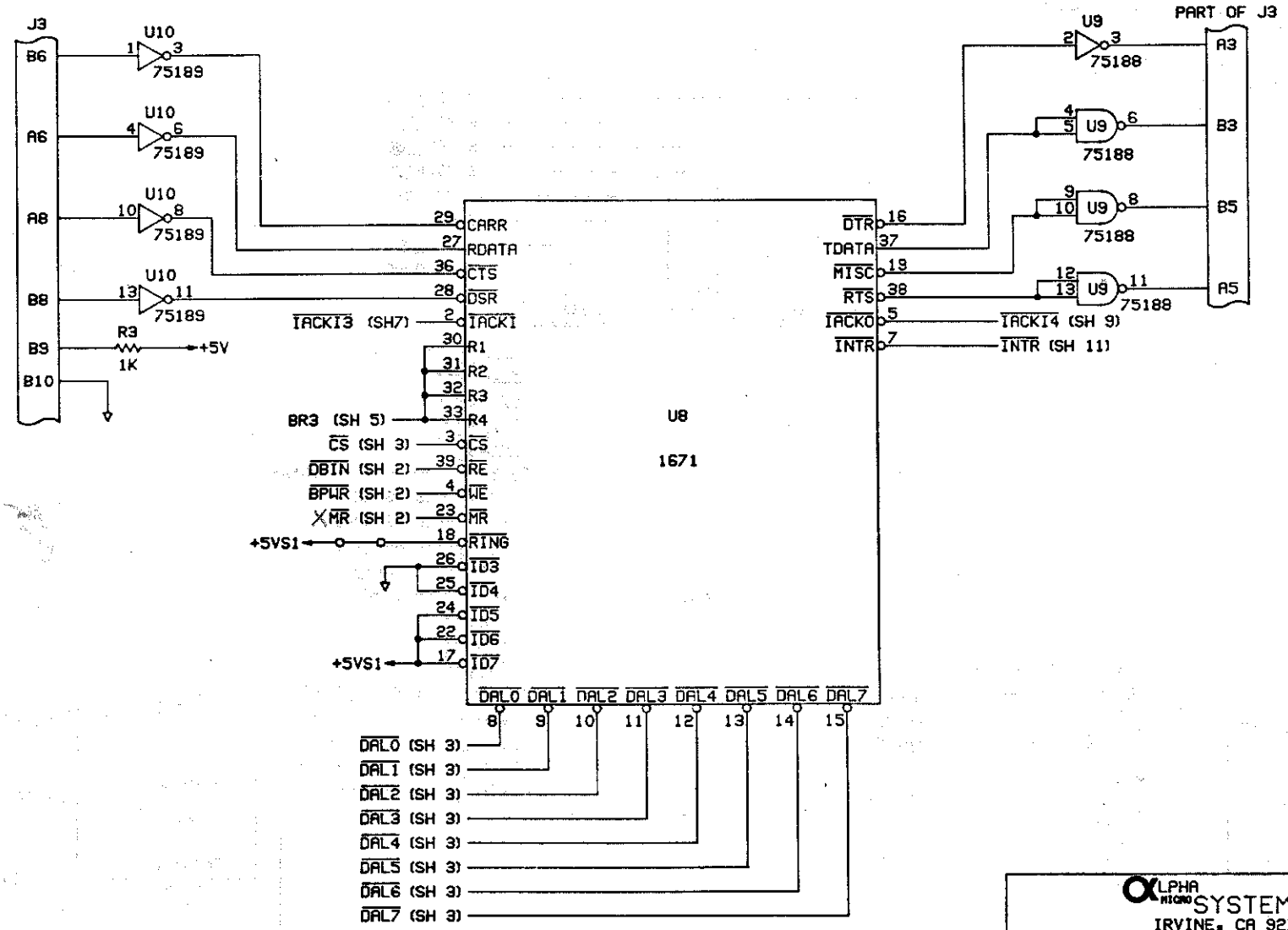

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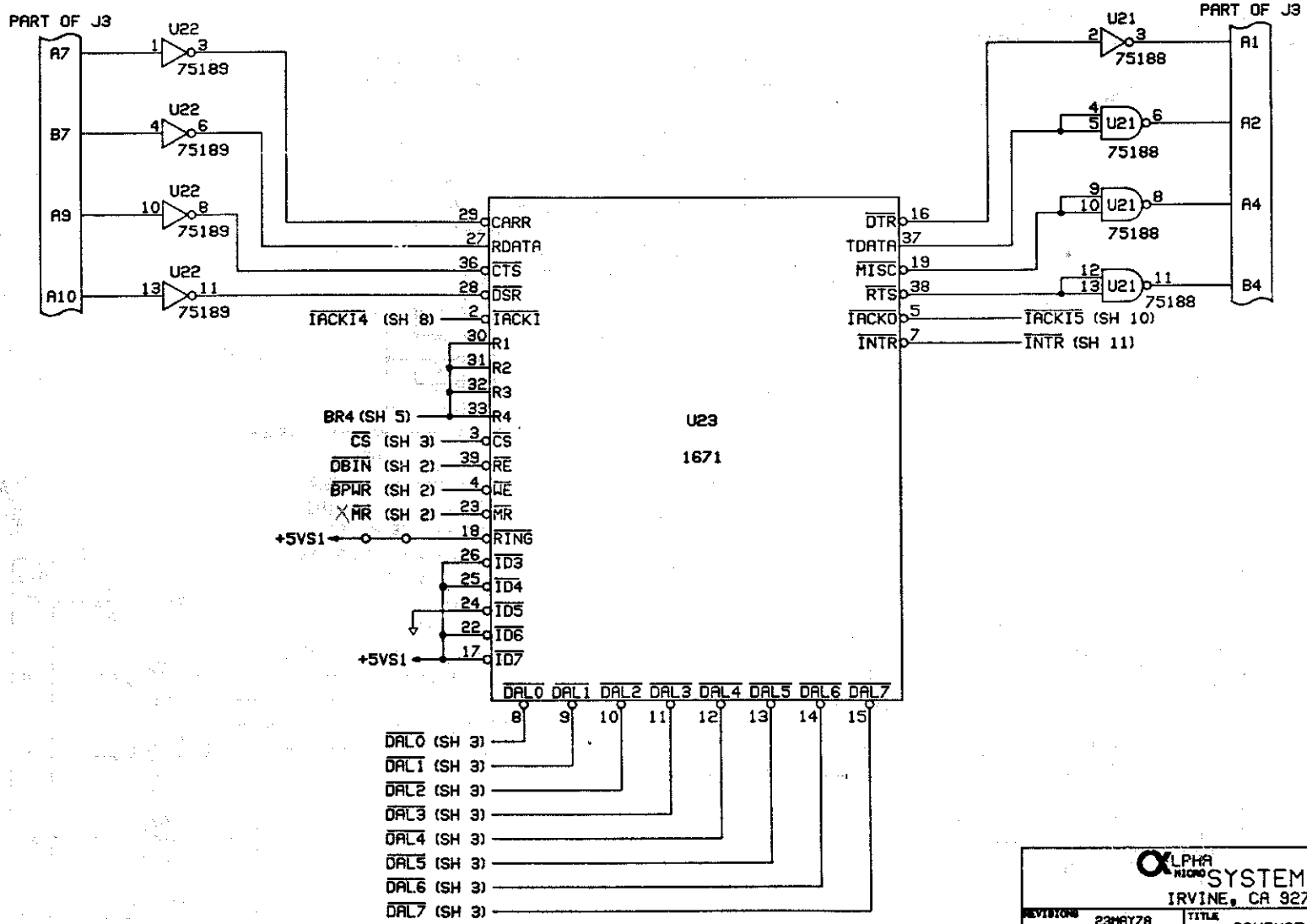

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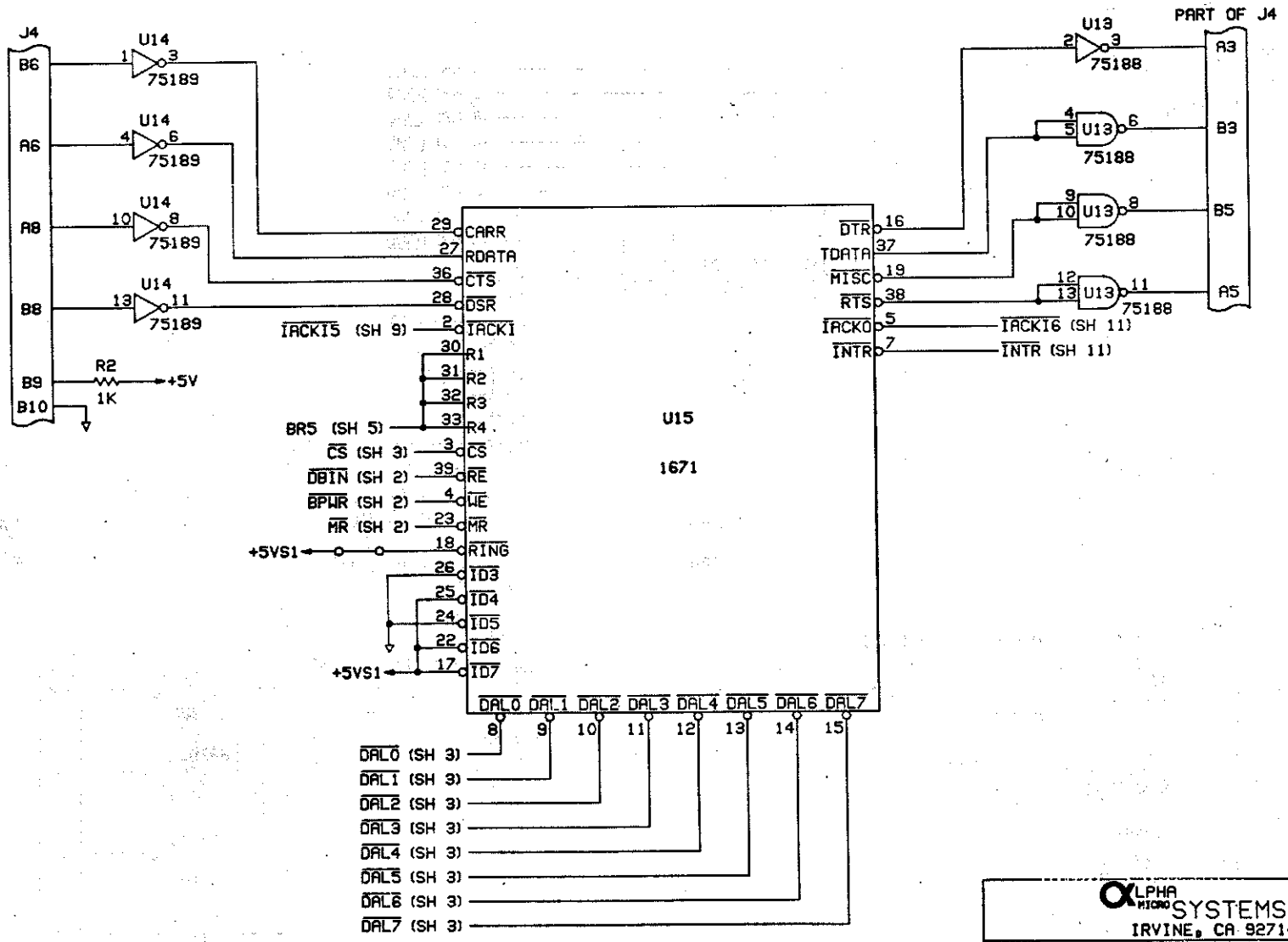
	DRAWING NO. DWL-00300-00



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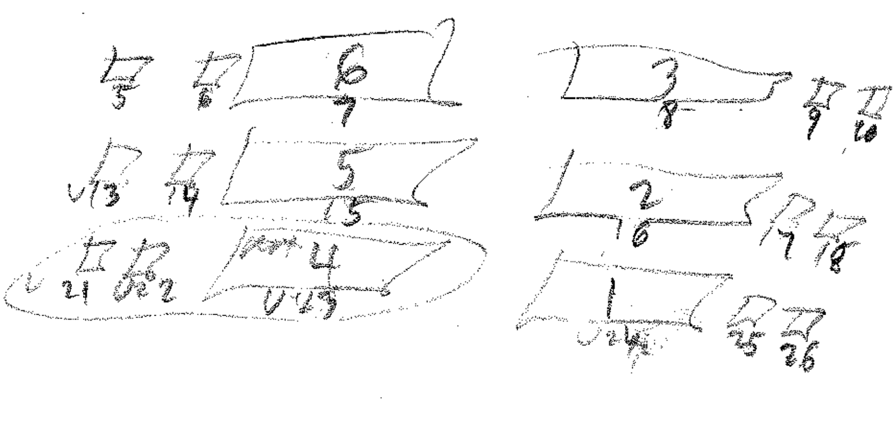
Trouble Shooting

① Clock circuits. Each chip controls 2 ports
If 2 ports go bad & they are pairs (1,2 — 3,4 — 5,6)
It's probably the clock chip

② 1 STRO or 2 receiver driver/chips – If only one port goes bad, check above



SECTION I
GENERAL DESCRIPTION

1.0 INTRODUCTION.

This manual provides operating and maintenance instructions for the AM-300 Six Port Serial I/O Board manufactured by Alpha Microsystems Inc. located in Irvine, California. Circuit board description, operating and usage instructions, programming, theory of operation, and maintenance instructions are included to provide the user with the information necessary to utilize this circuit board to its full capacity.

1.1 CIRCUIT BOARD DESCRIPTION.

The AM-300 circuit board is a six port serial Input/Output device that is S-100 bus compatible and provides six fully programmable RS-232 ports. Individual ports can be independently programmed to any of 16 baud rates up to 19,200 baud. The entire board can generate multilevel interrupts under program control. Both synchronous and asynchronous operating modes for each port are provided through Western Digital's Aysnchronous Synchronous Receiver/Transmitters (ASTRO-UC1671B).

A simplified block diagram of the circuit board is shown in Figure 1-1. For a complete detailed description of circuit board operation, see Section IV of this manual.

1.2 APPLICATION.

This circuit board provides the data conversion and processing necessary for RS-232 peripheral equipment to communicate with an S-100 bus computer system. The AM-300 fulfills this function in the Alpha Microsystems' Computer Systems or any other system with these requirements.

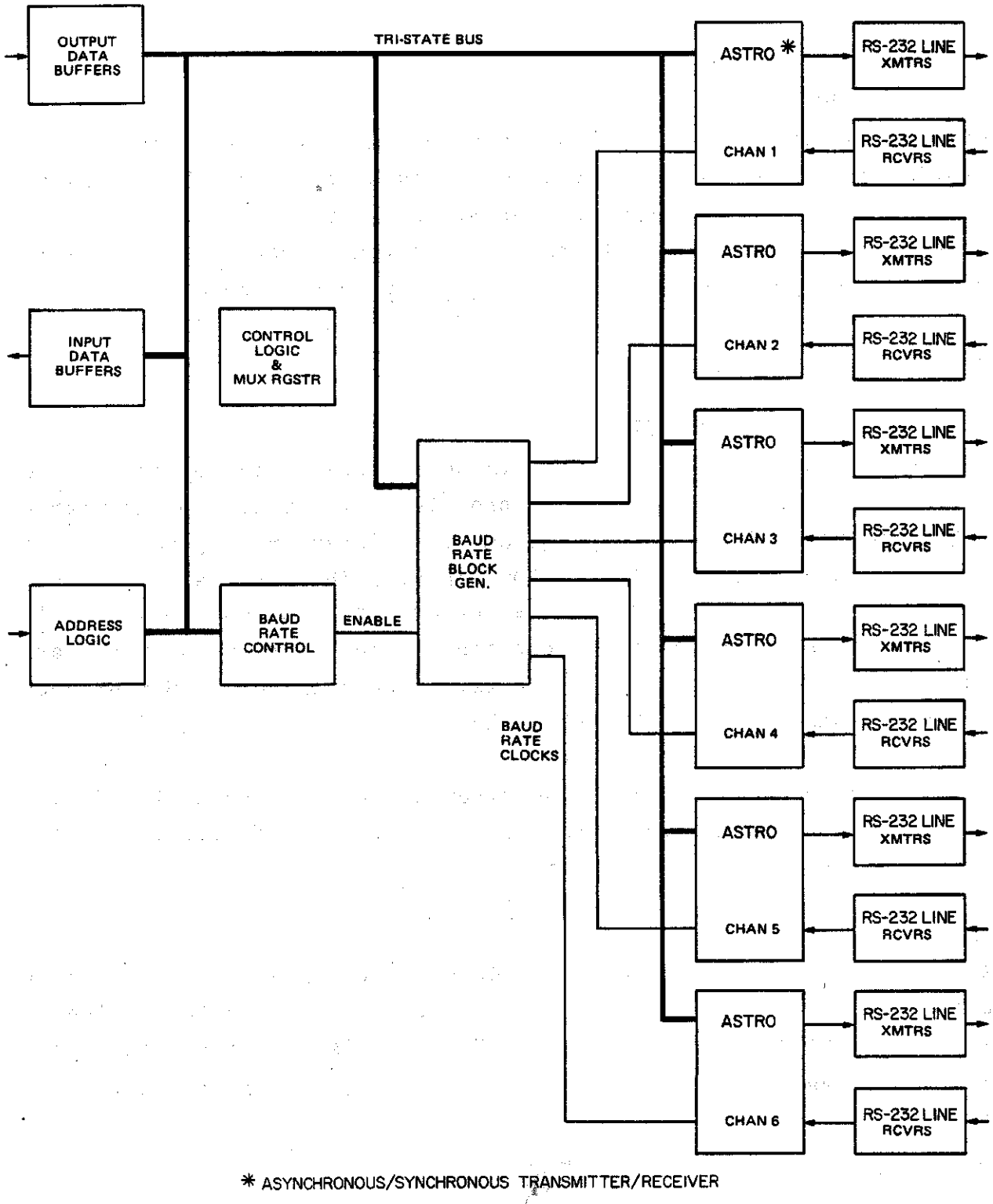


Figure 1-1. Six Port Serial I/O Board Simplified Block Diagram

SECTION II
OPERATING DATA

2.0 INTRODUCTION.

This section contains information on the use of the AM-300 Six Port Serial I/O Board. Capabilities, specifications, interface wiring, set-up and checkout procedures are provided for the successful integration of the board into the user's system.

2.1 CAPABILITIES AND SPECIFICATIONS.

This circuit board operates from the standard S-100 bus structure and provides RS-232 interface capability for up to six separate peripherals. Each of the six ports are individually programmable and can be set at any of 16 selectable baud rates. The entire board can generate multilevel interrupts under program control and can operate in either synchronous or asynchronous modes. Detailed specifications are listed in Table 2-1.

2.2 INTERFACE DESCRIPTION AND WIRING.

The AM-300 Six Port Serial Input/Output circuit board provides interface capability between the standard S-100 bus and peripheral equipment requiring serial data and controls.

2.2.1 S-100 Bus Interface.

The AM-300 circuit board is fully S-100 bus compatible. The six ports are addressed through the bus address lines and data lines as described in Section III. The S-100 bus connections are made via the bottom edge connector and are described in Table 2-2.

2.2.2 I/O Port Interface.

The AM-300 circuit board contains six programmble I/O ports that are compatible with most standard RS-232 interface peripherals. All six ports are identical and connections are made via the three connectors on the top edge of the circuit board.

Table 2-1. AM-300 Specifications.

Parameter	Specifications
Peripheral I/O ports	Six fully programmable
Operating Modes	Synchronous and Asynchronous
Baud Rates	16 selectable per I/O port under software control.

Code*				Baud Rate
D	C	B	A	
0	0	0	0	50
0	0	0	1	750
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	200
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200
				*See programming information Sec.III

Interface	RS-232C for peripherals S-100 bus for CPU
Addressing	Card and port addressed thru S-100 bus for CPU
Circuit Board	5.275" X 10.000" with 100 pin connector
DC Power Reqmts	+7.5v @ 0.8A +16v @ 0.1A -16v @ 0.1A

Table 2-2. Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
+7.5V	+ 7.5vdc Power	1
+16V	+ 16vdc Power	2
$\overline{VI8}$	Vectored Interrupt 8	3
$\overline{VI0}$	Vectored Interrupt 0	4
$\overline{VI1}$	Vectored Interrupt 1	5
$\overline{VI2}$	Vectored Interrupt 2	6
$\overline{VI3}$	Vectored Interrupt 3	7
$\overline{VI4}$	Vectored Interrupt 4	8
$\overline{VI5}$	Vectored Interrupt 5	9
$\overline{VI6}$	Vectored Interrupt 6	10
$\overline{VI7}$	Vectored Interrupt 7	11
RTC	Real Time Clock, 50Hz or 60Hz	12
POWFAIL	AC Power Failure Status	13
$\overline{VI9}$	Vectored Interrupt 9	14
A18	Address 18	15
A16	Address 16	16
A17	Address 17	17
$\overline{STATDSB}$	Status Disable	18
$\overline{C/CDSB}$	Command/Control Disable	19
GND	Ground	20

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{IODIS}}$	I/O Disable	21
$\overline{\text{ADDDSB}}$	Address Disable	22
$\overline{\text{DODSB}}$	Data Bus Disable	23
Ø2	Phase 2 Clock	24
$\overline{\text{STVAL}}$	Status and Address Valid	25
PHLDA	DMA Request Acknowledge	26
PWAIT	Processor Wait	27
N/U	Not Used	28
A5 A4 A3 A15 A12 A9	Address 5 Address 4 Address 3 Address 15 Address 12 Address 9	29 30 31 32 33 34
DOUT 1/D1 DOUT 0/DO	Data Bus Bit 1 Data Bus Bit 0	35 36
A10	Address 10	37

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
DOUT 4/D4	Data Bus Bit 4	38
DOUT 5/D5	Data Bus Bit 5	39
DOUT 6/D6	Data Bus Bit 6	40
DIN 2/D10	Data Bus Bit 10	41
DIN 3/D11	Data Bus Bit 11	42
DIN 7/D15	Data Bus Bit 15	43
SMI	Bus Master OP Code Fetch	44
SOUT	I/O Output Cycle	45
SINP	I/O Input Cycle	46
SMEMR	Memory Read Cycle	47
SHLTA	HLT Acknowledge	48
$\overline{\text{PERR}}$	Parity Error Pulse	49
GND	Ground	50
+7.5V	+7.5vdc Power	51
-16V	-16vdc Power	52
GND	Ground	53
$\overline{\text{SLAVECLR}}$	Reset Signal To All I/O Devices	54

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
$\overline{\text{DMA0}}$	DMA Controller Arbitration	55
$\overline{\text{DMA1}}$	Lines For Use With Standard	56
$\overline{\text{DMA2}}$	S-100 Bus DMA System	57
$\overline{\text{SXTRQ}}$	16 Bit Cycle	58
A19	Address 19	59
N/U	Not Used	60
A20 A21 A22 A23	Address 20 Address 21 Address 22 Address 23	61 62 63 64
$\overline{\text{ADVAL}}$	Address Valid On Data Bus	65
$\overline{\text{WRDIS}}$	Write Disable	66
$\overline{\text{PHANTOM}}$	ROM Memory Enable	67
N/U N/U	Not Used Not Used	68 69
Gnd	Ground	70
N/U	Not Used	71
PRDY	Processor Ready	72

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
N/U	Not Used	73
$\overline{\text{PHOLD}}$	DMA Request	74
$\overline{\text{PRESET}}$	Preset	75
PSYNC	Processor Sync, Start of Bus Cycle	76
$\overline{\text{PWR}}$	Write Strobe	77
PDBIN	Data Bus Input Command	78
A0	Address 0	79
A1	Address 1	80
A2	Address 2	81
A6	Address 6	82
A7	Address 7	83
A8	Address 8	84
A13	Address 13	85
A14	Address 14	86
A11	Address 11	87
DOUT 2/D2	Data Bus Bit 2	88
DOUT 3/D3	Data Bus Bit 3	89
DOUT 7/D7	Data Bus Bit 7	90
DIN 4/D12	Data Bus Bit 7	91
DIN 5/D13	Data Bus Bit 13	92
DIN 6/D14	Data Bus Bit 14	93
DIN 1/D9	Data Bus Bit 9	94
DIN 0/D8	Data Bus Bit 8	95

Table 2-2.(con't) Alpha Micro Bus Interface Signals List

MNEMONIC	NAME	PIN NO.
SINTA	Interrupt Acknowledge	96
$\overline{\text{SWO}}$	Bus Master Output	97
$\overline{\text{ERROR}}$	Memory Error Interrupt	98
$\overline{\text{BERR}}$	Bus Error	99
GND	Ground	100

Interface wiring is described in Table 2-3 and is in accordance with EIA Specification RS-232C. Cabling requirements and jumpers are illustrated in Figure 2-1.

2.3 SETUP AND CHECKOUT.

When the AM-300 circuit board is received, it is ready for use. No adjustment or calibration is required for operation. The hardware requirements for use are described in this section and the software requirements are described in Section III.

2.3.1 Wiring Connections.

First ensure that the proper power wiring is available and the correct voltages are connected to the various pins as described in paragraph 2.2. All power connections are made through the bottom edge connector.

All functional connections are made to the S-100 bus through the bottom edge connector and connections to peripherals are through the three connectors on the top edge of the card, as described in paragraph 2.2. Ensure that these connections are correct before plugging the AM-300 circuit board into the system.

2.3.2 User Options.

Address Code. Before the AM-300 circuit board can be used in the system, the card address must be set up to provide correct software selection of I/O ports. Five I/O ports are required by the AM-300. These I/O ports are defined in Section III. The I/O port base address is jumper settable in blocks of eight. Figure 2-2 illustrates the procedure for setting this address. Addressing of the five ports on the circuit board are provided by codes on the data lines as described in Section III.

Interrupt Lines. Each AM-300 board requires a separate vectored interrupt. Figure 2-3 illustrates the procedure for setting up the interrupt vector.

Table 2-3. I/O Port Interface Signals List (RS-232)

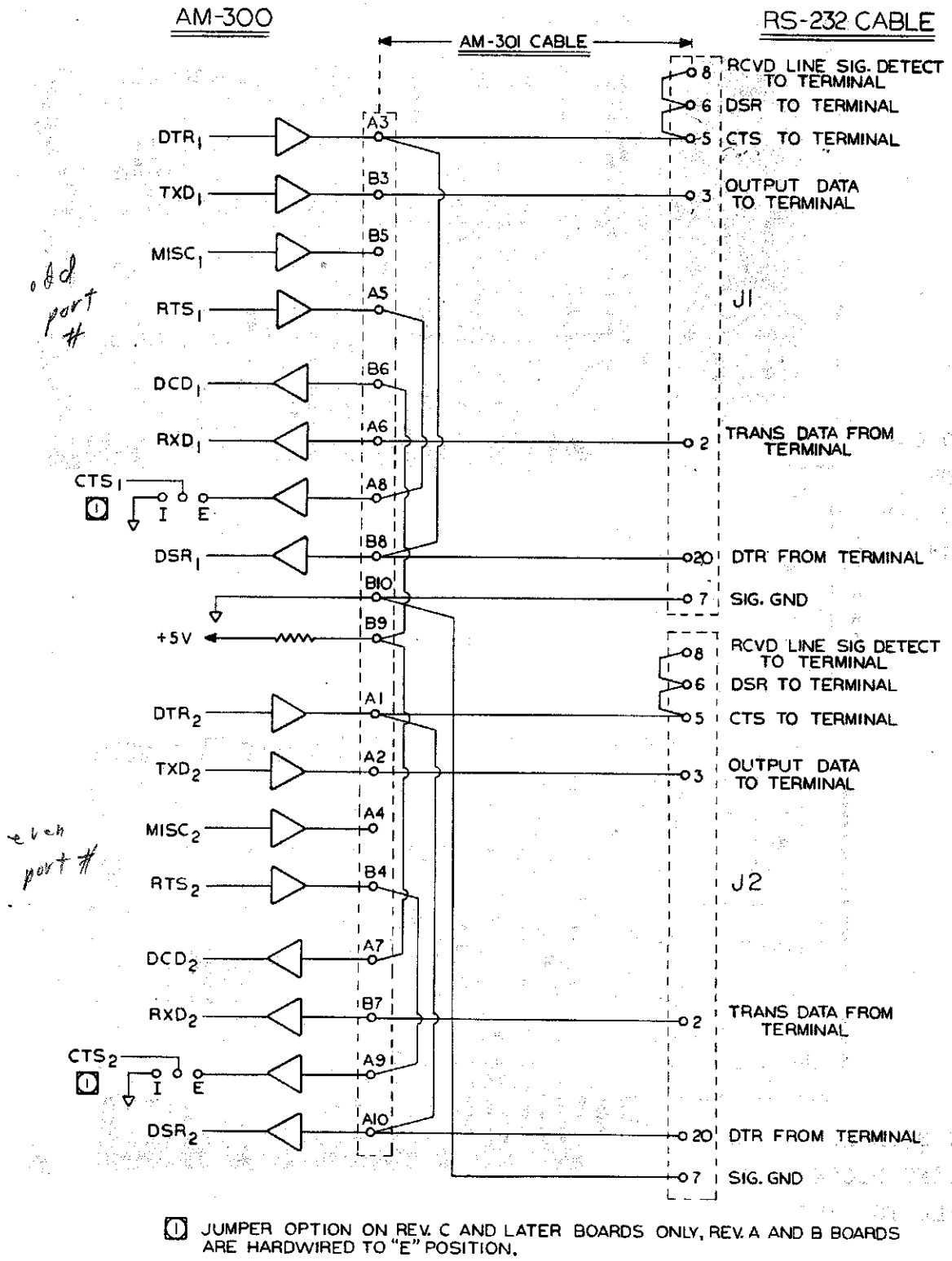
AM-300 SIGNAL	PIN	NMEMONIC	FUNCTION
Ground	B10	GND	Signal Ground.
+5V	B9	+5V	5 volt output through 1K resistor.
Data Terminal Ready	A3	CD	AM-300 output. Controls switching of the data of the data communication equipment to the communication channel (ASTRO pin 16).
Transmitted Data	B3	BA	AM-300 output. Serial data output from the AM-300 to peripheral (ASTRO pin 37). Data is not transmitted unless the following signals are in the ON condition: 1. Request to Send (CA) 2. Clear to Send (CB) 3. Data Set Ready (CC) 4. Data Terminal Ready (CD)
Request to Send	A5	CA	AM-300 output. Conditions the peripheral for data transmission (ASTRO pin 38). Remains low during transmitted data.

Table 2-3. (Con't) I/O Port Interface Signals List (RS-232)

AM-300 SIGNAL	PIN	MNEMONIC	FUNCTION
Data Terminal Ready	A1	CD	Same as pin A3 on other channel.
Transmitted Data	A2	BA	Same as pin B3 on other channel.
Request to Send	B4	CA	Same as pin A5 on other channel.
Miscellaneous Control	A4	M	Same as pin B5 on other channel.
Received Data	B7	BB	Same as pin A6 on other channel.
Clear to Send	A9	CB	Same as pin B8 on other channel.
Data Set Ready	A10	CC	Same as pin B8 on other channel.
Ring Indicator	A7	CE	Same as pin B6 on other channel.

Table 2-3. (Con't) I/O Port Interface Signals List (RS-232)

AM-300 SIGNAL	PIN	MNEMONIC	FUNCTION
Miscellaneous Control	B5	M	AM-300 output. Controlled by a bit in the control register of the ASTRO used as an extra programmable signal (ASTRO pin 19).
Received Data	A6	BB	AM-300 input. Serial data input from peripheral (ASTRO pin 27).
Clear to Send	A8	CB	AM-300 input. Generated by the peripheral to indicate whether or not it is ready to transmit data (ASTRO pin 36). Enables ASTRO transmitter.
Data Set Ready	B8	CC	AM-300 input. Indicates the status of the peripheral. An ON condition indicates that the peripheral is ready to transmit data (ASTRO pin 28).
Ring Indicator	B6	CE	AM-300 input. Ring indicator from the peripheral. Generates an interrupt if Data Terminal Ready is ON (ASTRO pin 29).



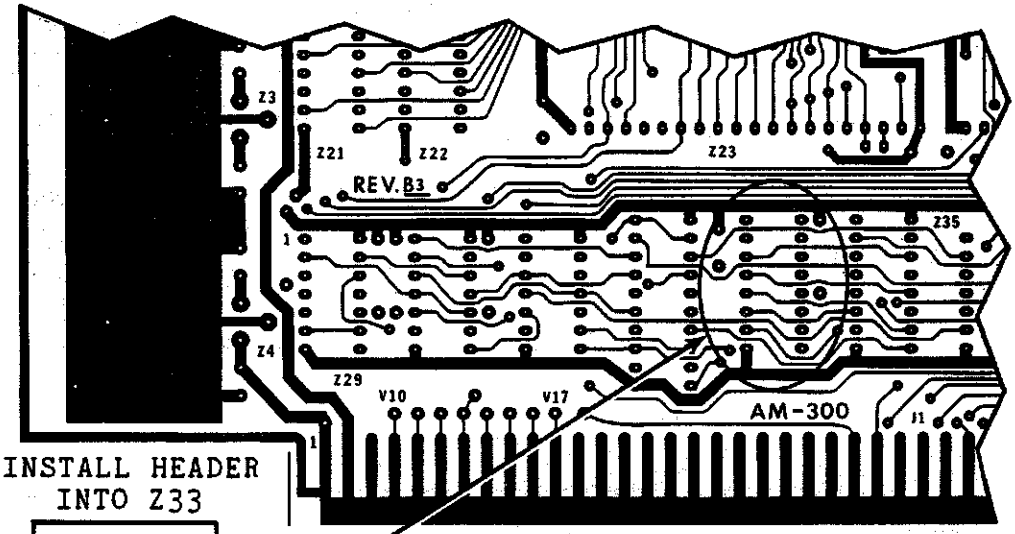
[1] JUMPER OPTION ON REV. C AND LATER BOARDS ONLY, REV. A AND B BOARDS ARE HARDWIRED TO "E" POSITION.

Figure 2-1. AM-300 Cabling and Jumper Requirements

STANDARD I/O BASE ADDRESS IS :F8 (SHOWN)

2ND AM-300 I/O BASE ADDRESS IS :E8

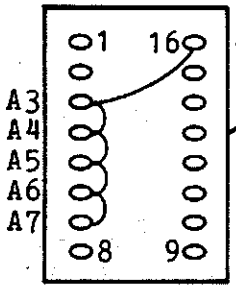
3RD AM-300 I/O BASE ADDRESS IS :D8



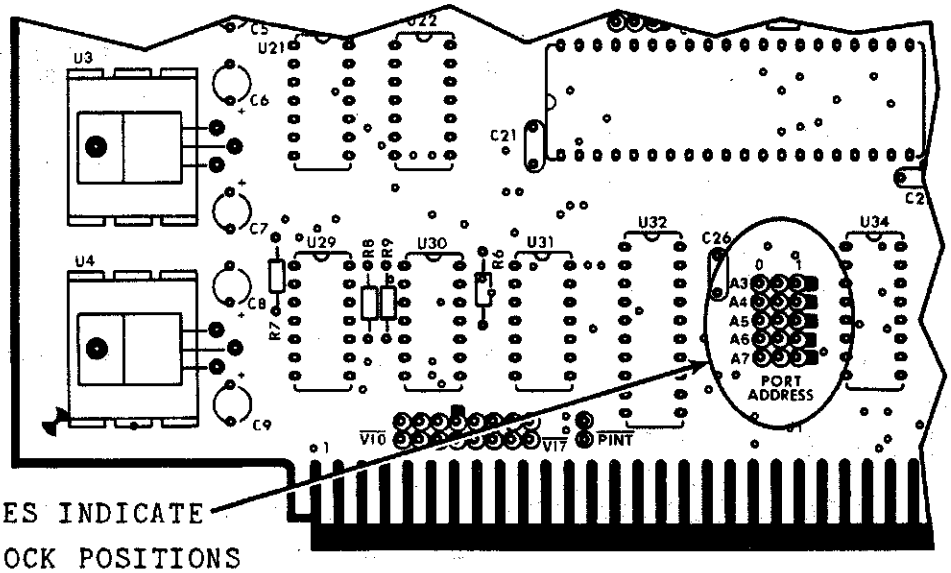
JUMPER TO GND FOR "0"

JUMPER TO +5V FOR "1"

INSTALL HEADER INTO Z33



(Board Rev A & B)

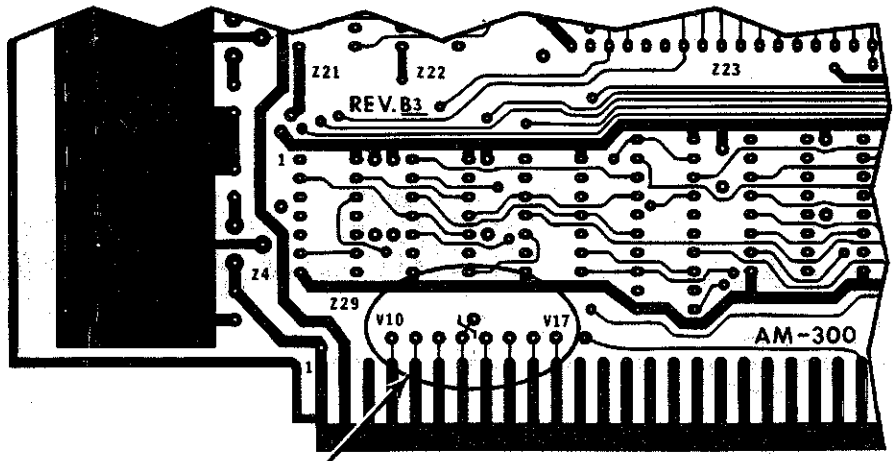


DARK SQUARES INDICATE SHORTING BLOCK POSITIONS (ALL TO "1"S SIDE)

Board Rev C And Later

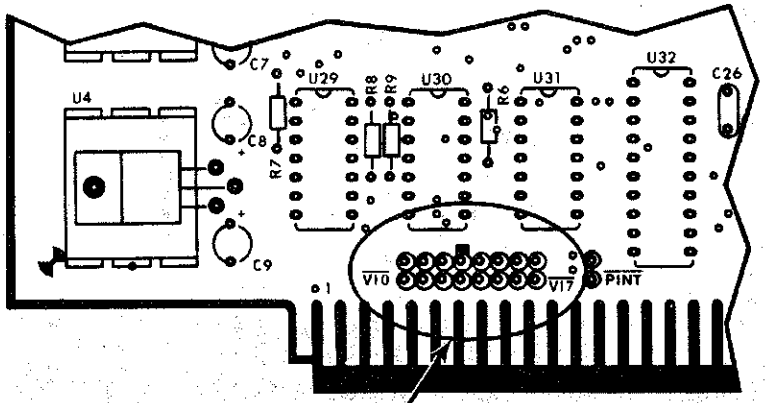
Figure 2-2. AM-300 I/O Port Address Jumper Setting

STANDARD VECTOR INTERRUPT IS LEVEL 3
2ND AM-300 VECTOR INTERRUPT IS LEVEL 6
3RD AM-300 VETOR INTERRUPT IS LEVEL 7



TO CHANGE FROM LEVEL 3
TO ANOTHER LEVEL, CUT ETCH ON COMPONENT
SIDE AS SHOWN AND JUMPER PAD TO DESIRED
VECTORED INTERRUPT LEVEL.

(Board Rev A & B)

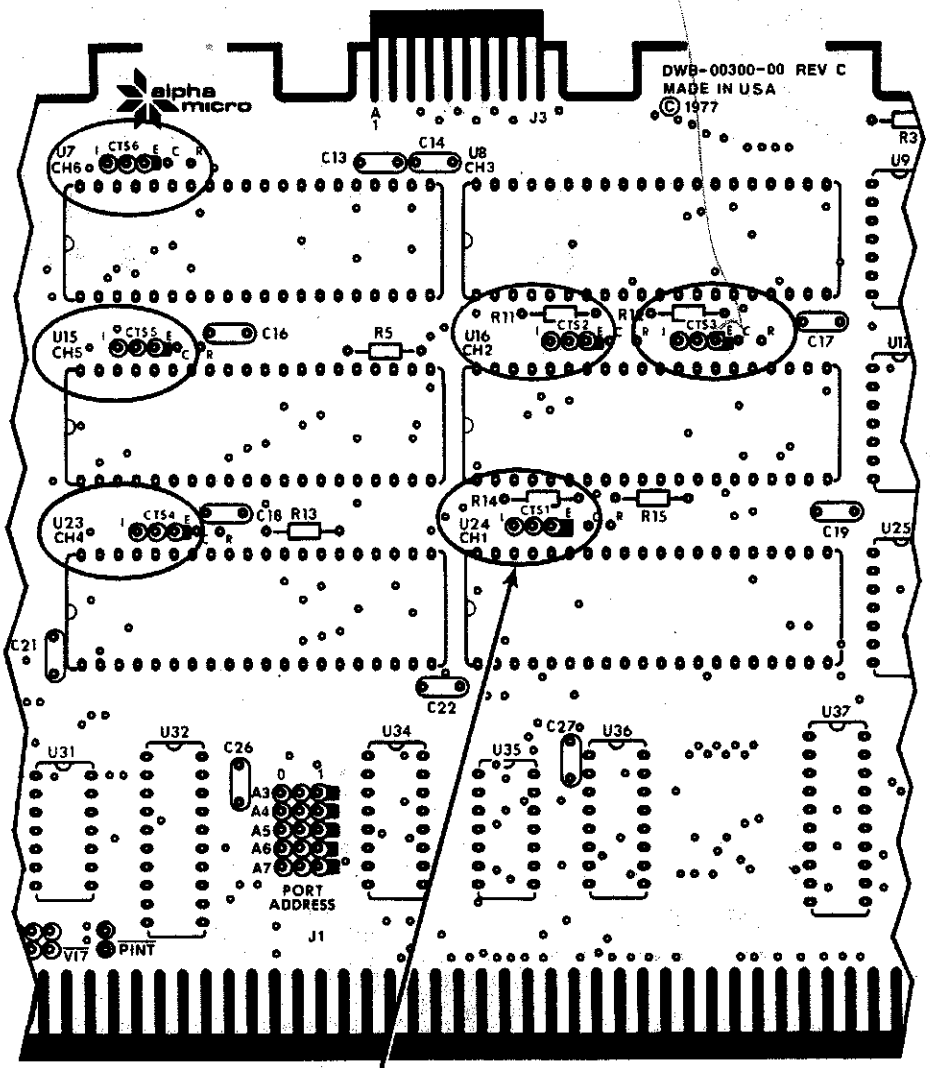


DARK SQUARE INDICATES STANDARD
SHORTING BLOCK POSITION (LEVEL 3).
TO ALTER VECTOR INTERRUPT LEVEL, SIMPLY
REPOSITION SHORTING BLOCK TO DESIRED LEVEL.

Board Rev C And Later

Figure 2-3. AM-300 Vector Interrupt Jumper Setting

CTS Jumpering. (Rev C and later boards only). Each RS-232 channel may be configured so that CTS is always asserted, or is controlled externally by the peripheral to which it is attached. Figure 2-4 illustrates these jumpers. Note: This can be accomplished in the external cabling or using the on-board shorting blocks.



CTS JUMPERS, 6 PLACES
SHOWN BY DARK SQUARES IN THE
EXTERNAL POSITION (E).
INTERNAL POSITION (I) ALWAYS
ASSERTS CTS.

Figure 2-4. AM-300 CTS Jumper Options (Rev C and Later)

SECTION III
PROGRAMMING

3.0 INTRODUCTION.

This section describes the programming requirements for the AM-300 circuit board. Input/Output port addressing, baud rate selection, and interrupt programming are described for complete system compatibility. Listings for the AM-300 interface driver are contained in Figure 3-1.

3.1 I/O PORT DEFINITIONS.

Five I/O ports are required by the AM-300. These are summarized in Tables I and II.

Note that the first four I/O addresses are contained in the Western Digital Corporation UC1671B ASTRO. See the data sheet on the chip for a detailed explanation of the register contents.

In addition to the registers contained in the UC1671B, there are three other functions that must be considered:

A. MUX Control Register

See Table II for description of control bits.

B. Baud Rate Programming

The baud rate for a given serial I/O channel can be programmed as follows:

1. Set up the MUX Control Register with bit 3 set to a "1" and bits 0-2 set to address the appropriate channel.

Table 3-1. I/O Port Definitions

I/O Port Address (1)	Input	Output	Comments
X0	Control Register 1	Control Register 1	See UC1671B spec
X1	Control Register 2	Control Register 2	See UC1671B spec
X2	SYN and DLE Register	Status Register	See UC1671B spec
X3	Receiver Holding Register	Transmitter Holding Register	See UC1671B spec
X4	---------	MUX Control Register	See Table II

(1) the base I/O port address (shown as 0) is jumper selectable to any block of eight I/O addresses.

Table 3-2. MUX Control Register (X4)

Bit	Function	Comments
0	Multiplex Control Bit 0	3 bit code addresses the appropriate RS-232 channel. Legal addresses are 1-6.
1	Multiplex Control Bit 1	
2	Multiplex Control Bit 2	
3	Program Baud Rate	Set to "1" to program addressed channel's baud rate. Set to "0" to program addressed channel's ASTRO.
4	Interrupt Enable	
5	Read Interrupt	Set to "1" to enable reading of interrupt vector.

2. Write to port XO with bits 0-3 used to select the appropriate baud rate. The Western Digital Dual Baud Rate Clock Generator (BR1941L) is utilized to provide the programmable baud rates. See the BR1941L spec sheet for detailed baud rate codes.

C. Interrupt Programming

Interrupts can be enabled by setting bit 4 of the MUX Control Register to a "1". Once set, any of the six channels can generate an interrupt to the CPU. A single line interrupt is used for all channels. To determine which channel has generated an interrupt, the following sequence must be programmed.

1. After receiving the interrupt, set up the MUX Control Register with bit 5 set on a "1" and bits 0-3 set to a "0".

2. Read port XO. The AM-300 will return the address of the channel that has generated the interrupt according to the following format:

Bit 7	MSB
Bit 6	
Bit 5	Interrupting
Bit 4	Channel Number
Bit 3	LSB
Bit 2	1 = Read Interrupt 0 = Write Interrupt

The channels have been prioritized such that I/O channel 1 has the highest priority and I/O channel 6 has the lowest.

RS-232 INTERFACE.

Three edge connectors are provided at the top of the AM-300 to allow connection to RS-232 compatible peripherals. Each connector contains interface signals for two I/O channels. The following RS-232 signals are provided:

Pin			
~~Inputs:~~ 3	1.	BB	Received Data
5	2.	CB	Clear to Send
6	3.	CC	Data Set Ready
8	4.	CF	Carrier Detector
~~Outputs:~~ 20	1.	CD	Data Terminal Ready
2	2.	BA	Transmitted Data
4	3.	CA	Request to Send
	4.	Misc	Miscellaneous

Figure 2-1 illustrates the standard cable configuration.

AM300.MAC


```
                        ;*************************************************************
                        ;                                                            *
                        ;              AM-300 TERMINAL INTERFACE DRIVER              *
                        ;                                                            *
                        ;*************************************************************
                        ;
                        ;Copyright (C) 1977, 1978, 1979 - Alpha Microsystems, Irvine CA 92174
                        ;
                        ;Edit History:
                        ;
                        ;25 August 79.  Shift BITs into left half to be AM-100/T compatible.
                        ;

                                .COPY   SYS
                        ;THE FOLLOWING TWO EQUATES DEFINE THE BOARD ADDRESS AND INTERRPUT LEVEL
                        ;THEY MUST BE CHANGED TO RUN THIS DRIVER AS A SECOND AM-300 HANDLER
                        ;THE INTERRUPT VECTOR JUMPER ON THE AM-100 CPU MUST ALSO BE WIRED IN
177770                  AMX=177770              ;BOARD ADDRESS
000003                  AMV=3                   ;INTERRUPT VECTOR LEVEL

                        DEFINE  PORTJ   PORT
                                OFFSET  OUT'PORT
                                WORD    0
                                OFFSET  IN'PORT
                                WORD    0
                                ENDM

                        ;********************
                        ;*      AM3         *
                        ;********************
                        ;TERMINAL DRIVER COMMUNICATIONS AREA
000000 000444           AM3:    BR      CHROUT          ;CHARACTER OUTPUT ROUTINE
000002 000400                   BR      INIT            ;INITIALIZE ROUTINE

                        ;********************
                        ;*      INIT        *
                        ;********************
                        ;INITIALIZE THE AM-300 PORT
                        ;R1 MUST CONTAIN THE BAUD RATE CODE (0-17)
000004 156503 000004    INIT:   MOVB    4(R5),R3        ;PICK UP THE INTERFACE ADDRESS
000010 004307                   ADDI    10,R3           ;MAKE INTO BAUD RATE CONTROL COMMAND
000012 150337 177774            MOVB    R3,@#AMX+4      ;  AND SET INTO MUX REGISTER
000016 150137 177770            MOVB    R1,@#AMX        ;SET BAUD RATE INTO RATE GENERATOR
000022 004347                   BICI    10,R3           ;STRIP OFF THE BAUD RATE CONTROL BIT
000024 150337 177774            MOVB    R3,@#AMX+4      ;  AND SELECT THE ASTRO
000030 152737 000011 177771     MOVB    #11,@#AMX+1     ;INITIALIZE THE ASTRO
000036 152737 000205 177770     MOVB    #205,@#AMX
                        ;STORE THE TERMINAL DEFINITION ADDRESS IN THE INPUT AND OUTPUT ROUTINES
000044 071167 000206            LEA     R1,IN1-12.      ;SET BASE INDEX
000050 004113                   ADDI    12.,R1          ;ADVANCE TO CORRECT ROUTINE PAIR
000052 073302                   SOB     R3,.-2
000054 130561 000002            MOV     R5,2(R1)        ;STORE THE TERMINAL DEFINITION ADDRESS
```

Figure 3-1. AM-300 Terminal Interface Driver (SH 1 of 3)

```
000060  130561  000010                  MOV     R5,10(R1)
                                ;INITIALIZE THE INTERRUPT VECTOR
000064  071167  000050                  LEA     R1,INTRPT       ;INDEX THE INTERRUPT ROUTINE
000070  133704  000050                  MOV     @#50,R4         ;INDEX THE INTERRUPT VECTOR TABLE BASE
000074  004407                          ADDI    16-<2*AMV>,R4   ;BUMP TO CORRECT VECTOR ENTRY
000076  020401                          SUB     R4,R1           ;MAKE ENTRY ADDRESS INTO AN OFFSET
000100  130114                          MOV     R1,@R4          ;STORE INTERRUPT ROUTINE OFFSET IN TABLE
000102  152737  000020  177774          MOVB    #20,@#AMX+4     ;ENABLE AM300 INTERRUPTS
000110  000037                  INX:    RTN
                                ;********************
                                ;*      CHROUT      *
                                ;********************
                                ;OUTPUT CHARACTER INITIATION ROUTINE
                                ;ENABLE THE ASTRO TRANSMITTER WHICH GENERATES AN INITIAL INTERRUPT
000112  131305                  CHROUT: MOV     @R3,R5          ;SET TERMINAL DEFINITION INDEX
000114  156503  000004                  MOVB    4(R5),R3        ;SET ASTRO ADDRESS
000120  004317                          ADDI    20,R3
000122  150337  177774                  MOVB    R3,@#AMX+4      ;SELECT ASTRO
000126  152737  000207  177770          MOVB    #207,@#AMX      ;ENABLE TRANSMITTER
000134  000062                          LCC     2               ;SET V-BIT TO DEQUEUE THE CLOCK ENTRY
000136  000037                          RTN
                                ;********************
                                ;*      INTRPT      *
                                ;********************
                                ;INTERRUPT HANDLER FOR MULTIPLEXED BOARD INTERRUPTS
000140  000012                  INTRPT: SAVE                    ;SAVE REGISTERS
000142  132767  000020  000002          MOV     #20,INLP+2      ;RESET THE INTERRUPT LOOP COUNT
000150  106327  000020          INLP:   DECB    #20             ;DECREMENT THE INTERRUPT LOOP COUNTER
000154  001442                          BEQ     INTX            ;  AND ALLOW CLOCK IF 20 SEQUENTIAL LOOPS
000156  152737  000040  177774          MOVB    #40,@#AMX+4     ;READ AM-300 INTERRUPTS
000164  153701  177770                  MOVB    @#AMX,R1
000170  006701                          TJMP    R1              ;DIRECTED JUMP ON DEVICE CODE + I/O FLAG
000172  000070                          OFFSET  INTX
000174  000066                          OFFSET  INTX
000176  000064                          OFFSET  INTX
000200  000062                          OFFSET  INTX
000202  000076  000000  000064          PORTJ   1
000212  000102  000000  000070          PORTJ   2
000222  000106  000000  000074          PORTJ   3
000232  000112  000000  000100          PORTJ   4
000242  000116  000000  000104          PORTJ   5
000252  000122  000000  000110          PORTJ   6
000262  152737  000020  177774  INTX:   MOVB    #20,@#AMX+4     ;ENABLE AM300 INTERRUPTS
000270  000011                          RRTT

                                ;********************
                                ;*      PORTIO      *
                                ;********************
                                ;ROUTINES FOR HANDLING THE INPUT AND OUTPUT INTERRUPTS FROM EACH PORT
                                ;THIS IS A BRUTE FORCE METHOD DUPLICATING THE CODE 6 TIMES FOR SPEED PURPOSES
                                DEFINE  PORTIO  PX
                                IN'PX:  MOV     #0,R5           ;SET TERMINAL DEFINITION ADDRESS
```

Figure 3-1. AM-300 Terminal Interface Driver (SH 2 of 3)

```
                                        BR      INPR
                                OUT'PX: MOV     #0,R5           ;SET TERMINAL DEFINITION ADDRESS
                                        BR      OUTPR
                                        ENDM

                                ;THE FOLLOWING MACRO CALLS SET UP THE ABOVE ROUTINES FOR THE SIX AM300 PORTS
000272  132705  000000  000441        PORTIO  1               ;PORT 1
000306  132705  000000  000433        PORTIO  2               ;PORT 2
000322  132705  000000  000425        PORTIO  3               ;PORT 3
000336  132705  000000  000417        PORTIO  4               ;PORT 4
000352  132705  000000  000411        PORTIO  5               ;PORT 5
000366  132705  000000  000403        PORTIO  6               ;PORT 6

                                ;INPUT CHARACTER PROCESSING
000402  156537  000004  177774 INPR:  MOVB    4(R5),@#AMX+4   ;SELECT THE PORT
000410  153701  177772          MOVB    @#AMX+2,R1      ;READ THE STATUS REGISTER
000414  122701  000002          BIT     #2,R1           ;CHECK FOR INPUT CHARACTER READY
000420  001404                  BEQ     INFI            ;  BUT SKIP TO OTHER IF NOT SO
000422  153701  177773          MOVB    @#AMX+3,R1      ;READ THE ASTRO DATA REGISTER
000426  000127                  TRMICP                  ;GO PROCESS THE CHARACTER
000430  000647                  BR      INLP

                                ;FALSE INPUT INTERRUPT - CHECK FOR DSR INTERRUPT
000432  123727  177770  001000 INFI:  BIT     @#AMX,#2_8.     ;BYPASS IF TRANSMITTER IS ENABLED
000440  001243                  BNE     INLP
000442  122701  000100          BIT     #100,R1         ;CHECK DATASET READY
000446  001640                  BEQ     INLP
000450  152737  000207  177770        MOVB    #207,@#AMX      ;ENABLE THE ASTRO TRANSMITTER
000456  000634                  BR      INLP

                                ;OUTPUT CHARACTER PROCESSING
000460  156537  000004  177774 OUTPR: MOVB    4(R5),@#AMX+4   ;SELECT THE PORT
000466  123727  177772  040000        BIT     @#AMX+2,#100_8. ;CHECK FOR DATA SET BUSY
000474  001405                  BEQ     OPRD            ;  AND GO TO FULL NELSON IF SO
000476  000130                  TRMOCP                  ;GET NEXT OUTPUT CHARACTER
000500  005201                  TST     R1              ;DATA AVAILABLE?
000502  100006                  BPL     OPRG            ;  YES
000504  042715  000200          BIC     #200,@R5        ;CLEAR THE OIP FLAG
000510  152737  000205  177770 OPRD:  MOVB    #205,@#AMX      ;DISABLE THE ASTRO TRANSMITTER FOR THIS PORT
000516  000614                  BR      INLP
000520  150137  177773        OPRG:  MOVB    R1,@#AMX+3      ;SEND CHARACTER TO ASTRO DATA REGISTER
000524  000611                  BR      INLP
000526                          END
```

Figure 3-1. AM-300 Terminal Interface Driver (SH 3 of 3)

SECTION IV
FUNCTIONAL THEORY OF OPERATION

4.0 INTRODUCTION.

The AM-300 I/O interface board contains integrated circuit elements for the necessary data processing for the performance of the functions as described in Sections I, II and III of this manual. This chapter describes the functional theory of operation of the circuit board and also provides information for each of the integrated circuit elements.

4.1 CIRCUIT BOARD OPERATION.

This circuit board provides six programmable I/O ports that interface with the system S-100 bus and RS-232 type peripherals. The functional block diagram is shown in Figure 4-1 and the circuit board schematic is contained in Section VI of this manual. Table 4-1 contains a list of the signals used in this circuit board with a definition of their functions.

4.1.1 Addressing.

Address data is received from the S-100 bus on lines A0-A7 and the data lines D00-D03.

The circuit board address (A3-A7) lines provide one input to comparator Z34. The other comparator input comes from the board address jumpers. The address code from jumpers on an address block permit user selection of the circuit board address in an eight port block. The address coding jumper wires are connected to either ground or +5V to generate the selected address. Signal ADRE (Address Enable) goes true when the input address compares with the address of the card.

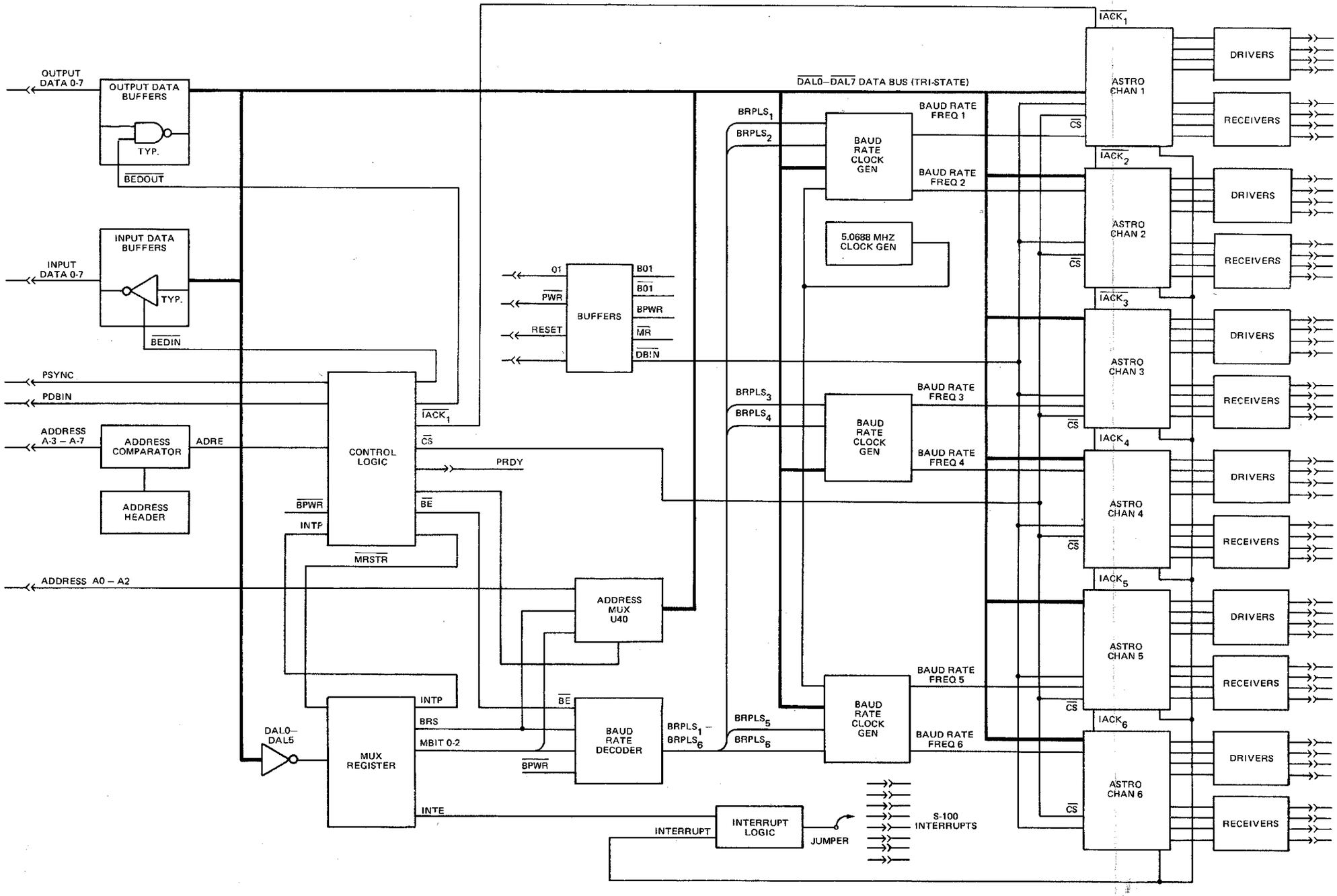


Figure 4-1. AM-300 I/O Circuit Board Functional Block Diagram

Table 4-1. AM-300 Signal List

SIGNAL	NAME	SCHEM PAGE	FUNCTION
AO-A7	Address Lines	2,3	Channel (Port) address lines.
ADRE	Address Enable	2	True when address input compares with address of card.
BE	Baud Enable	2,3,5	Enables Baud Rate Loading Decoder.
BEDIN	Buffer Enable Data Input	2,3,4	Enables DAL lines to CPU input.
BEDOUT	Buffer Enable Data Output	2,3,4	Enables DAL lines to CPU input.
BPWR	Write Enable	2,5,6,7 8,9,10,11	True when CPU is writing data.
BR1-BR6	Baud Rate Pulse 1-6	5,6,7,8 9,10,11	Enable pulse used to load baud rate into baud rate clock generator.

Table 4-1. (Con't) AM-300 Signal List

SIGNAL	NAME	SCHEM PAGE	FUNCTION
BRS	Baud Rate Select	2,3,5	1 = Program Baud Rate 0 = Program ASTRO
CS	Chip Select	3,6,7,8 9,10,11	Identifies a valid address on the DAL lines during read and write operations.
DAL0-DAL7	Data Access Lines	2,3,6,7 8,9,10, 11	Eight bit bi-directional bus used for transfer of data, control, status and address information.
DBIN	Read Enable	2,7,8,9 10,11	True when the CPU is reading data.
IACK1-IACK7	Interrupt Acknowledge	3,6,7, 8,9,10, 11	Indicates that an external I/O channel is ready to transmit or receive.
INTE	Interrupt Enable	2,11	Enables interrupt logic so the interrupting channel can output to the selected S-100 bus interrupt lines.

Table 4-1. (Con't) AM-300 Signal List

SIGNAL	NAME	SCHEM PAGE	FUNCTION
INTP	Interrupt Polling	2,3 9,10,11	Initiates polling sequence when chip select (CS) signal is true.
INTR	Interrupt	6,7,8 9,10,11	Low when one of the communication interrupt interrupt conditions occurs.
MBIT0-MBIT2	Baud Rate Bits	2,3,5	Baud Rate Code.
MR	Master Reset	2,3,6,7, 8,9,10,11	Reset signal from S-100 bus.
MRSTR	MUX Register Strobe	2	Clocks data from internal data bus into MUX Register.
5MHZ	5.0688 MHZ Clock	2,5	5.0688 MHZ clock.

The address must be loaded into the MUX register with signal ' BRS=0. This is accomplished by addressing the card with address lines A3-A7 and setting A2=1. Data lines DAL0-DAL2 contain the port address and are loaded into the MUX register by clock input MRSTR generated from A2 and BEDOUT. This address then becomes MBIT -MBIT applied to tri-state buffer U40 to DAL3-DAL5 for addressing the ASTRO modules. Address lines A0 and A1 then contain information to control the ASTRO registers as described in paragraph 4.1.4.

4.1.2 Baud Rate Programming.

The Baud Rate clock can be programmed for any one of 16 frequencies as shown in Table 4-2. Two instructions are required; the first to address the I/O port to be programmed and the second to set the baud rate.

The first input sets Bit 3 of the input to a 1. This sets DAL3, which is inverted in Z39 and sets DAL3 into the MUX Register by MRSTR from the addressing control logic. The D flip-flops in the MUX register store DAL3 setting BRS to a 1 enabling the Baud Rate Loading Decoder Z20. At the same time bits 0-2 contain the address of the I/O port to be programmed. This is set on DAL0-DAL3 and is also stored in the MUX register as MBIT -MBIT .

When the Baud Rate Loading decoder is enabled, one of its outputs BR -BR enables the selected clock generator.

The second input sets bits 0-3 with the selected baud rate code. This data is applied to DAL0-DAL3, is inverted on Z39, and enters the selected baud rate clock generator. The clock generator output on either pin 3 or 17 corresponds to the frequency of the input code.

4.1.3 Interrupts.

Interrupt capability can be enabled so that any of the six channels can generate an interrupt to the CPU. A single line interrupt is used, jumpered to any of the user selected interrupt lines PINT or VIO-VI7. Interrupt capability is enabled by setting bit 4 of the MUX control register to a 1. This is stored in the D flip-flop as INTE (Interrupt Enable) which enables the interrupt output lines.

When the interrupt is received by the CPU, bit 5 is set to a 1 and bits 0-3 set to 0. This data is stored in the D flip-flops as INTP (Read Interrupt), MUX control bits MBIT0-MBIT2 and BRS (Baud Rate Select). Since the Chip Select flip-flop is set, CS is low enabling all six ASTRO channels. INTP and CS are anded generating Interrupt Acknowledge IACK, to I/O channel 1. The channels are then polled, one at a time beginning with channel 1, which has the highest priority. If channel 1 does not have an interrupt, ASTRO number 1 generates a low signal (IACK) to ASTRO number 2 and on down the line. The first interrupting channel in the chain places its ID code on bit positions DAL3-DAL7, and bit 2 is set to a logical 1 for a read interrupt and to a logical 0 for a write interrupt. The next polling cycle resets the interrupt condition.

4.1.4 Data I/O.

All data, control, and status words are transferred over the Data Address Lines DAL0-DAL7. Data from the peripheral to the CPU passes through the DIN port on U36 and data from the CPU to the peripheral passes through the DOUT port on U37. All input/output terminology is referenced to the CPU so that a read or input takes data from the ASTRO and places it on the DAL lines, while a write or output places data from the DAL lines into the ASTRO.

A read operation is initiated when the CPU places an address on the address lines. When the circuit board is addressed and PSYNC is true, CS goes low and the six ASTRO modules compare the address in bits 3-7 on the DAL lines with their own address and become selected on a match condition. Bits A0 and A1 of the address are used to select ASTRO registers to read from as follows:

Bits 1&0	Selected Register
00	Control Register 1
01	Control Register 2
10	Status Register
11	Receiver Holding Register

When the Read Enable line (DBIN) to pin 39 is set to a low condition by the CPU, the ASTRO gates the contents of the addressed register onto the DAL. The read operation terminates and the device becomes unselected when both CS and DBIN return to a logic high. Bit 0 must be a logic 0 in read or write operations.

A write operation is initiated when the CPU places an address on the address lines. When the circuit board is addressed and PSYNC is true, CS goes low and the six astro modules compare the address in bits 3-7 on the DAL lines with their own address and become selected on a match condition. Bits A0-A2 of the address are used to select ASTRO registers to be written into as shown on the next page.

Bits 2-0	Selected Register
000	Control Register 1
001	Control Register 2
010	SYN and DLE Register
011	Transmitter Holding Register
100	MUX Control Register (U28)

When the Write Enable line (BPWR) to pin 4 of the ASTRO is set to a low condition by the CPU, the ASTRO gates the data from the DAL into the addressed register. If data is written into the transmitter holding register, the THRE status bit is cleared to a logical 0.

The 010 address loads both the SYN and DLE registers. After writing into the SYN register, the device is conditioned to write into the DLE if followed by another write pulse with the 010 address. Any intervening read or write operation with other addresses resets this condition such that the next 010 addresses the SYN register.

4.2 CIRCUIT MODULE DESCRIPTION.

This section describes the operation of the individual circuit packages (DIPS) contained on the AM-300 circuit board. Most of the data processing is handled by the Dual Baud Rate clock and the Asynchronous/Synchronous Receiver/Transmitter modules so these are described in detail. The control logic and interface modules are also described with logic and connection diagrams for each one.

4.2.1 Baud Rate Clock (U11, U19, U27).

The Baud Rate clock consists of a Western Digital BR1941L DIP with an external crystal generated clock with a frequency of 5,0688 MHz.

The crystal oscillator utilizes a voltage controlled oscillator (U41) with an external crystal. This oscillator runs continuously supplying the necessary clock frequency for the Baud Rate clock module.

The Baud Rate clock module generates any one of 16 selected clock rates determined by the input code. Each DIP contains two complete clock generators to supply two receiver/transmitter modules. A block diagram is shown in Figure 4-3 and pin connections are shown in Figure 4-2.

The output runs at a frequency selected by the address inputs according to Table 4-2.

TABLE 4-2. Clock Generator Output Frequencies

Transmit/Receive Address				Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16× Clock	Percent Error	Duty Cycle %	Divisor
D	C	B	A						
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.83	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

Pin Connections

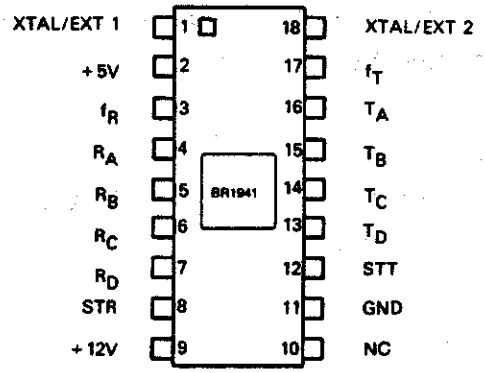


Figure 4-2. Baud Rate Clock Connections

Block Diagram

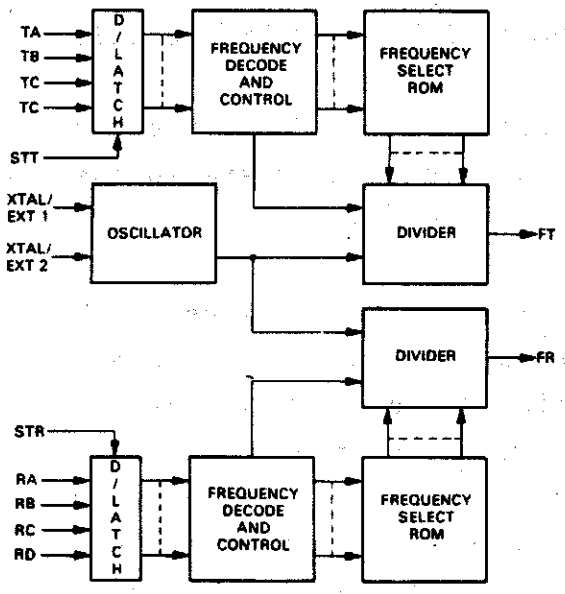


Figure 4-3. Baud Rate Clock Block Diagram

4.2.2 Asynchronous/Synchronous Receiver/Transmitter (ASTRO) (U7, U8, U15, U16, U23, U24).

The ASTRO is a device that interfaces a serial data communications channel to the parallel digital system. Each ASTRO module handles one full-duplex (receiving and transmitting) channel with either synchronous or asynchronous systems. Its operation is programmed by the processor via the data bus (DAL0-DAL7) and all data transfers are accomplished over the bus lines.

4.2.2.1 Organization.

The ASTRO pin connections are shown in Figure 4-4 and the block diagram is shown in Figure 4-5. The primary sections include receiver, transmitter, control, and bus interface. Input and output signals are described in Table 4.3.

Receiver Register. This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. The incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeros filling out any unused high-order bit positions.

Receiver Holding Register. This 8-bit parallel buffer register presents assembled receiver characters to the DAL bus lines when requested through a Read operation.

Comparator. The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

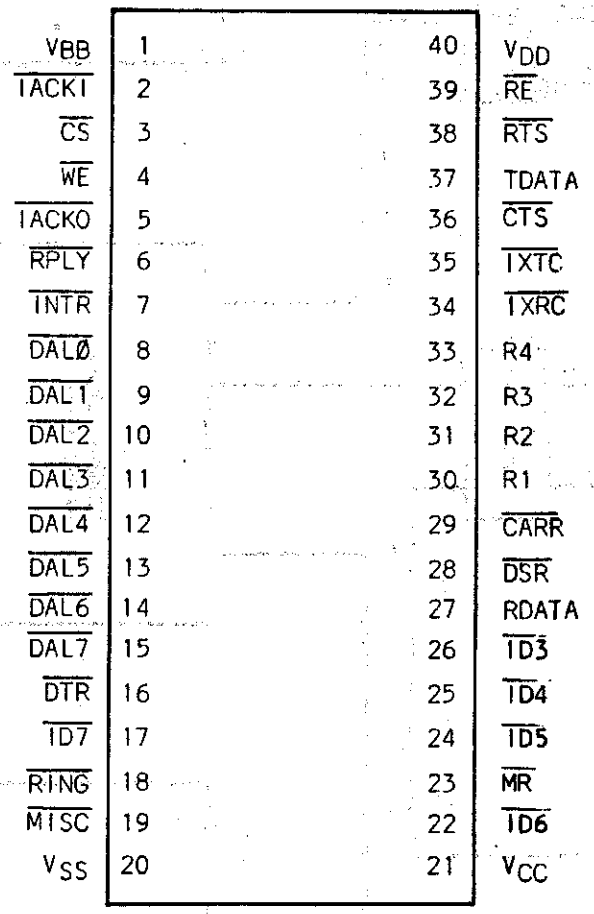


Figure 4-4. ASTRO Connections

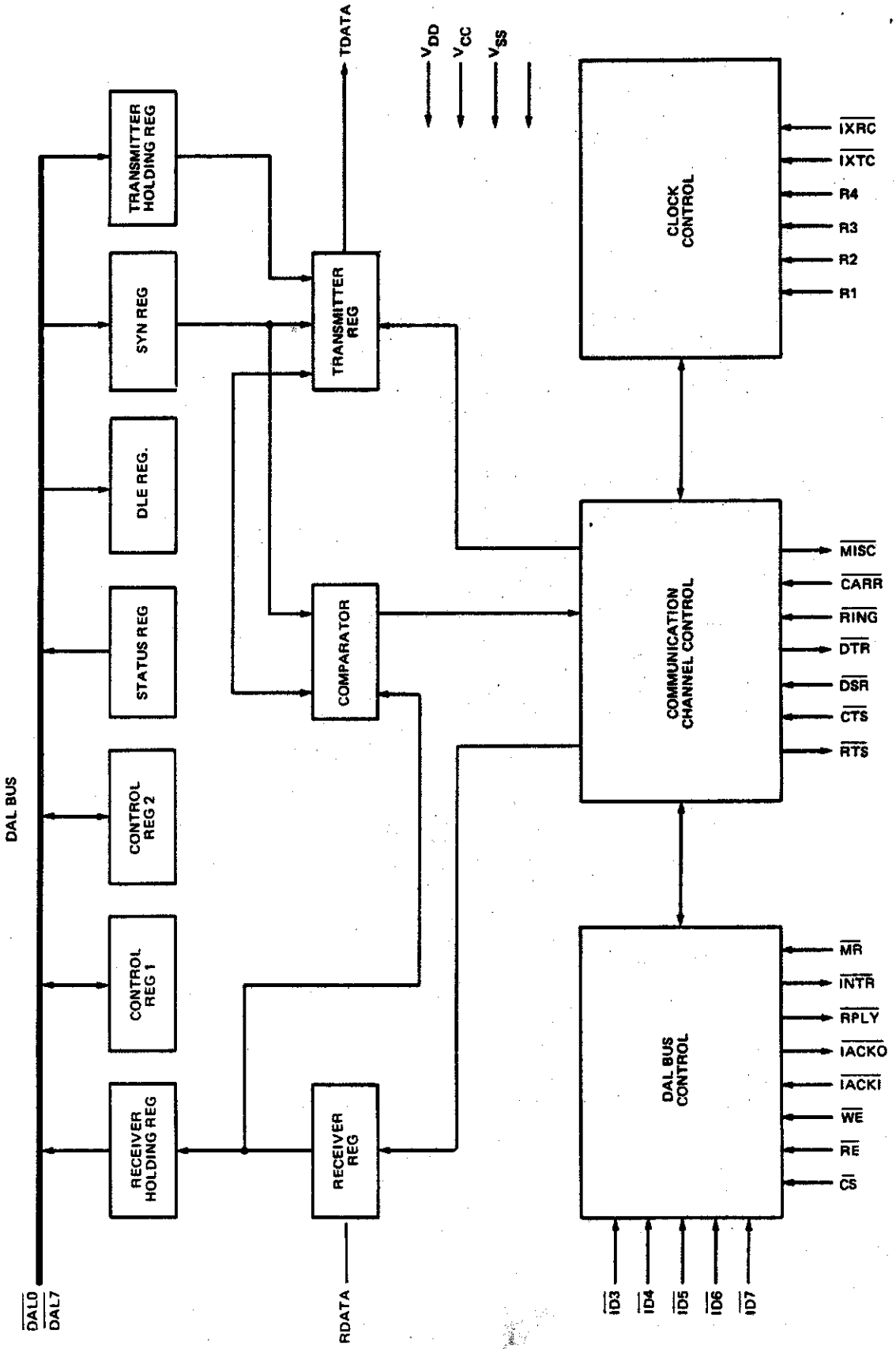


Figure 4-5. ASTRO Block Diagram

Table 4-3. ASTRO Signal List

SIGNAL	PIN	FUNCTION
VBB VCC VDD VSS POWER SUPPLIES	1 21 40 20	-5V +5V +12V Ground
$\overline{MR}$ MASTER RESET	23	The Control and Status Registers and other controls are cleared when this input is low.
$\overline{DAL0}$-$\overline{DAL7}$ DATA ACCESS LINES	8-15	Eight-bit bi-directional bus used for transfer of data, control, status, and address information.
$\overline{ID7}$-$\overline{ID3}$ SELECT CODE	17,22 24,25 26	Five input pins which when hardwired, assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
$\overline{CS}$ CHIP SELECT	3	The low logic transition of $\overline{CS}$ identifies a valid address on the DAL bus during Read and Write operations.

Table 4-3. (Con't) ASTRO Signal List

SIGNAL	PIN	FUNCTION
$\overline{RE}$ $\overline{READ\ ENABLE}$	39	This signal, when low, gates the contents of an addressed register from a selected ASTRO onto the DAL.
$\overline{WE}$ $\overline{WRITE\ ENABLE}$	4	This signal, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
$\overline{INTR}$ $\overline{INTERRUPT}$	7	This open drain output is made low when one of the communication interrupt conditions occur.
$\overline{IACKI}$ $\overline{INTERRUPT}$ $\overline{ACKNOWLEDGE\ IN}$	2	This input becomes low when polling takes place on the bus by the Controller to determine the interrupting source. When this signal is received, the ASTRO places its ID code on the DAL if it is requesting interrupt, otherwise it makes $\overline{IACKO}$ a low.
$\overline{IACKO}$ $\overline{INTERRUPT}$ $\overline{ACKNOWLEDGE\ OUT}$	5	This output is made a logic low in response to a low $\overline{IACKI}$ if the ASTRO receiving an $\overline{IACKI}$ input is not the interrupting device.