LH5749/J

CMOS 64K (8K × 8) OTPROM/EPROM

FEATURES

- 8,192 × 8 bit organization
- Access times:
  LH5749J: 55/70 ns (MAX.)
  LH5749: 70 ns (MAX.)
- Low power consumption:
  394 mW/(MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- High speed programming:
  SHARP original programming algorithm
  (32 second programming)
- Pin compatible with Bipolar PROM
- Packages:
  EPROM
  24-pin, 600-mil CERDIP
  OTPROM
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 300-mil SDIP
- JEDEC standard pinout (CERDIP/DIP)

DESCRIPTION

The LH5749J is a high-performance 64K, UV erasable, electrically programmable read-only-memory, organized as 8,192 × 8 bits. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming only 75 mA.

The LH5749J is packaged in 24-pin CERDIP which is pin-compatible to bipolar PROM.

The LH5749 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

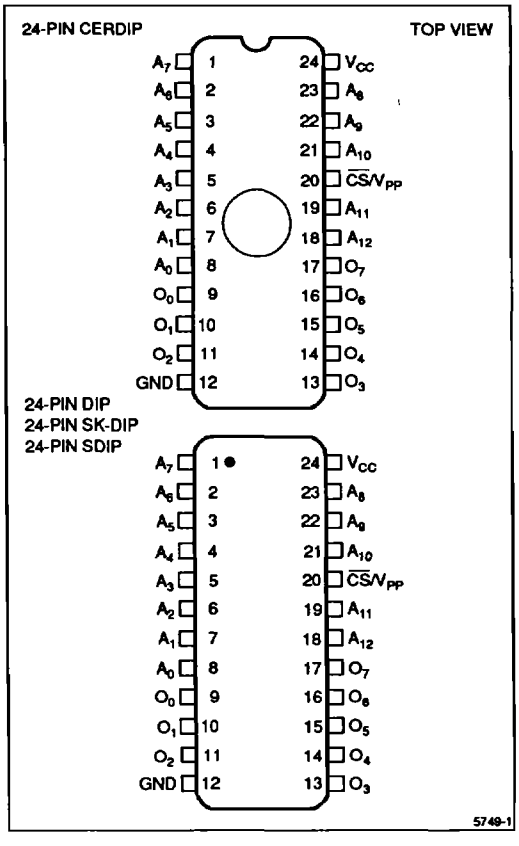

Figure 1. Pin Connections for CERDIP, DIP, SK-DIP and SDIP Packages

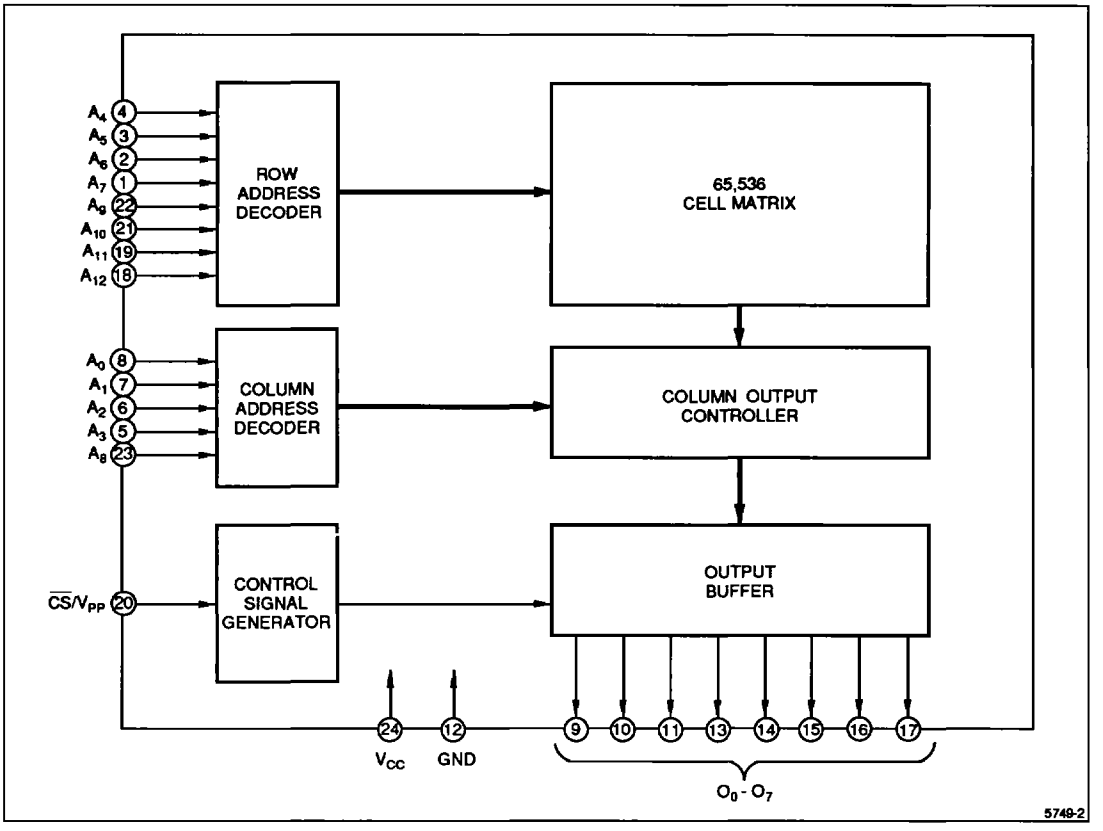

Figure 2. LH5749/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{12}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CS}/V_{PP}$	Chip Select/Program input	

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	CS/V_{PP}	V_{CC}	NOTE
Read	Read	Data out	L	+5 V	1
	Output disable	High-Z	H	+5 V	
Program	Program	Data in	+13 V	+6 V	
	Program inhibit	High-Z	H	+6 V	1
	Program verify	Data out	L	+6 V	

NOTE:
1. H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	$\overline{CS}/V_{PP}$	-0.6 to +14.0		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input "Low" voltage	V_{IL}	-0.1		0.8	
Input "High" voltage	V_{IH}	2.0		V_{CC} +0.3	

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	CMOS input			75	mA	1, 2
	I_{CC2}	TTL input			75	mA	1, 3
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.0		V_{CC} + 0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 5%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH5749J-55		LH5749J-70 LH5749/D/T-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address valid to output valid	t_{ACC}		55		70	ns
Chip select to output valid	t_{CS}		25		25	ns
Chip disable to output in High Z	t_{DF}	0	20	0	25	ns
Output hold from address	t_{OH}	10		10		ns

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

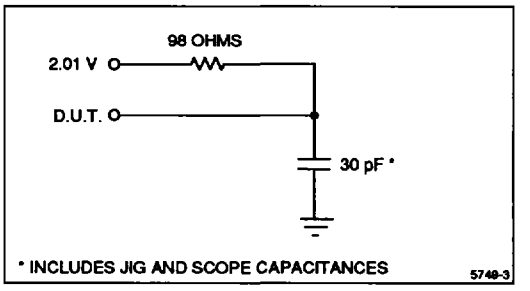

Figure 3. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

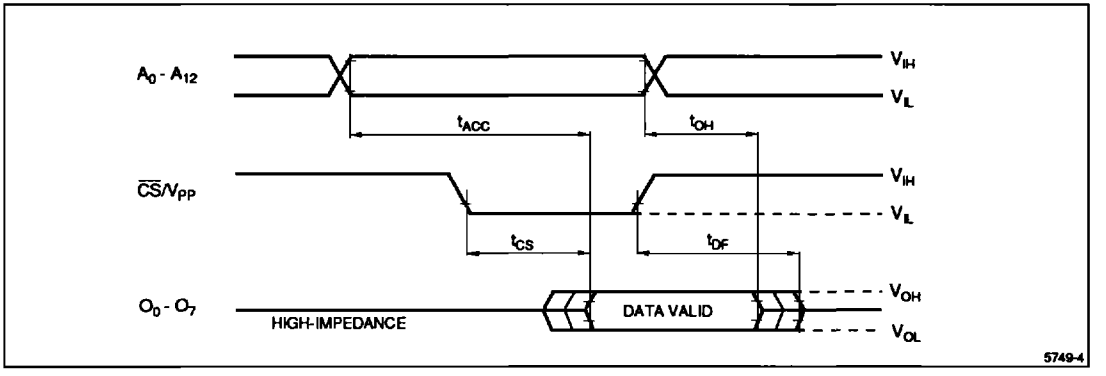

Figure 4. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.0	6.25	V
Program voltage	$\overline{CS}/V_{PP}$	12.7	13.0	13.3	V
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 6.0 V ± 0.25 V, $\overline{CS}/V_{PP}$ = 13.0 ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{IN} = V_{CC} or 0.45 V	-10		10	µA
$\overline{CS}/V_{PP}$ current	I_{PP}	Programming			75	mA
V_{CC} supply current	I_{CC}				75	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 16 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -4 mA	2.4			V

NOTES:

1. *The program pulse $\overline{CS}/V_{PP}$ must be applied after V_{CC} is stable and inhibited before V_{CC} is turned off.*
2. $\overline{CS}/V_{PP}$ must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (Program mode)

(V_{CC} = 6.0 V ± 0.25 V, $\overline{CS}/V_{PP}$ = 13.0 V ± 0.3 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address setup time	t_{AS}	2			µs
$\overline{CS}/V_{PP}$ rise time	t_R	1		100	µs
$\overline{CS}/V_{PP}$ fall time	t_F	1		100	µs
Data setup time	t_{DS}	2			µs
Chip select delay time	t_{CS}			30	ns
Address hold time	t_{AH}	0			µs
Data hold time	t_{DH}	2			µs
Output disable time	t_{DF}			30	ns
V_{CC} setup time	t_{VCS}	2			µs
$\overline{CS}/V_{PP}$ pulse width	t_{PW}	0.95	1.0	1.05	ms
Add $\overline{CS}/V_{PP}$ pulse width *	t_{OPW}	2.85		78.75	ms
Program pulse count	N	1		25	TIMES

* This width is defined by the Program Flowchart (Figure 6).

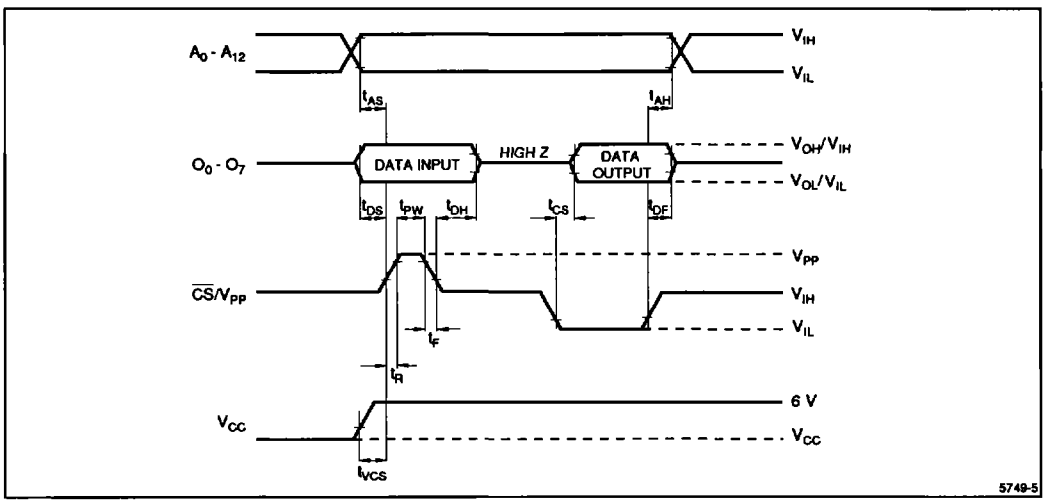

Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see Erasure section), the LH5749 and LH5749J have all 8192 × 8 bits in the "1", or high state. "0's" are loaded into the LH5749 and LH5749J through the procedure of programming.

The programming mode is entered when +13.0 V is applied to the $\overline{CS}/V_{PP}$ pin. A 0.1 µF capacitor between $\overline{CS}/V_{PP}$ and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH5749J to an ultraviolet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH5749J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH5749J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH5749J and similar devices, will erase with light sources having wavelength shorter than 4,000 Å. Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH5749J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will gradually erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

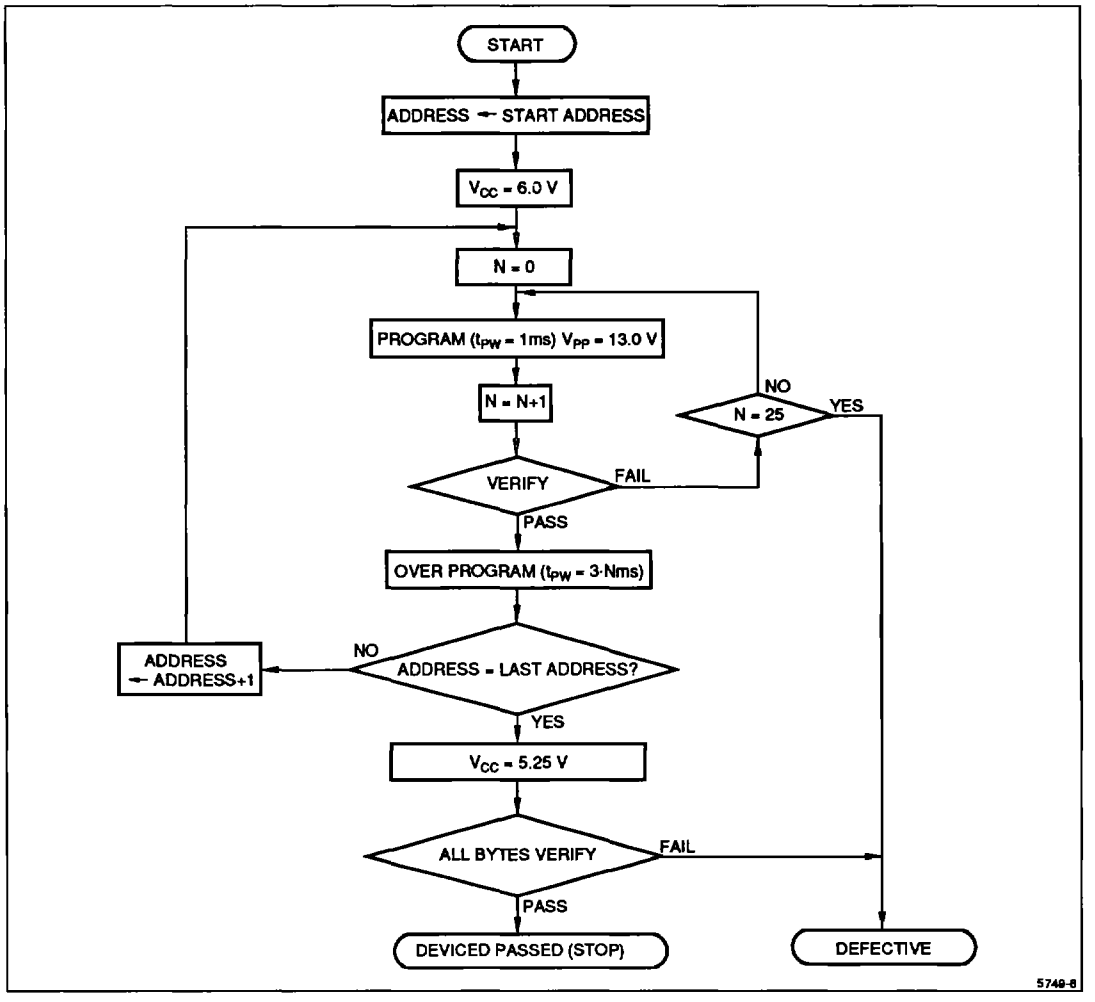

Figure 6. Programming Flowchart

ORDERING INFORMATION