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NTE2716
Integrated Circuit
NMOS, 16K UV Erasable PROM

Description:

The NTE2716 is a 16,384–bit (2048 x 8–bit) Erasable and Electrically Reprogrammable PROM in a 24–Lead DIP type package designed for system debug usage and similar applications requiring non-volatile memory that could be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

The NTE2716 operates from a single power supply and has a static power down mode.

Features:

- Single 5V Power Supply
- Automatic Power–Down Mode (Standby)
- Organized as 2048 Bytes of 8Bits
- TTL Compatible During Read and Program
- Access Time: 350ns
- Output Enable Active Level is User Selectable

Absolute Maximum Ratings: (Note 1)

All Input or Output Voltages (with respect to V_{SS}) . . . . . +6 to –0.3V
V_{PP} Supply Voltage (with respect to V_{SS}) . . . . . +28 to –0.3V
Temperature Under Bias (V_{PP} = 5V) . . . . . –10° to +80°C
Operating Temperature Range, T_{opr} . . . . . 0° to +70°C
Storage Temperature Range. T_{stg} . . . . . –65° to +125°C

Note 1. Permanent device may occur if “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to “Recommended Operating Conditions”. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Note 2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

Mode Selection:

Mode	Pin Number					
	9–11, 13–17 DQ	12 V_{SS}	18 $\overline{E}$/Progr	20 $\overline{G}$ (Note3)	21 V_{PP}	24 V_{CC}
Read	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{CC} (Note 3)	V_{CC}
Output Disable	High Z	V_{SS}	Don't Care	V_{IH}	V_{CC} (Note 3)	V_{CC}
Standby	High Z	V_{SS}	V_{IH}	Don't Care	V_{CC}	V_{CC}
Program	Data In	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IH}	V_{PPH}	V_{CC}
Program Verify	Data Out	V_{SS}	V_{IL}	V_{IL}	V_{PPH}	V_{CC}
Program Inhibit	High Z	V_{SS}	V_{IL}	V_{IH}	V_{PPH}	V_{CC}

Note 3. In Read Mode if $V_{PP} \geq V_{IH}$, then $\overline{G}$ (active low)
$V_{PP} \leq V_{IL}$, then G (active high)

Capacitance: (f = 1MHz, T_A = +25°C, periodically sampled rather than 100% tested)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	4.0	6.0	pF
Output capacitance	C_{out}	V_{out} = 0V	–	8.0	12.0	pF

Note 4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$

DC Operating Conditions and Characteristics: (Full Operating Voltage and Temperature Range unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Recommended DC Read Operating Conditions						
Supply Voltage	V_{CC}, V_{PP}	Note 5	4.75	5.0	5.25	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}+1.0	V
Input Low Voltage	V_{IL}		–0.1	–	+0.8	V
Recommended DC Operating Conditions						
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	I_{in}	V_{in} = 5.25V	–	–	10	µA
Output Leakage Current	I_{LO}	V_{out} = 5.25V, $\overline{G}$ = 5V	–	–	10	µA
V_{CC} Supply Current (Standby)	I_{CC1}	$\overline{E}$/Progr = V_{IH}, $\overline{G}$ = V_{IL}	–	–	25	mA
V_{CC} Supply Current (Active)	I_{CC2}	Outputs Open, $\overline{G}$ = $\overline{E}$/Progr = V_{IL}	–	–	100	mA
V_{CC} Supply Current	I_{PP1}	V_{PP} = 5.25V, Note 5	–	–	5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = –400µA	2.4	–	–	V

Note 5. V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would then be the sum of I_{PP1} and I_{CC}.

AC Operating Conditions and Characteristics: (Full Operating Voltage and Temperature Range, Note 6, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Address Valid to Output Valid	t_{AVQV}	$\overline{E}$/Progr = $\overline{G}$ = V_{IL}	–	–	350	ns
$\overline{E}$/Progr to Output Valid	t_{ELQV}	Note 7	–	–	350	ns
Output Enable to Output Valid	t_{GLQV}	$\overline{E}$/Progr = V_{IL}	–	–	150	ns
$\overline{E}$/Progr to High Z Output	t_{EHQZ}		0	–	100	ns
Output Disable to High Z Output	t_{GHQZ}	$\overline{E}$/Progr = V_{IL}	0	–	100	ns
Data Hold from Address	t_{AXDX}	$\overline{E}$/Progr = G = V_{IL}	0	–	–	ns

Note 6. Input Pulse Levels . . . . . 0.8V and 2.2V
Input Rise and Fall Times 20ns
Input and Output Timing Levels . . . . 2.0 and 0.8V

Note 7. t_{ELQV} is referenced to $\overline{E}$/Progr or stable address, whichever occurs last.

DC Programming Conditions and Characteristics: (T_A = +25°C ±5°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Recommended Programming Operating Conditions						
Supply Voltage	V_{CC}, V_{PPL}		4.75	5.0	5.25	V
	V_{PPH}		24.0	25.0	26.0	V
Input High Voltage for Data	V_{IH}		2.2	–	V_{CC}+1.0	V
Input Low Voltage for Data	V_{IL}		–0.1	–	+0.8	V
Programming Operating DC Characteristics						
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	I_{LI}	V_{in} = 5.25V/0.45V	–	–	10	µA
V_{PP} Programming Pulse Supply Current	I_{PP2}	V_{PP} = 25V ±1V, $\overline{E}$/Progr = V_{IH}	–	–	30	mA
V_{CC} Supply Current	I_{CC}	Outputs Open	–	–	160	mA

AC Programming Operating Conditions and Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Address Setup Time	t_{AVEH}		2.0	–	–	µs
Output Enable High to Program Pulse	t_{GHEH}		2.0	–	–	µs
Data Setup Time	t_{DVEH}		2.0	–	–	µs
Address Hold Time	t_{ELAX}		2.0	–	–	µs
Output Enable Hold Time	t_{ELGL}		2.0	–	–	µs
Data Hold Time	t_{ELQZ}		2.0	–	–	µs
V_{PP} Setup Time	t_{PHEH}		0	–	–	ns
V_{PP} to Enable Low Time	t_{ELPL}		0	–	–	ns
Output Disable to High Z Output	t_{GHQZ}		0	–	150	ns
Output Enable to Valid Data	t_{GLQV}	$\overline{E}$/Progr = V_{IL}	–	–	150	ns
Program Pulse Width	t_{EHEL}	Note 8	1	–	55	ms
Program Pulse Rise Time	t_{PR}		5	–	–	ns
Program Pulse Fall Time	t_{PF}		5	–	–	ns

Note 8. If shorter than 45ms (min) pulses are used, the same number of pulses should be applied after the specific data has been verified to ensure that good programming levels have been written.

Programming Instructions:

Before programming, the memory should be submitted to a full ERASE operation to ensure every bit in the device is in the “1” state (represented by Output High). Data are entered by programming zeros (Output Low) into the required bits. The words are addressed the same way as in the READ operation. A programmed “0” can only be changed to a “1” by ultraviolet light erasure.

To set the memory up for Program Mode, the V_{PP} input (Pin21) should be raised to +25V. The V_{CC} supply voltage is the same as for the Read operation and $\overline{G}$ is at V_{IH}. Programming data is entered in 8–bit words through the data out (DQ) terminals. Only “0 s” will be programmed when “0 s” and “1 s” are entered in the 8–bit data word.

After address and data setup, a program pulse (V_{IL} to V_{IH}) is applied to the $\overline{E}$/Progr input. A program pulse is applied to each address location to be programmed. To minimize programming time, a 2ms pulse width is recommended. The maximum program pulse width is 55ms; therefore, programming must not be attempted with a DC signal applied to the $\overline{E}$/Progr input.

Multiple NTE2716s may be programmed in parallel by connecting together like inputs and applying the program pulse to the $\overline{E}$/Progr inputs. Different data may be programmed into multiple NTE2716s connected in parallel by using the PROGRAM INHIBIT mode. Except for the $\overline{E}$/Progr pin, all like inputs (including Output Enable) may be common.

The PROGRAM VERIFY mode with V_{PP} at +25V is used to determine that all programmed bits were correctly programmed.

Read Operation:

After access time, data is valid at the outputs in the READ mode. With stable system addresses, effectively faster access time can be obtained by gating the data onto the bus with Output Enable.

The Standby mode is available to reduce active power dissipation. The outputs are in the high impedance state when the $\overline{E}$/Progr input pin is high (V_{IH}) independent of the Output Enable input.

Erasing Instructions:

The NTE2716 can be erased by exposure to high intensity shortwave ultraviolet light, with a wavelength of 2537 angstroms. The recommended integrated dose (i.e. UV–intensity X exposure time) is $15Ws/cm^2$. As an example, using the “Model 30–000” UV–Eraser (Turner Designs, Mountain View, CA 94043) the ERASE–time is 36 minutes. The lamps should be used without shortwave filters and the NTE2716 should be positioned about one inch away from the UV–tubes.

Recommended Operating Procedures:

After erasure and reprogramming of the EPROM, it is recommended that the quartz window be covered with an opaque self–adhesive cover. It is important that the self–adhesive cover not leave any residue on the quartz if it is removed to allow another erasure.

Pin Connection Diagram