GENERAL INSTRUMENT | **28C04** | PRELIMINARY INFORMATION

4K (512 x 8) CMOS Electrically Erasable PROM

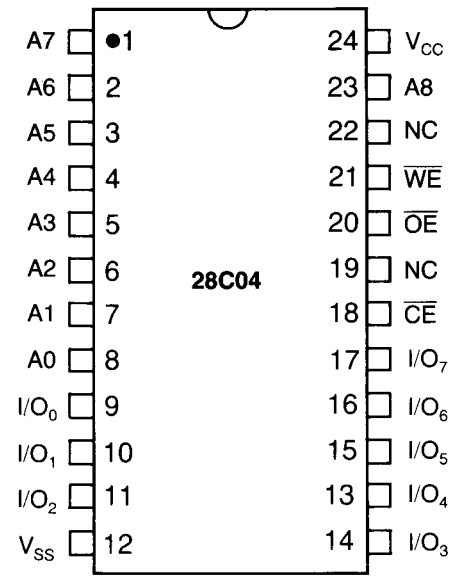
34 Res orig 006048 6048 GI

FEATURES

- Fast Read Access Time — 150ns
- High Performance CMOS Technology for Low Power Dissipation
  - — 100μA Standby
  - — 30mA Active
- Fast Byte Write Time — 200μs or 1ms
- High Endurance 10^5 Erase/Write Cycles
- Automatic Write Operation
  - — Internal Control Timer
  - — Auto-Clear Before Write Operation
  - — On-Chip Address and Data Latches
- $\overline{\text{Data}}$ Polling
- Chip Clear Function
- Enhanced Data Protection
  - — V_{CC} Detector
  - — Power-Up Timer
- Data Retention > 10 Years
- 5-Volt-Only Operation
- JEDEC-Approved Byte-Wide Pinout
- Full Commercial and Industrial Temperature Ranges:
  - 0° to +70°C Commercial (28C04)
  - −40° to +85°C Industrial (28C04I)
- Also Available in Military Temperature Range:
  - −55° to +125°C (28C04MR)

PIN CONFIGURATION

Top View



PIN NAMES

A_0–A_8	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_0–I/O_7	DATA INPUTS/OUTPUTS
NC	NO CONNECT
V_{CC}	+5V POWER
V_{SS}	GROUND

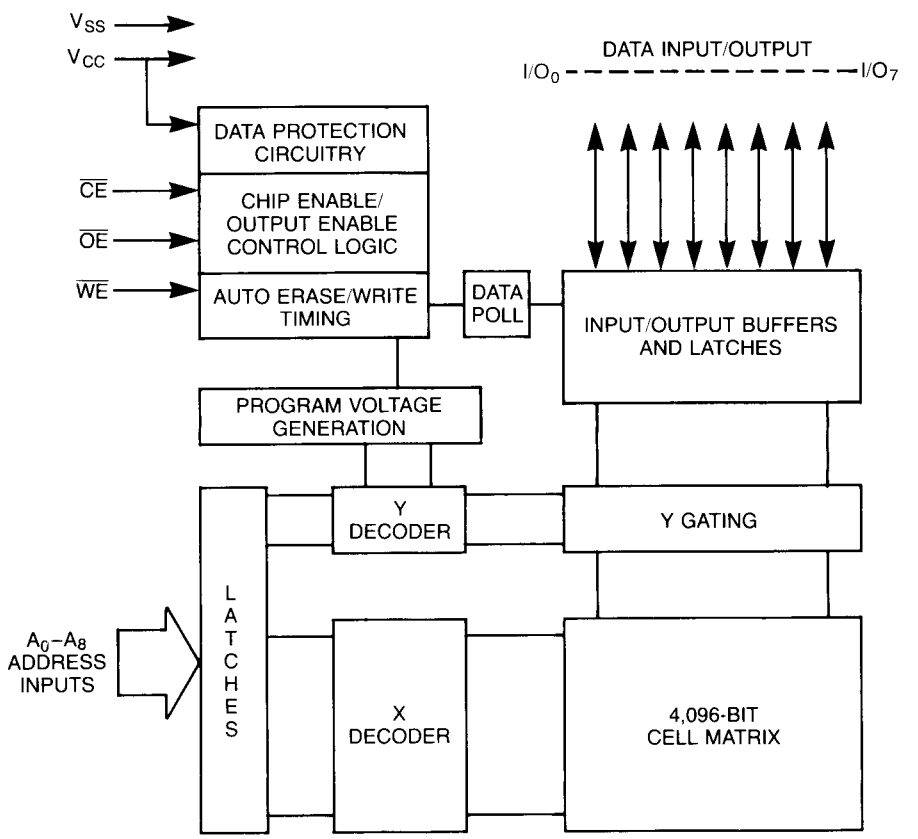
DESCRIPTION

The General Instrument Microelectronics 28C04 is a low-power, high-performance 512 x 8-bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with General Instrument's advanced and reliable non-volatile CMOS technology.

The 28C04 is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write," the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear the addressed memory cells and write the latched data using an internal control timer. Data polling can be used to determine whether or not the write cycle is complete.

The 28C04 operates from a single 5V supply and is packaged in standard JEDEC-approved packages. All necessary programming voltages are internally generated and timed.

CMOS technology in the device offers a combination of fast access times (150ns (28C04-15)) and low power dissipation (30mA). When the chip is deselected, the standby current is less than 100μA. The 28C04's fast memory access time allows for direct polling with microprocessors without waiting.



FUNCTIONAL BLOCK DIAGRAM
28C04

DEVICE OPERATION

The General Instrument 28C04 has four basic modes of operation — read, standby, write inhibit, and byte write — as outlined in the following table.

PIN / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
READ	L	L	H	D_{OUT}
STANDBY	H	X	X	High Z
WRITE INHIBIT	H	X	X	High Z
WRITE INHIBIT	X	L	X	—
WRITE INHIBIT	X	X	H	—
BYTE WRITE	L	H	L	D_{IN}
BYTE CLEAR	Automatic Before Each "Write"			

READ MODE

The 28C04 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The 28C04 is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

DATA PROTECTION

To ensure data integrity, especially during critical power up and power down transitions, the following enhanced data protection circuits are incorporated.

First, an internal V_{CC} detect (3.8 volts typical) will inhibit the initiation of a non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip. In addition, on power up an internal timer (5ms typical) will inhibit the recognition of any program operation. During this period, all normal read functions will be operational. After both the V_{CC} detection and the internal timer have elapsed, normal programming operation can be performed.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 20ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high, or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

WRITE MODE

The 28C04 has a write cycle similar to that of a static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched.

DATA POLLING

The 28C04 features Data Polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O_7 (I/O_0 to I/O_6 are indeterminable). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip. This eliminates the need for external hardware.

OPTIONAL CHIP CLEAR

All data can be cleared to ones in a single chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

RETENTION/ENDURANCE

Read retention for data written into the 28C04 is greater than 10 years, with up to 10^5 write cycles. There is no limit to the number of times data can be read.

ELECTRICAL CHARACTERISTICS
Absolute Maximum Ratings

Temperature Under Bias . . . . . −10°C to +85°C (Industrial: −50°C to +95°C)
Storage Temperature . . . . . −65°C to +125°C
All Input Voltages with Respect to Ground . . . . . +6.25V to −0.6V
All Output Voltages with Respect to Ground . . . . . V_{CC} +0.6V to −0.6V
Voltage on $\overline{OE}$ with Respect to Ground . . . . . +13.5V to −0.6V

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

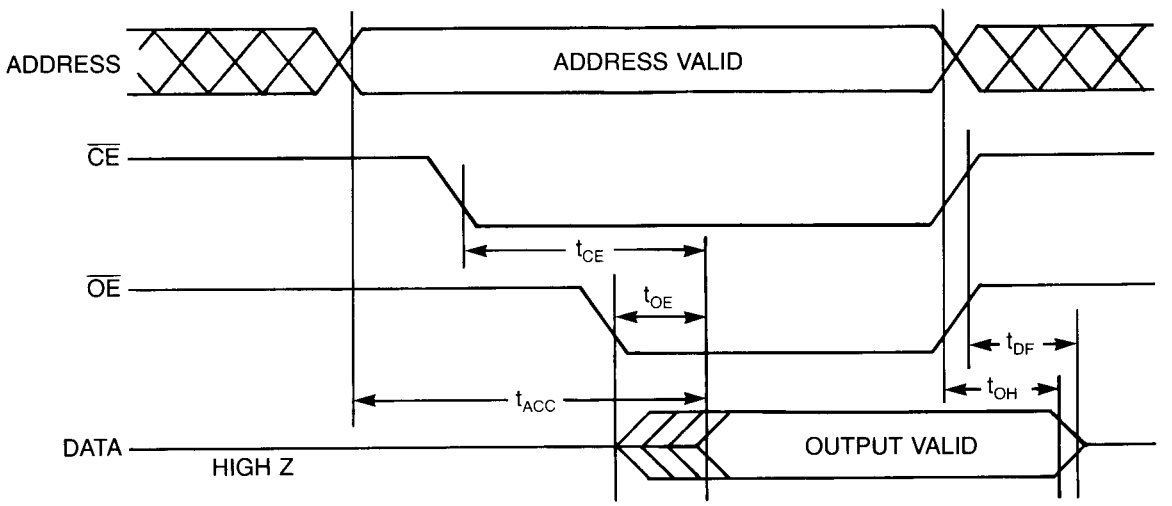
DC CHARACTERISTICS

28C04 T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, unless otherwise specified.
28C04I T_A = −40°C to +85°C, V_{CC} = 5V ± 10%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage Current		10	µA	−0.1 to V_{CC} +1
I_{LO}	Output Leakage Current		10	µA	−0.1 to V_{CC} +0.1
I_{CC}	V_{CC} Current Standby		100 2 3	µA mA mA	$\overline{CE}$ = V_{CC} −0.3 to V_{CC} +1 $\overline{CE}$ = V_{IH} (0°C to +70°C) $\overline{CE}$ = V_{IH} (−40°C to +85°C)
I_{CC}	V_{CC} Current Active		30	mA	f = 1 MHz
V_{IL}	Input Low Voltage	−0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400µA

AC CHARACTERISTICS — READ CYCLE

SYM	PARAMETER	28C04-15		28C04-20		28C04-25		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{ACC}(1)	Address to Output Delay		150		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		150		200		250	ns	$\overline{OE}$ = V_{IL}
t_{OE}	$\overline{OE}$ to Output Delay		70		80		120	ns	$\overline{CE}$ = V_{IL}
t_{DF}(2,3)	$\overline{OE}$ High to Output Float	0	50	0	55	0	70	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first.		10		10		10	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}



Notes:
1. $\overline{OE}$ can be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. This parameter is only sampled and is not 100% tested.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

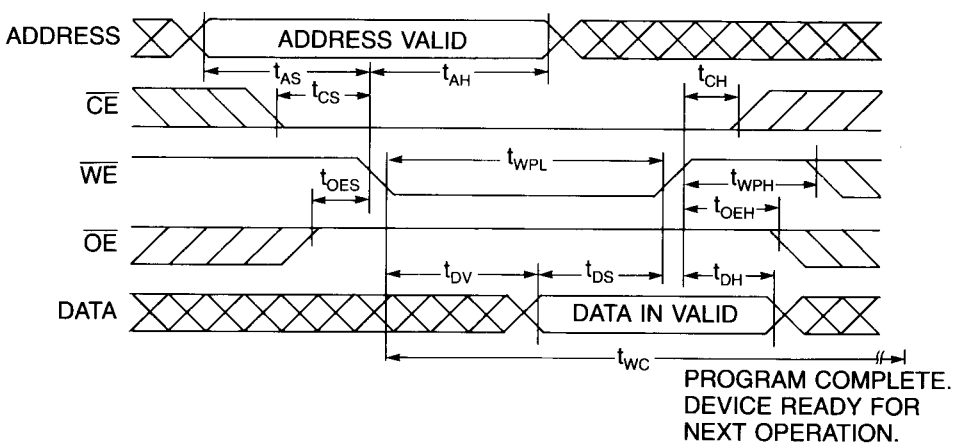
AC CHARACTERISTICS — BYTE WRITE CYCLE

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
t_{AS}	Address Setup Time	10		ns	
t_{AH}	Address Hold Time	50		ns	
t_{CS}	Write Setup Time	0		ns	
t_{CH}	Write Hold Time	0		ns	
t_{WPL}	Write Pulse Low Time	100		ns	Note 1
t_{WPH}	Write Pulse High Time	50		ns	
t_{OES}	Output Enable Setup Time	10		ns	
t_{OEH}	Output Enable Hold Time	10		ns	
t_{DV}	Data Valid Time		1000	ns	Note 2
t_{DS}	Data Setup Time	50		ns	
t_{DH}	Data Hold Time	10		ns	
t_{WC}	Write Cycle Time 28C04		1	ms	Typically 0.5ms
	28C04F		200	μs	Typically 100μs

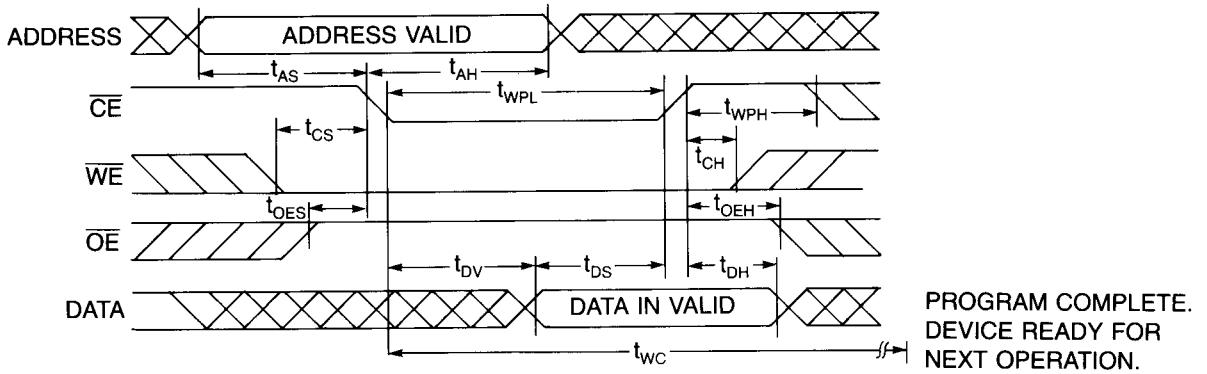
Note 1: A write cycle can be initiated either by $\overline{CE}$ or $\overline{WE}$ going low, whichever occurs last. The data are latched on the positive edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.

Note 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first.

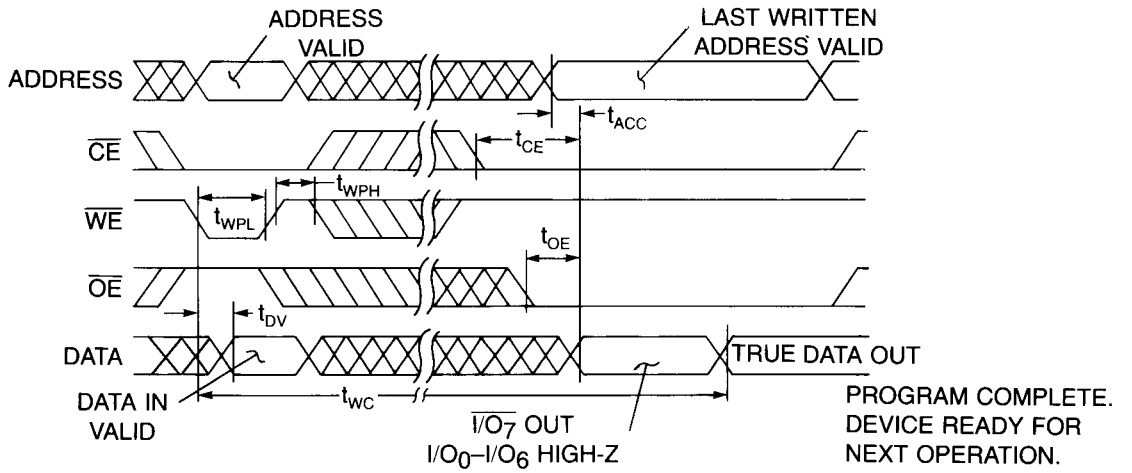
$\overline{WE}$ CONTROLLED WRITE CYCLE



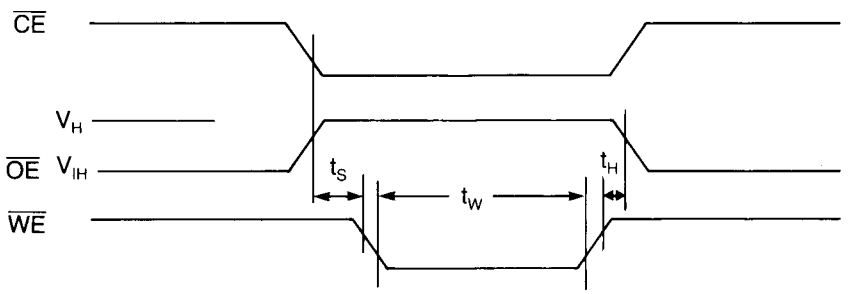
$\overline{CE}$ CONTROLLED WRITE CYCLE



$\overline{DATA}$ POLLING

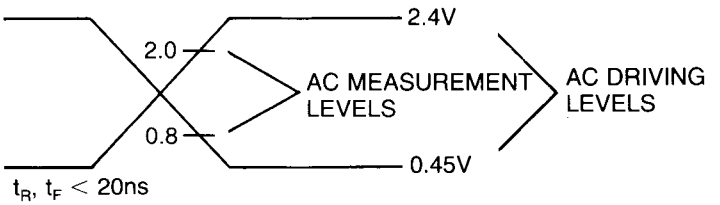


CHIP CLEAR



NOTE:
t_w = 10 ms
t_s = 1 μs
t_H = 1 μs
V_H = 12.0 to ± 0.5V

AC TESTING, INPUT AND OUTPUT WAVEFORMS



AC testing inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.