INTERSIL

IM6657/IM6658 8192 Bit CMOS UV Erasable PROM

FEATURES

- Organization—IM6657: 2048 x 4
  IM6658: 1024 x 8
- Low Power—550μW Maximum Standby
- High Speed
  —300ns 10V Access Time for IM6657/58 AI
  —450ns 5V Access Time for IM6657/58
- Single +5V supply operation
- UV erasable
- Synchronous operation for low power dissipation
- Three-state outputs and chip select for easy system expansion
- Full −55°C to +125°C MIL range devices—IM6657/58 M, IM6657A/68A M
- Fully compatible with Intersil standard CMOS ROM/EPROM family

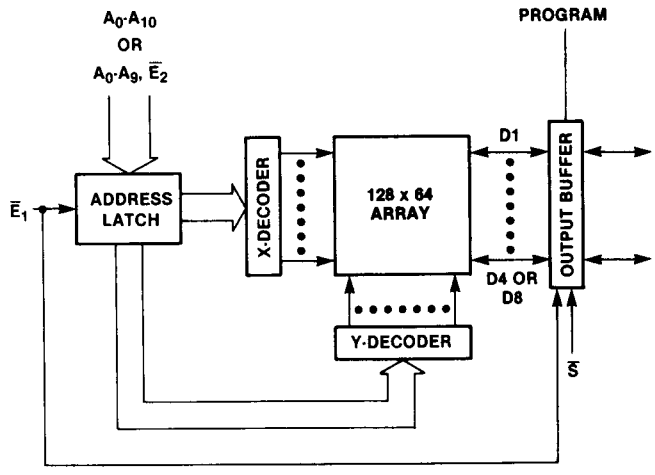
GENERAL DESCRIPTION

The Intersil IM6657 and IM6658 are fully decoded 8192 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Intersil's advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

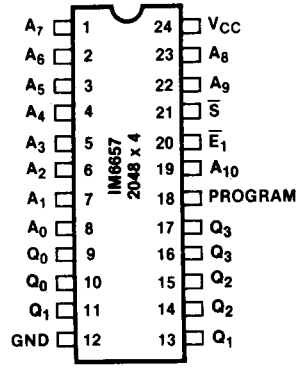
The IM6657 and IM6658 are specifically designed for program development applications where rapid program change turn-around is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

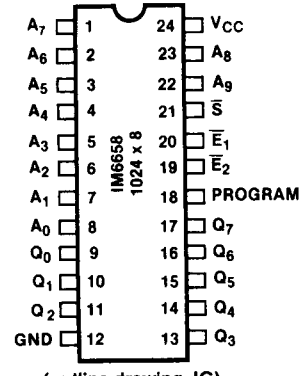
The IM6657 and IM6658 are fully compatible with standard CMOS Read Only Memories, the IM6653/54 4K CMOS EPROMs and the IM6316 16K CMOS ROM.

BLOCK DIAGRAM



PIN CONFIGURATION





(outline drawing JG)

ORDERING INFORMATION

24 Pin CERDIP PACKAGE	SELECTION/TEMPERATURE			
	INDUSTRIAL		MILITARY	
	5V	10V	5V	10V
IM6657/58	IJG	AIJG	MJG	AMJG

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ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{CC} 11V

Input or Output Voltage Supplied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
- Temperature
  - Industrial ..... −40°C to +85°C
  - Military ..... −55°C to +125°C
- Voltage
  - 6657/58 AI, AM 4.5-10.5V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4.5V to 10.5V, T_A = Operational Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6657/58AI, AM		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1, \overline{S}$	V_{CC} −2.0		V
	V_{IH}	Address Pins, $\overline{E}_2$	V_{CC} −2.0		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \le V_{IN} \le V_{CC}$	−1.0	1.0	µA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC} −0.01		V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$		GND +0.01	
Output Leakage	I_{OZ}	$GND \le V_O \le V_{CC}$	−1.0	1.0	µA
Standby Supply Current	I_{CC}	$V_{IN} = V_{CC}$		100	
Operating Supply Current	I_{CCOP}	f = 1 MHz		25	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

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Note 1: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, C_L = 50pf, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6657/58 AI		IM6657/58 AM		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		300		350	ns
Output Enable Time	TSLQV		60		70	
Output Disable Time	$TE_1HQZ/TSHQZ$		60		70	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	125		125		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	300		350		
Address Setup Time	$TAVE_1L$	0		0		
Address Hold Time	TE_1LAX	60		60		
Chip Enable Setup Time (6658)	TE_2VE_1L	0		0		
Chip Enable Hold Time (6658)	TE_1LE_2X	60		60		

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{CC} ..... +8.0V

Input or Output Voltage Supplied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
- Temperature
  - Industrial ..... −40°C to +85°C
  - Military ..... −55°C to +125°C
- Voltage
  - 6657/58 I 4.5-5.5
  - 6657/58 M 4.5-5.5

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ±10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6657/58I, M		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\bar{E}_1, \bar{S}$	V_{CC} −2.0		V
	V_{IH}	Address Pins E_2	V_{CC} −2.0		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \le V_{IN} \le V_{CC}$	−1.0	1.0	μA
Logical "1" Output Voltage	V_{OH2}	$I_{OUT} = 0$	V_{CC} −0.01		V
Logical "1" Output Voltage	V_{OH1}	I_{OH} = −0.2mA	2.4		
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$		GND +0.01	
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 2.0mA		0.45	
Output Leakage	I_{OZ}	$GND \le V_O \le V_{CC}$	−1.0	1.0	μA
Standby Supply Current	I_{CC}	$V_{IN} = V_{CC}$		100	
Operating Supply Current	I_{CCOP}	f = 1 MHz		15	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

Note 1: These parameters guaranteed but not 100% tested.

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AC CHARACTERISTICS

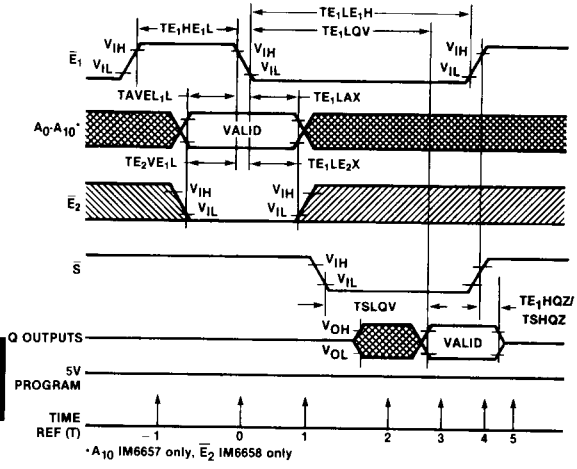
TEST CONDITIONS: V_{CC} = 5V ±10%, C_L = 50pf, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6657/58 I		IM6657/58 M		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\bar{E}_1$	TE_1LQV		450		600	ns
Output Enable Time	TSLQV		130		150	
Output Disable Time	$TE_1HQZ/TSHQZ$		130		150	
$\bar{E}_1$ Pulse Width (Positive)	TE_1HE_1L	140		150		
$\bar{E}_1$ Pulse Width (Negative)	TE_1LE_1H	450		600		
Address Setup Time	$TAVE_1L$	0		0		
Address Hold Time	TE_1LAX	90		100		
Chip Enable Setup Time (6658)	TE_2VE_1L	0		0		
Chip Enable Hold Time (6658)	TE_1LE_2X	90		100		

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8, 22-23	A_0-A_7, A_9-A_8	—	Address Lines
9-11, 13-17	Q_0-Q_7	—	Data Out lines, 6658
	Q_0-Q_3	—	Data Out lines, 6657
12	GND	—	
18	Program	—	Programming pulse input
20	$\overline{E}_1$	L	Strobe line, latches address lines and, on 6658, Chip enable $\overline{E}_2$
21	$\overline{S}$	L	Chip select line, must be low for valid data out
19	A_{10}	—	Additional address line for 6657
	$\overline{E}_2$	L	Chip enable line, latched by Chip enable $\overline{E}_1$ on 6658
24	V_{CC}	—	Chip V^+ Supply

READ CYCLE TIMING



*A_{10} IM6657 only, $\overline{E}_2$ IM6658 only

READ MODE OPERATION

In a typical READ operation address lines and chip enable $\overline{E}_2$* are latched by the falling edge of chip enable $\overline{E}_1$ (T = 0). Valid data appears at the outputs one access time (TE_1L-QV) later, provided level-sensitive chip select line $\overline{S}$ is low (T = 3). Data remains valid until either $\overline{E}_1$ or $\overline{S}$ returns to a high level (T = 4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}_2$ must be valid one setup time before ($TAVE_1L$), and one hold time after (TE_1LAX), the falling edge of $\overline{E}_1$ starting the read cycle. Before becoming valid, Q output lines become active (T = 2). The Q output lines return to a high-Z state one output disable time (TE_1HQZ) after any rising edge on $\overline{E}_1$ or $\overline{S}$.

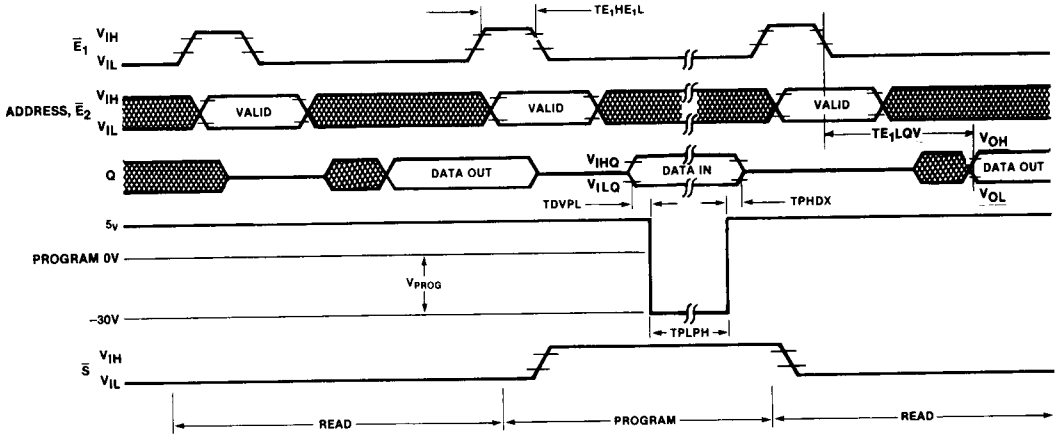
The program line remains high throughout the READ cycle. Chip enable line $\overline{E}_1$ must remain high one minimum positive pulse width (TE_1HE_1L) before the next cycle can begin.

FUNCTION TABLE

TIME REF	$\overline{E}1$	$\overline{E}2$*	$\overline{S}$	A	OUTPUTS Q	NOTES
-1	H	X	X	X	Z	DEVICE INACTIVE
0	↘	L	X	V	Z	CYCLE BEGINS: ADDRESSES, $\overline{E}_2$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E}_1$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↗	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS -1)

* A_{10} IM6657 only, $\overline{E}_2$ IM6658 only

READ AND PROGRAM CYCLES



DC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: V_{CC} = 5V ±5%, T_A 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pin Load Current	I_{PROG}			40	100	mA
Programming Pulse Voltage	V_{PROG}		-29	-30	-31	V
V_{CC} Current	I_{CC}			40	100	mA
Address, $\bar{E}_1$, $\bar{E}_2$, $\bar{S}$ Input High Voltage	V_{IHA}		V_{CC} -2.0			V
Address, $\bar{E}_1$, $\bar{E}_2$, $\bar{S}$ Input Low Voltage	V_{ILA}				0.8	
Data Input High Voltage (Q)	V_{IHQ}		V_{CC} -2.0			
Data Input Low Voltage (Q)	V_{ILQ}				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: V_{CC} = 5V ±5%, T_A = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pulse Width	TPLPH	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
Program Pulse Duty Cycle					75%	
Data Setup Time	TDVPL		9			µs
Data Hold Time	TPHDX		9			
Strobe Pulse Width	TE_1HE_1L		150			ns
Address, $\bar{E}_2$ Setup Time	$TAVE_1L$		0			
Address, $\bar{E}_2$ Hold Time	TE_1LAX		100			
Access Time After Program	TE_1LQV				1000	

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PROGRAM MODE OPERATION

Initially, all 8192 bits of the EPROM are in logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode V_{CC} is tied to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at V_{CC} -2V minimum. Low logic levels must be set at GND + .8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\bar{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\bar{E}_1$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{CC} to -30V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5µs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences, such as the Intersil 6920 CMOS EPROM programmer, is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

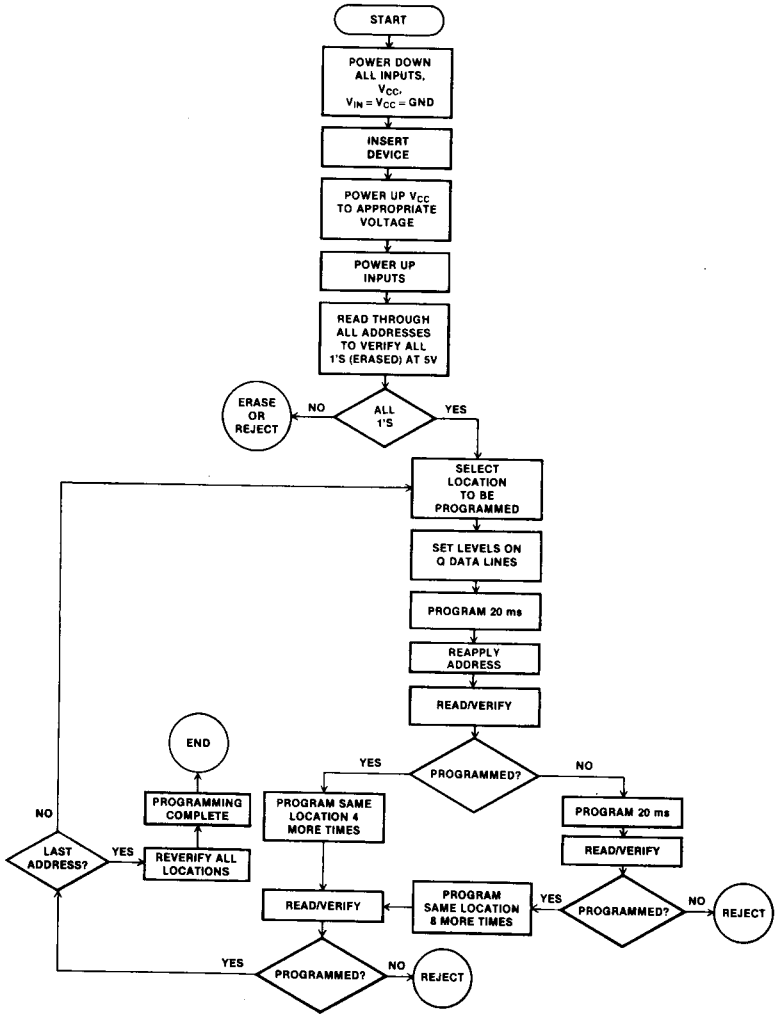
1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{CC} to −30 volts (±1V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at a V_{CC} of 5V ±5%.
4. Programming is to be done at room temperature.

ERASING PROCEDURE

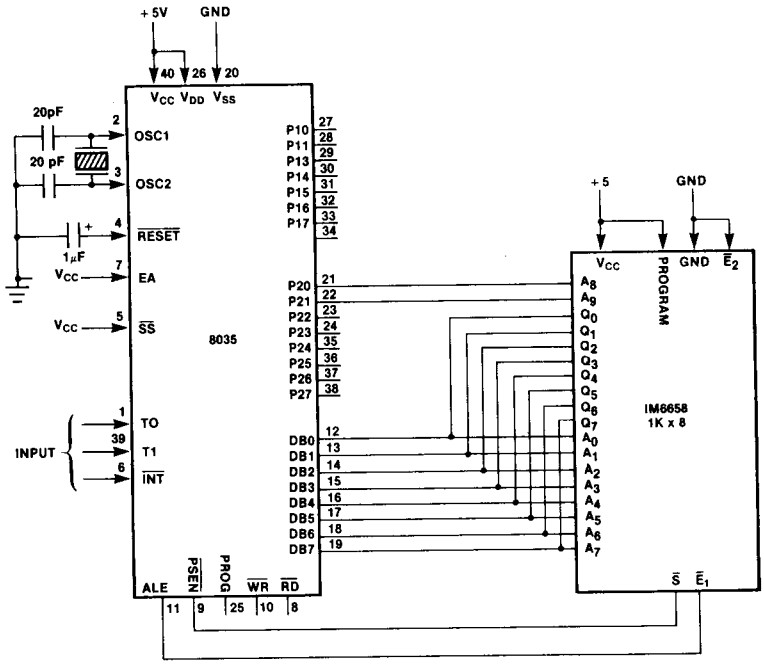
The IM6657/58 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537 Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W sec/cm^2. The lamps should be used without short-wave filters, and the IM6657/58 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cummulative. Care should be taken to protect EPROMs from exposure to direct sunlight or florescent lamps radiating UV light in the 2000Å to 4000Å range.

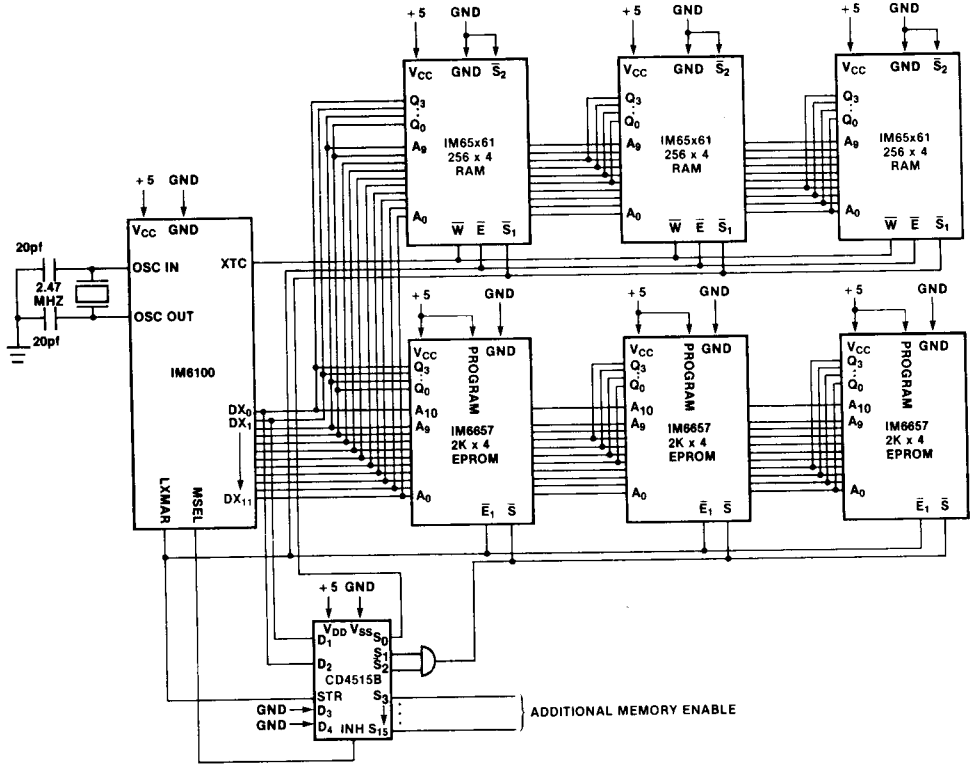
PROGRAMMING FLOW CHART



IM6658 CMOS EPROMS AS EXTERNAL PROGRAM MEMORY WITH THE 8035



IM6657 CMOS EPROMS AS PROGRAM MEMORY WITH THE IM6100



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