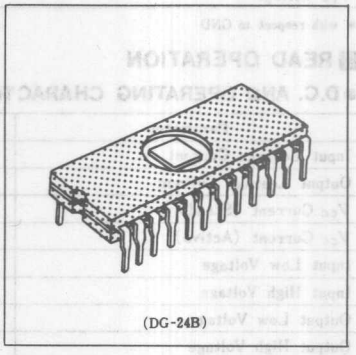
HN482732AG-20, HN482732AG-25, HN482732AG-30

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The HN482732A is a 4096-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 24 pin dual-in-line package with transparent lid.

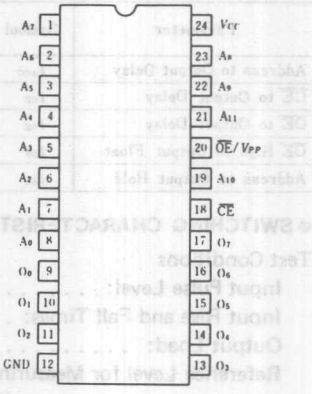
The transparent lid on the package allow the memory content to be erased with ultraviolet light.



■ FEATURES

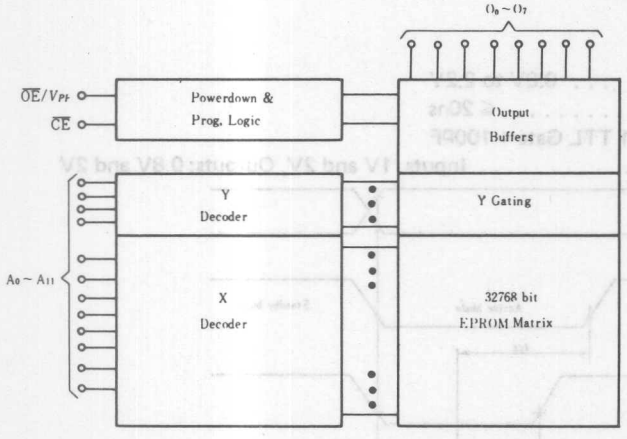
- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program Voltage: +21V D.C
  Program with one 50ms Pulse
- Static..... No clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time ..... HN482732AG-20 200ns (max)
  HN482732AG-25 250ns (max)
  HN482732AG-30 300ns (max)
- Absolute Max. Rating of Vpp Pin ... 26.5V
- Low Stand-by Current ..... 35mA (max)
- Compatible with Intel 2732A

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

MODE \ Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	D_{out}
Stand by	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{in}
Program Verify	V_{IL}	V_{IL}	+5	D_{out}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
All Input and Output Voltages*	V_{in}, V_{out}	−0.3 to +7	V
V_{PP} Voltage*	$\overline{OE}/V_{PP}$	−0.3 to +26.5	V
V_{CC} Voltage*	V_{CC}	−0.3 to +7	V

* with respect to GND

■ READ OPERATION

● D.C. AND OPERATING CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±5%)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V	—	—	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IL}$	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE}=\overline{CE}=V_{IL}$	—	—	150	mA
Input Low Voltage	V_{IL}		−0.1	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V

● AC CHARACTERISTICS (Ta=0 to 70°C, V_{CC}=5V±5%)

Parameter	Symbol	Test Conditions	HN482732AG-20		HN482732AG-25		HN482732AG-30		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	—	200	—	250	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$	—	200	—	250	—	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	10	90	10	100	10	150	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}=V_{IL}$	0	80	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	—	0	—	0	—	ns

● SWITCHING CHARACTERISTICS

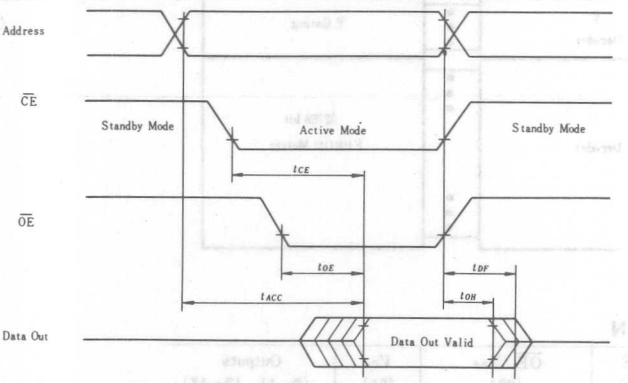
Test Conditions

Input Pulse Level: . . . . . 0.8V to 2.2V

Input Rise and Fall Times: . . . . . ≦ 20ns

Output Load: . . . . . 1 TTL Gate + 100PF

Reference Level for Measuring Timing . . . . . Inputs, 1V and 2V, Outputs; 0.8V and 2V



● CAPACITANCE (Ta=25°C, f=1MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$)	C_{IN1}	V_{IN}=0V	—	—	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}	V_{IN}=0V	—	—	20	pF
Output Capacitance	C_{out}	V_{out}=0V	—	—	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN}=V_{IL}$ or V_{IH}	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V
Output High Voltage During Verify	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
V_{CC} Supply Current	I_{CC}		—	—	150	mA
Input Low Level	V_{IL}		−0.1	—	0.8	V
Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)	V_{IH}		2.0	—	V_{CC}+1	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{PP}$	—	—	30	mA

● AC PROGRAMMING CHARACTERISTICS (Ta=25℃±5℃, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{OE}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
Chip Enable to Output Float Delay*	t_{DF}		0	—	130	ns
Data Valid from $\overline{CE}$	t_{DV}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IL}$	—	—	1	μs
$\overline{CE}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{OE}$ Pulse Rise Time During Programming	t_{PRT}		50	—	—	ns
V_{PP} Recovery Time	t_{VR}		2	—	—	μs

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

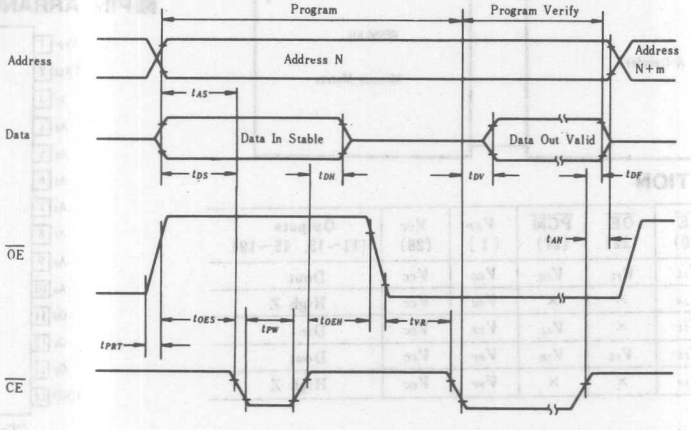
● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level . . . . . 0.8V to 2.2V

Input Rise and Fall Time . . . . . ≦20ns

Reference Level for Measuring Timing: . . . . . Inputs 1V and 2V; Outputs 0.8V and 2V



● ERASE

Erasure of HN482732A is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm^2.