M5L 2732K, K-6

32 768-BIT(4096-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

These are ultraviolet-light erasable and electrically reprogrammable 32 768-bit (4096-word by 8-bit) EPROMS. They incorporate N-channel silicon-gate MOS technology, and are designed for microprocessor programming applications.

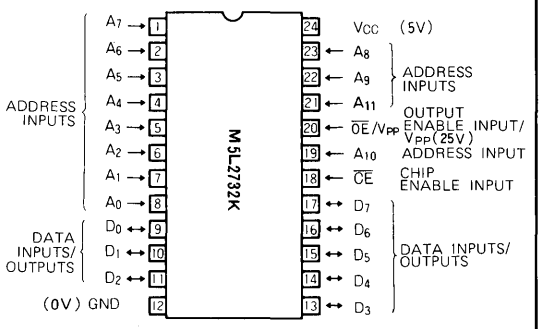
FEATURES

- Fast programming: 200s/32 768 bits (typ)
- Access time M5L 2732K: 450ns (max)
  M5L 2732K-6: 550ns (max)
- Static circuits are used throughout
- Inputs and outputs TTL-compatible in read and program modes
- Single 5V power supply for read mode
  (25V power supply required for program)
- Low power dissipation: Operating: 787mW (max)
  Standby: 157mW (max)
- Single-location programming
  (requires one 50ms pulse/address)
- Interchangeable with Intel's 2732 in pin configuration

APPLICATION

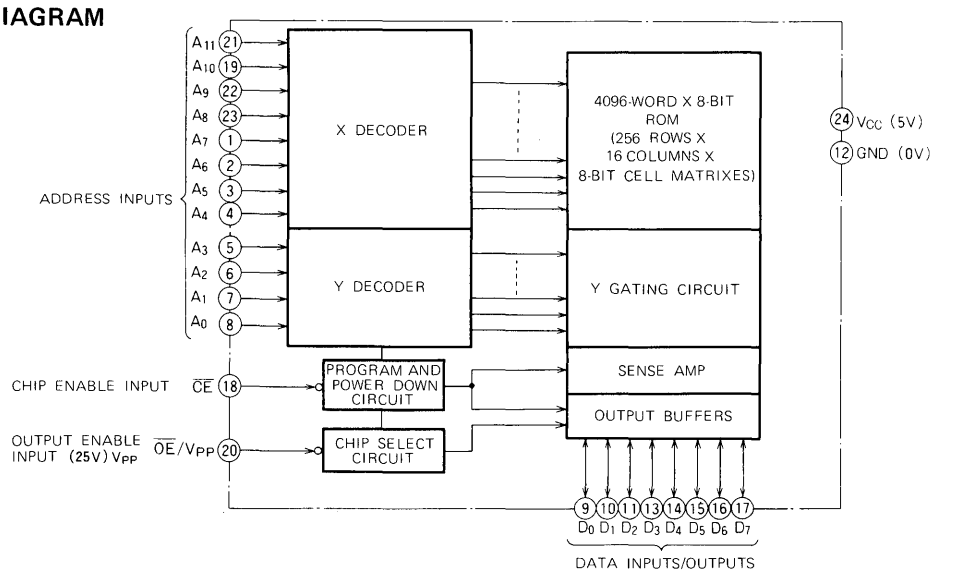
- Computers and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 24K10

BLOCK DIAGRAM



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FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low-level). Low-level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{11}$) make the data contents of the designated address location available at the data inputs/outputs ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data inputs/outputs ($D_0 \sim D_7$) are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming

The chip enters the programming mode when 25V is supplied to the $\overline{OE}/V_{PP}$ input. A location is designated by address signals $A_0 \sim A_{11}$, and the data to be programmed must be applied at 8 bits in parallel to the data inputs $D_0 \sim D_7$. A program pulse, an active low pulse, to the $\overline{CE}$ at this state will effect the programming operation. Only one programming is required, but its width must satisfy the condition $45ms \leqq t_{W(CE)} \leqq 55ms$.

Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately $15Ws/cm^2$.

Mode selection

(Unit: V)

Mode \ Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5	Output
Deselect	$V_{IL} \sim V_{IH}$	V_{IH}	5	Floating
Power down	V_{IH}	$V_{IL} \sim V_{IH}$	5	Floating
Program	Pulsed V_{IH} to V_{IL}	25	5	Input
Program verify	V_{IL}	V_{IL}	5	Output
Program inhibit	V_{IH}	25	5	Floating

HANDLING PRECAUTIONS

1. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent window should be covered with opaque tape.
2. High voltages are used when programming, and the conditions under which is it performed must be carefully controlled to prevent the application of excessively high voltages. Specifically, the voltage applied to V_{PP} should be kept below 26V including overshoot. Special precautions should be taken at the time of power-on.
3. Before erasing, clean the surface of the transparent lid to remove completely oily impurities or paste, which may impede irradiation and affect the erasing characteristics.

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ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Conditions	Limits	Unit
V_{I1}	Input voltage, $\overline{OE}/V_{PP}$ input	With respect to GND	−0.3～26.5	V
V_{I2}	Input voltage, V_{CC}, address, $\overline{CE}$, data inputs		−0.3～6	V
T_{opr}	Operating free air temperature range		0～70	℃
T_{stg}	Storage temperature range		−65～125	℃

READ OPERATION

Recommended Operating Conditions (T_a = 0 ～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage		0		V
V_{IL}	Low-level input voltage	−0.1		0.8	V
V_{IH}	High-level input voltage	2.2		V_{CC}+1	V

Electrical Characteristics (T_a = 0 ～70℃, V_{CC} = 5V ±5%, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ (Note 1)	Max	
I_{IL1}	High-level input current. address, $\overline{CE}$ input	V_I = 5.25V			10	μA
I_{IL2}	High-level input current, $\overline{OE}/V_{PP}$ input	V_I = 4.75V			10	μA
I_{OZ}	Off-state output current	V_O = 5.25V, $\overline{OE}$ = 5 V			10	μA
I_{CC1}	Supply current from V_{CC} (standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}		15	30	mA
I_{CC2}	Supply current from V_{CC} (operating)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}		85	150	mA
V_{OL}	Low-level output voltage	I_{OL} = 2.1mA			0.45	V
V_{OH}	High-level output voltage	I_{OH} = −400μA	2.4			V

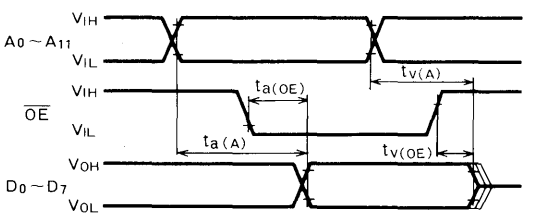
Switching Characteristics (T_a = 0 ～70℃, V_{CC} = 5 V + 5 %, unless otherwise noted.)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ (Note 1)	Max	
$t_{a(A)}$	Address access time	M5L 2732K	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	$t_r \leqq 20$ns			450	ns
		M5L 2732K−6		$t_f \leqq 20$ns			550	ns
$t_{a(CE)}$	Chip enable access time	M5L 2732K	$\overline{OE}$ = V_{IL}	V_{IL} = 0.8V			450	ns
		M5L 2732K−6		V_{IH} = 2.2V			550	ns
$t_{a(OE)}$	Output enable access time	M5L 2732K	$\overline{CE}$ = V_{IL}	Load:		100	150	ns
		M5L 2732K−6		100pF+1TTL			200	ns
$t_{v(OE)}$	Data valid time after output enable		$\overline{CE}$ = V_{IL}		0		100	ns
$t_{v(CE)}$	Data valid time after chip select		$\overline{OE}$ = V_{IL}		0		100	ns
$t_{v(A)}$	Data valid time after address		$\overline{OE}$ = $\overline{CE}$ = V_{IL}		0			ns

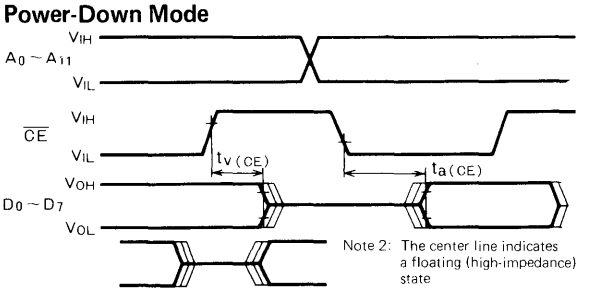
Note 1: at Ta = 25°C and normal supply voltage.

TIMING DIAGRAMS (Read Operation)

When power-Down Mode Not Used



Power-Down Mode



Note 2: The center line indicates a floating (high-impedance) state

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PROGRAM MODE

Recommended Operating Conditions (Ta = 25 ± 5 °C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	24	25	26	V
GND	Supply voltage		0		V
V_{IL}	Low-level input voltage	−0.1		0.8	V
V_{IH}	High-level input voltage	2.2		V_{CC} + 1	V

Electrical Characteristics (Ta = 25 ± 5 °C, V_{CC} = 5 V ± 5 %, V_{PP} = 25 ± 1 V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{IL}	High-level input current. address, $\overline{CE}$ inputs	V_{IN} = 5.25V			10	μA
I_{PP}	Supply current from V_{PP}	$\overline{CE}$ = V_{IL}			30	mA
I_{CC}	Supply current from V_{CC}				150	mA

Timing Requirements (Ta = 25 ± 5 °C, V_{CC} = 5 V ± 5 %, V_{PP} = 25 ± 1 V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(A-CE)}$	Address setup time before chip enable		2			μs
$t_{su(OE-CE)}$	Output enable setup time before chip enable		2			μs
$t_{su(DQ-CE)}$	Data input setup time before chip enable		2			μs
$t_{h(CE-A)}$	Address hold time after chip enable		2			μs
$t_{h(CE-OE)}$	Output enable hold time after chip enable		2			μs
$t_{h(CE-DQ)}$	Data input hold time after chip enable		2			μs
$t_{h(V_{PPL}-CEH)}$	Chip enable high hold time after V_{PP} low		2			μs
$t_{w(CE)}$	Chip enable pulse width		45	50	55	ms

Switching Characteristics Ta = 25 ± 5 °C, V_{CC} = 5 V ± 5 %, V_{PP} = 25 ± 1 V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{v(CE)PR}$	Data valid time after chip enable in program mode		0		120	ns

Timing Diagram (for Program and Verify)