

2K × 8 Bit EEPROM with Latches and Auto-Write

FEATURES

- Simple Byte Write
 - Single TTL Level Write Signal
 - Latched Address and Data
 - Automatic Internal Erase-before-Write
 - Automatic Write Timing
- Enhanced Write Protection
- Single 5 volt Supply
- Byte Write: 10ms max
- Fast Access Time: 250ns
- Power: 50mA—Standby (max)
110mA—Operating (max)
- Two Line Control-Eliminates Bus Contention
- 10,000 Cycle Endurance
- JEDEC Byte-wide Memory Pinout

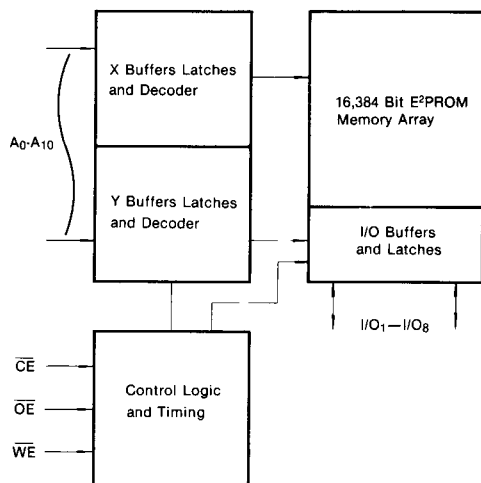
GENERAL DESCRIPTION

The KM2816A is a 16,384 bit Electrically Erasable and Programmable Read-Only-Memory organized as 2,048 words by 8-bits. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

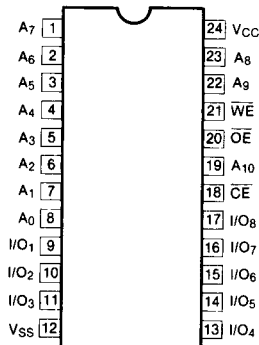
Writing data into the KM2816A is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 10ms (max) write period.

The KM2816A is fabricated with the well defined floating gate NMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A ₀ -A ₁₀	Address Inputs
I/O ₁ -I/O ₈	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
WE	Write Enable
V _{CC}	Power (+ 5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}	- 1 to +7.0	V
Temperature Under Bias	T_{bias}	- 40 to +85	°C
Storage Temperature	T_{stg}	- 65 to +125	°C
Short Circuit Output Current	I_{OS}	5	mA

*NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS} , $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC} + 1$	V
Input Low Voltage	V_{IL}	- 1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = OPEN Other Inputs = V_{CC}	—	110	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$ All I/O's = OPEN Other Inputs = V_{CC}	—	50	mA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to 5.5V	—	10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 0$ to 5.5V	—	10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400 \mu\text{A}$	2.4	—	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1 \text{ mA}$	—	0.4	V
Write Inhibit V_{CC} Level	V_{WI}		3.5	—	V

CAPACITANCE ($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $f = 1.0 \text{ MHz}$)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	C_{IO}	$V_{IO} = 0\text{V}$	—	10	pF
Input Capacitance	C_{IN}	$V_{IN} = 0\text{V}$	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

\overline{CE}	\overline{OE}	\overline{WE}	Mode	I/O	Power
L	L	H	Read	D _{OUT}	Active
L	H	L	Write	D _{IN}	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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AC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C _L = 100 pF

READ CYCLE

Parameter	Symbol	KM2816A-25		KM2816A-30		KM2816A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	250		300		350		ns
Chip Enable Access Time	t _{CE}		250		300		350	ns
Address Access Time	t _{AA}		250		300		350	ns
Output Enable Access Time	t _{OE}		120		120		120	ns
Chip Enable to Output in Low-Z	t _{LZ}	10		10		10		ns
Chip Disable to Output in High-Z	t _{HZ}	10	100	10	100	10	100	ns
Output Enable to Output in Low-Z	t _{OLZ}	50		50		50		ns
Output Disable to Output in High-Z	t _{OHZ}	10	60	10	80	10	100	ns
Output Hold from Address Change	t _{OH}	20		20		20		ns

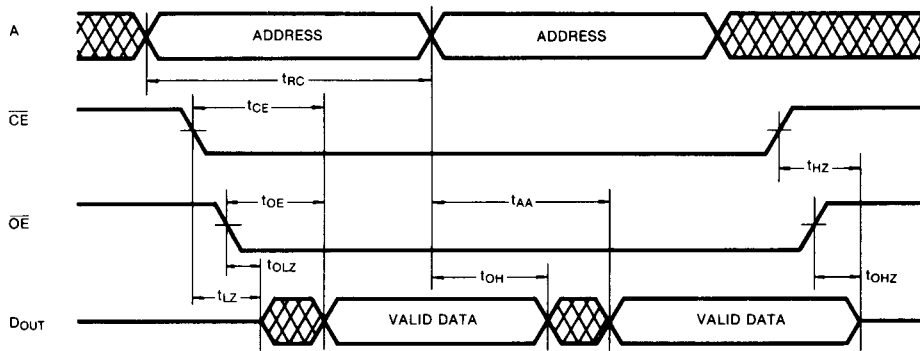
WRITE CYCLE

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}	10		ms
Address Set-up Time	t_{AS}	10		ns
Address Hold Time	t_{AH}	70		ns
Write Set-up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
Chip Enable to End of Write Input	t_{CW}	100		ns
Output Enable Set-up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width	t_{WP}	100		ns
Data Latch Time	t_{DL}	50		ns
Data Valid Time	t_{DV}		1	μ s
Data Set-up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	15		ns

TIMING DIAGRAMS

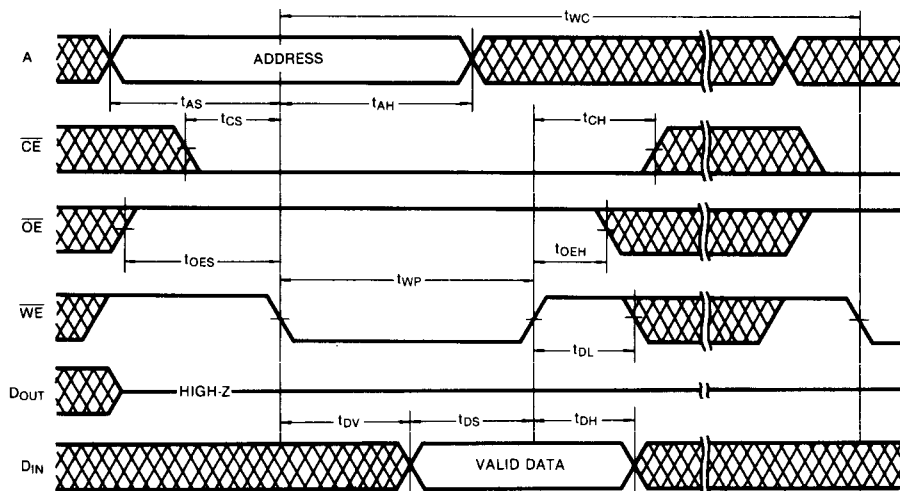
READ CYCLE

$\overline{WE} = V_{IH}$

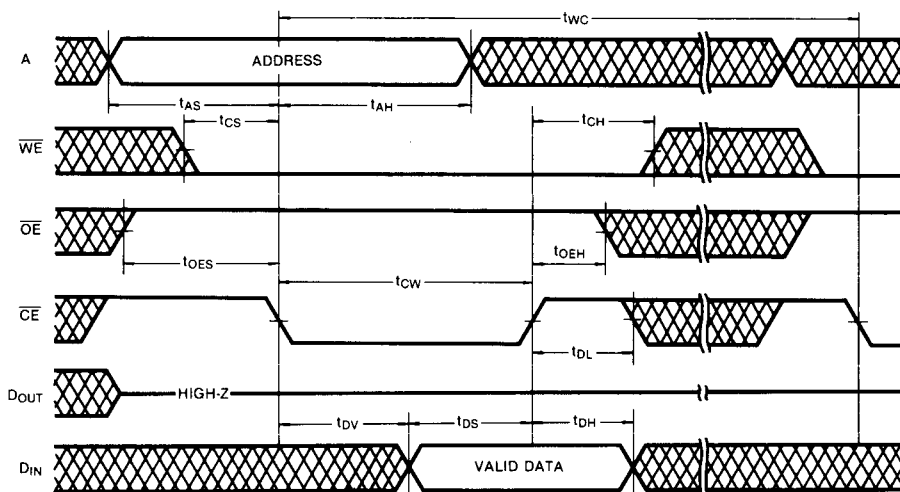


TIMING DIAGRAMS (Continued)

\overline{WE} CONTROLLED WRITE CYCLE



\overline{CE} CONTROLLED WRITE CYCLE



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DEVICE OPERATION

Read

Reading data from the KM2816A is similar to reading data from a static RAM. A read cycle occurs when \overline{WE} is high and both \overline{CE} and \overline{OE} are low. If either \overline{CE} or \overline{OE} goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever \overline{CE} or \overline{OE} is high.

Write

Writing data into the KM2816A is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a static RAM.

A write cycle occurs when \overline{OE} is high and both \overline{CE} and \overline{WE} are low. The address is latched by the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the rising edge of \overline{CE} or \overline{WE} , whichever occurs first. Address and data are conveniently latched in less than 200ns during a write operation. Once a byte write cycle is initiated it will automatically continue to completion within 10 ms or less. The existing data at the selected address is automatically erased and the new data is automatically written.

Standby

Power consumption may be reduced about 60% by deselecting the device with a high input on \overline{CE} .

Whenever \overline{CE} is high, the device is in the standby mode and $I/O_1 - I/O_8$ are in the high impedance state, regardless of the state of \overline{OE} or \overline{WE} .

Data Protection

Features have been designed into the KM2816A that prevent unwanted write cycles during power supply transitions and system noise periods.

Write cycles are inhibited when V_{CC} is less than $V_{WI} = 3.5$ volts, the Write Inhibit V_{CC} level. During power-up the KM2816A automatically prevents any write operation for a period of 9 ms (Typical) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring \overline{WE} or \overline{CE} to a high level before a write can occur. Read cycles can be executed during this initialization period.

Holding either \overline{OE} low or \overline{WE} high or \overline{CE} high during power-on and power-off with inhibit inadvertent writes.

Endurance and Data Retention

The KM2816A is designed for applications requiring, up to 10,000 write cycles per E²PROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation, and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.



PACKAGE DIMENSIONS

24 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)

