WSI

WAFERSCALE INTEGRATION, INC.

WS57C191/291

PRELIMINARY

2K × 8 CMOS PROM

KEY FEATURES

- **Fast Access Time**
  — 45 ns
- **Low Power Consumption**
  — 225 mW Active Power
- **Fast Programming**
- **Pin Compatible with AM27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

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GENERAL DESCRIPTION

The WS57C191/291 is now available as a PROM. It utilizes the same design as the previously released RPROM™ from WSI. The difference is the PROM version is available in plastic packages and is not re-programmable. The plastic packaging is ideal for high volume applications which require automatic insertion. The plastic packaging also provides an economic benefit when compared to a windowed cerdip package. For applications requiring reprogrammability, contact your WSI sales representative for information on the WSI family of RPROMs.

The WS57C191/291 is a High Performance 16K-bit CMOS PROM. It is manufactured in an advanced CMOS EPROM process which enables it to operate at bipolar speeds while consuming only 25% of the power of bipolar.

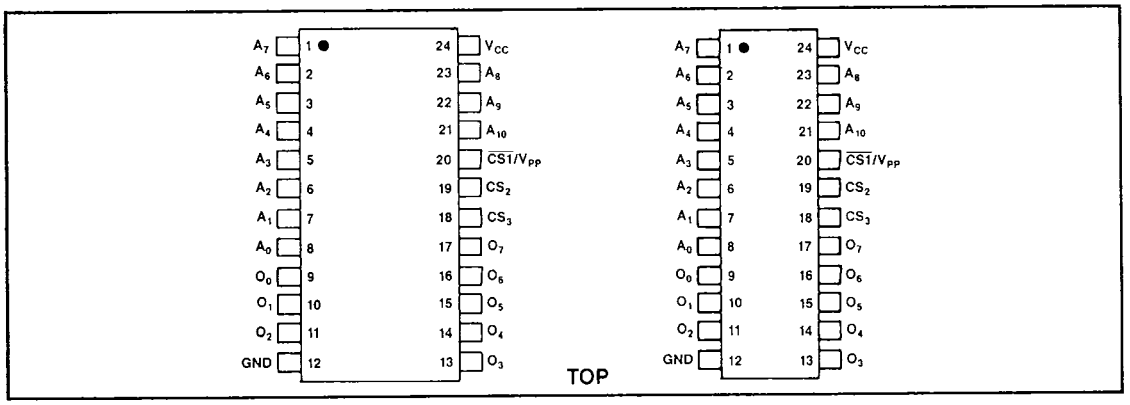
The WS57C191/291's patented CMOS EPROM technology enables the entire memory array to be fully programmed and erased prior to assembly. This capability ensures nearly 100% programming yield. Devices manufactured with other types of technologies utilize various types of fuses which cannot be tested without permanently programming the fuse. This results in a relatively high programming fallout at the packaged level.

Other testability features were designed into the 57C191/291 which enable it to be tested for speed after assembly without programming the memory array. This feature insures that the device will meet all A.C. as well as D.C. data sheet parameters.

Another feature of the WS57C191/291 is its uniquely designed output structure. When compared with other high speed devices, the output structure of the WS57C191/291 virtually eliminates the introduction of switch related noise into the system environment.

The WS75C191/291 is configured in the standard Bipolar PROM pinout. The WS57C191 is offered in a 600 mil wide Dip and the WS57C291 is offered in a 300 mil wide Dip.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C191/291-45	WS57C191/291-55
Address Access Time (Max)	45 ns	55 ns
Output Enable Time (Max)	20 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65° C to +150° C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l.	0° to +70°C	+5V ± 5%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

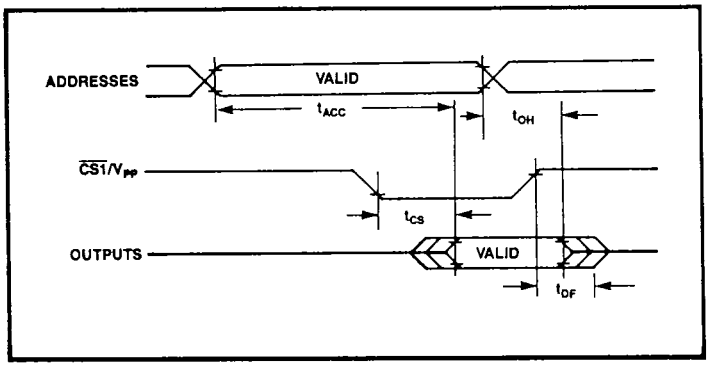
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		20	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		25	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		110	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

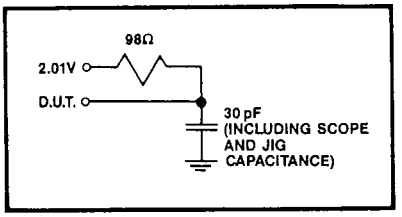
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C191/291-45		WS57C191/291-55		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		45		55	ns
CS to Output Delay	t_{CS}		20		30	
Output Disable to Output Float	t_{DF}		20		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD
(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 1.5V

T-46-13-25

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or Gnd	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	$V_{CC} + 0.3$	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = -4mA)	V_{OH}	2.4		V

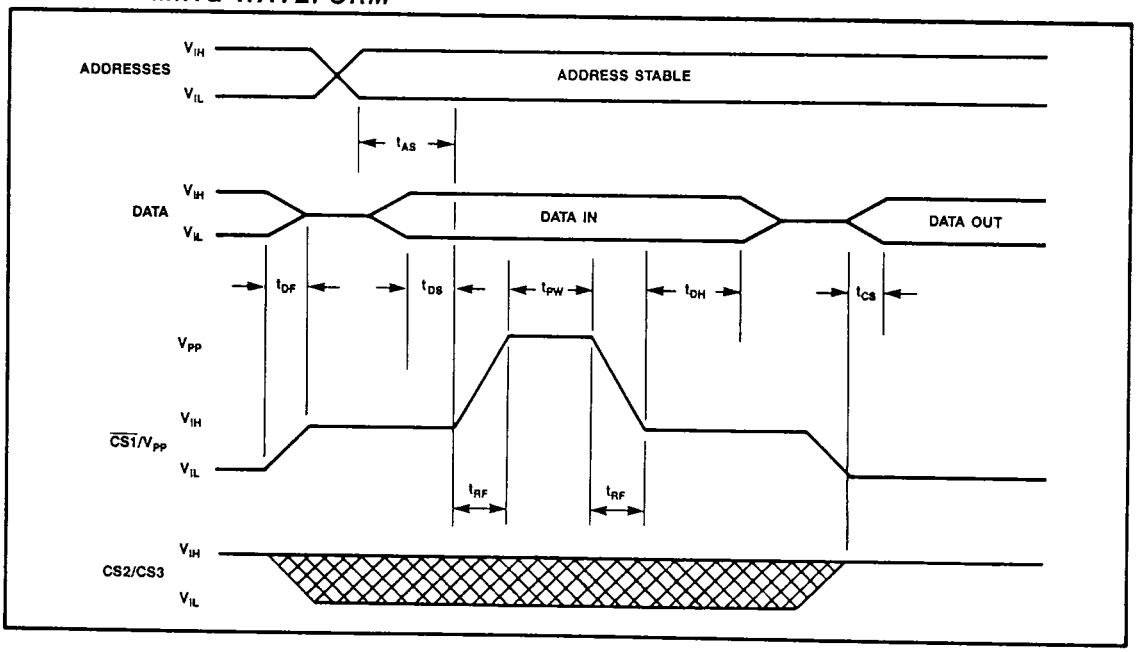
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}	2		30	ns
Data Set Up	t_{DS}	2			μs
Program Pulse Width (Note 6)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTE: 6) For programmers utilizing a one shot programming pulse, a 10 ms pulse width should be used.

PROGRAMMING WAVEFORM



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PROGRAMMING

Upon delivery from WaferScale Integration, Inc., the WS57C191/291 has all 2048×8 bits in the "1," or high state. "0's" are loaded into the WS57C191/291 through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by temoving the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

PROGRAMMERS

Data I/O Unipak 2 or 2B, family/pinout code 7B/21; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191-45P	45	24 Pin PDIP, 0.6″	P2	Comm'l	Standard
WS57C291-45S	45	24 Pin PDIP, 0.3″	S1	Comm'l	Standard
WS57C191-55P	55	24 Pin PDIP, 0.6″	P2	Comm'l	Standard
WS57C291-55S	55	24 Pin PDIP, 0.3″	S1	Comm'l	Standard