F2708

1024 x 8 UV ERASABLE PROM

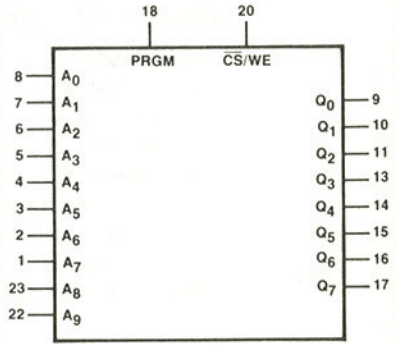
FAIRCHILD ISOPLANAR SILICON GATE NMOS

GENERAL DESCRIPTION — The Fairchild F2708 is an 8,192-bit ultraviolet light erasable and electrically reprogrammable Read Only Memory manufactured using the Isoplanar n-channel silicon gate technology. Organized 1024 x 8, the F2708 is ideally suited for non-volatile data storage in applications such as 8-bit microprocessor systems, where reprogrammability, high bit density, maximum performance, and simple interfacing are essential parameters. All inputs and outputs are TTL compatible. The 3-state outputs become high impedance when the F2708 is deselected, allowing a direct interface capability which is useful in many computer bus structures.

The F2708, which is pin-for-pin compatible with the Fairchild 3508 8K-bit ROM, provides inexpensive, non-volatile storage of data/program code in applications where fast turn-around and data/program code experimentation are important requirements. Thus, the F2708 provides the system development vehicle whereby system prototypes using the F2708 may be released into volume production by directly substituting 3508 devices for F2708 devices. For systems requiring higher density, the 3516E Fairchild 16K ROM is also available.

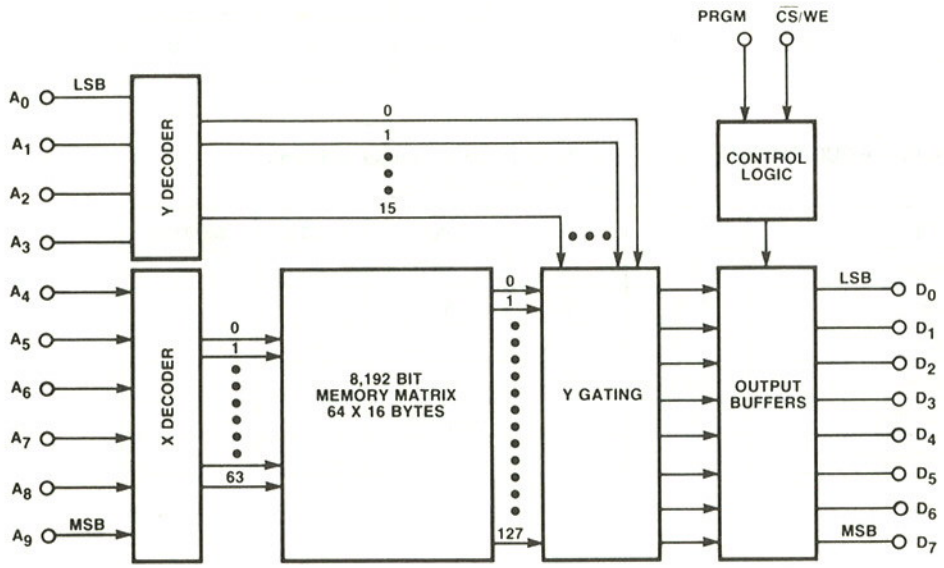
- **1024 x 8 BITS ORGANIZATION**
- **FAST ACCESS TIME: 350 nx MAX (F2708-1)**
- **TTL COMPATIBLE ON INPUTS AND OUTPUTS**
- **3-STATE OUTPUTS FOR OR-TIE CAPABILITY**
- **STANDARD POWER SUPPLIES +12 V, +5 V, -5 V**
- **CHIP SELECT INPUT FOR MEMORY EXPANSION**
- **STATIC OPERATION**
- **PIN COMPATIBLE TO 8K AND 16K ROMs FOR LOW COST PRODUCTION**
- **LOW POWER DURING PROGRAMMING**
- **CONTENTS ERASABLE WITH ULTRAVIOLET LIGHT**

LOGIC SYMBOL

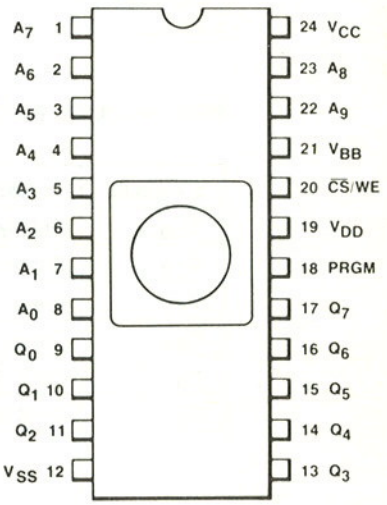


V_{DD} = Pin 19
V_{CC} = Pin 24
V_{BB} = Pin 21
V_{SS} = Pin 12

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



 Printed in U.S.A. 203-11-0006-087 15M

464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

PIN NAMES

A_n	Address Inputs (10)
Q_n	Output Data (8)
PRGM	Program Pulse Input
$\overline{CS}$/WE	Chip Select/Write Enable
V_{DD}	+12 V Supply
V_{CC}	+5 V Supply
V_{SS}	Ground
V_{BB}	−5 V Supply

ABSOLUTE MAXIMUM RATINGS (All Voltages With Respect to V_{BB})

V_{DD} Supply Voltage	−0.3 V to +20 V
V_{CC} or V_{SS} Supply Voltage	−0.3 V to +15 V
PRGM Input Voltage During Programming	−0.3 V to +35 V
$\overline{CS}$/WE Input Voltage During Programming	−0.3 V to +20 V
Any Other Input During Programming	−0.3 V to +15 V
Any Input or Output During Read	−0.3 V to +15 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−65°C to +125°C
Power Dissipation	1.8 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS DURING READ OR PROGRAMMING MODES

MODE	Data I/O	V_{SS} Supply	PRGM	V_{DD} Supply	$\overline{CS}$/WE	V_{BB} Supply	V_{CC} Supply
	9-11, 13-17	12	18	19	20	21	24
READ	Output Data	GND	GND	+12 V	V_{IL}	−5 V	+5 V
PROGRAM	Input Data	GND	Pulsed 26V	+12 V	+12 V	−5 V	+5 V
DESELECT	High Impedance	GND	GND	+12 V	V_{IH}	−5 V	+5 V

READ MODE DC ELECTRICAL REQUIREMENTS: T_A = 0°C to 70°C unless otherwise indicated.
All Voltages Referenced to V_{SS}

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	V	
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
V_{SS}	Supply Voltage	0	0	0	V	1
V_{BB}	Supply Voltage	−5.25	−5.0	−4.75	V	
V_{IH}	Input HIGH Voltage	3.0		V_{CC}+1.0	V	
V_{IL}	Input LOW Voltage	V_{SS}		0.65	V	

READ MODE DC ELECTRICAL CHARACTERISTICS: (Over Full Range of Voltage and Temperature unless otherwise indicated)

SYMBOL	PARAMETER (See Note 1)		MIN	TYP	MAX	UNITS	NOTES
I_{DD}	Average V_{DD} Current			50	65	mA	2
I_{CC}	Average V_{CC} Current			6	10	mA	2
I_{BB}	Average V_{BB} Current			30	45	μA	2
I_{IN}	Input Leakage Current			1.0	10	μA	3
I_{OUT}	Output Leakage Current			1.0	10	μA	4
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA	2.4			V	
		I_{OH} = −100 μA	3.7			V	
V_{OL}	Output LOW Voltage	I_{OL} = 1.6 mA			0.45	V	
P_D	Power Dissipation	T_A = 70°C			800	mW	5
C_{IN}	Input Capacitance			4.0	6.0	pF	6
C_{OUT}	Output Capacitance			8.0	12	pF	7

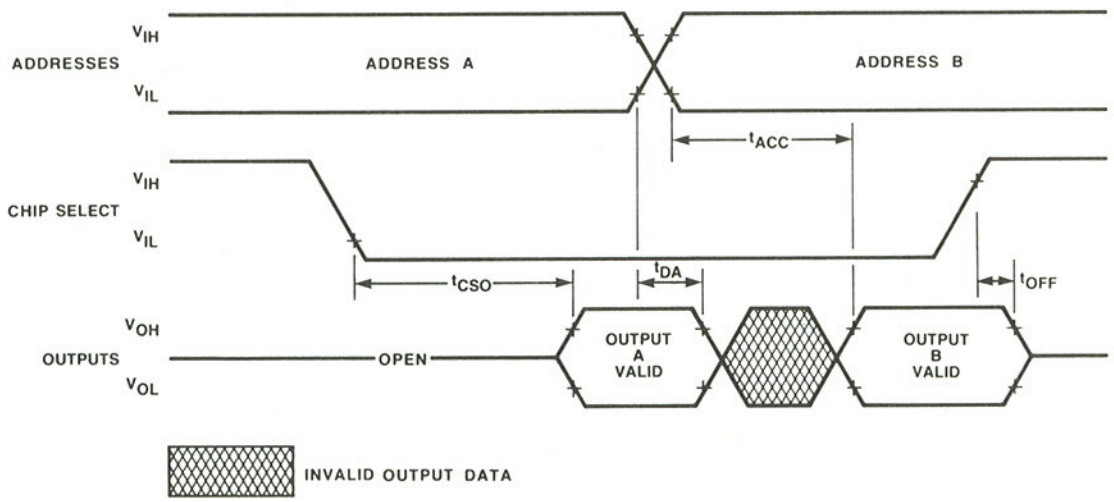
READ MODE: AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER (See Note 8)	F2708-1		F2708		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{ACC}	Address to Output Delay Time		350		450	ns	
t_{CSO}	Chip Select to Output Delay Time		120		120	ns	
t_{OFF}	Chip Deselect to Output High Impedance		120		120	ns	
t_{DA}	Data Valid After Address Time	0		0		ns	

NOTES:

1. All voltage levels are referenced to V_{SS} = 0 V.
2. Worst case supply currents occur when all inputs are HIGH (including $\overline{CS}$/WE = 5.0 V) and the ambient temperature is T_A = 0°C.
3. Measured both with V_{IN} = 5.25 V and V_{IN} = V_{IL} (min) = V_{SS}.
4. Measured both with V_{OUT} = 5.25 V and $\overline{CS}$/WE = 5.0 V.
5. The total power dissipation of the 2708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC} and I_{BB}) multiplied by their respective voltages, since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC} and I_{BB} currents should be used to determine power supply capacity only.
6. Measured with V_{IN} = 0 V, T_A = 25°C and f = 1.0 MHz.
7. Measured with V_{OUT} = 0 V, T_A = 25°C and f = 1.0 MHz.
8. Timing parameters are measured with input logic levels of V_{IL} (max) = 0.65 V and V_{IH} (min) = 3.0 V. Timing measurement reference levels are 0.8 V and 2.8 V for inputs and 0.8 V and 2.4 V for outputs. An output load of 1 TTL gate plus 100 pF is assumed.

READ MODE TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

After the completion of an ERASE operation, every memory cell in the F2708 is in the logic "1" state (as indicated by a HIGH level at the data outputs). An 8-bit byte of data is entered into the memory by programming logic "0"s into the appropriate cell locations at some given address. Word locations in the memory are addressed in the same way as in READ operations. Once a cell is programmed to a logic "0", it can only be altered through ultraviolet light erasure.

In order to program the F2708, the $\overline{CS}$/WE input must first be set to 12 V. Data to be programmed is entered in 8-bit bytes through the output data terminals (Q_0 through Q_7). Input logic levels for the data lines, addresses, and supply voltages are the same as in a READ operation.

Programming is accomplished by executing a number (N) of passes through a programming loop, each of which involves sequencing through all 1024 locations in the address space. In each pass through the loop, a single, high voltage (26 V) pulse is applied to the PRGM input, once at each address. Logic "0"s applied to the data pins (Q_0 through Q_7) are written into the proper bit positions at the location specified by the address inputs (A_0 through A_7). There must be N successive passes through the programming loop in order to guarantee reliable programming of information. The required number of loops (N) is a function of the pulse width (t_{PW}) of the high voltage programming pulse applied to the PRGM input. Total programming time is given by the relationship:

$$t_{TOTAL} = N \times t_{PW} \geq 100 \text{ ms} \quad (1)$$

The allowed range of pulse widths is from 0.1 ms to 1.0 ms. This implies that the minimum value of N must be in the range of 100 to 1000. WARNING: Applying more than one programming pulse in succession to the same address is not permitted since it will result in damage to the device. At the end of a program sequence, the $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from the PROGRAM mode to the READ mode. The PRGM pin should be pulled down to approximately V_{SS} (i.e., ground) with an low impedance device since this pin sources several milliamps of current when $\overline{CS}$/WE is at 12 V and the PRGM pin is LOW.

PROGRAMMING EXAMPLES

The programming relationship in Equation 1 above should always be used in determining values of t_{PW} and N.

Example 1 The full capacity of 1024 bytes could be programmed using 0.2 ms programming pulse widths. In this case, the minimum number of passes through the programming loop would be

$$N = \frac{t_{TOTAL}}{t_{PW}} = \frac{100 \text{ ms}}{0.2 \text{ ms}} = 500 \text{ loops.} \quad (2)$$

Each of the 500 programming loops must sequence through address locations 0 through 1023.

Example 2 Word locations 0 to 200 and 300 to 700 are to be programmed. All other bits are "don't cares". The programmed pulses are 0.5 ms wide. Thus, the minimum number of program loops is

$$N = \frac{100 \text{ ms}}{0.5 \text{ ms}} = 200 \text{ loops.} \quad (3)$$

The data entered into the "don't care" locations should consist of all logic "1"s. Even though portions of the address space are not used (or "don't cares"), the programming loop should still sequence through all 1024 addresses on each pass.

Example 3 Extending the case of Example 2, the F2708 is now to be updated to include new data at locations 850 to 880 which previously were programmed as "don't cares"; in this case, logic "1"s. The minimum number or programming loops is the same as in Example 2, N = 200 loops. Address locations 0 to 200 and 300 to 700 must be reprogrammed with their original data pattern. The remaining unused addresses should again be programmed as logic "1"s.

ERASING INSTRUCTIONS

The contents of the F2708 EPROM can be erased by exposure to high intensity shortwave ultraviolet (UV) light with a wavelength of 2537 Angstroms (Å). This can be accomplished with ultraviolet light EPROM erasure devices which are available from several U.S. manufacturers. These erasure devices contain a UV light source which is usually placed approximately one or two inches from the EPROM such that the transparent window on top of the device is illuminated. The minimum required integrated dose (intensity x exposure time) of UV light energy incident on the window of the device in order to reliably insure complete erasure is 12.5 Watt-sec/cm^2. The UV erasure unit should be periodically calibrated if minimum exposure times are to be used. (Minimum exposure times range from 10 to 45 minutes, depending on model type and age of UV lamp). If longer exposure times are possible, variations in the output light intensity of the UV light source are not critical.

PROGRAM MODE DC ELECTRICAL REQUIREMENTS

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage		11.4	12.0	12.6	V	
V_{CC}	Supply Voltage		4.75	5.0	5.25	V	
V_{SS}	Supply Voltage		0	0	0	V	1
V_{BB}	Supply Voltage		−5.25	−5.0	−4.75	V	
V_{IHP}	Input HIGH Voltage During Programming	Address and Data	3.0	–	V_{CC}+1.0	V	
		$\overline{CS}$/WE Input	11.4	12.0	12.6	V	
		PRGM Input	25	–	27	V	2
V_{IL}	Input LOW Voltage	PRGM Input	V_{SS}	–	1.0	V	2
		All Other Inputs	V_{SS}		0.65	V	

PROGRAM MODE DC ELECTRICAL CHARACTERISTICS

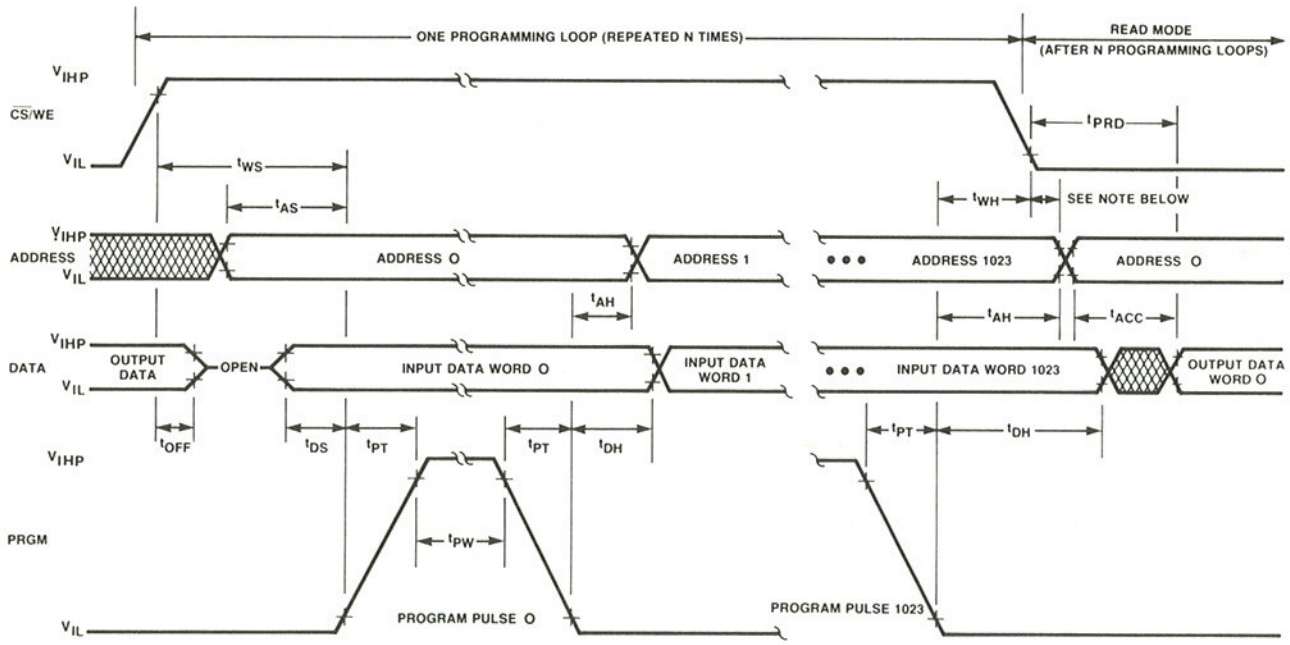
SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	NOTES
I_{DD}	Average V_{DD} Current			50	65	mA	3
I_{CC}	Average V_{CC} Current			6	10	mA	3
I_{BB}	Average V_{BB} Current			30	45	μA	3
I_{IN}	Input Leakage Current, Addresses and $\overline{CS}$/WE		−10		10	μA	4
I_{PRGM}	PRGM Input Current	HIGH			20	mA	
		LOW			3.0	mA	5

NOTES:
1. All voltage levels are referenced to V_{SS} = 0 V.
2. The voltage differential between V_{IH} and V_{IL} at the PRGM input pin should be greater than or equal to 25 V.
3. Worst case supply currents occur when all inputs are HIGH (including $\overline{CS}$/WE = 5.0 V) and the ambient temperature is T_A = 0°C.
4. Measured both with V_{IN} = 5.25 V and V_{IN} = V_{IL} (min) = V_{SS}.
5. This is a current sourced by the PRGM pin when it is in the LOW state and when $\overline{CS}$/WE = 12 V.

PROGRAM MODE: AC ELECTRICAL REQUIREMENTS AND CHARACTERISTICS

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
t_{AS}	Address Setup Time		10	–	μs	
t_{AH}	Address Hold Time		1.0	–	μs	
t_{WS}	Write Enable Setup Time		10	–	μs	
t_{WH}	Write Enable Hold Time		0.5	–	μs	
t_{DS}	Data Setup Time		10	–	μs	
t_{DH}	Data Hold Time		1.0	–	μs	
t_{PW}	Program Pulse Width		0.1	1.0	ms	
t_{PT}	Program Pulse Transition Time	Rise	0.5	2.0	μs	
		Fall	0.5	2.0	μs	
t_{PRD}	Program to Read Delay		–	10	μs	
t_{OFF}	Output Buffer Turn-off Delay		0	120	ns	

PROGRAM MODE TIMING DIAGRAM



NOTE: The falling edge of $\overline{CS}$/WE must occur after the falling edge of the program pulse and before the address transition.

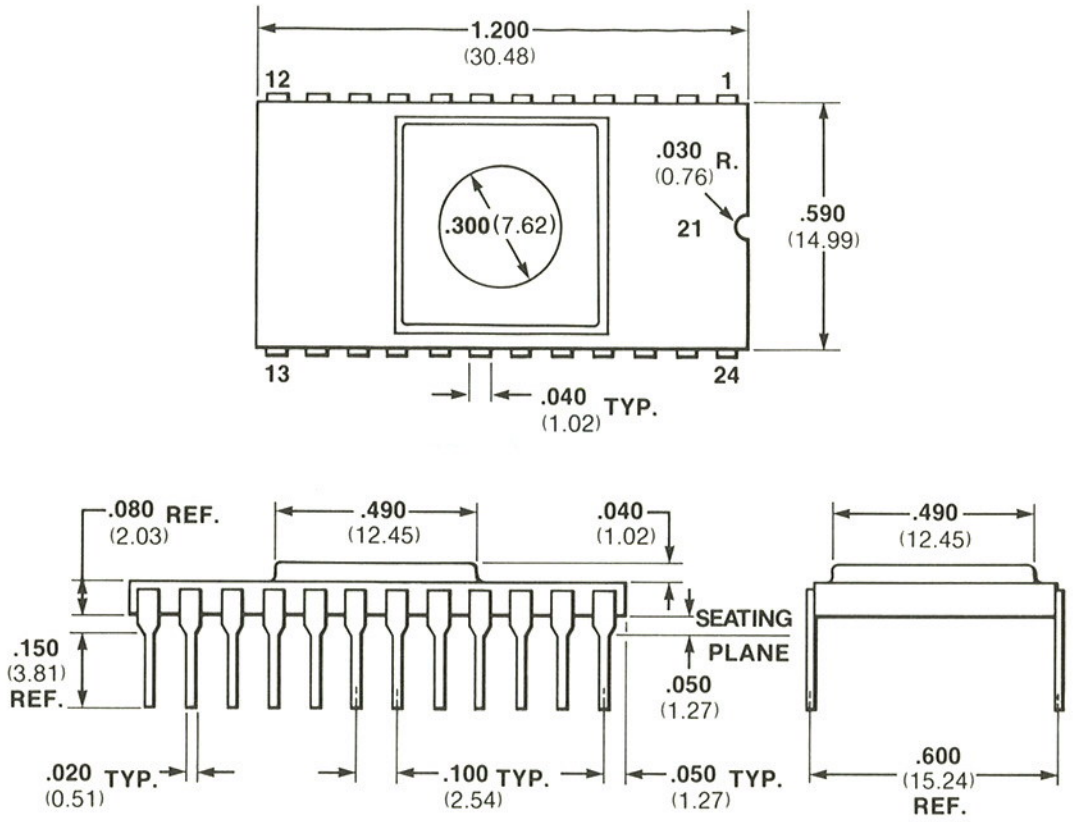
DON'T CARE INPUT CONDITION OR INVALID OUTPUT DATA.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	TEMPERATURE RANGE	PACKAGE	ORDER CODE
F2708-1	350 ns	0° to 70°C	CERAMIC	F27081DC
F2708	450 ns	0° to 70°C	CERAMIC	F2708DC
F2708	450 ns	−55° to 85°C	CERAMIC	F2708DL
F2708	450 ns	−55° to 125°C	CERAMIC	F2708DM

PACKAGE OUTLINE

24 PIN SIDEBRAZED CERAMIC DIP



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)
Optical aperture is .300 (7.62) dia.
Header is white ceramic
Lid is gold plated kovar with glass window
Pin No. 21 is common to substrate
Package is hermetic
Package weight is 4.5 grams

FAIRCHILD