2804A
Timer E^2
4K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1988

Features

- ***High Endurance***
  - ***— 10,000 Cycles/Byte Minimum***
- ***On-Chip Timer***
  - ***— Automatic Erase and Write Time Out***
- ***All Inputs Latched by Write or Chip Enable***
- ***Direct Replacement to 512 x 8 EEPROMS***
- ***5 V ± 10% Power Supply***
- ***Power Up/Down Protection Circuitry***
- ***250 ns max. Access Time***
- ***Low Power Operation***
  - ***— 80 mA max. Active Current***
  - ***— 40 mA max. Standby Current***
- ***10 Year Data Retention***
- ***JEDEC Standard Byte-Wide Pinout***

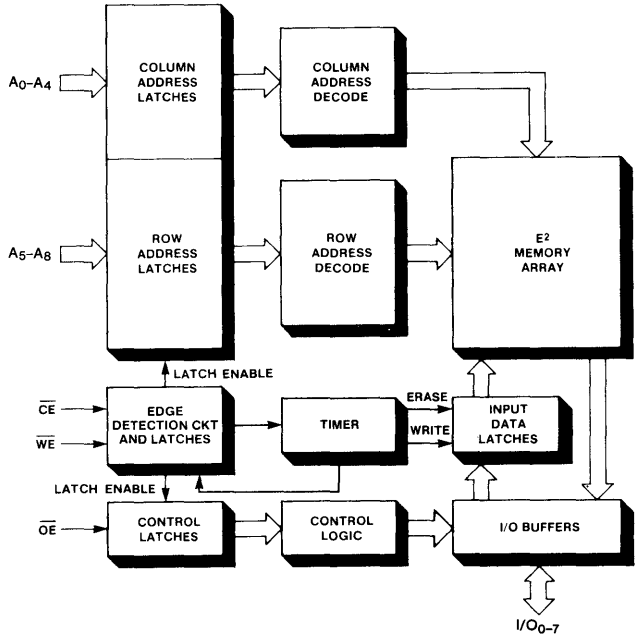
Description

SEEQ's 2804A is a 5 V only, 512 x 8 electrically erasable programmable read only memory (EEPROM). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times that a byte may be written, is 10 thousand cycles for the 2804A.

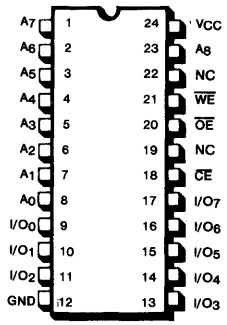
This device has an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable ($\overline{WE}$) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system for other tasks during the write time. The write time is 10 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

(Continued on page 2)

Block Diagram



Pin Configuration



Pin Names

A_0-A_4	COLUMN ADDRESSES
A_5-A_8	ROW ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE) DATA OUTPUT (READ)

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Device Operation

There are four operational modes (see Table 1) and only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$ and data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode. The 2804A ignores attempts to read or write while the internal write cycle is in progress.

Absolute Maximum Stress Ratings*

Temperature
Storage ..... −65°C to +150°C
Under Bias ..... −10°C to +80°C
All Inputs or Outputs with
Respect to Ground ..... +6V to −0.3V

Recommended Operating Conditions

	2804A
Temperature Range	(Ambient) 0°C to 70°C
V_{CC} Supply Voltage	5 V ± 10%

Mode Selection (Table 1)

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write	X	V_{IL}	X	HI Z/D_{OUT}
Inhibit	X	X	V_{IH}	HI Z/D_{OUT}

X – Any TTL Level.

Power Up/Down Considerations

The 2804A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. V_{CC} is less than 3 V.[1]
2. A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

DC Operating Characteristics T_A=0° to 70°C; V_{CC}=5 V ± 10%, unless otherwise noted.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Condition
I_{CC}	Active V_{CC} Current		80	mA	$\overline{CE}$=$\overline{OE}$=V_{IL}; All I/O open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IL}; All I/O's Open; Other Inputs = 5.5 V
I_{IL}	Input Leakage Current		10	μA	V_{IN}=5.5 V
I_{OL}	Output Leakage Current		10	μA	V_{OUT}=5.5 V
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH}=-400 μA

NOTE:
1. Characterized. Not tested.

AC Characteristics

Read Operation T_A=0° to 70°C; V_{CC}=5 V ± 10%, unless otherwise noted.

Symbol	Parameter	Limits				Units
		2804A-250		2804A-300		
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		ns
t_{CE}	Chip Enable Access Time		250		300	ns
t_{AA}	Address Access Time		250		300	ns
t_{OE}	Output Enable Access Time		90		100	ns
t_{LZ}	$\overline{CE}$ to Output in Low Z	10		10		ns
t_{HZ}	$\overline{CE}$ to Output in HI Z		100		100	ns
t_{OLZ}	$\overline{OE}$ to Output in Low Z	50		50		ns
t_{OHZ}	$\overline{OE}$ to Output in HI Z		100		100	ns
t_{OH}[1]	Output Hold from Address Change	20		20		ns
t_{PU}[1]	$\overline{CE}$ to Power-up Time	0		0		ns
t_{PD}[1]	$\overline{CE}$ to Power Down Time		50		50	ns

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O}$ = 0 V

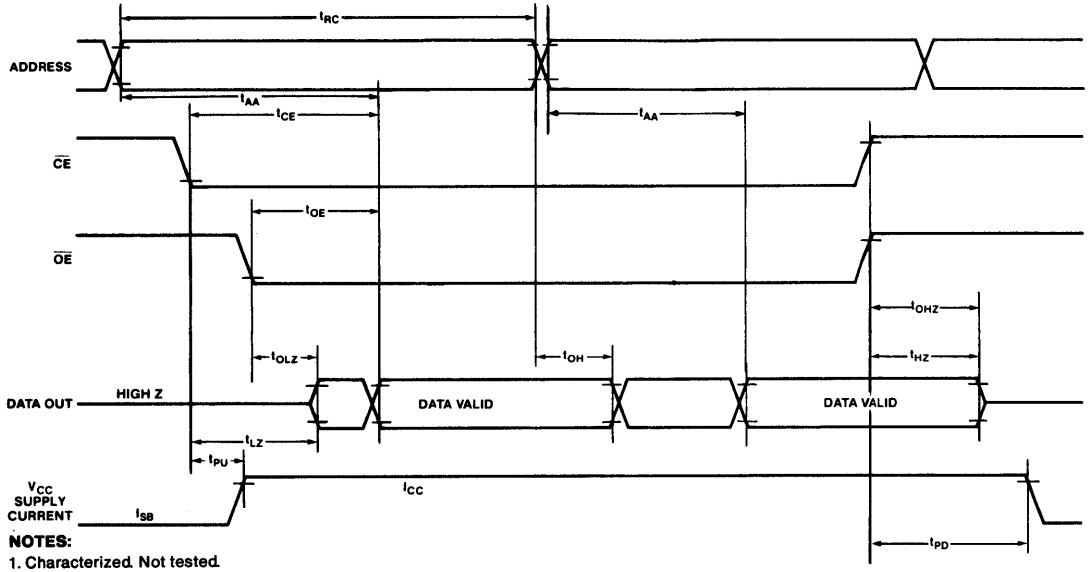
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[1]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Read Cycle Timing



NOTES:
1. Characterized. Not tested.
2. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

AC Characteristics

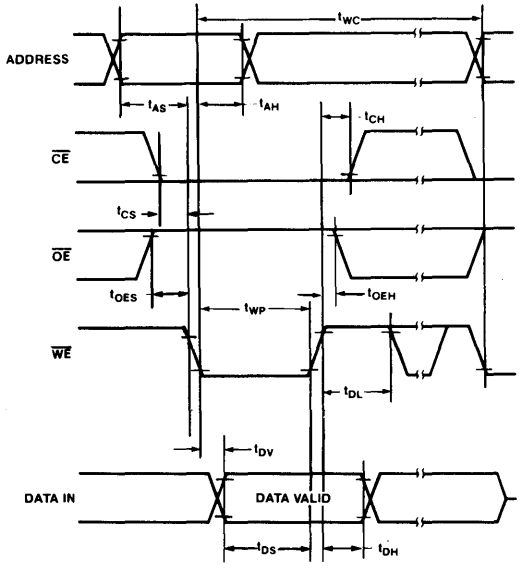
TTL WRITE CYCLE T_A=0° to 70°C; V_{CC}=5 V ± 10%, unless otherwise noted.

Symbol	Parameter	2804A-250		2804A-300		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Set Up Time	10		10		ns
t_{AH}	Address Hold Time	50		70		ns
t_{CS}	Write Set Up Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ to End of Write Input	150		150		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		ns
t_{WP}[1]	$\overline{WE}$ Write Pulse Width	150		150		ns
t_{DL}	Data Latch Time	50		50		ns
t_{DV}[2]	Data Valid Time		1		1	µs
t_{DS}	Data Set Up Time	50		50		ns
t_{DH}	Data Hold Time	0		0		ns

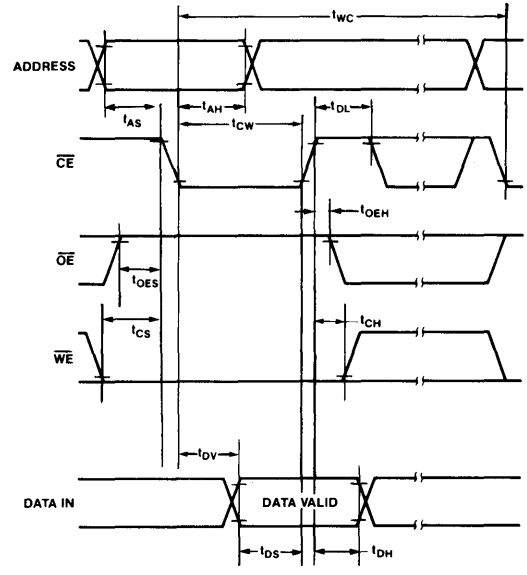
NOTES:
1. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 µs maximum after the initiation of a write cycle. Characterized, not tested.

TTL Byte Write Cycle

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



Ordering Information