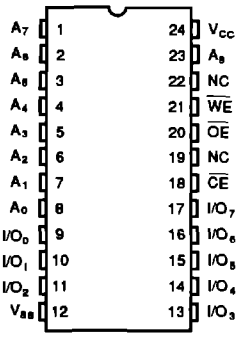
512 X 8 Electrically Erasable PROM

FEATURES

- Fast Read Access Times
  — 250ns, 300ns, 350ns, 450ns
- 5 Volt-only Operation
  — Including Write
- Industrial Temperature Range Available (XLE2804A)
- Fast Nonvolatile Write Cycle
  — Internally Latched Data and Address
  — 150ns Byte-load Cycle
  — 10ms Nonvolatile Write Cycle
- Automatic Erase Before Write
- Automatic Write Timeout
- On-chip Inadvertent Write Protection
- Unlimited Read Cycle Endurance
- 10,000 Rewrites per Byte
- 10 Year Secure Data Retention
- TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Memory Pinout

PIN CONFIGURATION

24 Pin PDIP
Type "P" Package



PIN NAMES

A_0-A_8	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

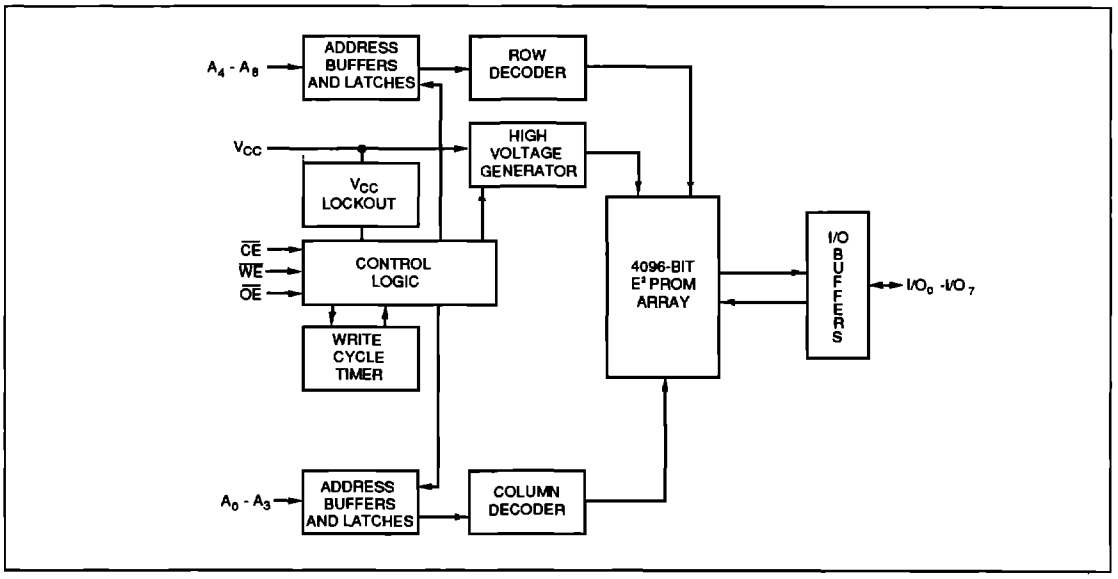
OVERVIEW

The XL2804A is a full-featured, 512 x 8 bit E^2PROM (Electrically Erasable Programmable Read Only Memory). Read access times are as low as 250ns; standby current, less than 40mA. The device is fully functional with a single 5V power supply, and the XL2804A is manufactured with EXEL's 1.5µ NMOS E^2PROM process.

The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and inadvertent write protection circuitry. It fits into a standard SRAM socket and responds to typical SRAM write commands.

The XL2804A features V_{CC} lockout, $\overline{OE}$ write inhibit logic, and noise protected $\overline{WE}$, to inhibit inadvertent writes.

BLOCK DIAGRAM



The XL2804A is compatible with industrial standard 512 x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

APPLICATIONS

The XL2804A provides secure and reliable data storage thoughout your system's lifetime both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL2804A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL2804A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL2804A is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION-STANDARD MODES

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL2804A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode

Data is read from the XL2804A by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Write Mode
In the XL2804A the write cycle is initiated by applying a logical "0" to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is logical "1". The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both addresses and data are latched in a brief 200ns interval using a 5V supply and TTL write signals. Once the data is latched, the XL2804A will automatically erase the selected byte and write the new data in less than 10ms. The system is therefore freed to proceed with other operations while the XL2804A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress. (See Figures 3 and 4.)

Output Disable Mode
If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a HIGH impedance state.)

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a HIGH impedance state. Standby power dissipation is less than 100 µA with CMOS level inputs. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase — High Voltage Mode
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding the data on the I/O pins HIGH. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to Mode Selection chart.)

WRITE PROTECT MECHANISMS

The XL2804A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{OE}$ Write Disable
If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table below. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

V_{CC} Lockout
The XL2804A has a specialized power supply monitor circuit integrated to protect the device from inadvertent write commands asserted by the system during low V_{CC} conditions. This circuitry constantly evaluates the power supply voltage level applied to the XL2804A and actively inhibits the initiation of nonvolatile write cycles if the applied supply voltage falls below V_{WI}. This circuitry does not abort or affect nonvolatile write cycles already in progress yet inhibits new cycles from being initiated.

Noise Protection
Write pulses of less than 20ns duration on the $\overline{WE}$ pin will not initiate nonvolatile write cycles.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐‾⌐	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⌐‾⌐	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IH}	Chip Erase*	Data In=V_{IH}	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL for details.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -10°C to +85°C
Storage temperature ..... -65°C to +120°C
Voltage on any pin* ..... -0.5V to +6.0V
DC output current 5mA
*With respect to ground

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V±5% unless otherwise specified

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current-Active		80	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5 25V
I_{SB}	V_{CC} Current-Standby		40	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5 25V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = 0 to 5.25V
I_{LO}	Output Leakage Current		±10	µA	V_{OUT} = 0 to 5.25V
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 µA
V_{WI}	V_{CC} Trip Voltage for Write Protection	3.0	3.5	V	
V_H	High Voltage for Chip Erase	15	18	V	

CAPACITANCE

T_A = +25°C, f = 1.0 MHz

Symbol	Test	Max.	Units	Test Conditions
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)

T_A = 0°C to +70°C, V_{CC} = 5V±5%, unless otherwise specified.

Symbol	Parameter	XL2804A-250 Limits		XL2804A-300 Limits		XL2804A-350 Limits		XL2804A-450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		100		120		135		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	100	10	100	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	70	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

WRITE CYCLE (See Figures 3 and 4)

T_A= 0°C to +70°C, V_{CC} = 5V±5%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Nonvolatile Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	70		ns
t_{CS}	Chip Enable or Write Setup Time	0		ns
t_{CH}	Chip Enable or Write Hold Time	0		ns
t_{CW}	Chip Enable to End of Write Input	150		ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP}*	Write Enable Pulse Width	150		ns
t_{WPH}	Write Pulse Recovery	50		ns
t_{DV}	Data Valid Time		1	µs
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{INIT}	Power-up Initialization Period	5	20	ms

* NOTE: A write pulse of less than 20ns will not initiate a write cycle

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

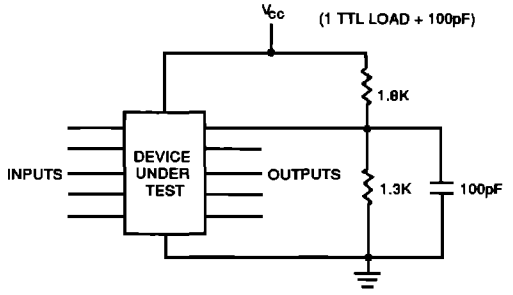


FIGURE 1. AC TEST CONDITIONS

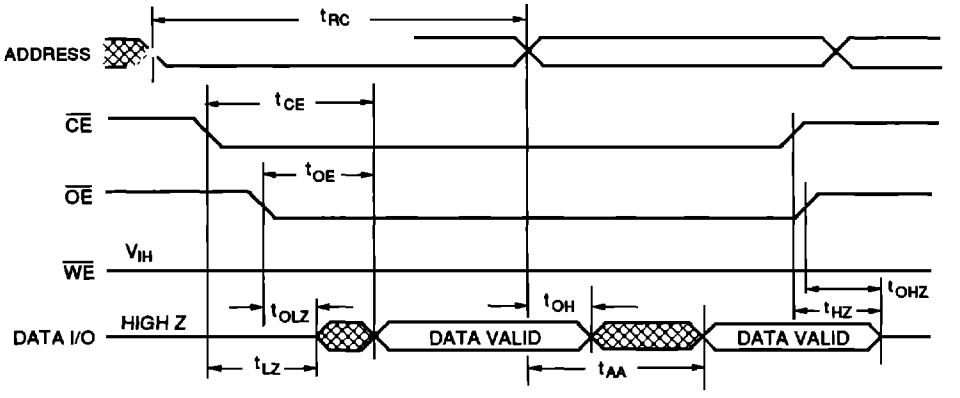


FIGURE 2. READ CYCLE TIMING

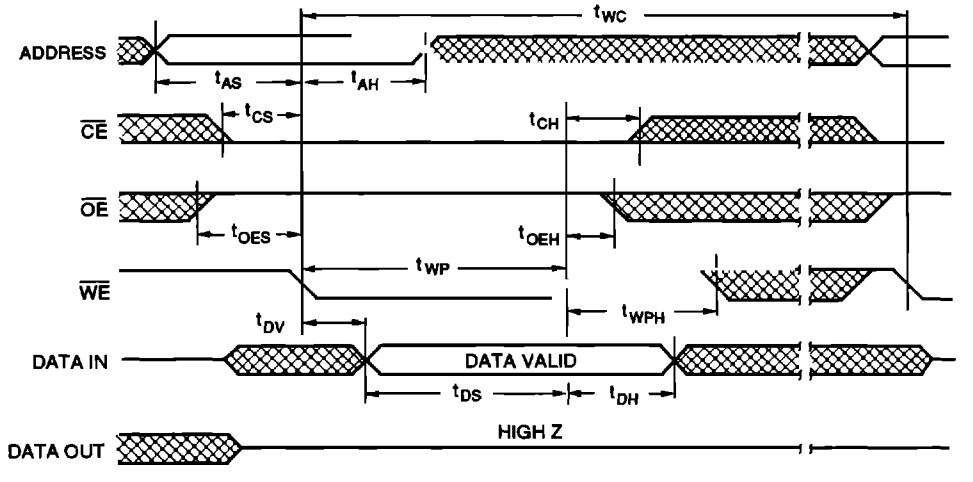


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

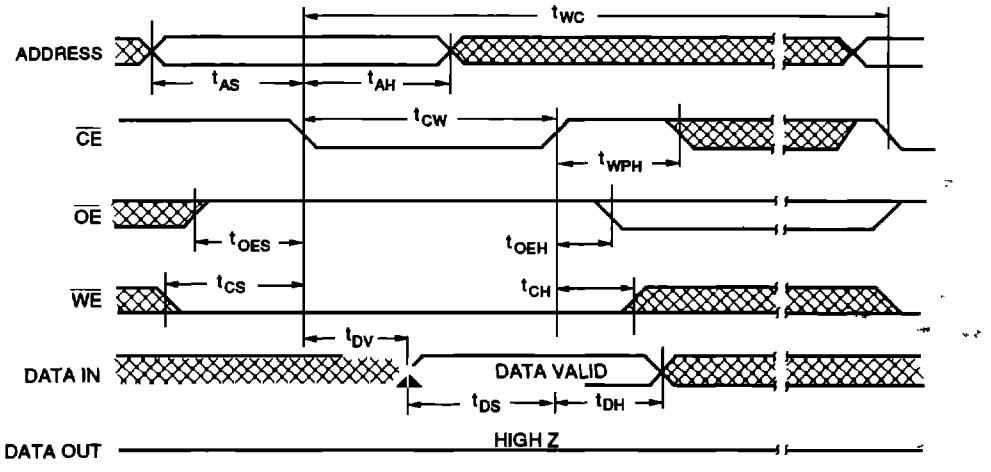


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING