

CP/M 2.2b for Tarbell SD Controller (Track Buffered CP/M 2.2)

This version of CP/M 2.2 is for the Tarbell single density floppy controller with an IMSAI SIO board for I/O. The console, punch, reader, and list devices all use the first port on the SIO board.

The BIOS uses full track buffering on both reads and writes to improve performance. Performance is 20%-70% faster than the non-buffered BIOS for typical disk based operations. Disks are fully interchangeable with the non-buffered versions of CP/M 1.4 and 2.2.

The disk image file, CPM22B10-48K-SSSD.DSK, is sized for 48K of RAM and includes the source files and utilities required to transfer files to/from a PC, backup/restore disk images, and size CP/M for a different amount of RAM with MOVCPM. The MOVCPM on this disk is custom for this version of CP/M and *does not* require the boot loader or BIOS to be patched into the CP/M image.

In order to fit in the boot tracks of a standard SSSD IBM format soft sectored 8" disk, the code/initialized data portion of this BIOS can only be 380h bytes long. This restriction substantially reduces the features that can be provided by this BIOS and required a few tricks in the code to save space. The source file has a conditional assembly statement to detect when this size limit is exceeded. Look for "BIOS IS TO BIG *****" as an error statement when assembling.