1702 EPROM Timing Issues

1702 access time is typically 1.0us worst case. This falls on a timing boundary of wait state selection on a 2 MHz 8080 CPU. Based on the degraded performance I have seen with aging 1702 EPROMs, use two wait states on an EPROM board (1.0us-1.5us) vs one wait state (0.5us-1.0us).

The Altair 88-PMC EPROM board turns -9v power (Vgg on the 1702) on and off for groups of two EPROMs at a time in order to conserve power. Access time from assertion of Vgg is a documented spec for the 1702 and is within the listed access time of the EPROM. However, it appears this spec can degrade substantially with aging 1702s – more so than standard access time if Vgg is already present.

I have seen especially bad Vgg access degradation with the National Semiconductor 1702 and with early Intel 1702s (e.g., the white ceramic packages with the fragile legs). With these parts, access time from assertion of Vgg was beyond two wait states. The only way to achieve proper operation with these parts was to leave Vgg asserted. Reprogramming the part did not improve performance.