

8800b Turnkey Module Notes

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INTRODUCTION

There are two versions of the Altair 8800b Turnkey Module board: the older version is identified as "8800b TURNKEY MODULE REV 0", and the newer version is identified by the assembly number 200372-01. (The older version can easily be identified by the presence of eight 2102 SRAM chips above the row of EPROM sockets.) MITS generated a System Bulletin, called 88-SYS-CLG, which described modifications intended to make the older revision boards function the same as the newer version boards. These modifications were not entirely successful. (See below.)

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TURNKEY MODULE FUNCTIONS

The 8800b Turnkey Board provides a variety of functions, critical to the operation of an Altair 8800bt, but also useful in Altairs that include a full front panel, such as the Altair 8800b.

1. PROM

The Turnkey Module includes four 1702A PROM sockets, for a total of 1K-bytes of PROM space. These PROMs are normally addressed at FC00h through FFFFh, using the "PROM ADDR" switches:

SW-2	SW-3	Function
xx11	1111	Normal address for PROMs

Addressed this way, the PROM sockets have the following addresses:

Socket	Address	Normal Function
L1	FC00h	HDBL (Hard disk boot loader)
K1	FD00h	TURMON or UBMON (System monitor)
J1	FE00h	MBL (multi-boot loader for paper tape or cassette)
H1	FF00h	DBL, MDBL, or CDBL (Boot loader for floppy disk)

The Turnkey Module generates one wait state for each PROM access.

Newer Turnkey Modules, as well as older ones with the 88-SYS-CLG modification, attempt to disable ("phantom") the onboard PROM once any read from port FFh occurs. This functionality did not work correctly, as explained below.

2. SRAM

Only on the older version of the Turnkey Module (without the 88-SYS-CLG rework) contains 1K-bytes of SRAM. This SRAM is normally addressed at F800h through FBFFh, using the "RAM ADDR" switches:

SW-1	SW-2	Function
1111	10xx	Normal address for RAM

3. SIO

The SIO is a 6850-based ACIA, intended to be used as the Terminal Port, and compatible with Port A on an 88-2SIO. This port is normally addressed at 10h, using the "SIO ADDR" switches. (A switch is binary "1" when it is to the right.)

SW-4	SW-5	Function
0001	000x	Normal address for SIO

The Turnkey Module generates one wait state for each SIO access.

The SIO's interface mode is set up with the following jumpers:

Mode	Jump	Jump	Jump	Jump	Jump
RS232	X3-X4	K3-P3 (disables DCD)	K2-P2 (disables CTS)		
TTY	X1-X2	K4-P5	K3-P3	K2-P2	
TTL	X2-X3	K4-P4	K3-P3	K2-P2	K1-P1 (no ext. clk)

The SIO's baud rate is set by jumpers S1-S4:

S3	S2	S1	S0	/16 Rate	/32 Rate	Synchronous
				110 baud	27.5 baud	1760 baud
			Jump	150 baud	37.5 baud	2400 baud
		Jump		300 baud	75 baud	4800 baud
		Jump	Jump	2400 baud	600 baud	38400 baud
	Jump			1200 baud	300 baud	19200 baud
	Jump		Jump	1800 baud	450 baud	28800 baud
	Jump	Jump		4800 baud	1200 baud	76800 baud
	Jump	Jump	Jump	9600 baud	2400 baud	153600 baud
Jump				2400 baud	600 baud	38400 baud
Jump			Jump	600 baud	150 baud	9600 baud
Jump		Jump		200 baud	50 baud	3200 baud
Jump		Jump	Jump	134.5 baud	33.375 baud	2152 baud
Jump	Jump			75 baud	18.75 baud	1200 baud
Jump	Jump		Jump	50 baud	12.5 baud	800 baud
Jump	Jump	Jump	x	External Clk	External Clk	External Clk

SIO connection is via connector J2, at the top right of the Turnkey Module. J2 Pinout is as follows. Note that pin 1 is on the right side of this connector.

Pin	Direction	Signal	DB25 Pin
1	Out	TTL RTS	
2	Out	TTY TxD	
3	In	TTY RxD	
4	In	RxD	2
5	In	DCD	8
6	In	CTS	5
7	In	Ext Clk	(15)
8		GND	7
9	Out	RTS	4
10	Out	TxD	3

4. Autostart

The autostart circuit forces execution at an address set by the eight "START ADDR" DIP switches. Here are some common switch settings. (A switch is binary "1" when it is to the right.)

SW-8	SW-9	Function
1111	1100	Auto-start HDBL to boot from Altair Hard Disk
1111	1101	Autostart TURMON or UBMON
1111	1110	Autostart MBL to boot from paper tape or cassette
1111	1111	Autostart DBL, MDBL, or CDBL to boot from floppy disk

5. Sense Switches

DIP switches SW-6 and SW-7 replace the front panel sense switches when used in an 8800bt (which has no front panel). These are normally set to specify the load port (for MBL) and the Terminal port (for Basic and DOS). A sense switch is binary "1" when it is up. The high-order bit is on the left.

6. Truncated Front Panel Interface

The Turnkey Module connects to the the 8800bt's truncated front panel board. This front panel displays the state of +5V, INT, INTE, HLTA, and I/O (SOUT or SIN), and has switches for RUN/STOP and RESET.

The front panel connects to the Turnkey Module via connector J1, at the top left of the Turnkey Module. J1 Pinout is as follows. Note that pin 1 is on the right side of this connector.

Pin	Direction	Signal	Function
1	Out	+5V	Regulated +5 volts
2	Out	/BHLTA	Active low HALT signal
3	Out	/BINTE	Active low Interrupt Enable signal
4	Out	BI/O	Active low Input or Output signal
5	Out	/BINT	Active Low Interrupt signal
6		GND	Ground reference
7	In	/PRESET	Active low Processor Reset signal
8	In	PRDY	Active high Processor Ready signal (low STOPS the processor)
9-10			Not used

OPERATION WITH A FULL FRONT PANEL

You can use a Turnkey Module with an Altair that has a front panel (e.g. an Altair 8800b), by performing the following modifications:

8800bt setting	With Front Panel	Purpose
M1 - M2	Jumper removed	Disconnect MWRT from bus
B - S	B - +5V	Disable Turnkey Sense Switches

Connector J1 should be left unconnected.

AUTOSTART OPERATION

The Autostart circuitry operates in an unorthodox manner: The Turnkey Module jams a Jump instruction on the bus in the first 3 cycles after a Reset, by forcing the MEMR S-100 signal low (inactive) to prevent any other memory board from driving data onto the bus, and at the same time driving the 3 bytes of the Jump instruction onto the data bus. The MEMR signal is forced low with a big transistor (on older-version boards) or with the combined power of six open-collector inverters in parallel (on newer-version boards), overdriving the MEMR signal that is generated by the CPU board.

PHANTOM

The newer Turnkey Module eliminated the onboard RAM and added a "Phantom" circuit. The "Phantom" circuit was intended to allow access to the PROMs immediately following Reset, but to allow full 64K of RAM later. The concept is that the PROMs are enabled at Reset, and remain so until the first Input or Output instruction from or to I/O port FEh or FFh. Other memory boards are prevented from driving the data bus

with the same circuit as the Autostart circuit: during PROM access, the MEMR signal is overdriven by the Turnkey Module.

Unfortunately, the timing of this circuit did not work. As designed, the PROMs become disabled whenever any Input or Output instruction was executed. This bug was corrected with Service Bulletin 007, which used an OR gate (IC C pins 4-6) to insert the /PDBIN signal into the logic that sensed access to I/O ports FEh and FFh, thereby qualifying the I/O address by a correct timing signal. This Service Bulletin has the side effect of disabling the PROMs only on an Input instruction (not an Output instruction).

Phantom PROM Issues

Using the input from the Sense Switches as a mechanism for disabling the PROMs was clever in that it allows existing programs, such as Altair Basic, to use the full 64K of memory without modification: Basic reads the sense switches anyway during its initialization to determine the Terminal port, which also disables the PROMs and enables 64K of RAM.

Unfortunately, this mechanism does not work perfectly, causing systems to behave differently than (and incorrectly compared to) systems without a Turnkey Board that generates Phantom.

1. Front Panel Reset

Once initialized, Altair Basic does not perform any further inputs from the sense switches. Therefore, if an Altair that is running Basic is reset from the front panel, and then run from address 0 (either using Examine on a full front panel or using the "J" instruction in a PROM monitor such as TURMON or UBMON), then the PROMs will once again be enabled and the top 1K of RAM will be disabled - but Basic will still assume the full 64K of RAM is available. This may cause unexpected behavior from Basic.

2. Reading the Sense Switches from PROM

Since reading the Sense Switch port disables the PROMS, PROM code must not read the sense switches. In particular, boot loaders must not read the sense switches in order to determine which port is the Terminal Port, as is done by various Altair loader programs. (This is why DBL and other Altair PROM loaders do not set the 2SIO stop bits, as specified by the sense switches.) Because the MITS's MBL PROM reads the sense switches to determine the load port, MITS's MBL will not work on a Turnkey Module.

88-SYS-CLG MODIFICATION

MITS created this extensive modification to the older-version Turnkey Modules to provide PROM Phantom functionality, attempting to be compatible with the newer-version Turnkey Modules. This modification both permanently disabled the RAM, and also added a Phantom circuit similar to the one on the newer-version Turnkey Module.

The Phantom circuit portion of this modification does not work correctly. Because the Sense Switch address decoding does not incorporate the PDBIN signal, it will (somewhat randomly) glitch the Phantom flip-flop (IC T pin 5) during any Input instruction. So, for example, when TURMON reads from the console, it will (probably) glitch the Phantom circuit and disable the PROMS.

As part of this modification, the RAM was disabled, because the above Phantom method will not prevent writes to the "phantomed" memory board: writes to the Turnkey Module's onboard RAM would also write to an S-100 memory board that is at the same address.

Note that PROM programs that were written to run on an unmodified older-version Turnkey Module will require an external RAM board in the address range F800h through FBFFh in order to run on a modified board (or a newer-version board), if these PROM programs used the Turnkey Module's onboard RAM for stack space.

88-SYS-CLG Rework

88-SYS-CLG included the following rework:

Operation	Side	Location
Cut trace from D-12 to Q2	Comp.	Near IC D-12
Cut trace from D-12 to D-11	Comp.	Between D-12 and D-11
Cut trace from D-11 to S100-47	Comp.	Near D-11
Cut trace from B-11 to C-4	Comp.	At via near B-7 (above R16)
Cut trace from M1-14 to Q-7	Solder	Near Q-7
Cut trace from M1-13 to IRQ pad	Solder	Near M1-13
Jumper from D-11 to E-5	Solder	Use pad beneath SW-3 of E-5
Jumper from Q2-C to S100-47	Solder	Use pad near D-8 for S100-47
Jumper from M1-13 to S100-47	Solder	Use pad near E-7 for S100-47
Jumper from Q-7 to IRQ pad	Solder	Use pad near P1-1 for IRQ pad
Jumper from T-2 to T-6	Solder	
Jumper from T-7 to U-14	Solder	
Jumper from T-10 to T-11	Solder	
Jumper from T-5 to W-4	Solder	
Jumper from W-2 to M1-15	Solder	
Jumper from D-12 to T-8	Solder	(See below)
Jumper from B-11 to B-7	Solder	(See below)

Disabling Phantom on a Reworked Board

It is possible to undo the effect of this modification without completely reversing the above rework. The following steps will re-enable the onboard RAM, and disable the broken PROM Phantom circuit. (The Jumpstart Phantom will remain functional.)

Operation	Side	Note
Remove jumper from D-12 to T-8	Solder	
Jumper from B-11 to T-1	Solder	Enables onboard RAM
Remove jumper from B-11 to B-7	Solder	
Jumper from D-12 to D-14	Solder	Disables PROM Phantom circuit

Correcting 88-SYS-CLG's Problems with 88-SYS-CLG2

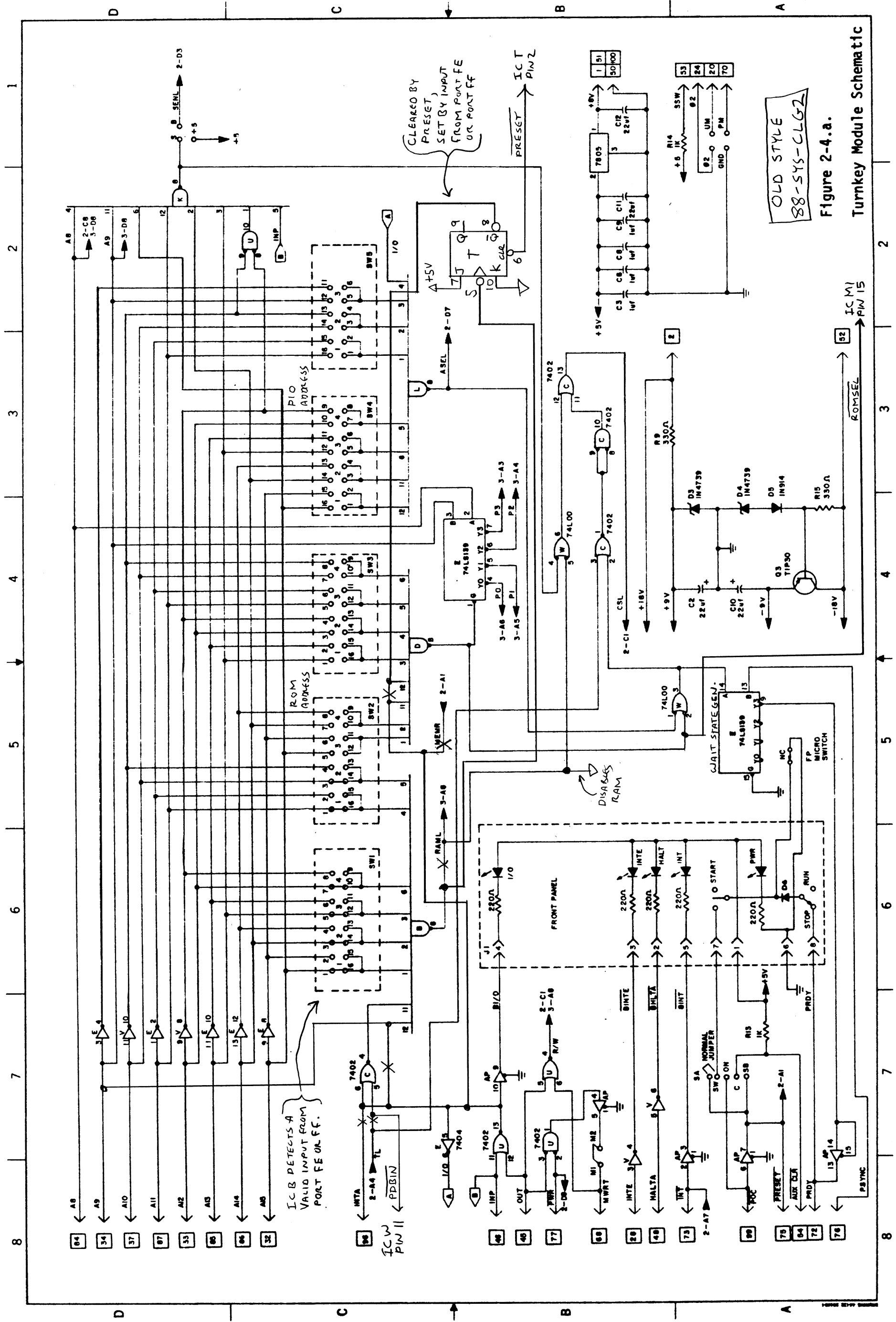
Alternatively, the following additional rework (called 88-SYS-CLG2) will make the Phantom circuit work correctly. This makes the circuit nearly identical to the newer-version Turnkey Module with the rework of Service Bulletin 007, and will allow full 64K of S-100 RAM to be used, once an Input instruction accesses port FEh or FFh.

Operation	Side	Location
Remove jumper from T-5 to W-4	Solder	
Remove jumper from B-11 to B-7	Solder	
Cut trace from C-6 to S100-96	Comp.	Near C-6
Cut trace from C-5 to C-3	Comp.	Near C-5
Cut trace from B-8 to W-5 & the RAM	Solder	Close to B-8
Cut trace from B12 to E5 etc.	Comp.	Near B-8 & R16
(Re)jumper from B-11 to C-4	Solder	Use pad near B-7 for C-4
Jumper from B12 to E3	Solder	
Jumper from W-5 to W-14	Solder	(disables RAM)
Jumper from B-8 to T-5	Solder	
Jumper from C-6 to E-5	Solder	Use pad near U-8 for E-5
Jumper from C-5 to W-11	Solder	
Set all "RAM ADDR" switches to the right ("1" position)		

Note that the eight 2102 SRAM chips may be removed to reduce power consumption.

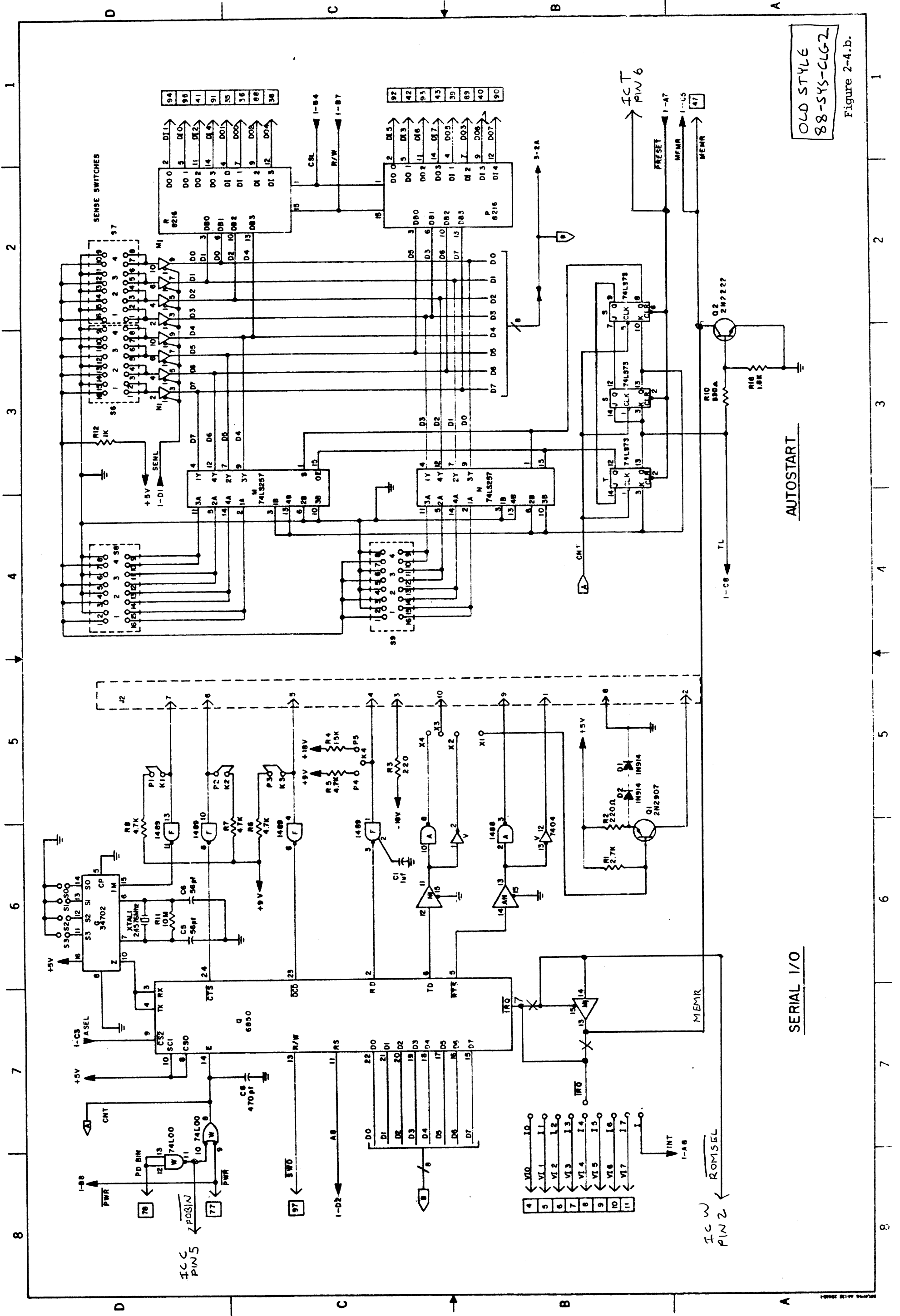
88-SYS-CLG2 Schematics

The following pages are the schematics for the older version Turnkey Module, as modified with 88-SYS-CLG2 rework.



OLD STYLE
88-SYS-CLG2

Figure 2-4.a.
Turnkey Module Schematic



OLD STYLE
88-SYS-CLG2

Figure 2-4.b.

AUTOSTART

SERIAL I/O

IC W
PIN 2 ← ROMSEL

IC T
PIN 6

SENSE SWITCHES

- 94 DO 0 2 D1 1
- 95 DO 1 5 D1 0
- 96 DO 2 11 D1 2
- 97 DO 3 14 D1 4
- 98 DO 4 17 D1 7
- 99 DO 5 20 D1 10
- 00 DO 6 23 D1 13
- 01 DO 7 26 D1 16
- 02 DO 8 29 D1 19
- 03 DO 9 32 D1 22
- 04 DO 10 35 D1 25
- 05 DO 11 38 D1 28
- 06 DO 12 41 D1 31
- 07 DO 13 44 D1 34
- 08 DO 14 47 D1 37
- 09 DO 15 50 D1 40
- 10 DO 16 53 D1 43
- 11 DO 17 56 D1 46
- 12 DO 18 59 D1 49
- 13 DO 19 62 D1 52
- 14 DO 20 65 D1 55
- 15 DO 21 68 D1 58
- 16 DO 22 71 D1 61
- 17 DO 23 74 D1 64
- 18 DO 24 77 D1 67
- 19 DO 25 80 D1 70
- 20 DO 26 83 D1 73
- 21 DO 27 86 D1 76
- 22 DO 28 89 D1 79
- 23 DO 29 92 D1 82
- 24 DO 30 95 D1 85
- 25 DO 31 98 D1 88
- 26 DO 32 101 D1 91
- 27 DO 33 104 D1 94
- 28 DO 34 107 D1 97
- 29 DO 35 110 D1 100
- 30 DO 36 113 D1 103
- 31 DO 37 116 D1 106
- 32 DO 38 119 D1 109
- 33 DO 39 122 D1 112
- 34 DO 40 125 D1 115
- 35 DO 41 128 D1 118
- 36 DO 42 131 D1 121
- 37 DO 43 134 D1 124
- 38 DO 44 137 D1 127
- 39 DO 45 140 D1 130
- 40 DO 46 143 D1 133
- 41 DO 47 146 D1 136
- 42 DO 48 149 D1 139
- 43 DO 49 152 D1 142
- 44 DO 50 155 D1 145
- 45 DO 51 158 D1 148
- 46 DO 52 161 D1 151
- 47 DO 53 164 D1 154
- 48 DO 54 167 D1 157
- 49 DO 55 170 D1 160
- 50 DO 56 173 D1 163
- 51 DO 57 176 D1 166
- 52 DO 58 179 D1 169
- 53 DO 59 182 D1 172
- 54 DO 60 185 D1 175
- 55 DO 61 188 D1 178
- 56 DO 62 191 D1 181
- 57 DO 63 194 D1 184
- 58 DO 64 197 D1 187
- 59 DO 65 200 D1 190
- 60 DO 66 203 D1 193
- 61 DO 67 206 D1 196
- 62 DO 68 209 D1 199
- 63 DO 69 212 D1 202
- 64 DO 70 215 D1 205
- 65 DO 71 218 D1 208
- 66 DO 72 221 D1 211
- 67 DO 73 224 D1 214
- 68 DO 74 227 D1 217
- 69 DO 75 230 D1 220
- 70 DO 76 233 D1 223
- 71 DO 77 236 D1 226
- 72 DO 78 239 D1 229
- 73 DO 79 242 D1 232
- 74 DO 80 245 D1 235
- 75 DO 81 248 D1 238
- 76 DO 82 251 D1 241
- 77 DO 83 254 D1 244
- 78 DO 84 257 D1 247
- 79 DO 85 260 D1 250
- 80 DO 86 263 D1 253
- 81 DO 87 266 D1 256
- 82 DO 88 269 D1 259
- 83 DO 89 272 D1 262
- 84 DO 90 275 D1 265
- 85 DO 91 278 D1 268
- 86 DO 92 281 D1 271
- 87 DO 93 284 D1 274
- 88 DO 94 287 D1 277
- 89 DO 95 290 D1 280
- 90 DO 96 293 D1 283
- 91 DO 97 296 D1 286
- 92 DO 98 299 D1 289
- 93 DO 99 302 D1 292
- 94 DO 100 305 D1 295
- 95 DO 101 308 D1 298
- 96 DO 102 311 D1 301
- 97 DO 103 314 D1 304
- 98 DO 104 317 D1 307
- 99 DO 105 320 D1 310

1 2 3 4 5 6 7 8

OLD STYLE
88-SYS-CLG-2

Figure 2-4.c.

THESE RAMS ARE DISABLED (AND MAY BE REMOVED)

